TESTING TWO DESIGN PIXEL DETECTOR READOUT COMPONENTS FOR THE PHASE I UPGRADE OF THE CMS EXPERIMENT

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During Phase I (2018) of the Large Hadron Collider (LHC) upgrade, the Compact Muon Solenoid (CMS) pixel detector will need to handle a much higher data volume due to the doubling of the luminosity as well as the planned increase in the number of pixel modules. To meet this challenge, the readout scheme will be changed to digital readout and the readout frequency will be increased. The design of the new readout system includes the use of a voltage control oscillator (VCO) and data serializers. A possible VCO design was developed by the Paul Scherrer Institute. This thesis documents the computerized simulation of this design which predicted that it would perform adequately. Then, three prototype samples were built and tested experimentally. To determine radiation hardness, they were irradiated with ^{60}Co in 10 doses of 50 KGy, each. The measurements showed that this circuit will keep working under high doses of irradiation. The serializer has also been designed and studied via simulation determining its timing parameters. The circuit design performs as expected.

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Requerimientos para el grado de Maestría en Ciencias

PRUEBAS AL DISEÑO DE DOS COMPONENTES DEL SISTEMA DE LECTURA DEL DETECTOR DE PÍXELES EN LA FASE I DE ACTUALIZACIÓN DEL EXPERIMENTO CMS

Por

Indira Dajhana Vergara-Quispe

Julio 2013

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Durante la fase I (2018) de actualización del Gran Colisionador de Hadrones (LHC, por sus siglas en inglés), el detector de píxeles del Solenoide Compacto de Muones (CMS, por sus siglas en inglés) necesitará manejar un mayor volumen de datos debido a la duplicación en el valor de luminosidad y al incremento en el número de módulos de píxeles. Para superar este reto, el sistema actual de lectura será cambiado a uno completamente digital y la frecuencia de lectura será incrementada. El diseño del nuevo sistema de lectura incluye el uso de un oscilador controlado por voltaje (VCO) y serializadores de datos. Un posible diseño para el VCO fue desarrollado por el Instituto Paul Scherrer. Esta tesis documenta la simulación computadorizada de este diseño con la predicción de que tendriá un rendimiento adecuado. Tres muestras de prototipo fueron construidas y probadas experimentalmente. Para determinar el daño que les causará la alta radiación a la cual estarán expuestas, fueron irradiadas con 10 dosis de ^{60}CO, cada dosis de 50 KGy. Las mediciones mostraron que este circuito seguirá trabajando a altas dosis de radiación. El serializador también ha sido diseñado y estudiado a través de simulaciones determinando así los paraḿetros de tiempo. El circuito funciona como se espera.

To everybody, who inspired me everyday.

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CHAPTER 1
INTRODUCTION

Physics, through the course of time and with its attempt to explain existing phenomena in nature, has reached boundaries that long time ago no one imaged could have been reached. The Large Hadron Collider (LHC) and its experiments built at the European Organization for Nuclear Research (CERN) laboratory on the Franco-Swiss border are just some examples of the things mankind have, or are working with, in our contemporary times. Their goal is the study of the properties and interactions of the elementary particles as well as to validate or dismiss theories of particle physics, and to uncover the mysteries of the formation of the universe. At this point in the history of experimental particle physics, there is much expectation to get answers to some of the open questions which have been posed for many years. CERN has built the largest machine ever produced by mankind in order to study the smallest components of matter.

The LHC is a particle accelerator and collider that was built to achieve an energy of 14 TeV in the proton collisions and 1150 TeV in the lead ion collisions; as well as a luminosity of $10^{34} cm^{-2} s^{-1}$ for proton beam and $10^{27} cm^{-2} s^{-1}$ for lead ion beam. The lead ion beams circulate in the LHC one month per year while the proton beams circulate the rest of the time. In both cases two beams run in opposite directions through two rings of 27 km length. The protons that are input to the LHC come from a multi-stage accelerator complex. They are obtained by removing the electrons from hydrogen atoms. These protons gain 50 MeV of energy in a linear accelerator (LINAC2), and, then are accelerated in the Proton Synchrotron Booster (PSB) and Proton Synchrotron (PS) where they acquire 25 GeV and a bunch structure (the beams are not a continuous stream) of 25 ns; each bunch has 1.15 x 10^{11} protons. Before the protons arrive to the LHC, they pass through the Super Proton Synchrotron (SPS) which operates at 450

GeV. In the LHC, the protons circulate for 20 minutes while the beams stabilize at the maximum speed and energy before they are made to collide for periods covering hours [1]. When the beam intensity has declined, then the remaining protons are dumped and the beams are refilled to repeat the acceleration process. There are four collision points along the LHC (Figure 1–1); at any one given point, collisions typically occur every 25 ns. Collisions at a center of mass energy of 7 TeV and a luminosity of $10^{33} cm^{-2} s^{-1}$ were first achieved on March 30, 2010.

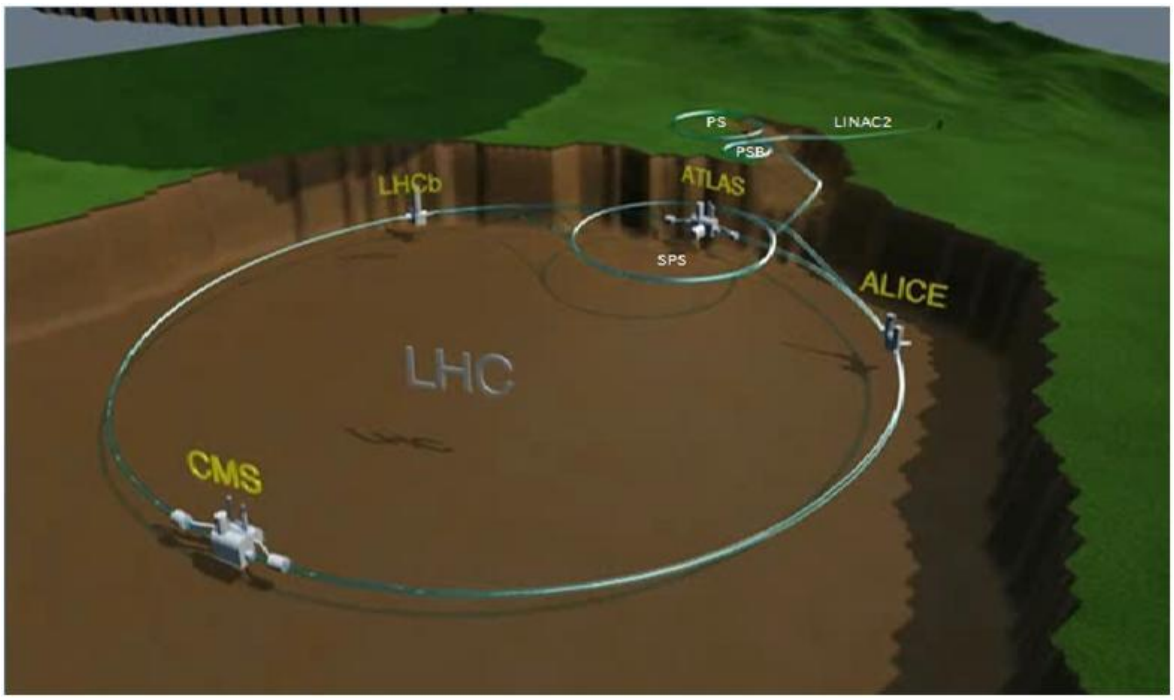

Figure 1–1: Overview of the LHC accelerator complex and detectors [2].

The Compact Muon Solenoid (CMS) is an experiment built at one of the four collision points of the LHC. This experiments chief goals are to study physics at the TeV level; search for the Higgs boson, supersymmetry, extra dimensions and dark matter; and

also to study heavy ion collisions [3]. The experiment is made up by different subdetectors; each one has a specific purpose even though its measurements are complementary to the others. A large solenoid provides a high magnetic field of 4 T. The muon detector is the outermost and has been placed outside of the solenoid as shown in Figure 1–2. Inside of the solenoid there are three subdetectors which are the hadronic calorimeter, the electromagnetic calorimeter and the tracker system.

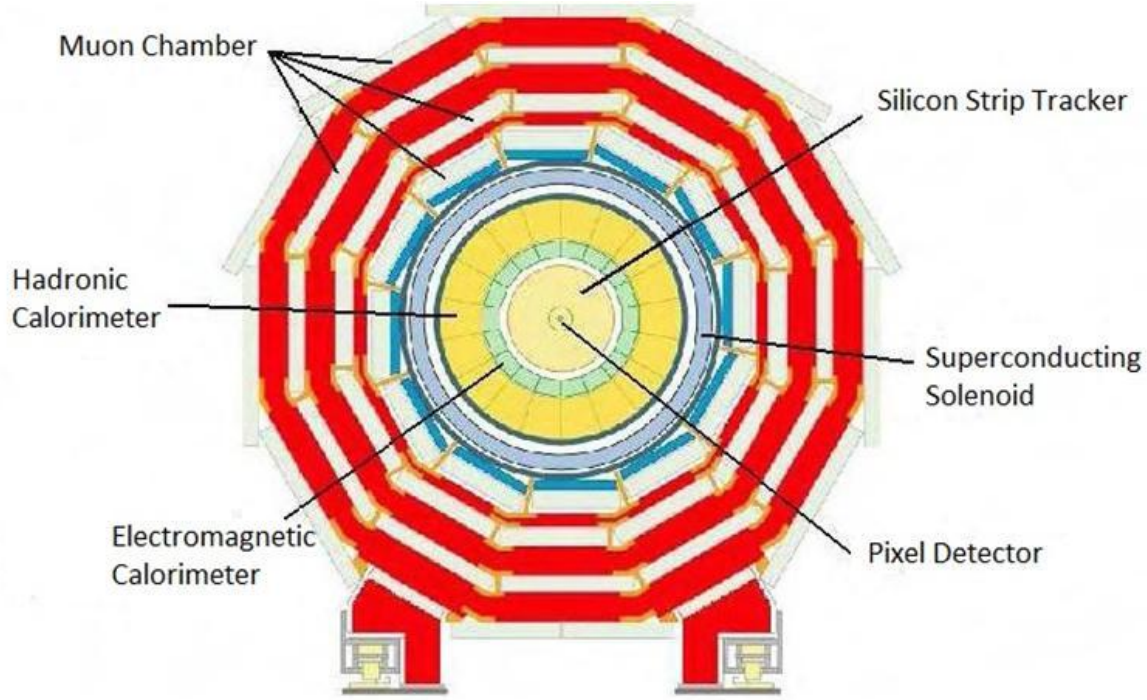

Figure 1–2: Transverse cross-section of the CMS detector [8].

Muon Chamber: One of the most important tasks of CMS is to detect muons which is done in this subdetector. The barrel part of the muon chamber is built with four layers of drift tubes and resistive plate chambers; this latter and cathode strip chambers are in the four disks in each endcap. The drift tubes and the cathode strips measure

the momentum of the muons while the resistive plate chambers are in both parts of the detector because they provide a trigger signal, i.e., decide if the muon data is right or not. Iron yokes are embedded in each layer of the barrel and disk in the endcaps returning the magnetic flux for the magnet and acting as muon absorbers [4].

Hadronic Calorimeter: It measures the relativistic kinetic energy of hadrons and helps to indirectly measure the energy of neutrinos by determining the missing energy. The central barrel (HB) and two endcaps (HE) of the hadronic calorimeter have a sandwich structure of brass (used as absorber material) and plastic scintillator tiles. It detects the energy deposited within. The two forward calorimeters (HF) use iron absorbers and embedded radiation-hard quartz fibers. It is located outside the magnet after the muon chamber endcaps. Similarly, the outer barrel hadronic calorimeter (HO) is covered with scintillators on the outside of the coil [5].

Electromagnetic Calorimeter: The electron and photon relativistic kinetic energy are measured in this detector. It is made of lead tungstate ($PbWO_4$) crystals which are read out by Silicon Avalanche Photodiodes (APDs) in the barrel and Vacuum Phototriodes (VPs) in the endcap. These two photodetectors (APDs and VPs) are glued onto the back of each crystal. In front of the endcaps are Preshower detectors that allow CMS to differentiate between single high energy photons and pairs of low energy photons [3].

Tracker Detectors: These detectors reconstruct the charged particle tracks. There are two tracker subdetectors made of silicon: Silicon Strip Tracker and Pixel Vertex Detector. The Silicon Strip Tracker has 10 barrel layers; the first four layers are called Tracker Inner Barrel (TIB) and the others six layers are Tracker Outer Barrel (TOB). The endcaps corresponding to TIB are 3 pairs of disks called Tracker Inner Disk (TID) and 9 disks for TOB called Tracker Endcap (TEC). The disks of TID are divided into 3 rings; and the disks of the TEC are divided into 7, 6, 5, and 4 rings, where the number of rings decreases for the more external disks [6]. The modules of this detector consist of

strip sensors placed parallel to the beamline, readout electronics and support structure. There are modules of different shapes and dimensions depending on the site to place it. The first two layers of the TIB and TOB have a second module mounted back to back with the first one, and the same is for the rings of the TID and TEC placed in the direction of those layers [7]. The Pixel Detector is the innermost subdetector and consists of 3 barrel layers and 2 endcaps in each side. Pixel modules are the bricks of the Pixel Vertex Detector. This detector allows finding the primary and secondary vertices of interactions.

1.1 Motivation

The LHC will start to increase luminosity up to $10^{35} cm^{-2} s^{-1}$ [9]. This increase will occur in two phases: in phase I, the luminosity will be 2 x $10^{34} cm^{-2} s^{-1}$; and in Phase II (SLHC project), the luminosity will be $10^{35} cm^{-2} s^{-1}$. This luminosity will increase the number of particles emerging from the collisions. Therefore, the subdetectors used in the experiments need to be upgraded.

The pixel detector upgrade consists in adding one layer for barrel and one disk in each endcap for a better resolution of the tracks. Figure 1–3 shows the difference between these two structures. The upgrade is designed for higher luminosity and lower material budget for which it is necessary to do some changes like new mechanical structure, use of CO_2 for cooling, including a new readout system and cabling. The increase in the number of particles produced in each beam crossing, and increasing the number of modules; the data volume will be greatly increased and this makes necessary to increase the size of the buffers in the modules (larger data storage capacity). A change from the current analog readout system to digital readout will result in increased speed. The new readout system is designed to reach transmission data speeds of 160 Mbit/s out of every pixel chip and 320 Mbit/s out of every group of chips called a module while the current readout has an equivalent speed of 100 Mbit/s. This increment of a factor of 3.2 in speed is sufficient

to compensate for the doubling of the luminosity and the 33% increase in the number of pixel channels as well as the expected increase in the number of hits per beam crossing. Among the circuits added to the new readout system are the Voltage Control Oscillator (VCO) and the Serializer. Both systems are designed to achieve the correct frequency of sending data out. This thesis concerns the design and testing of these new circuits.

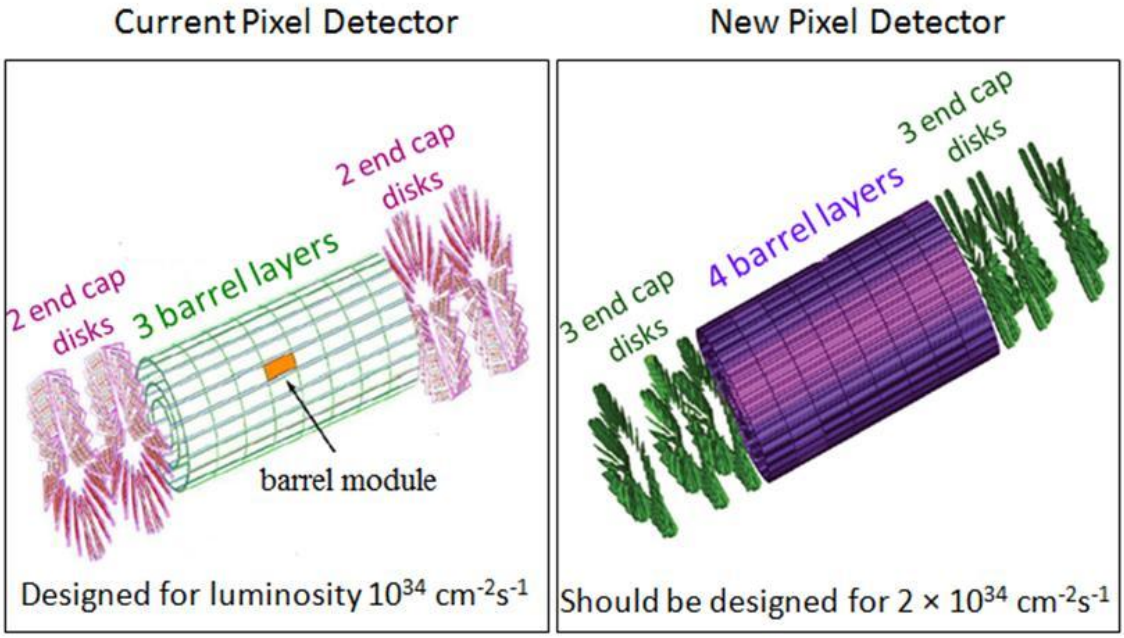

Figure 1–3: Current pixel detector and a new design for the pixel detector upgrade [7, 10].

1.2 Summary of the Following Chapters

This thesis began with an introduction of LHC and CMS, as well as, its subdetectors. The pixel detector, its readout system and upgrade are described in Chapter 2 in order to understand the changes to be made in it. Chapter 3 sets forth a short explanation of MOSFET transistors and CMOS technology which were used in the new components studied. The next two chapters explain the performance of two new circuits: Voltage Control Oscillator (VCO) and Serializer respectively. Chapter 4 shows the results of the

simulation and measurements done to 3 samples of VCO, before and after they were irradiated. In addition, the chapter describes the setup used in the test. The design of the Serializer is studied in Chapter 5 using electronic circuit simulations. Finally, the conclusions and future works are presented in Chapter 6.

CHAPTER 2
PIXEL DETECTOR AND UPGRADE

The pixel detector has two parts: the barrel and the disks also called barrel pixel (BPIX) and forward pixel (FPIX), respectively. The barrel consists of three concentric cylindrical layers of different radii: 4.4 cm, 7.3 cm and 10.2 cm; and their length is 53 cm. The two disks are placed in each end of the barrel [1]. The modules, the basic component of the barrel, were assembled in two half shells of the detector as shown in Figure 2–1. Full modules fill up most of the surface of the cylinders. Eight modules ordered in a straight line are assembled parallel to the cylinder axis on the inner and the outer surface of each cylinder layer. A few half-modules are needed on the ends placed sidewise to fill up the rest of the space [11].

In the FPIX, each disk with an internal and external radii of 6cm and 15cm, respectively, has 24 panels on both of its sides. There are two versions of panels, one is placed on the side nearest to the interaction region and it has four plaquettes and the other version has three plaquettes placed on the opposite side. The plaquettes are the basic component of the disk and there are five different sizes; the size depends on the number of pixel chips which runs from 2 to 10, thus depending on the plaquette position. The disks also were assembled in two halves (Figure 2–2) which are held in place by the FPIX service cylinder [11].

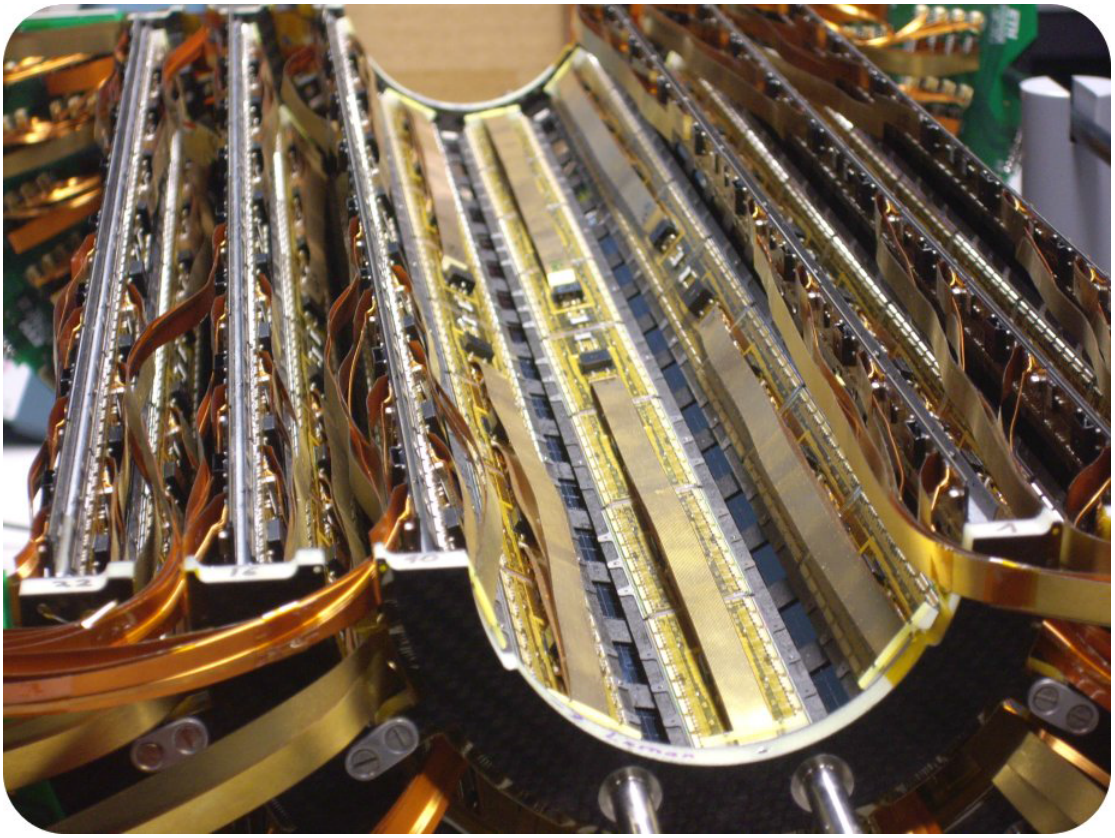

Figure 2–1: Barrel pixel detector half shells filled with 360 modules [12].

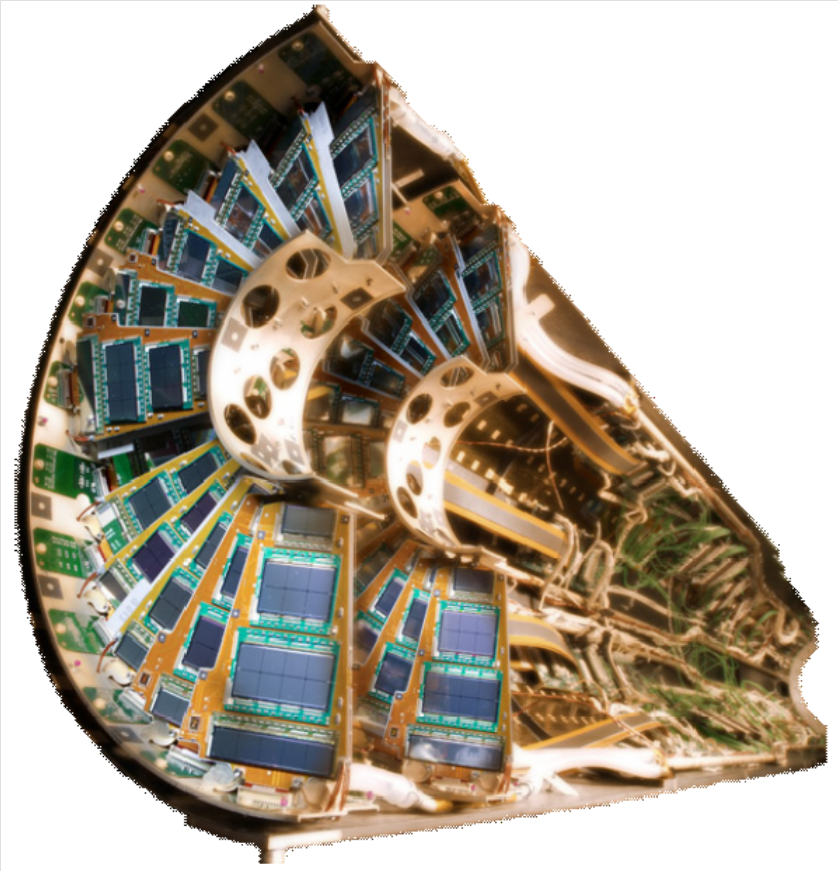

Figure 2–2: Half disks of the forward pixel detector in the FPIX service cylinder [13].

2.1 Pixel Detector Modules

BPIX modules and FPIX plaquettes have a similar structure. The details of the description here is for the BPIX module but the main difference with the FPIX plaquette is in the number of pixel chips. The module is a complex structure (Figure 2–3) composed of the pixel sensor, the readout chips (ROCs), a high density interconnect (HDI), a token bit manager (TBM), and power and kapton output cables.

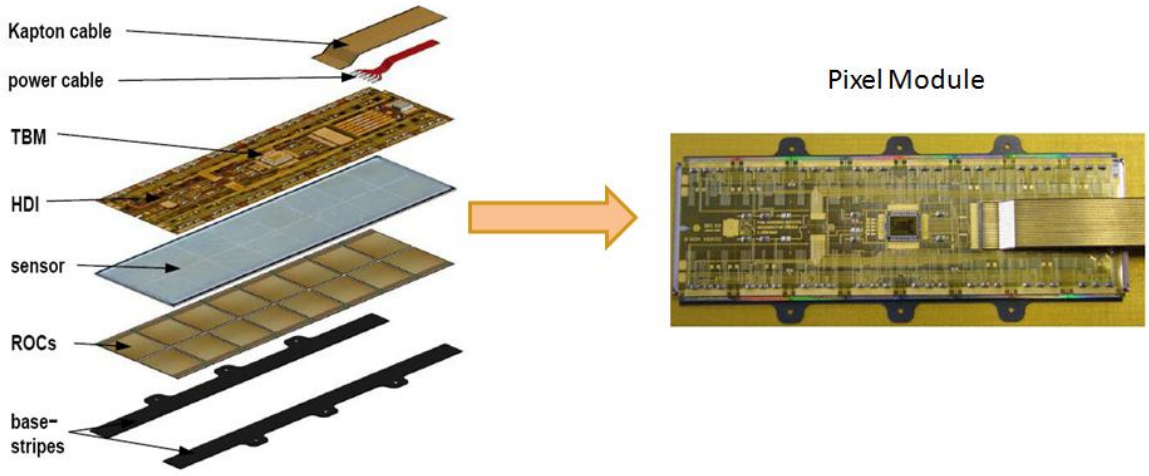

Figure 2–3: Components and view of the pixel module [14].

There are 66,560 pixels in each module. This part is the sensor that generates a signal current when a particle crosses it. The charge in the current is detected and measured by a PUC (Pixel Unit Cell), an electronic circuit located in the ROC. There is one PUC for every pixel. The pixel sensor is connected to the PUC via an indium bump bond. The PUCs are grouped into units called ROCs, made up of 4,160 PUCs and additional readout circuits; hence a module has sixteen ROCs. The size of the module is 66.6 mm in length and 26.0 mm in width [14].

2.1.1 Silicon Sensor

The silicon sensor (Figure 2–4) is made of n-substrate which has approximately $270\mu m$ of thickness and a size of 6.66 cm 1.86 cm with a p^+-layer on one side and n^+-implants on the other side. The p^+-layer is supplied by a negative high voltage (-150 V for unirradiated and up to -600 V for irradiated sensors) in order to enlarge the depletion region of what is essentially a silicon diode. Particles from LHC collisions will generate electron-hole pairs when crossing the pixel. The electric field present in the totality of the material when it is completely depleted moves the holes toward the p^+-layer and the electrons toward the n^+-implants. These charge carriers are not lost to recombination because the material is depleted.

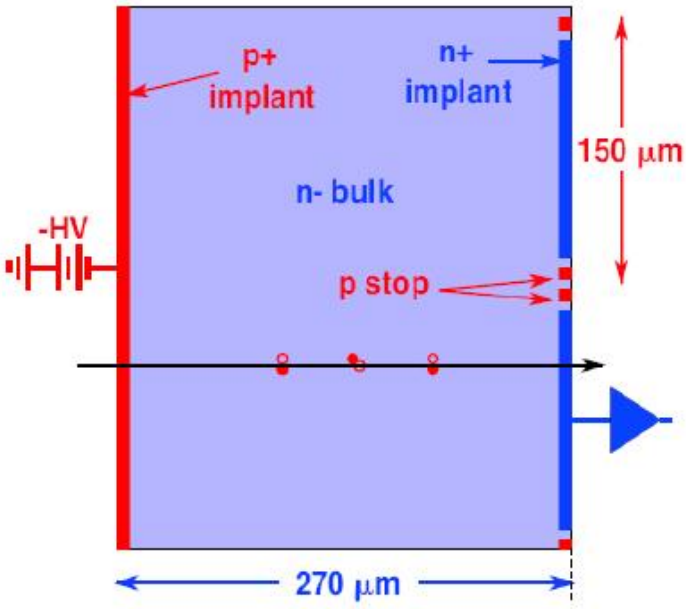

Figure 2–4: Structure of a pixel sensor [15].

The pixels are isolated from each other by one or two p^+-implants (also called p-stops), and they are connected to the readout system through indium bumps with diameter of roughly $20\mu m$ (Figure 2–5). This technique was developed at the Paul

Scherrer Institute and is called bump-bond. These implants segment the sensor into 66,560 pixels; each pixel has a size of 100μm x 150μm [3].

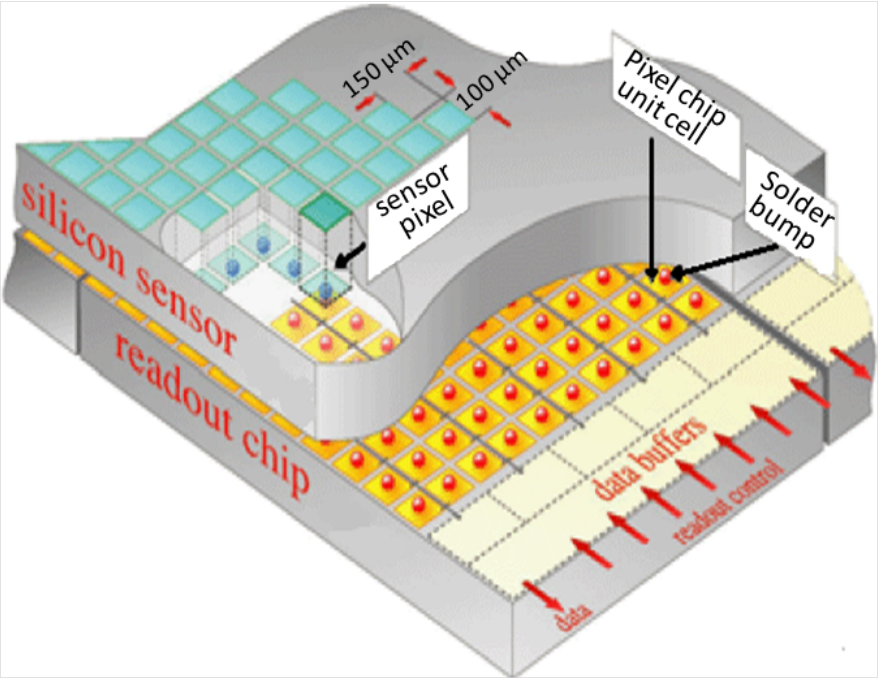

Figure 2–5: Schematic of the pixel sensors connected to the readout chip (ROC) by indium bumps [16].

2.1.2 Readout Chip

The readout chip (ROC) is the electronic part that reads the charge generated in the pixel sensor. There are sixteen ROCs per module; each ROC is divided into three different parts which are the Pixel Unit Cell (PUC) array, Double Column Interface (DCI), and Control and Interface Block (CIB). Each ROC has 4,160 PUCs arranged in 80 rows and 52 columns [7].

The PUC is the readout circuit in contact with the pixel sensor through the indium bump. Once the PUC has received the signal from the pixel sensor, it is amplified and then compared with a given threshold in order to decide if it is a hit (real signal) or

noise. If it is noise, then, it is erased; otherwise the signal is attached a PUC address and transferred to its Double Column. This process is outlined in Figure 2–6. The Double Column Interface is the space in the ROC which has 26 identical circuits; each one is called Double Column because it stores the signal and its respective address from 2 PUC columns (160 PUCs). When a hit is identified in the PUC comparator, the double column is notified and 1 time-stamp buffer is activated. The time stamp buffer stores the information about which bunch crossing belongs the data of the pixels stored in the data buffers. There are 12 time stamp buffers and 32 data buffers. A column drain control in the double column sends an internal token signal as a response to the notification about hits. When this token arrives in each PUC hit, the PUC will transfer the analog pulse height of the signal and its PUC address to the data buffers (Figure 2.8). Here, in the data buffers of the double column, the signal information waits to be read by an external token. The arrival of this external token tells the ROC to put the stored information onto the main data stream. The double column transfers the information from the data buffers to the Control and Interface Block which is the last part of the readout system in the ROC. The CIB receives the information from the 26 double columns and sends it to the Token Bit Manager (TBM).

2.1.3 High Density Interconnect

The high density interconnect (HDI) is a flexible printed circuit board that is glued on one side of the sensor and connected to the ROCs by wire-bonds at the lateral edges (Figure 2–8). This board distributes the power and control signals to the sensor and the ROCs, and also controls the readout of the module by the Token Bit Manager (TBM). The control and power signals are brought to the modules from outside by two cables: Kapton and power cables, respectively [12].

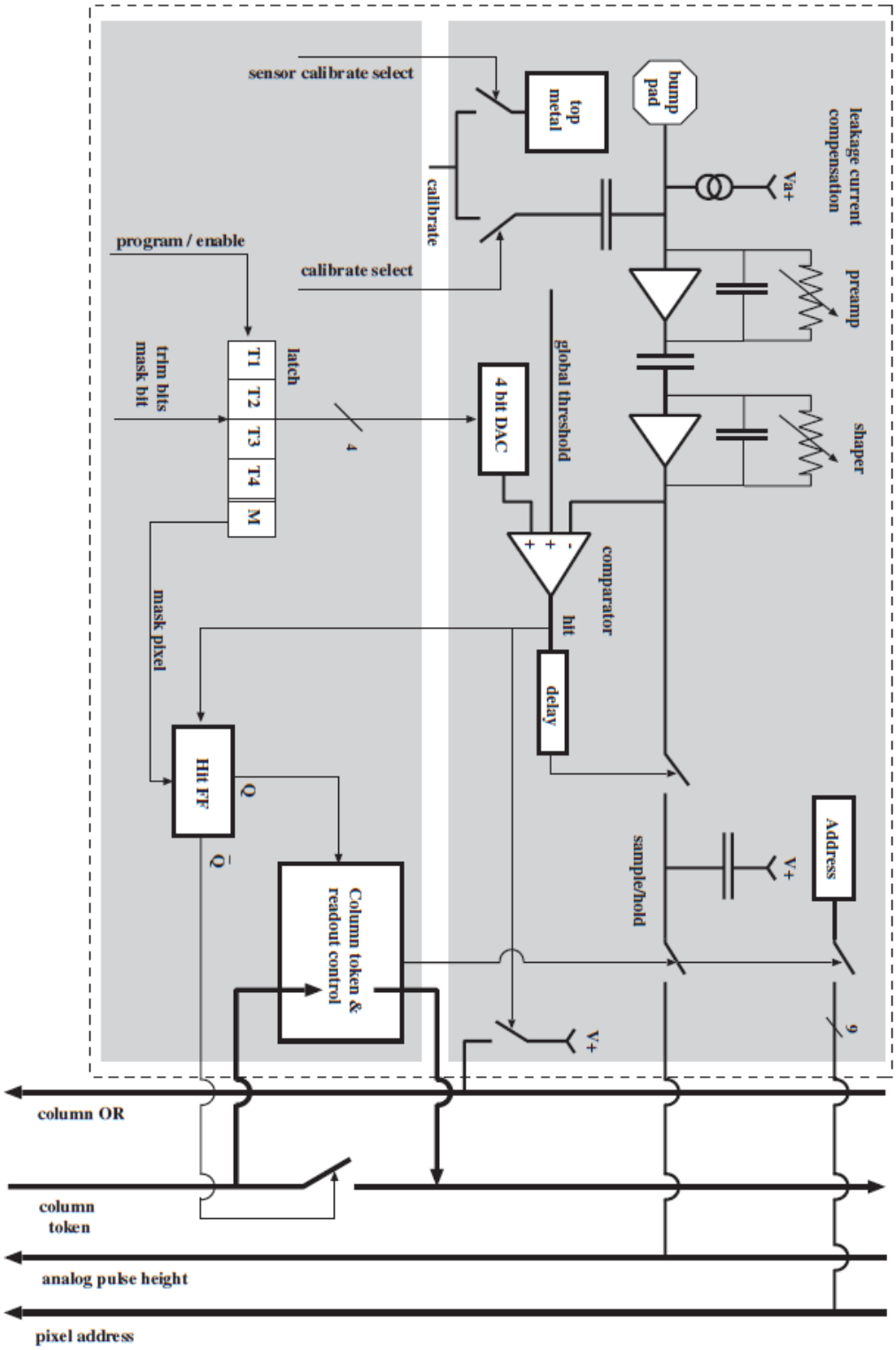

Figure 2–6: Readout system of the pixel unit cell (PUC) [17].

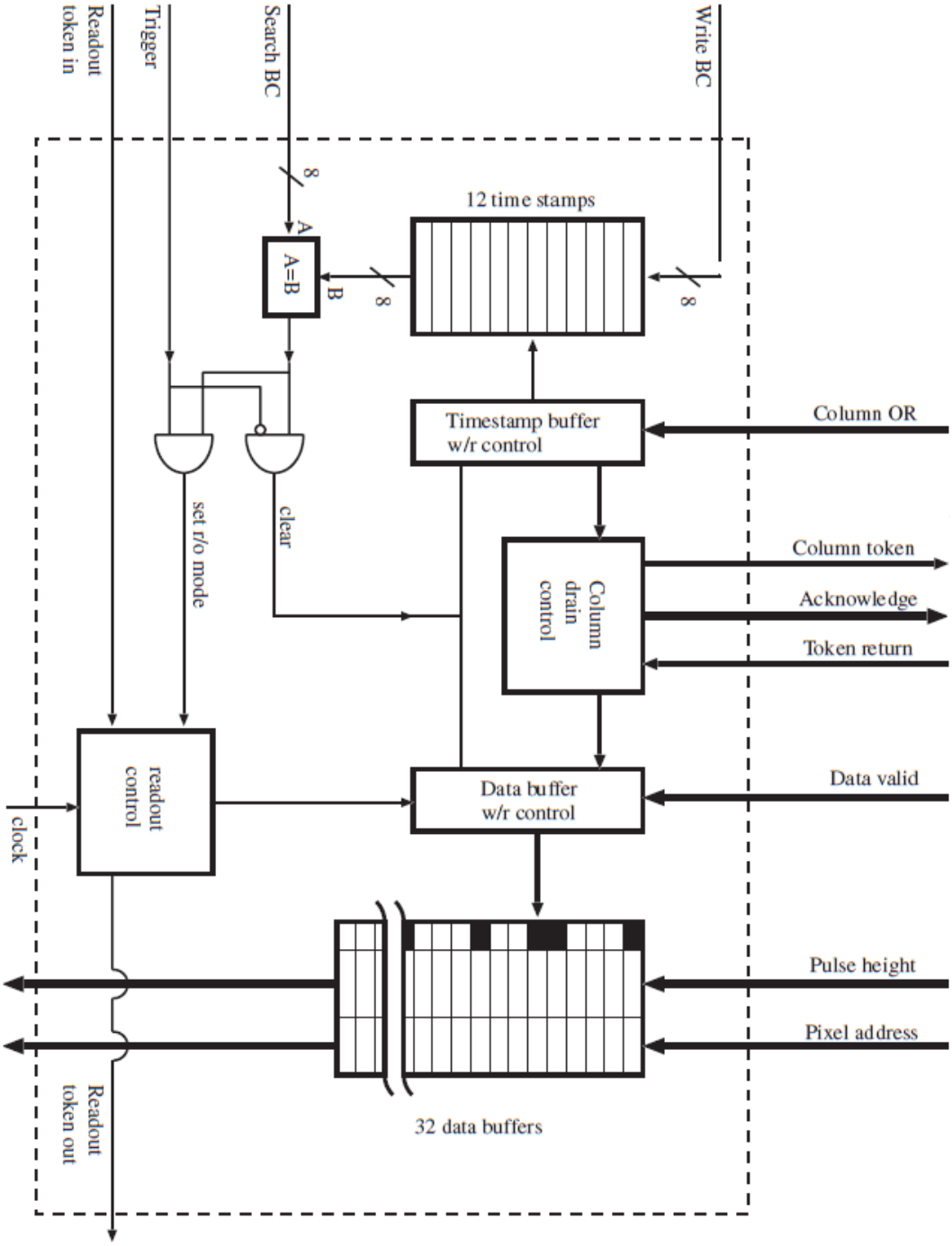

Figure 2–7: Readout system of the double column interfaceReadout system of the pixel unit cell (PUC) [17].

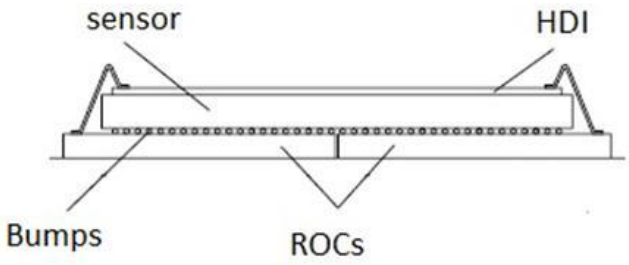

Figure 2–8: Transverse view of the assembly scheme of the module.

Kapton Cable: It transmits the control signals from the end flange printed circuit board (end flange PCB) to the module and brings the analog hit signals in the opposite direction through its 21 traces of which 14 traces transfer differential signals. The end of the kapton cable that connects to the module is connected to the HDI by wire-bonds [15].

Power Cable: This supplies the module with bias voltage (-150 V) to the sensor, digital (2.5 V) and analog (1.5 V) voltages.

Token Bit Manager: The ROCs receive the token and the clock signals from this chip. The TBM controls the readout of either 8 or 16 ROCs. The modules of the outermost layer are controlled by just one TBM while the modules of the inner layers need two TBM due to their higher hit density.

2.1.4 External Readout

The external readout involves the data out from the module to the electronic control room where is placed the pixel front end driver (pxFED), pixel front end controller (pxFEC) and front end control (FEC) and it is placed 100 meters from the detector [3].

The data is transferred by kapton cable to the end flange PCBs and, then, transferred to the analog level translator chip (ALT) on the supply tube which amplifies the signal before being converted to an analog optical signal by the Analog Optical Hybrid (AOH). After this process, the information is transferred by optical fibers to the FED where it is digitized and sent to the CMS data acquisition system (Figure 2–9) [3].

The control signal is provided by the Front End Control System in two different ways. One is the pixel Front End Controlled (pxFEC). That is a fast control and provides the triggers, clock information, and so on. The pxFEC sends the signal via optical fibers; then a Digital Optical Hybrid (DOH) converts the optical to an electric signal. The clock and trigger signal are separated by the Phase Locked Loop chips (PLLs) while the Delay chip adjusts the phases of all control signals. As the modules use Low Current Differential Signaling (LCDS), this current is obtained in the Gate-Keeper chip to convert the Low voltage Differential Signaling (LVDS). The LCDS is sent to the modules by the LCDS-Driver chips. The FED controls the whole detector where four communication and control unit boards (CCU) are used for the CMS barrel pixel which works with an I^2C protocol.

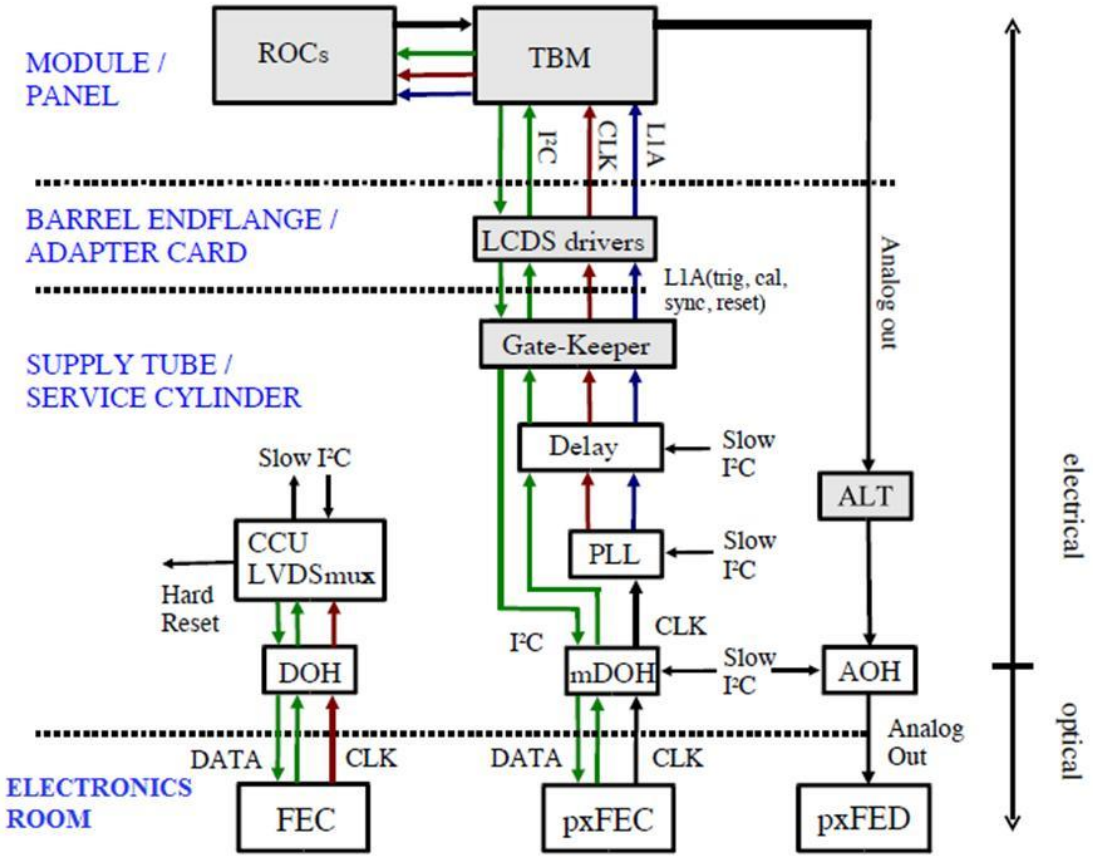

Figure 2–9: External readout of the pixel detector [3].

2.2 New Readout System

The pixel detector will have different changes for the upgrade (phase I) to get a higher data volume. However, the data will be sent out of the detector by the same amount of optical fibers as in the present because there is no more space to add optical fibers. Thus, it is necessary to perform two basic things: (1) The module must be able to handle and store a larger amount of data during each bunch crossing; (2) more data must be transferred through the same number of fibers in the same amount of time. To accomplish these goals, the main changes will be: changes to the data handling by the ROC, an increased readout frequency, and a change from an analog to a digital readout scheme. The first change will avoid data loss by overflows in the buffers; the second

change will allow achieving a higher data rate per ROC and per fiber while the last change is necessary because the current readout (analog) is multi-level and its rise and fall time arent fast enough. The new readout system is designed in order to achieve this new data rate which involves doing changes to the ROCs, DCIs, CIB, TBM, cabling and external readout.

2.2.1 New Double Column Interface

In the data buffers and time-stamp buffers of the DCI, pixel hit information is stored waiting for trigger verification. At higher luminosity, the dominating data loss will be by overflows in the buffers. For this reason, the size of the data and time-stamp buffers of the DCI has to be increased (Figure 2–10). The number of the data buffers will be increased to 80 and the time stamp buffers to 24.

2.2.2 New Double Column Interface

DCI buffers with trigger-verified data are blocked from further pixels hits until they are read out. This time will be large with increased luminosity because of the higher data traffic. An additional ROC global readout buffer is added in the CIB for that reason. The new buffer splits the readout in two stages: an internal readout of the double columns to the readout buffer and the external readout (from the readout buffer to TBM). At first stage, an internal token is started immediately if a trigger arrives. This token manages the readout from the double columns to the readout buffer. The readout buffer is able to store pixel hit information from different triggers. The ROC readout is initiated with an external token; pixel data corresponding to the particular trigger is sent to the external data bus (Figure 2–11).

The readout buffer sends 24 bits to a multiplexor. The number of bits corresponding to each unit of information is as follows: 6 for the DC address; 9 for the data buffer (analogous to the row address in the analog readout); 8 for the pixel hit information (PH); and 1 bit is an additional bit 0 and it will be placed in the middle of the PH.

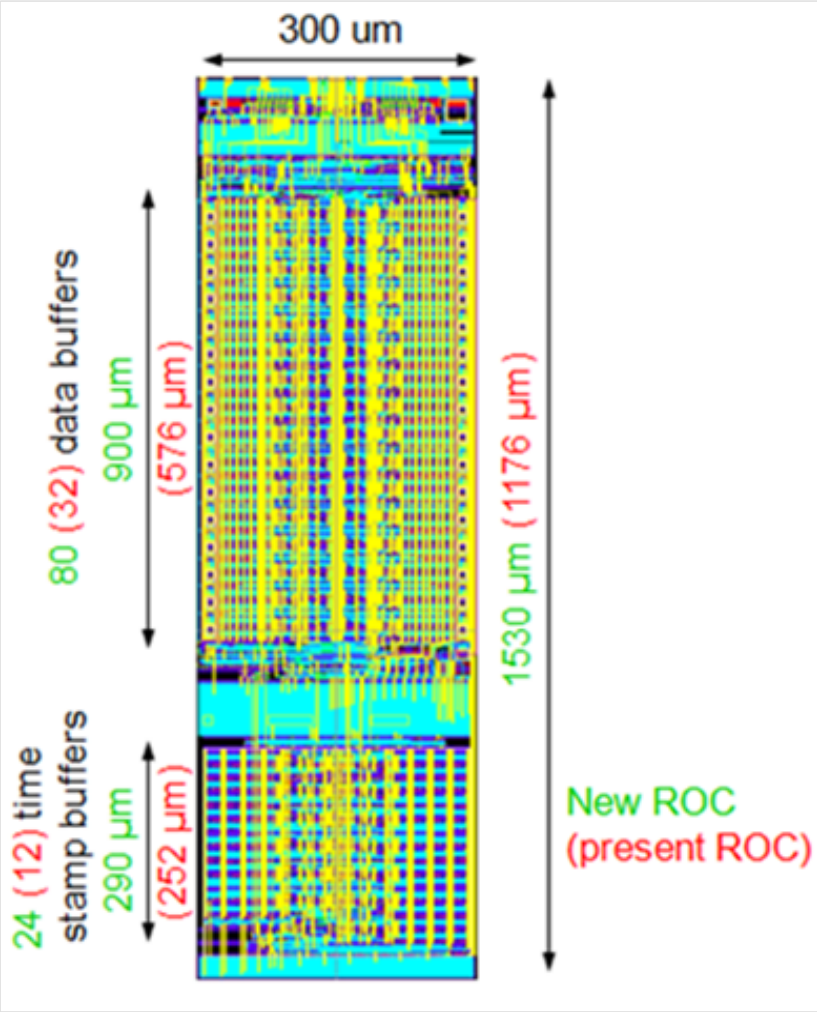

Figure 2–10: One of the twenty six Double Column Interface with size and number of buffers, for current (red) and new (green) ROC. interface [18].

The pixel address (row and column) are already digitized in the current readout. An 8 bit SAR-ADC circuit will be added to convert the analog PH to digital. The address information will be sent to the readout buffer at 80 MHz. The multiplexer will send this information (PH and pixel address) in groups of 4 bits each to a serializer that will transmit the information at 160 MHz. The serializer is one of the main new circuits added in the CIB which will receive 4 bits in parallel at 40 MHz each and serialize

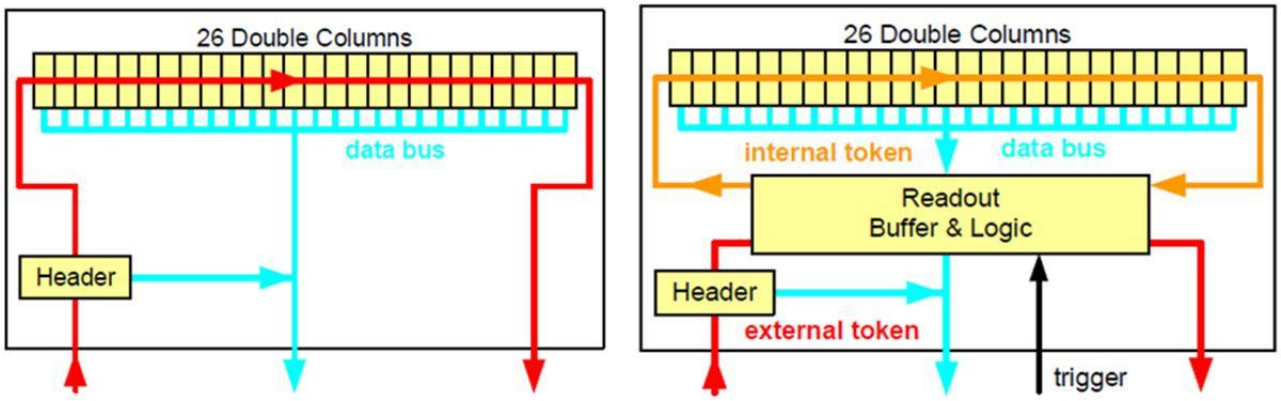

Figure 2–11: Present readout of the double column interface (left) and readout schema of the Double columns with a new buffer (right) [19].

it getting in the output 4bits/LHC clock while for the analog readout this is only 2.5 bits/LHC clock [13].

The other main circuit is the Phase-locked loop (PPL) because it distributes clock signals of different frequencies (40 MHz, 80 MHz and 160 MHz) to some circuits in the ROC. All these new circuits are illustrated as a the diagram in Figure 2–12.

2.2.3 New Token Bit Manager

The design of the new token bit manager chip involves the use of new circuits (Figure 2–13). The serializer will convert the TBM head and trailer signals from 40 MHz to 160 MHz of frequency, and a digital multiplexer will convert the two data streams (each data stream brings the information of 8 ROCs) to a serial data of 320 Mbit/s.

2.2.4 Data cable

The kapton cable will be replaced by micro-twisted pair cable whose length will be 1 m [15]. The kapton cables are currently connected to the end flange PCBs and these, in turn, connected to the supply tube as shown in Figure 2–14. The micro-twisted pair cables will allow omitting the end flange PCBs and their connectors because these new

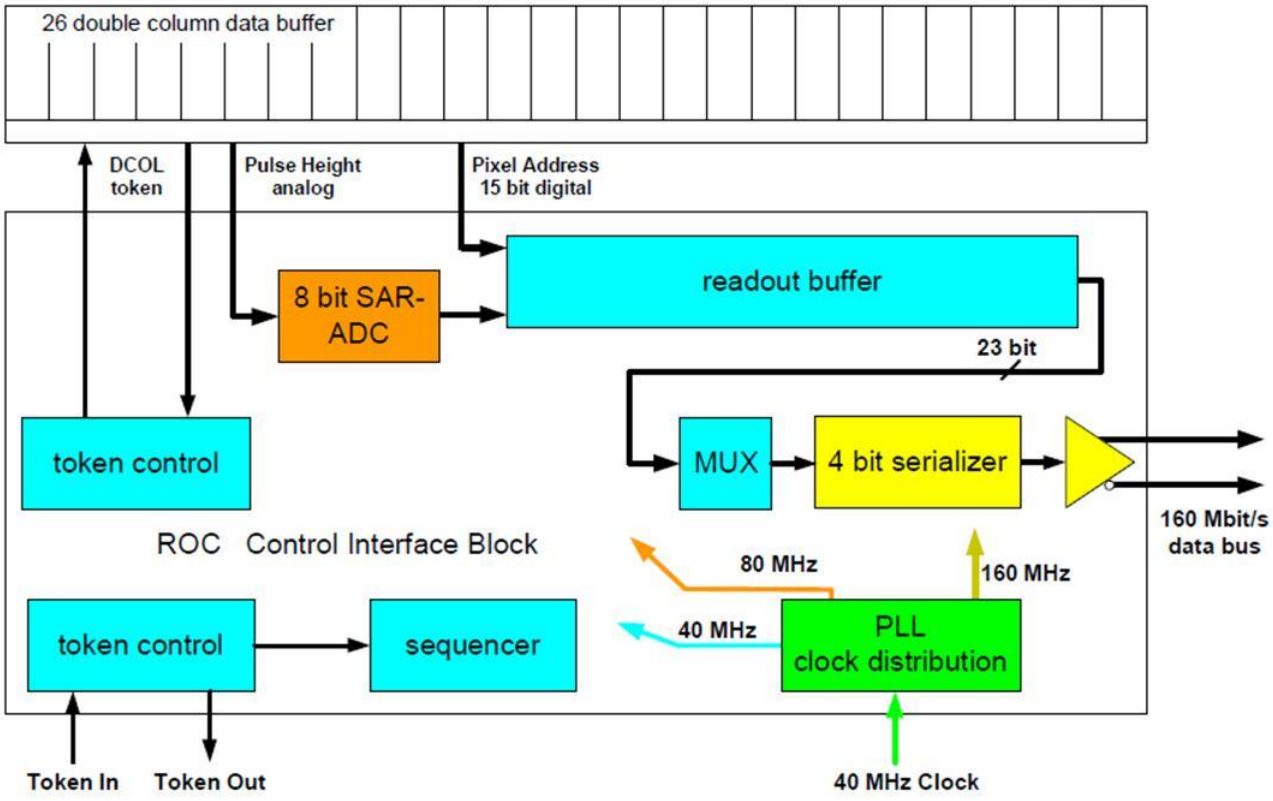

Figure 2–12: New components of the control interface block [13].

cables are much more pliable. This change will result in a significant reduction of the material budget in the

2.2.5 New External Readout

Besides the removal of the end flange PCBs, the pixel Front End Driver will require the addition of deserializers which will deserialize 4 bits to 40 MHz and preclude additional changes downstream of this point in the data acquisition system, therefore it will keep as in the present [18].

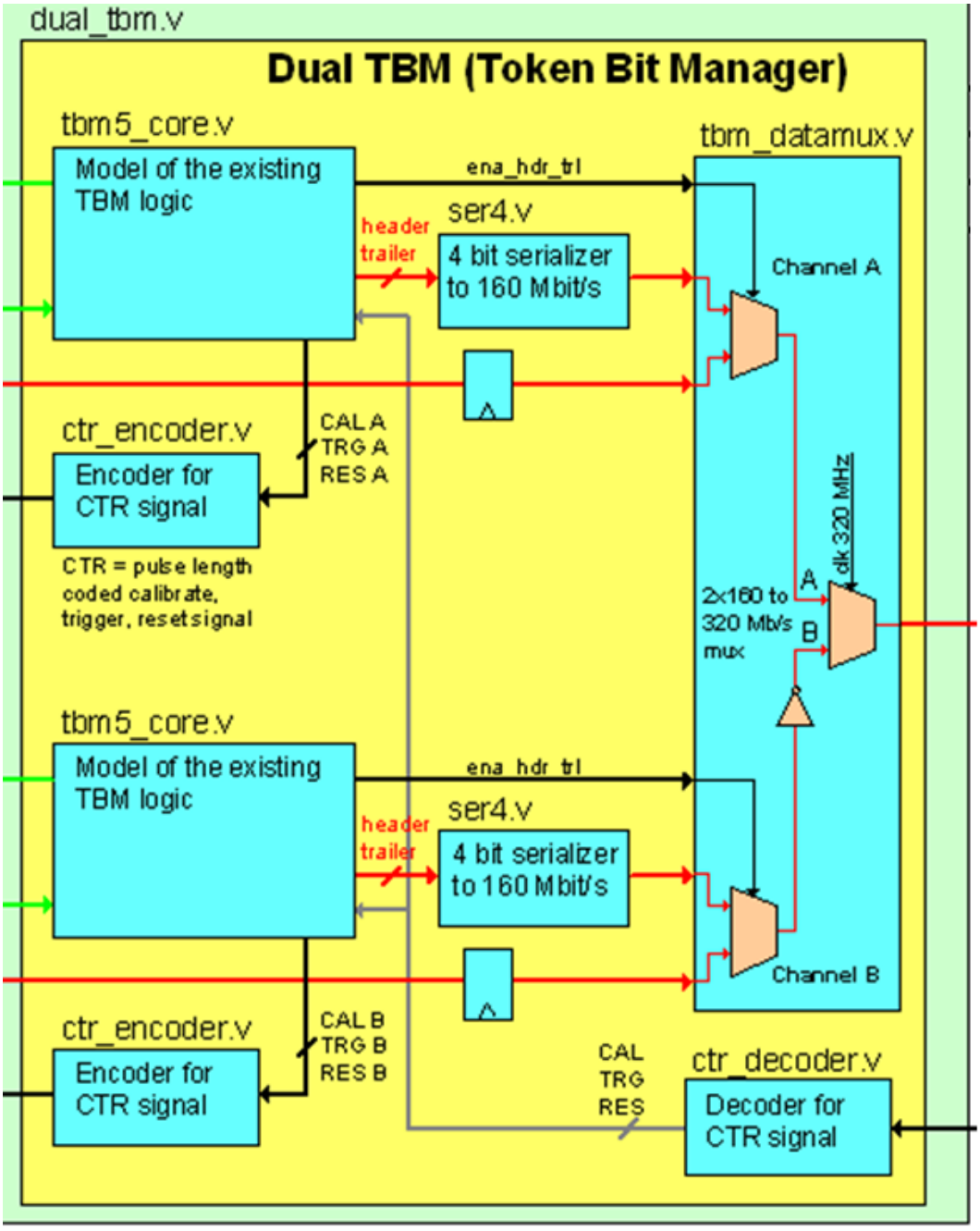

Figure 2–13: Design for new token bit manager chip [18].

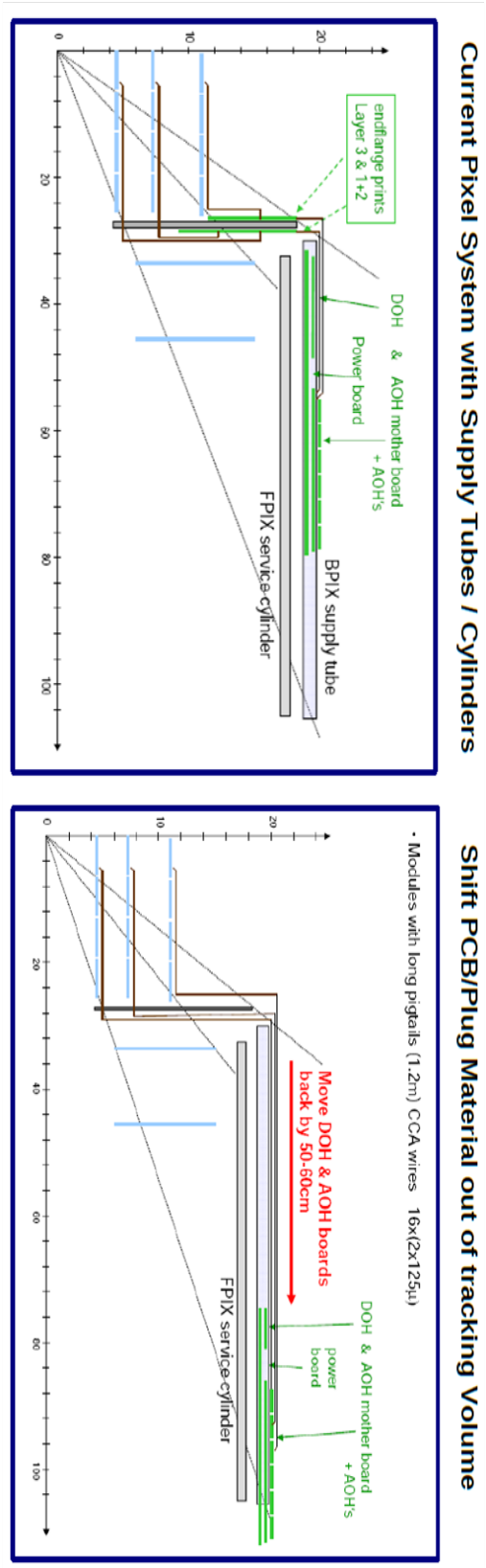

Figure 2–14: Changes in cabling and elimination of the end flange PCBs.

CHAPTER 3
DIGITAL ELECTRONICS

In this work I have made use of digital electronic logic circuits; for this reason, this chapter is an overview of some of the fundamentals involved in this technology. The components studied in this research were built of logic gates and these are presented in this chapter in order to understand how they will form the readout components of the pixel detector.

3.1 Digital signal

A signal is a function of one or more independent variables that contain information about the behavior and nature of some physical phenomenon [20]. An electric signal is based on the behavior of electrons in a medium, and it can be analog or digital. A digital signal is represented by a sequence of discrete numbers. In digital electronics, these signals are currents or voltages which take just two states. These states should be stable and are determined by two different voltage or current values; the most common used is voltage. In positive binary logic; for high voltage level, the state is defined as on, true, up, 1, or voltage. The other state is defined as off, false, down, 0, or no voltage [21].

Some parameters of the signals are amplitude, pulse width, risetime, fall time, and period. The amplitude is the maximum value taken by the signal whether voltage or current (usually voltage). The pulse width is the time during which the signal is 1. The rise and fall time are the time that the signal takes to reach the maximum or minimum voltage value respectively; the period is the time in which the signal repeats itself.

3.2 CMOS Technology

The complementary metal-oxide semiconductor (CMOS) technology is one of the most used to construct integrated circuits. This technology uses NMOS and PMOS transistors, also called nMOSFET or pMOSFET (MOSFET are acronym of Metal Oxide

Semiconductor Field Effect Transistor). The p and n transistors have 4 terminals which are bulk (B), source (S), drain (D), and gate (G). Both transistor types are built up from a p-substrate in which is grown an n-well (n–type substrate) for getting the PMOS (Figure 3–1).

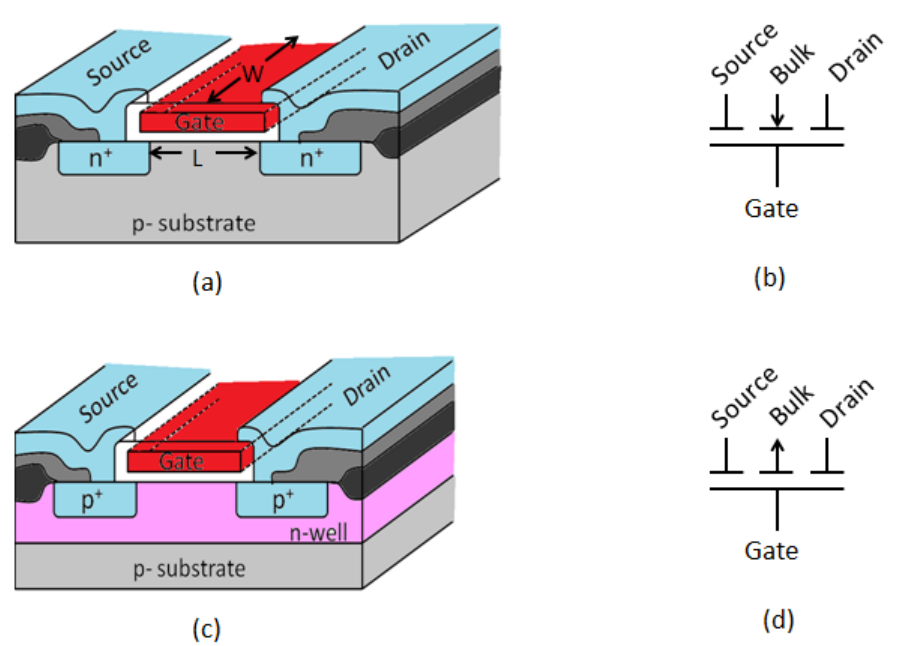

Figure 3–1: Cross-section view of an NMOS (a) and PMOS (c). MOS device symbol for NMOS (b) and PMOS (d) [22, 23].

The NMOS transistors have two n+ regions known as source and drain; while in the PMOS transistor those are formed by p+ regions. Between the source and drain is the gate which is made of aluminum for PMOS and can be aluminum or polycrystalline silicon for NMOS. This is separated from the substrate or well, as the case may be, by a layer of silicon dioxide (SiO2) [22].

This structure (gate, silicon dioxide, and substrate) performs as a capacitor; hence, when a voltage is applied to the gate terminal, there will appear an electric field which attracts electrons to the surface creating a channel (n-type) between the source and drain. The current flows from the drain to the source for NMOS and flows from the source to the drain for PMOS [23].

3.3 Logic Gates

Logic gates are the main components of digital electronic circuits which operate using the principles of Boolean algebra [24]. They have one or more inputs but only one output; among them are the gates described below. This section explains how some logic gates work. These logic gates are able to work when the bulk terminals of the PMOS are connected to a voltage called VDD and the bulk terminals of the NMOS are connected to ground.

3.3.1 Inverter

It is also called NOT gate. This gate produces in its output an opposite signal of the input (Table 3–1). The bulk and the source of the p-type transistor are connected to VDD voltage (state 1 or high), while bulk and the source of the n-type are connected to ground (state 0 or low), these connections can be seen in Figure 3–2. When the input is connected to VDD voltage; the p-type transistor cant create the channel because the voltage between the gate and the bulk is 0. This prevents the current flow through it. For this reason, in the output the voltage is 0 V and the logic state is low. But when the input is connected to 0 V, the voltage between the gate and the source of the p-type transistor is VDD voltage; it creates the channel between the source and the drain and the current can flow through it. The logic state in the output is high.

Table 3–1: Inverter truth table.

in	out
1	0
0	1

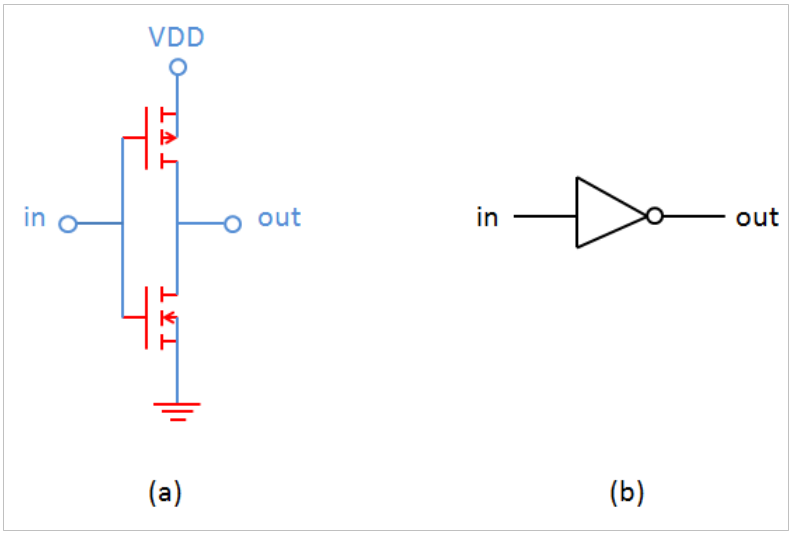

Figure 3–2: Inverter circuit on CMOS technology (a) and symbol (b) [24].

3.3.2 NAND Gate

A NAND gate is a CMOS structure composed of 2 n-type and 2 p-type MOSFETs connected between them. The 2 p-type MOSFETs are connected in parallel one to the other and this structure is connected in series with the 2 n-type MOSFETs (Figure 3–3). The source and bulk of the p-type transistors need to be connected to VDD voltage. To explain the logic operation of this circuit, the inputs in1 and in2 will be connected to VDD or 0 V. There are four possible input states (A through D in the following explanation).

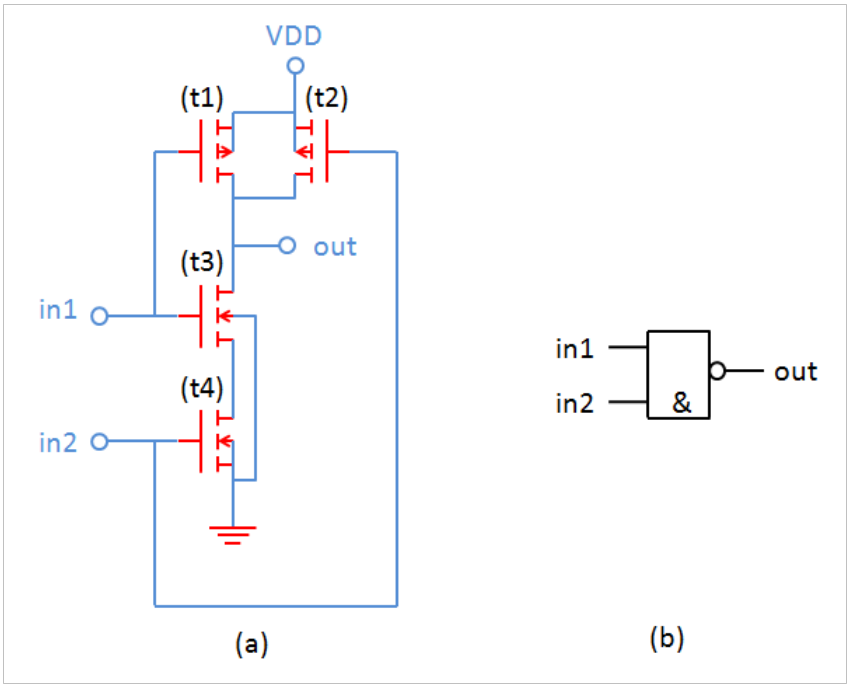

Figure 3–3: NAND gate on CMOS technology using two PMOS in parallel connection (t1 and t2), and two NMOS in serie (t3 and t4) (a); and symbol (b) [24].

State A: in1 = 0 V, in2 = 0 V These imply that in the transistor (t1) has been formed the p-channel and the current flows through it while the transistor (t3) the n-channel isnt created because its gate terminal is at 0 V. The same performance is for transistors (t2) and (t4) because their gate terminals are also connected to 0 V. Therefore, the current passes through the transistors (t1) and (t2) to drain of transistor (t3); accordingly the logic state is 1 or high in the output.

State B: in1 = 0 V, in2 = VDD

The transistors (t1) and (t3) work as in the state A because they are connected to the same voltage source (in1 = 0 V). The difference in this case is that the transistors (t2) and (t4) are connected to the VDD voltage. In the transistor (t2) current doesnt flow because the voltage between the gate and the bulk is 0 V; but in the transistor (t4) the current can flow between the drain and the source because the voltage between the

gate and the bulk is VDD and this creates a channel from the drain to the source. In this case, the circuit has 2 transistors through which current can flow but the transistor (t4) doesnt affect the current in the circuit because the transistor (t3) is placed before it and cuts off the current flow. The current only flows through the transistor (t1) until it gets to the drain of the transistor (t3) and therefore the logic state is 1 or high in the output.

State C: in1 = VDD, in2 = 0 V

The voltage between the gate and the bulk is 0V in the transistor (t1); therefore there isnt any current flow. However, the VDD voltage between the gate and the bulk allows the current to flow through the transistor (t3). The performance of the transistors (t2) and (t4) is the same as for the case of input A. The current passes by the transistors (t2) and (t3) until it gets to the drain of the transistor (t4). In this case the logic state is 1 or high in the output.

State D: in1 = VDD, in2 = VDD

The performance of the transistors (t1) and (t3) is the same as for input C and that of transistors (t2) and (t4) is the same as for input B. The transistors (t3) and (t4) have the channel by which they can pass the current. But in this case the current cant flow through them because the current comes from the sources of the PMOS connected to VDD, and need to pass through the transistors (t1) or (t2) which, in this case, are cutting the current flow. Thus the logic state is 0 or low in the output.

Hence, the truth table is:

Table 3–2: NAND gate truth table.

in1	in2	out
0	0	1
0	1	1
1	0	1
1	1	0

3.3.3 Transmission Gate

In some logic circuits there is a need for a third logical state. An example is an output point where the output desired might come sometimes from one circuit and under some other circumstances from a different circuit. Therefore one wants to have both circuits be connected to the same point but be able to enable or disable the output from each of the circuits in such a way that only one is enabled at any instance in time. When one of these circuits is disabled, its output is neither 0 nor 1 but rather in a state we will call Hi Z for high impedance. A transmission gate controls the flow of a logic signal by either passing it when it is enabled or stopping it when it is disabled.

This gate is made with 2 transistors (one is p-type and the other one is n-type) interconnected (Figure 3–4). The source of the p-type transistor is connected to the drain of the n-type transistor, and the drain of the p-type transistor is connected to the source of the n-type transistor. The bulk of the n-type and p-type transistors are connected to the ground and VDD voltage respectively. The gate terminals are connected to the Vp source for the p-type transistor and Vn source for the n-type transistor. The Vp source and the Vn source are always the opposite of each other. The performance

of the transmission gate is as follows: When the input (in) is connected to the power supply, the current flows through the two transistors and then gets to the output. The current flow through the transistors varies according the Vn and Vp voltages. When the Vn = VDD and Vp = 0 V, both transistors will have their channel formed; therefore, if the input is 1 the output will be 1 also, else for input 0 the output will be 0. When the Vn = 0 V and Vp = VDD, neither transistor can create the channel and the circuit will be open.

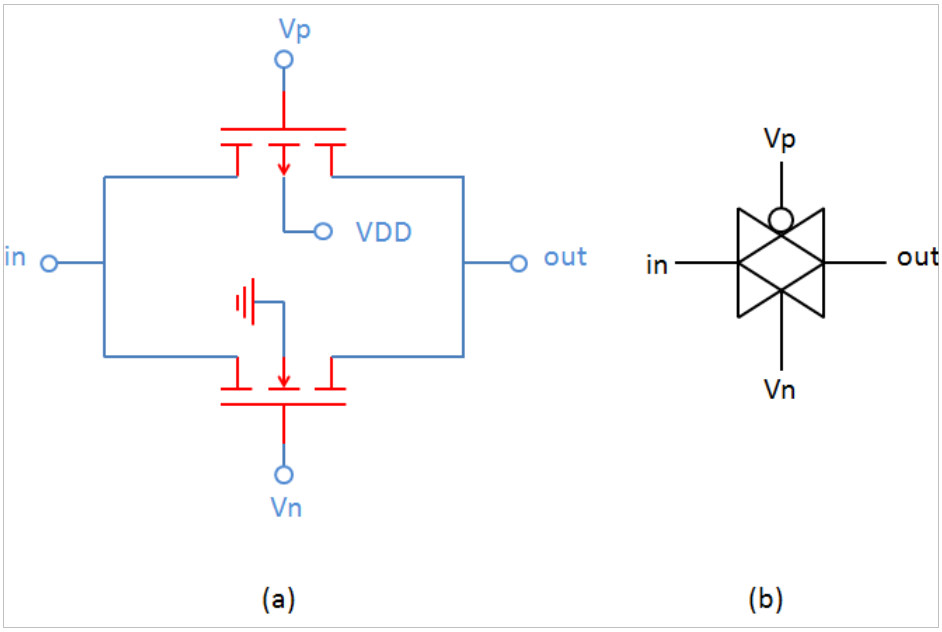

Figure 3–4: Transmission gate on CMOS technology using a NMOS and a PMOS transistors (a), and symbol (b).

The truth table for the transmission gate is:

Table 3–3: NAND gate truth table.

in	1	0	1	0
Vp	0	0	1	1
Vn	1	1	0	0
out	1	0	Hi Z	Hi Z

3.3.4 Tri state inverter buffer

This is a CMOS structure composed of 2 n-type and 2 p-type MOSFETs connected among them. The 2 NMOS and 2 PMOS are connected in series (Figure 3–5). This circuit works as an inverter controlled by the voltage applied to Cp and Cn terminals which are the opposites of each other.

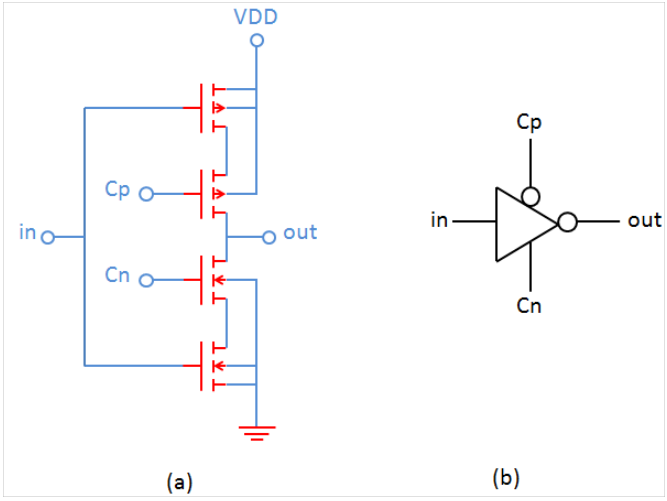

Figure 3–5: Tri state inverter buffer on CMOS technology built with two NMOS and two PMOS are connected in series (a), and symbol (b).

When Cp = 0 V and Cn = VDD, the gate is enabled to transfer the input signal. If in = 0, the channel is created in the first PMOS transistor and the current passes through the two PMOS transistors to get to the drain of the first NMOS getting "high" in the output. For in = 1, the last NMOS transistor will create its n-channel and the current can flow through it; however, the output will be "low" because the current flows from the first PMOS but this doesnt have its channel created. When Cp = VDD and Cn = 0 V, the transistors do not have the channels and the output is a higher impedance. Its truth table is shown in Table 3–4 :

Table 3–4: Tri state inverter truth table.

in	1	0	1	0
Cp	0	0	1	1
Vn	1	1	0	0
out	0	1	Hi Z	Hi Z

3.4 D flip-flop

Flip-flops are used to build sequential logic circuits, its symbol is shown in Figure 3–6. A flip-flop stores a bit for a short time and is made up of logic gates. The flip-flop has two parts: one is called master and the other one is called slave. The D flip-flop has: (1) an input D where the signal enters; (2) two clock inputs, and (3) two outputs which are the expected output, Q, and its inverse, _Q. The flip-flop needs two clock signals (*clk* and _clk are represented by a triangle inside the flip-flop box) to control the reading and storage of the input bit. The signal D is read by the clock signals when these are changing, clk from 1 to 0 (falling edge of the clk) and _clk from 0 to 1 (rising edge of

the _clk). Then the D signal is stored in the master part until the clock signals change again. When the clk signal is changing from 0 to 1 (rising edge) and _clk changes from 1 to 0 (falling edge) the signal can pass to the slave part and transfer to output [25]. Thus the input is stored during the time that the clk is at 0.

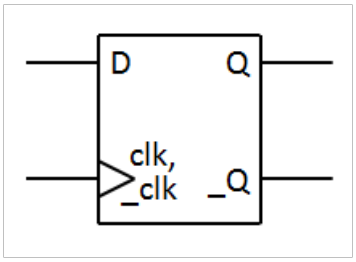

Figure 3–6: D flip-flop symbol, where D, clk, and _clk are inputs; and Q and _Q are outputs.

3.5 Metastability

Metastability occurs when the flip-flop cant read the input signal properly. At the time when the clock was reading, the input signal value wasnt 0 or 1. Therefore, in the output there will be an undefined signal. Metastability is related to two time parameters called setup time and hold time.

The setup and hold time (t_{su} and t_h) are the time regions before and after the clock edge in which the D signal should be stable [26]. In Case I (Figure 3–7), the signal D is stable before the rising edge of the clock signal and the correct Q is output (state 1). In the case II; the D signal is 0 and is stable in that state after th, getting a state 0 in the output. The case III illustrates the metastability that happens when the D input changes in the time interval delimited by t_{su} and t_h (aperture). The time during which the clock signal transfers the input to the output is named the clock to output delay (t_{co}).

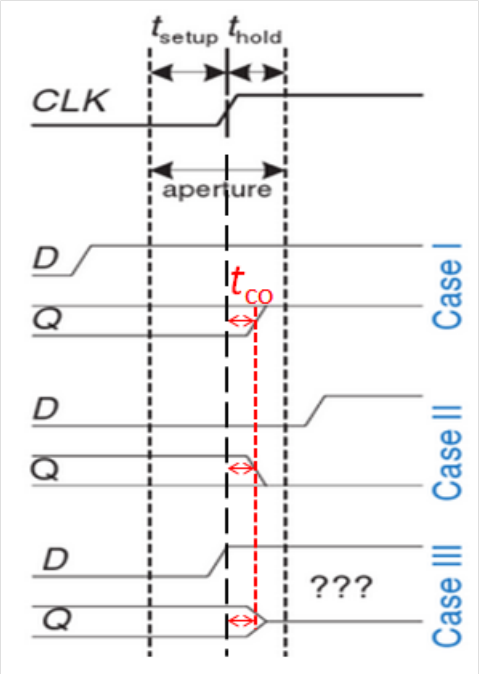

Figure 3–7: Three different cases in which D input signal is stable [26].

CHAPTER 4
VOLTAGE CONTROL OSCILLATOR

In the Control Block and Interface part of the ROC will be the place for the phase-locked loop (PLL) which generates clock signals of 40 MHz, 80 MHz, and 160 MHz. The last frequency is required for the serializer and is obtained by a Voltage Controlled Oscillator (VCO).

4.1 Design

The VCO is an oscillator circuit which can produce square and triangular waveforms. The frequency of the signal that it produces is controlled by an external voltage. [25] The Ring Oscillator is the way the 160 MHz VCO was implemented. The Ring Oscillator (RO) is a circuit composed of an odd number of stages (Figure 4–1). In this case it has 5 stages each built of a NAND gate and a transmission gate (TG). The stages are connected in a chain; the output of the last stage is fed back to the input of the first stage.

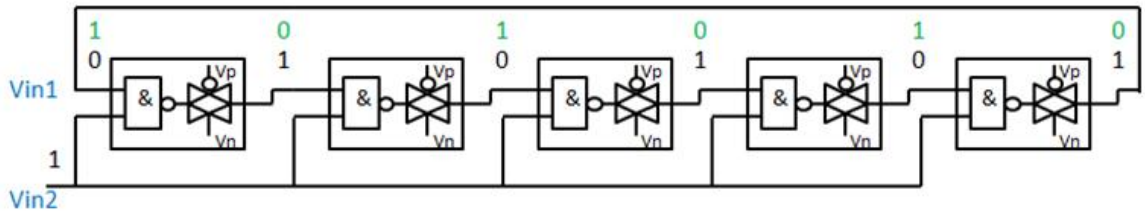

Figure 4–1: The VCO scheme to be used in new ROC design.

The VCO has 4 input control voltages; they are Vin2, Vp, Vn, and VDD where:

- The input Vin2 is connected to a fixed voltage such that it will be the logic state 1. This is one input of the NAND gate while the other input of the NAND gate is connected with the output of the previous stage and can take the logic state 1 or 0.
- Vp and Vn are inputs of the TG and control the output frequency.
- VDD is connected to the power supply which feeds into the source of the p-type transistors of the NAND gates.

The oscillation starts spontaneously. If Vin1 has the logic state 0 at time t0, then the output of the first stage is 1 (Vin2 is always at the logic state 1). The output of the second stage is 0, the output of the third stage is 1, for fourth stage is 0, and finally the fifth stage is 1. (In Figure 4–1 the logic states for this sequence are shown with black numbers). Therefore, when the input Vin1 = 0, the output of the fifth stage is 1. However, it takes some time for this logic sequence to operate. The output of the fifth stage appears at a time t1 > ¿ t0. This output is the input to the first stage. Thus, at time t1, Vin1 changes from 0 to 1. Now the outputs of each of the stages will change to the green numbers in Figure 4–2. The output of the fifth stage will be 0 at time t2 > t1. Since this is equal to Vin1, the starting point has been reproduced and the whole sequence will repeat in time indefinitely. Figure 4.2 is a graph of the VCO output signal as a function of time. It has the characteristics of a clock signal.

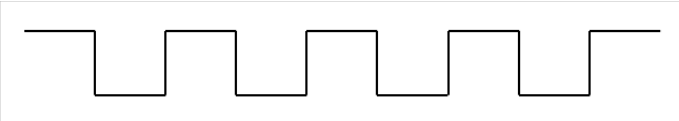

Figure 4–2: VCO output signal.

The frequency of this clock is proportional to the inverse of the propagation delay time (t_{PD} which is the time it takes for the output of one of the stages to change once there has been a change in the input. This time is related to the resistance and

capacitance values ($t_{PD} \sim RC$). The resistance comes mainly from the TG and the capacitance comes from the parasitic capacitance in the real circuit. The relation to the frequency is given by Equation (4.1) where n is the number of stages in the RO.

$$f = \frac{1}{2nt_{PD}} \tag{4.1}$$

4.2 Simulations

The free software Simetrix (SIMetrix-SIMPLIS Intro 5.60) was used to simulate the performance of the Ring Oscillator. This simulator is a version which works with the SIMetrix and SIMPLIS simulators. SIMetrix allows an easy and fast simulation of circuits that contain both digital and analog signals, and SIMPLIS carries out simulations and analysis of switching power systems. The simulations were operated in GUI (graphical user interface) mode. Simetrix (SIMetrix-SIMPLIS Intro 5.60) allowed making a VCO of 5 stages and connecting VDD, Vin2, Vp and Vn inputs to the DC sources. The sizes of the transistors were: width = $3.47\mu m$, length = 280 nm. For an easier data analysis the variables used were Vdiff (differential) and Vcom (common) which are related to the Vp and Vn variables in the following way:

$$V_{diff} = V_p - V_n \tag{4.2}$$

$$V_{com} = \frac{V_p + V_n}{2} \tag{4.3}$$

We were most interested in investigating how the frequency of the output signal changed with the voltage inputs. For this study, some voltages were held fixed: VDD = 2 V, Vin2 = 2 V. Different values for Vp and Vn were studied.

In Figure 4–3, each curve is for a different Vdiff value. The frequencies are maximum for Vcom = 1 V. The frequency peaks are not sharp which is good because the circuit

must have a stable frequency in its output. Figure 4–4 shows the complete range of frequencies that the output signal can have with Vcom = 1 V. The highest frequency is obtained when Vdiff = -2 V.

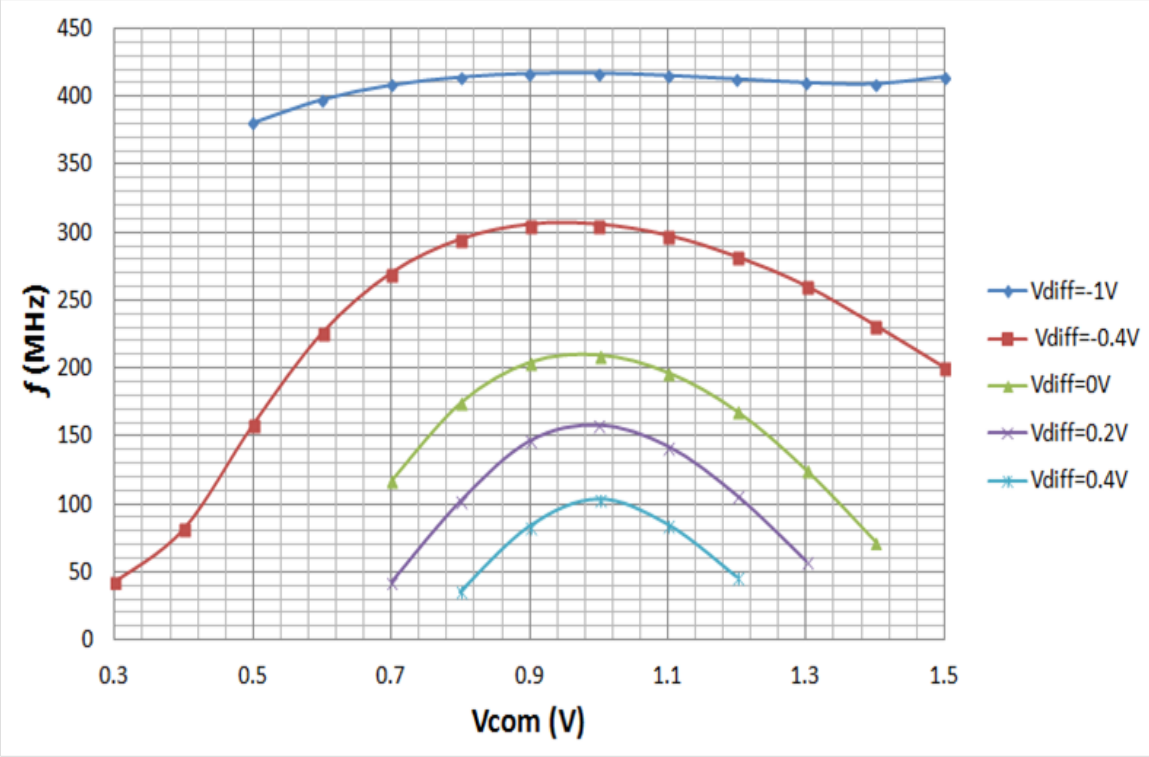

Figure 4–3: The VCO frequencies for different Vdiff and Vcom values, when VDD = 2 V.

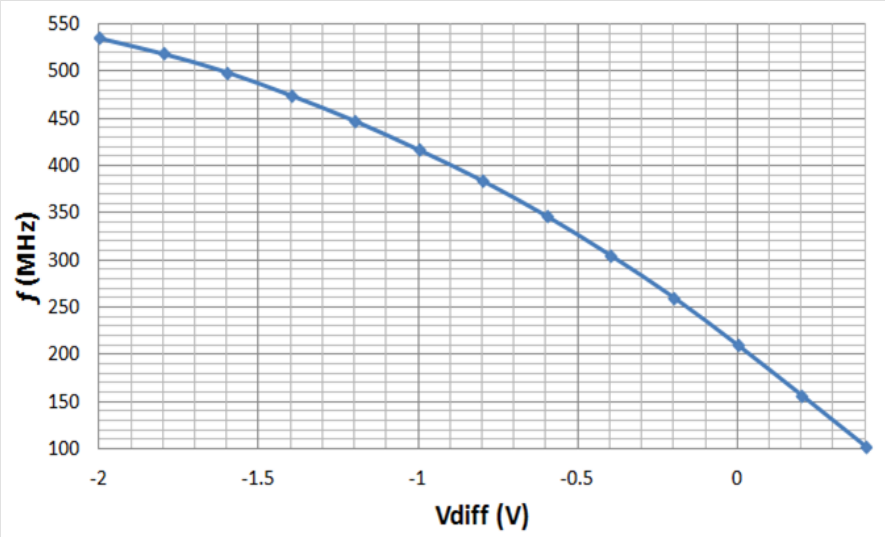

Figure 4–4: The VCO frequencies for different Vdiff values when VDD = 2 V and Vcom = 1 V.

The output frequency desired is 160 MHz. For Vdiff = 0.2 V the simulation predicts it will be 157 MHz, but the simulation is not completely realistic because in it the cables are ideal and the parasitic capacitance is not simulated. This capacitance is due to external components and we do not have a good estimate of its value. In any case, a Vdiff value of 0 V should give a frequency approximately equal to the nominal frequency of 160 MHz in a real circuit.

4.3 Setup of the VCO

The simulated VCO circuit was implemented as part of ICs built by a commercial firm according to our design. A test setup for the VCO was designed and implemented at the PSI laboratory. In the design of the test setup the following things were considered: (1) the location of the VCOs on the chip (IC), (2) the printed circuit board (PCB) design to be used in connecting to the VCO, (3) the structure of the connection pads, (4) the effect of the input and output wires.

4.3.1 First step: To localize the VCO on the chip

In the PSI_CDG001 chip, there were four test structures called: link_system, link_driver, ADC and sc_supply. The VCOs were in the link_system; one VCO with 5 stages and the other one with 7 stages. From the simulations (explained in the previous section), the frequency of 160 MHz is obtained in the output of the VCO with 5 stages.

In Figure 4–5 are marked with circles the pads used to connect to that VCO. Each different color circle is marking a different pad: the blue are the ground (GND), the yellow is Vp (VCO IN-), the green is Vn (VCO IN+), the pink is Vin 2 (VCO LF), the red is VDD, the orange is VDDIO, the purple is _reset and the `par_par` black is the output (VCO CLK).

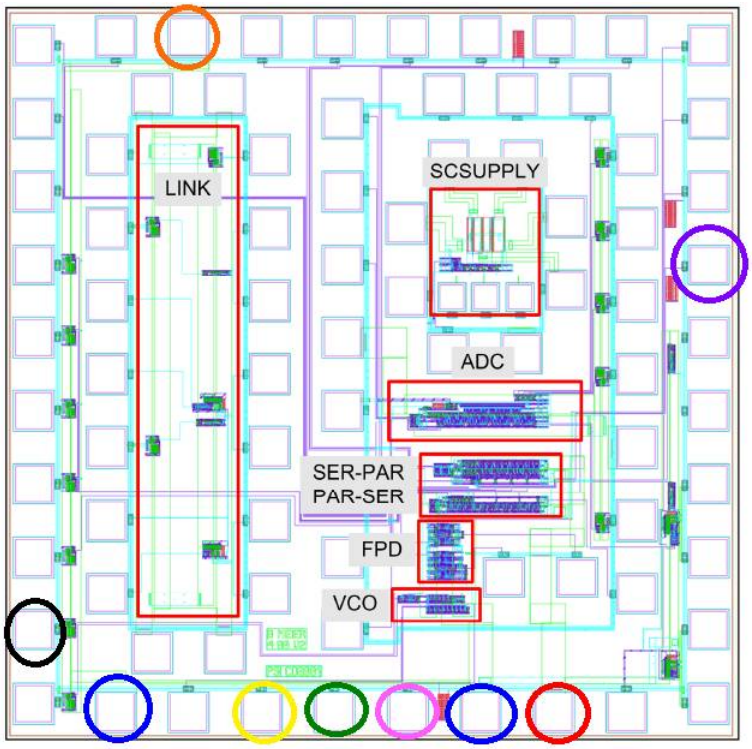

Figure 4–5: PSI_CDG001 chip scheme with different circuit to be tested including the VCO, designed in PSI.

Inkscape software was used to draw the connections on the PCB chosen as shown in Figure 4–6. Once the chips were soldered to the board and the pins where the sources would be connected were affixed, the connections themselves were studied.

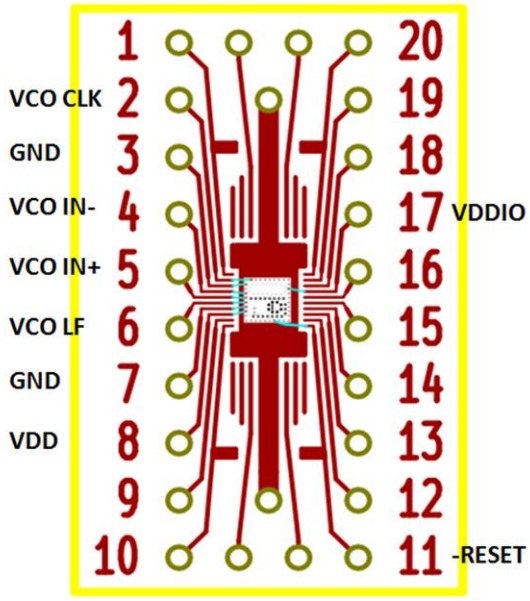

Figure 4–6: Sketch of PSI_CDG001 connected to board. (Board drawn by Silvan Streuli, PSI).

4.3.2 Second step: To study the connections between the chip and power supply

The current between the voltage source and Ring Oscillator is not constant in time even when the power supply is DC (direct current). This can be seen in Figure 4–7 which is a result from the simulation. This is not good because the inductance of the cables will vary the voltage values when the current is not constant. This change in the voltage will affect the frequency of the output signal. For input connections: In an inductor the voltage in its terminals is proportional to the inductance and the rate of change of current with time:

$$V_L = L\frac{\Delta l}{\Delta t} \tag{4.4}$$

In order to get some idea of the current variation from a source in the circuit, we looked at the results of the simulation shown in Figure 4–7. The amplitude of the current oscillations was approximately 75 μA.

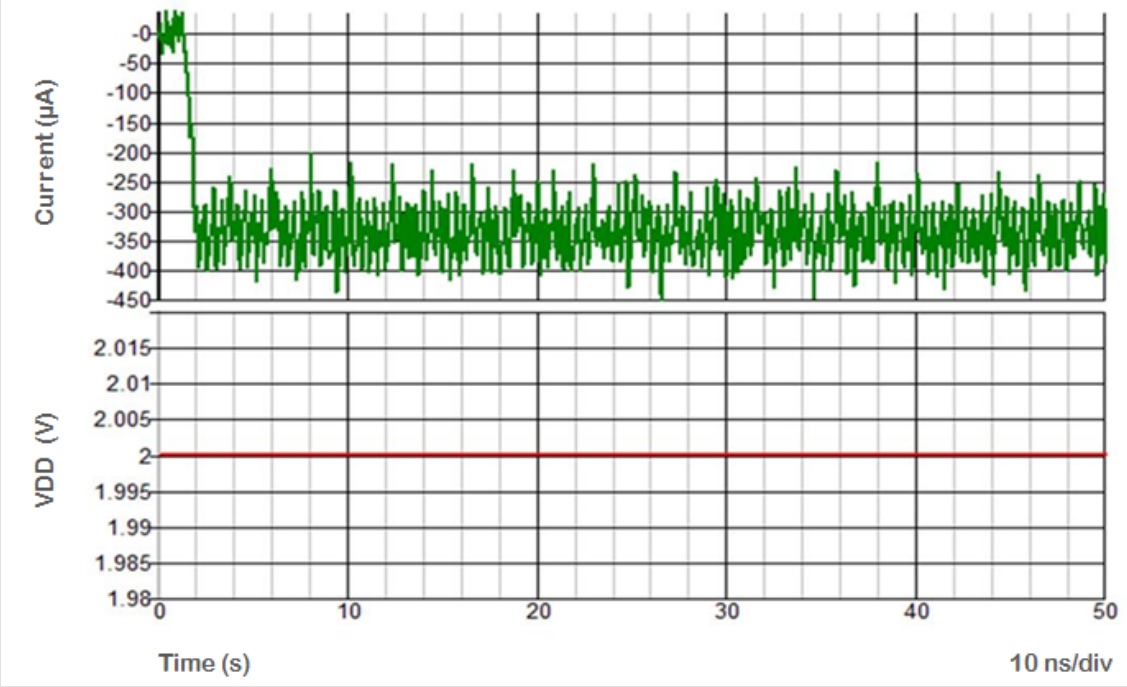

Figure 4–7: Green plot shows the current between source and VCO for a constant voltage represented by the red plot.

The solution to the problem of the cable inductance is to add a capacitor connected to ground. The equivalent circuit for the AC behavior is shown in Figure 4–8 where the cable is represented by a pure inductor and the VCO is represented by an AC current source and a resistor. The power supply can be simulated here by a connection to ground since we will be simulating only the AC behavior. This circuit was simulated for various values of inductance and capacitance and the AC frequency was swept in the range of 1 MHz to 10 GHz. (Of course, we are mainly interested in the behavior at 160

MHz.) We are interested in studying the voltage fluctuations at point I1 in the circuit which corresponds to the voltage that would be applied to the VCO in a real circuit with real cables. The AC current amplitude was set at 75 A. This equivalent circuit turns out to be an RLC parallel circuit which can, of course, be solved analytically. There will be resonance for certain combinations of inductance and capacitance where the voltage oscillations we fear will be maximal. We could just calculate the values of capacitance where such oscillations will occur and make sure we use a capacitor that puts us away from resonance. However, the simulation gives us a convenient and easy way of generating detailed graphs of the behavior of this circuit for a large range of frequencies and a variety of inductance, capacitance combinations.

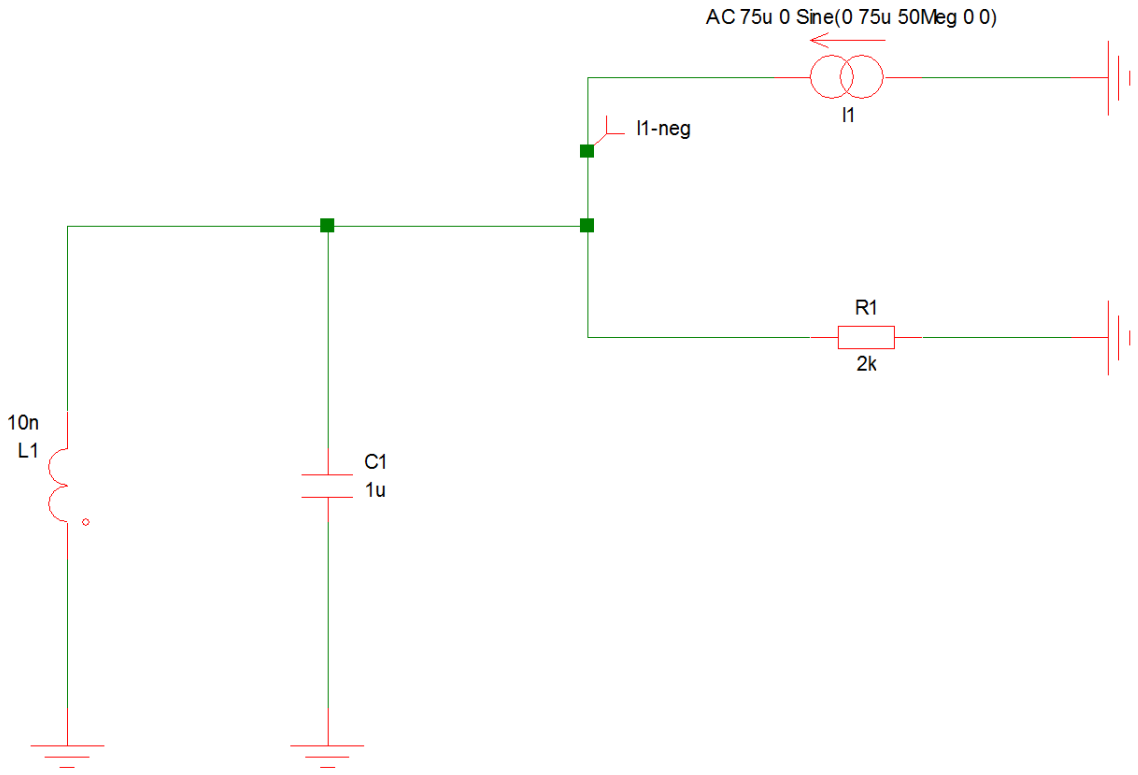

Figure 4–8: AC equivalent circuit for the connection to the power supply.

The results are shown in Figures 4–9 and 4–10. The variable plotted in the vertical axis is the amplitude of the AC voltage oscillations at point I1. In Figure 4–9, the capacitance values were 100 pF (red plot), 10 nF (green plot), and 1F (blue plot) while the inductance had a value of 10 nH. For the plots in Figure 4–10, the capacitance was kept at 1F while the inductance values were 1 pH, 100 pH, and 10 nH. The influence of these inductances are shown by the red, green, and blue plots, respectively.

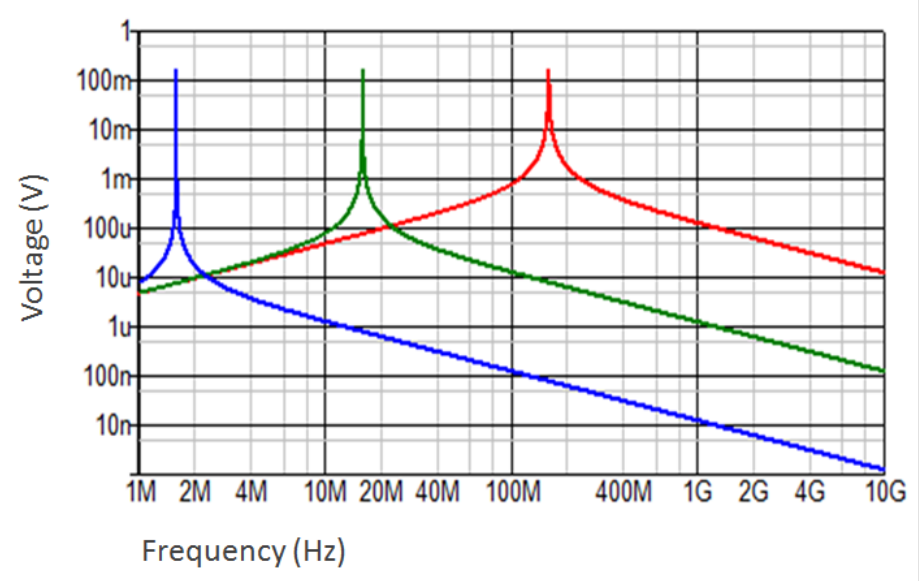

Figure 4–9: Voltage fluctuations as a function of frequency for a cable with 10 nH inductance. Each curve is for a connecting a different size capacitor in parallel. 100 pF (red), 10 nF (green), 1 F (blue).

We see that there are certain combinations of inductance/capacitance that do give us a peak near our operating frequency (red curves) but these are very sharp peaks. In Figure 4–10 we observed, for a cable inductance of 10 nH, voltage fluctuations in the order of 10 V or less at our operating frequency if the capacitor is chosen as 10 nF or larger. The data shown in Figure 4–10 the oscillation voltage never exceeds 100 nV even for a very low inductance value of 100 pH and the inductance would have to be

as unrealistically small as 1 pH in order for the resonance to occur near our operating frequency. In fact, although it is impossible to calculate a precise value for the inductance in the real circuit because it depends on the details of the connections, we can obtain an estimate for a straight cable of the appropriate diameter and length by using an approximate formula [28]. The estimated inductance is 200 nH just for the cable with a linear dependence on the length and a logarithmic dependence on the diameter. The rest of the connection scheme will add to this value. We conclude that a 1 F capacitor will keep us away from resonance with a large safety factor.

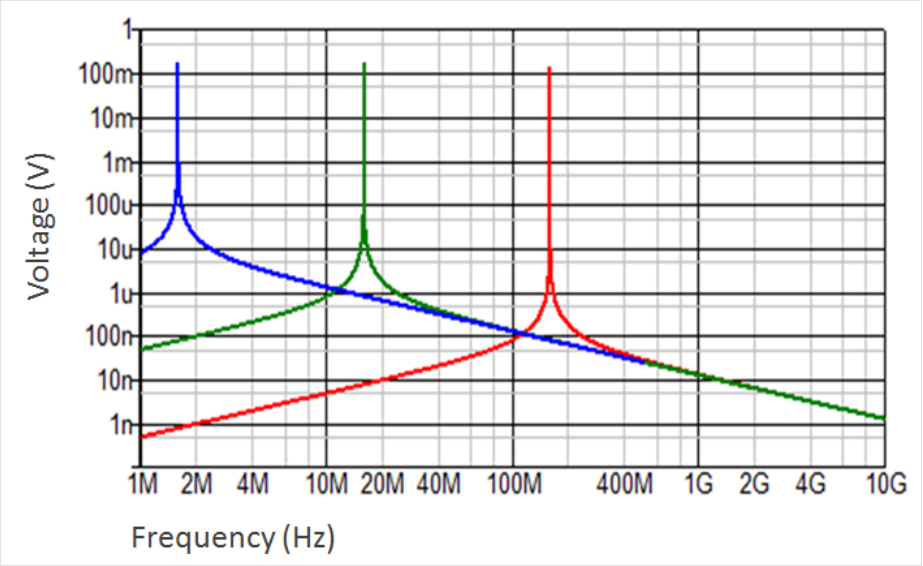

Figure 4–10: Voltage fluctuations as a function of frequency when adding a 1 F capacitor in parallel to the connecting cable. Each curve is for a different cable inductance. 1 pH (red), 100 pH (green), 10 nH (blue).

For output connections: For a maximum signal transfer, the receiver must have in its input a resistance of the same value as the impedance of the cable. The output cables have 50 of resistance so the same value has to be set in the input terminal of the oscilloscope.

4.3.3 Third step: To build the setup

Capacitors of 1 F were connected to the VCO IN- , VCO IN+, VCO LF, VDD and VDDIO input cables to keep a stable voltage. Two power supplies were used to feed the circuit. VDD and VDDIO were connected to 2 V and VCO LF, (_RESET) were connected to ground. VCO IN+ and VCO IN- were connected to a variable voltage source. For these measurements was used a 3 GHz oscilloscope which for each measurement gives the average of 15 103 data.

4.4 Results of the measurements

4.4.1 Measurement of the unirradiated chips

The chips were tested before they were irradiated in order to be sure that they work properly. The measured frequency curves of the chips (Figure 4–11) are similar to the simulation curve. The measured frequencies are somewhat smaller than the values predicted by the simulation because the parasitic capacitance is not simulated; however, the difference is not large.

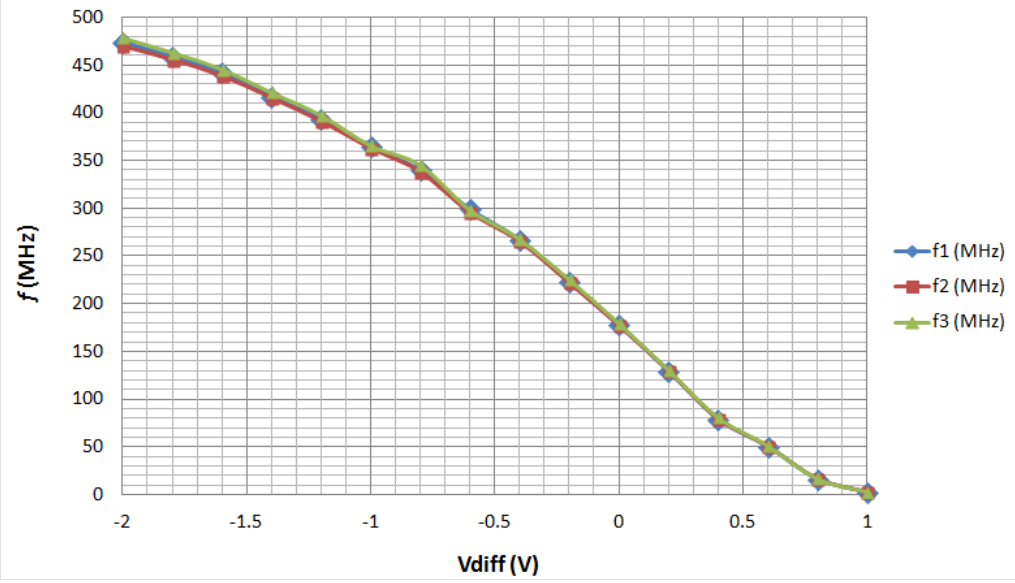

Figure 4–11: Frequencies in unirradiated chips for Vcom = 1 V and VDD = 2 V.

The operation frequency is obtained with Vcom = 1 V and a Vdiff value near 0 V. Actually, for Vdiff = 0 V the test chips ran at 178 MHz on average with some chip-to-chip variation (standard deviation for three samples at Vdiff = 0 were 0.21 MHz, 0.37 MHz, and 0.22 MHz). In the real system the frequency will be controlled to get 160 MHz by adjusting the control voltages. Meanwhile, in this work for simplicity we take Vdiff = 0 V as the operating value.

4.4.2 Measurement of irradiated chips

The three samples were irradiated with ^{60}Co. They received 10 doses of 5 Mrad (50 KGy) each. The total dose received by chips was 50 Mrad which corresponds to 1.5 x $10^{15} n_{eq}/cm^2$. This is somewhat higher than the total irradiation expected at the innermost pixel barrel layer during all of phase I. After each irradiation, the chips were tested and kept at room temperature until the next dose. Figure 4–12 shows the average frequencies measured in the 3 test chips for each dose and the first data point (0 Mrad) is for the unirradiated samples. No error bars are shown in this graph since, for all points, the standard deviations were less than 1.0 MHz. Most of the points lie on a smooth curve except for the second and third. The frequencies for those points are believed to be lower due to a problem with the setup connections which was fixed for the fourth point onwards. For the tenth dose, the average frequency was 147 MHz which is not far from the required operation frequency. These results show that the VCO will work after receiving 50 Mrad of irradiation and will keep sending the correct clock signal to the serializer.

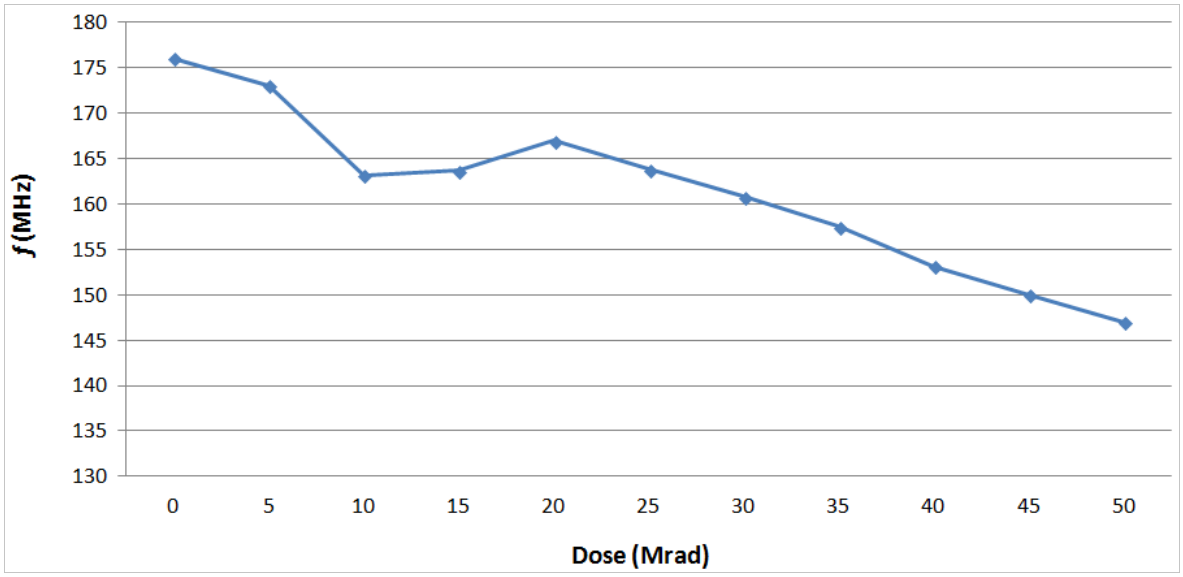

Figure 4–12: Average operation frequency for 3 irradiated test chips (VDD = 2 V, Vcom = 1 V, Vdiff = 0 V.

CHAPTER 5
SERIALIZER

The necessity to achieve a fast readout of 160 Mbit/s out of the ROC requires the use of a serializer. This circuit changes the frequency of the data signal from 40 MHz to 160 MHz and converts 4 parallel bits to 4 serialized bits. The signal of each parallel bit has a period of 25 ns while the 4 serialized bits will make up a signal of 160 MHz. The serializer will be placed in the Control and Interface Block (the last part of the readout system in the ROC) and there will be another serializer in the TBM. The serializer in the ROC will change the frequency of the pixel data which are the pulse height and pixel address, while the serializer in the TBM will change the frequency of the header and trailer data.

5.1 Design

The serializer has 4 inputs each receiving one bit simultaneously. These bits need to be stored temporarily until they are output in sequence. Flip-flops will be used as the data storage elements. The serializer also needs a circuit to control the data transmission. This circuit will control the input of the data to each storage flip-flop. In the output there will be an en-flip-flop with an input "en" synchronized with the data storage into the flip-flops.

The serializer needs two types of flip-flops. D flip-flops will be used for the data storage and the flip-flops that control the sending of the data will be built with an adapter logic circuit added to a D flip-flop to make a special flip-flop structure.

The serializer is arranged as follows:

- Storage Structure: Four D flip-flops store the 4 bits (one bit in each flip-flop) at the same time. These D flip-flops (block 2 in Figure 5–2) need to be connected in series. In

this way they can pass the sequentialized data. Each flip-flop has a data input arranged in parallel with the others. (See Figure 5–1).

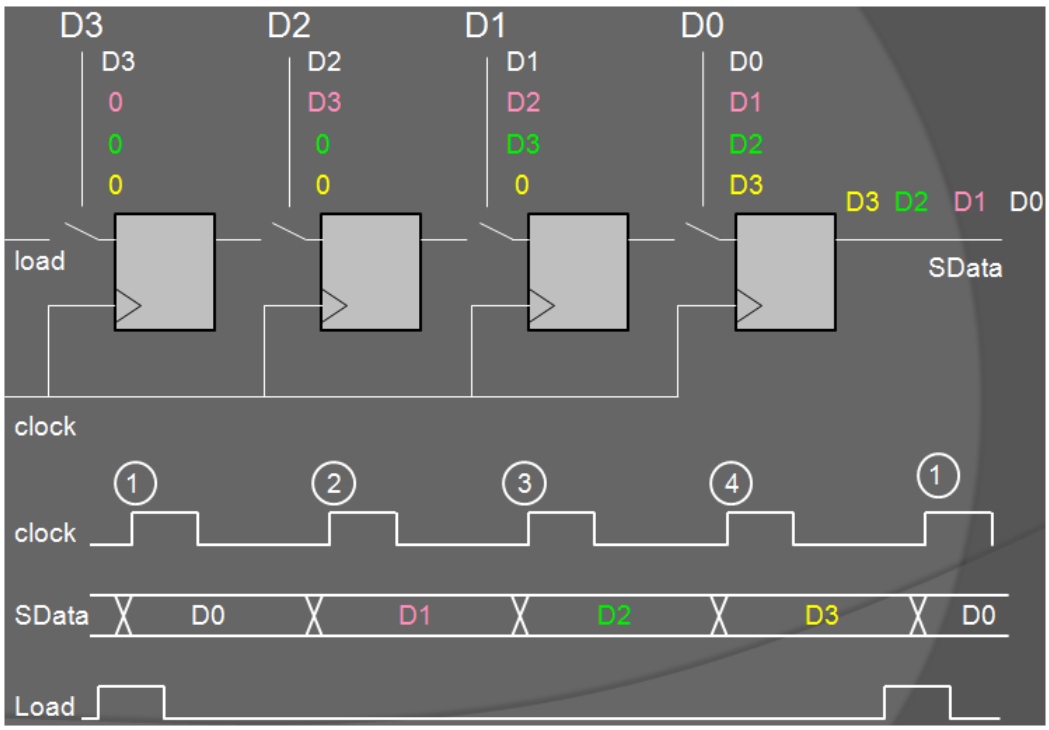

Figure 5–1: Reading system for 4-bits.

• Control Structure: The data will be read out of the serializer once per serclk pulse at 160 MHz, i.e., every 6.25 ns, but it will be input to the serializer only once every 25 ns. In other words, there will be four output cycles for every input cycle. At every serclk pulse the storage D flip-flops will either input data or pass the data to the next D flip-flop. Every storage D flip-flop has an attached circuit (block 4 in Figure 5–2) which controls whether the flip-flop will input data or pass it based on the state of the load line. The load line runs at 40MHz.

Another part of the control structure is that formed by two D flip-flops and a logic gate (upper left hand part of Figure 5–2). This structure generates the load signal. The output of the first flip-flop is connected to an input of the logic gate while the other input of the logic gate and the input of this first flip-flop are connected to the parclk signal (the 40 MHz clock). The output of the logic gate is the ld signal which is transferred to the other flip-flop. The load signal is in the output of this last flip-flop. This signal needs to have a period of 25 ns and a width of 6.25 ns. The circuit designed achieves these goals. The serclk input to the flip-flops is the 160 MHz clock.

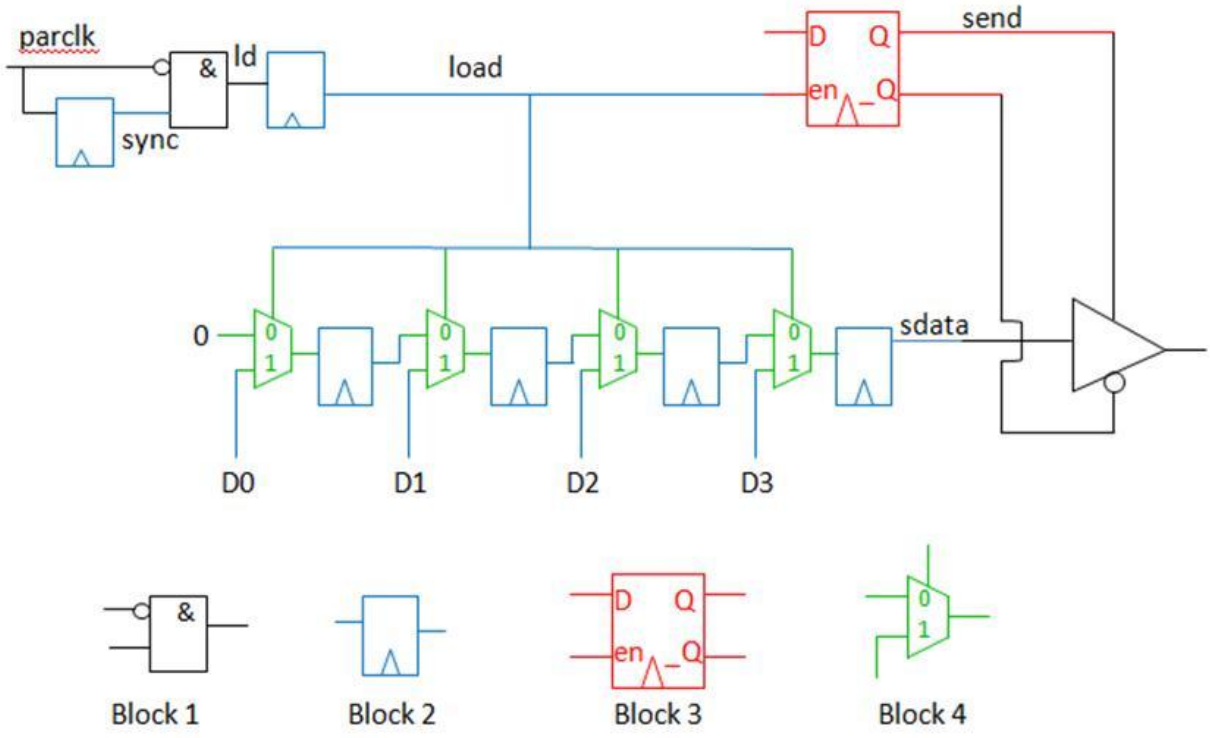

Figure 5–2: Serializer components. The triangles in the flip-flops are the serclk and _serclk inputs.

The third part of the control structure is an en-flip-flop (block 3 in Figure 5–2) that controls the data output from the serializer. The name comes from the fact that it has an enable input. The "en" input is the load signal which will be used to determine the start of the output process and the outputs Q and _Q need to have a width of 25ns which is the time it will take to output four data bits. Q and _Q are connected to a buffer for controlling the data output. The output should only occur when a "write" signal has been received in the D input. This write signal is used so that the serializer outputs its data at the correct time within the module's output sequence when this particular ROC has received the token from the TBM.

5.2 Simulations for each block

Different circuits which work as desired were simulated for each block type in order to get the most optimal design for this serializer. CADENCE is an electronic design automation software which was used to do these simulations. The simulations were done separately for each block. The input signal parameters were known for each block and were some of the specifications for the simulation. These parameters were: (1) delay time, the time before signal rise, (2) risetime, (3) fall time, (4) pulse width, and (5) period. These parameters are defined in Section 3.1. The rise and fall times were set to 0.1 ns for every signal. The delay time specifies the relative timing of the signal. It is defined with respect to the clock signal; delay = 0 corresponds to the midpoint of the clock signal rise. The _clock delay was always set to one half of the clock's period so that this signal was always the opposite of the clock signal. The voltage used for the logic state 1 is 2 V and for the state 0 is 0 V in each signal.

5.2.1 Block 1

There were two alternatives to design this block. The block on the left in Figure 5–3 is built with an AND gate while the block on the right uses a NOR gate. Both gates

have an inverter in one of their inputs. the truth table for both circuits is shown in Table 5–1.

Figure 5–3: Two equivalent gates for the first serializer block.

Table 5–1: Inverter truth table.

A	B	C
1	1	0
1	0	0
0	1	1
0	0	0

The inverters link to the A input in the first circuit and the B input in the second one and could be removed if these inputs were connected to the inverse clock signal (_clk). The AND gate was built using a NAND gate and an inverter (6 transistors) and the output signal had 76 ps for rise time and 112 ps for fall time. In the NOR gate 4 transistors were used and its output signal had 58 ps for rise time and 26 ps for fall time.

5.2.2 Block 2

This block is represented by the light blue block in Figure 5–2. It is a D flip-flop with only one input signal; its other pins correspond to the clocks and the output. For this block two D flip-flop designs were simulated: one called dff and the other called dffr.

The first flip-flop design (dff) uses tri-state inverter buffers and plain inverters placed as shown in Figure 5–4. The input and flow of the D signal by the flip-flop is controlled by the clk and _clk signal of the tri-state inverter buffers. When the clk = 0 and _clk = 1, the tri-state inverter buffers on the ends let pass the signal. But when the clk = 1 and _clk =0, the tri-state inverter buffers that let pass the signal are in the middle of the flip-flop. The tri-state which is between the two inverters is what transfers the D signal to the output.

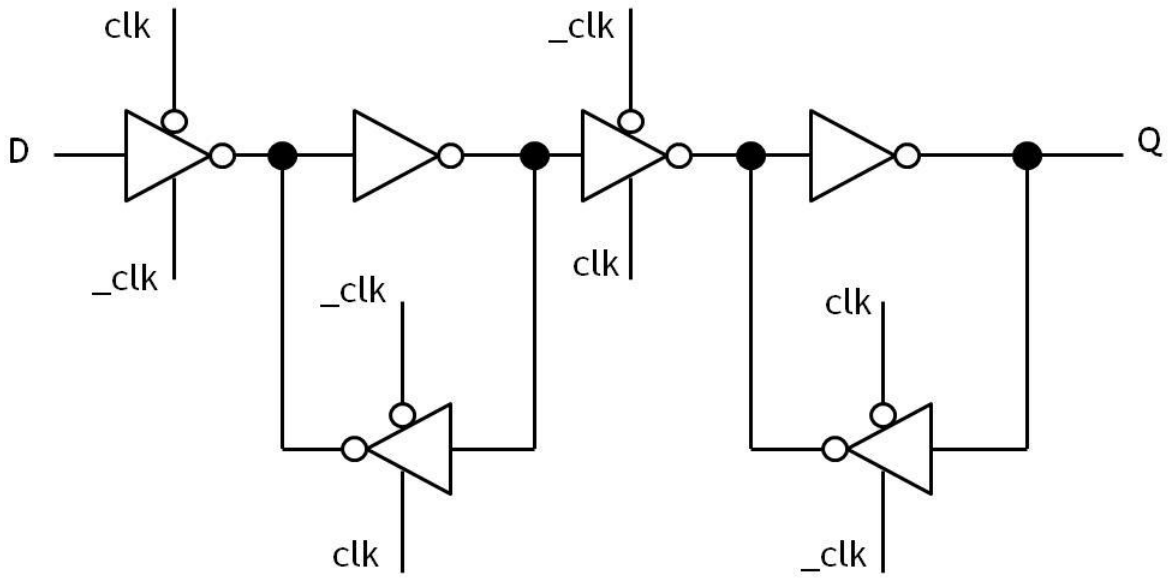

Figure 5–4: D flip-flop design called dff.

The other D flip-flop design (dffr) simulated for block 2 uses a tri-state inverter buffer, plain inverters, NAND gates and transmission gates (see Figure 5–5). The reading of the D signal is controlled by the clocks (clk and _clk) and _reset signals. As in the dff design, the tri-state inverter buffer and the TGs of the far right let pass the signal when the clk = 0 and _clk = 1. When the clk = 1 and _clk = 0, the signal passes through the TGs placed in the middle. Another input of this design is _reset which is linked to one input of each of the NAND gates and the output is 0 (reset) when the _reset is 0.

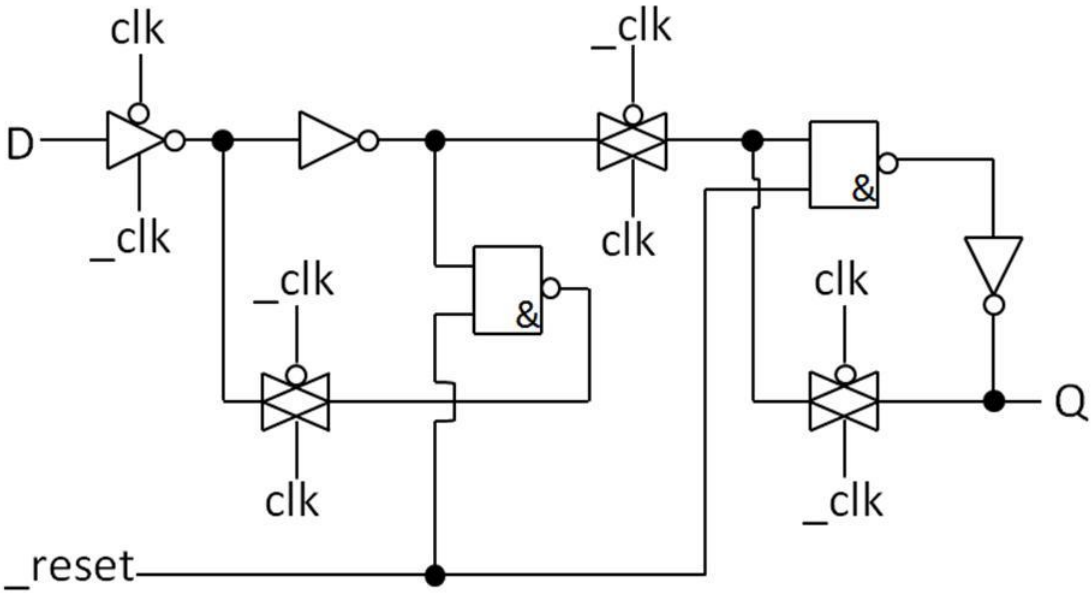

Figure 5–5: D flip-flop design with a _reset input called.

To know if the two D flip-flop designs work, it was necessary to do simulations. The input signal parameters were set as follows: (1) the D input and the clock had a period of 4.2ns, a pulse width of 2ns and rise and fall times of 0.1 ns, (2) the D delay was -0.7 ns. Although the period for this clock does not coincide with the one that will be used in the real serializer, the results from this simulation are still valid when they are interpreted correctly.

The input signals and the output signal obtained from the simulation of the dff are shown in Figure 5–6. The signals are represented by different colors: purple for output Q, black for D, red for clk, and blue for _clk. Looking at Figure 5–6 it is seen that the dff design works correctly; it reads the D signal at the clk rising edge and transfers it to output. (Due to a glitch in the simulation, the first clk pulse is missing.) The output is maintained until the next clk rising edge. During that cycle, the input D goes low but this is not reflected in the output because it does not coincide with the clk rising edge.

At the second clk rising edge, D is back to being high, so the output Q is maintained high.

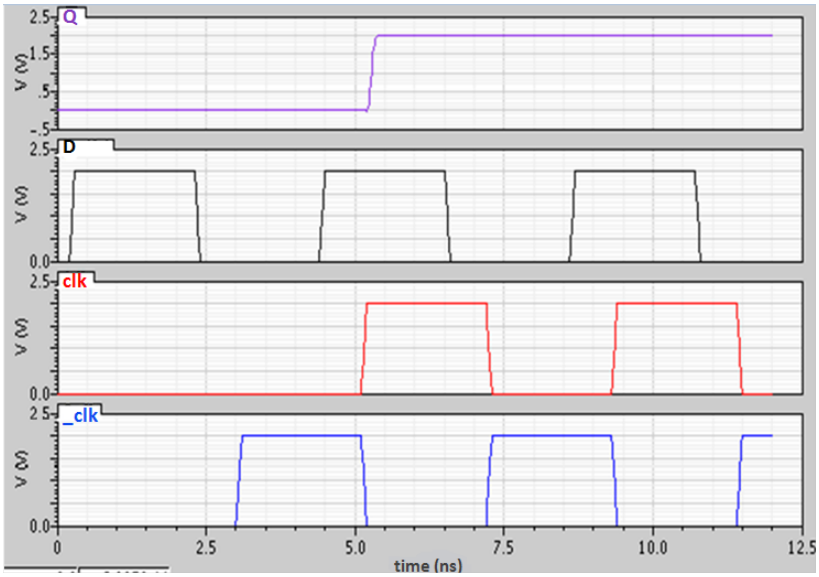

Figure 5–6: Output (Q), Input (D), Clock, and _Clock, and signals for dff design.

For the simulation of the second design (dffr), the same input signals were used and a _reset signal was added. This signal was started in the reset position (_reset = 0). The reset was lifted (_reset = 1) 0.9 ns after a clk rise and kept open during 8ns at which point a second reset was issued and maintained during 2ns. The results of this simulation are shown in Figure 5–7 where the same colors have been used as before and a green graph has been added for the _reset signal.

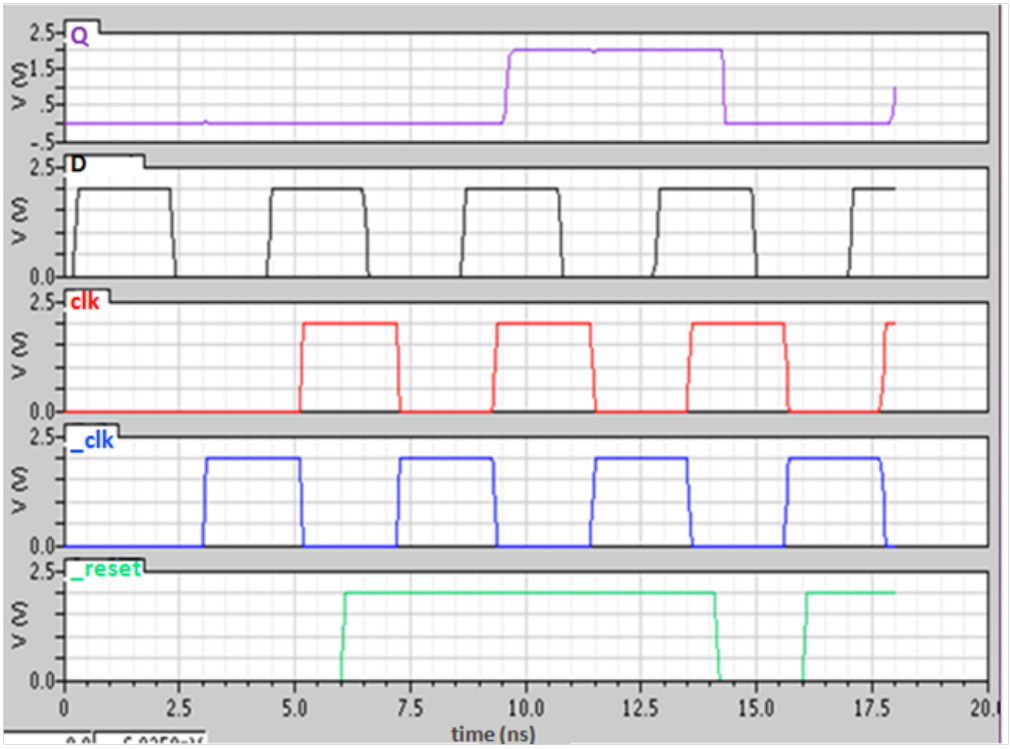

Figure 5–7: Output (Q) Input (D), Clock, _Clock and _Reset signals for dffr design.

This design also works correctly. This time the circuit is in the reset mode when the first clk cycle arrives so the output stays low. The output goes high only at the second clk rising edge when the reset has been lifted. At the third clk rise, the input is high so the output stays high but then the output goes low in the middle of a cycle when the circuit is reset (when _reset goes low). Although both designs were found to be viable, the dffr design was chosen because it is useful to have the capability to reset the flip-flop.

5.2.3 Block 3

Block 3 will use the dffr design with some additional gates that will control the data output. We will study the stability of the circuit, i.e. what are the requirements to be met by the input signal timing parameters in order to achieve stable operation. The enable signal parameters (delay and width) are specified as inputs to the simulation

through the use of two variables: setup time (t_{su}) and hold time (t_h) (Figure 5–8). The delay time is $-t_{su}$ and the pulse width is $t_{su} + t_h - 0.1ns$. In other words, the enable signal arrives t_{su} before the clk signal. It continues high for an interval of $t_h - 0.1$ ns after the rising edge of the clk where 0.1 ns corresponds to the rise and fall time of these signals. In the simulation it is sufficient to generate only one enable pulse. Its timing is taken with respect to the second clk pulse that appears in the graphs. We want to determine the minimum values for t_{su} and th necessary to achieve stable operation.

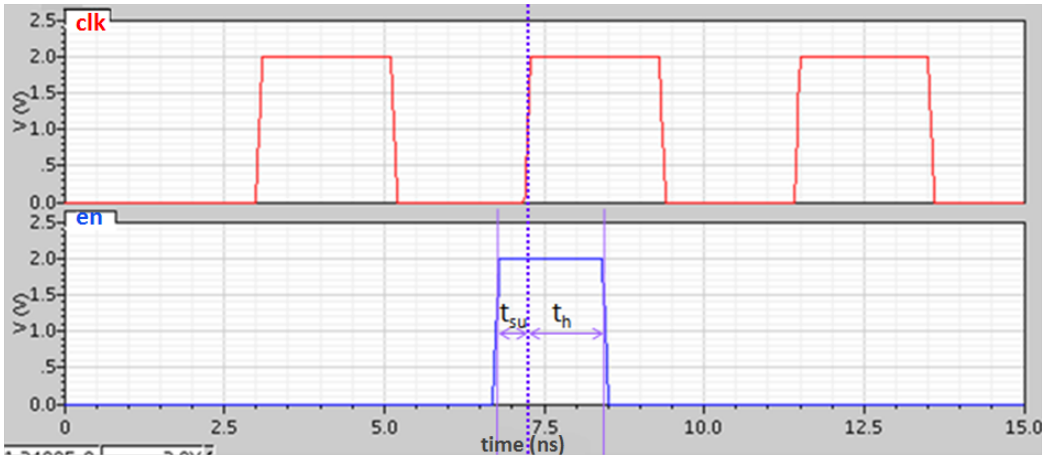

Figure 5–8: Parameters of the enable signal.

The input signals for block 3 are D (write), clock, enable and _reset. The values for the clock parameters used in the simulation were the same as for blocks 1 and 2. The write signal (D) is a very long single pulse that precedes the clock by 1.5ns. The parameters for the enable signal ($t_{su} and t_h$) will be varied. Only one enable pulse will be generated. The effects of the _reset input will be the same as for block 2 since the _reset is fed into the dffr which we have already studied. The _reset signal and its effect are not shown in the results below.

The most important result from the simulation will be the timing parameter of the output signal Q. This is measured as the clock to output delay time (tco).

In the design for Block 3 (Figure 5–9), two transmission gates are connected so that the Cp of one TG is connected to the Cn of the other TG and vice versa. Both these signals are derived from the enable input; one directly and the other after it has gone through an inverter. The D (write) signal will come into the input of the TG that has its Cn connected to the enable. The input of the other TG is connected to the output of the D flip-flop (dffr) used for this design. The outputs of the two TGs are connected to the input of the D flip-flop. The tri-state logic allows this connection of two outputs since only one of the outputs will be enabled at any one time and the other will be in the Hi Z state. This line is called "gena".

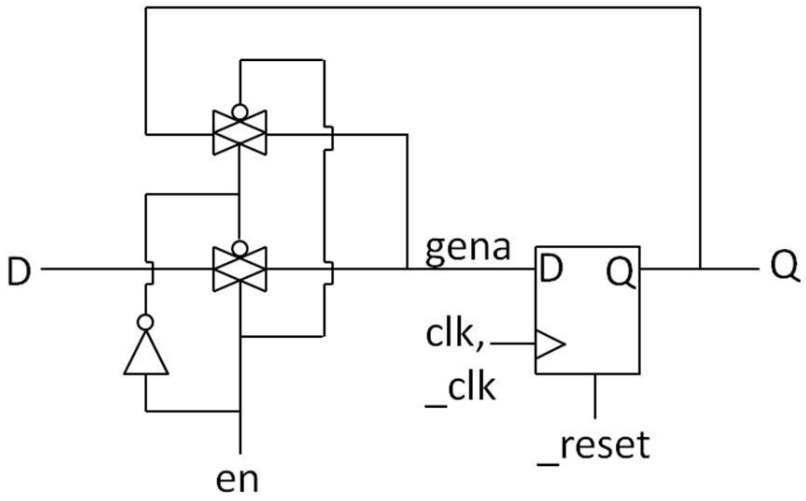

Figure 5–9: Two transmission gates interconnect between them and join to a D flip-flop with a _reset input to make up the block 3 design.

In this design the D signal is read when enable goes to 1 but, when enable goes back to 0, the output is keeping the last reading of the D signal. Figure 5–10 is an example of the signals input to the simulation and the resulting output calculated by the simulation.

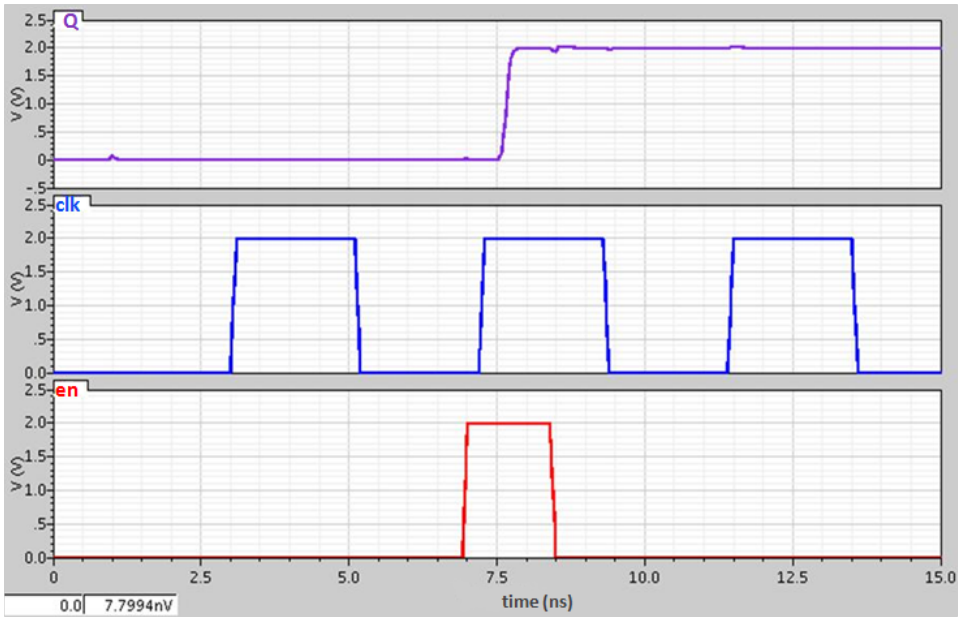

Figure 5–10: Enable (en), clock, and output (Q) signals for block 3.

For a first study, t_{su} was varied while keeping t_h constant at 1.2 ns. The results are shown in Figure 5–11 whith tco as a function of t_{su}. No output was obtained for $t_{su} < 0.29\ ns$, and t_{su} has to be $> 0.5\ ns$ before stability is achieved (constant t_{co}). Thus, 0.5 ns is the minimum setup time required here. The clock to output delay is 0.28 ns.

The next study was to vary th while keeping t_{su} constant at 1.5 ns (Figure 5–12). The conclusion was that the minimum hold time is 0.3 ns as can be seen from the graph.

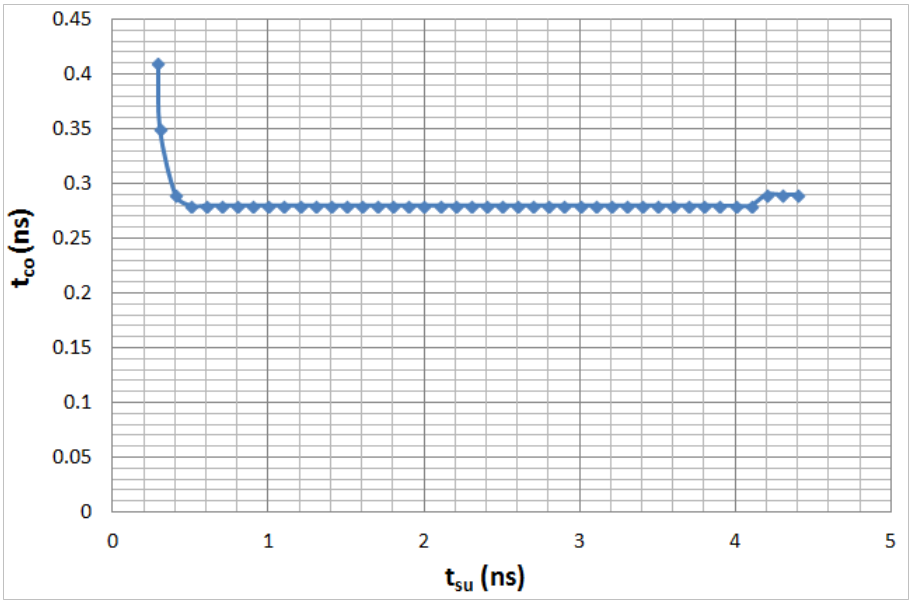

Figure 5–11: t_{co} values for different tsu values with a $t_h = 1.2$ ns.

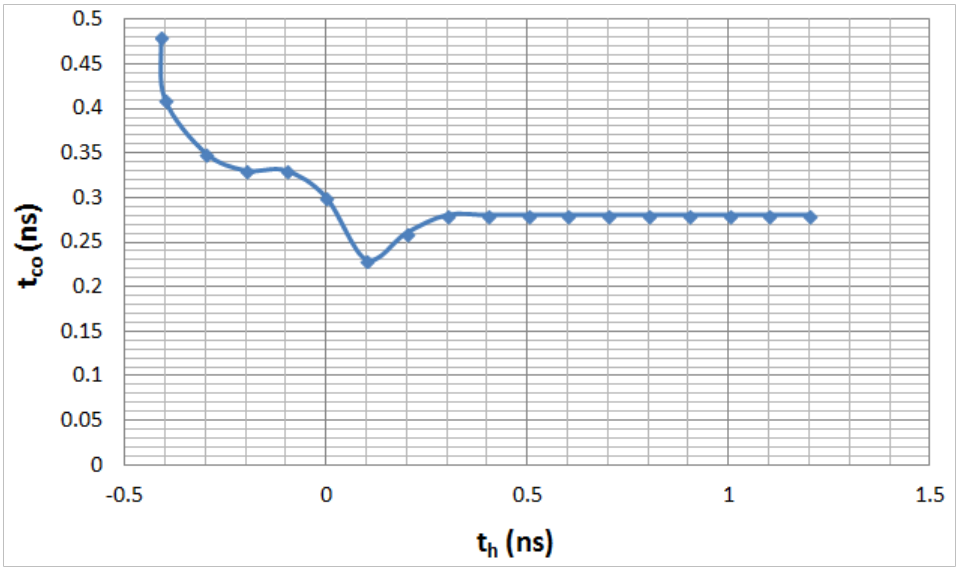

Figure 5–12: t_{co} values for different th values with 1.5 ns of t_{su}.

5.2.4 Block 4

This circuit will either input a data bit from one input line or pass the data in a second input line. It is controlled by a load pulse. In Figure 5–13 which shows the design for this block the two inputs are called in1 and in2. The design consists of two interconnected TGs which receive the input signals. The Cp of one TG is connected to the Cn of the other TG and vice versa. This is the entry point for the load signal. The other interconnection corresponds to _load. The data coming from the previous flip-flop is in in1. The data coming from the double column buffers is in in2. The design assures that when one TG is transferring data the other one is in the Hi Z state.

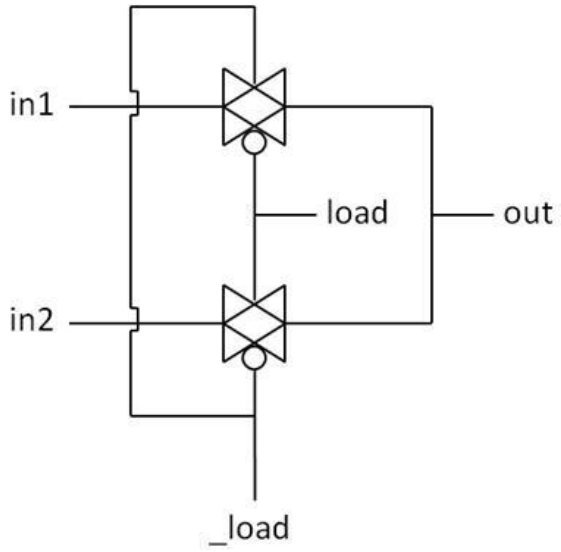

Figure 5–13: Block 4 design using 2 transmission gates interconnected.

5.3 Signal Synchronization Considerations

In studying the separate blocks, it was found that some required certain conditions on the signal times in order to function correctly. However, the blocks are interconnected; the inputs for some come from the outputs from another. Therefore, it is necessary to

determine whether the blocks can work together to make a viable serializer. In particular, one needs to determine whether there is a range of signal parameters of the input signals which will result in successful operation. Figure 5–14 is a graph of all the signal lines but most of these are internal signals generated by the serializer. The only external signals whose parameters can be controlled externally are the parclk, the serclk and the write. The parclk is our standard; the timing of the other two will be defined with respect to the parclk. It is a 40 MHz clock. The frequency of the serclk is fixed at 160 MHz clock but its delay with respect to the parclk can be controlled (by a circuit external to the serializer). This is one of the parameters we wish to study. The timing and width of the write signal can also be controlled externally and those are the other two parameters we will study.

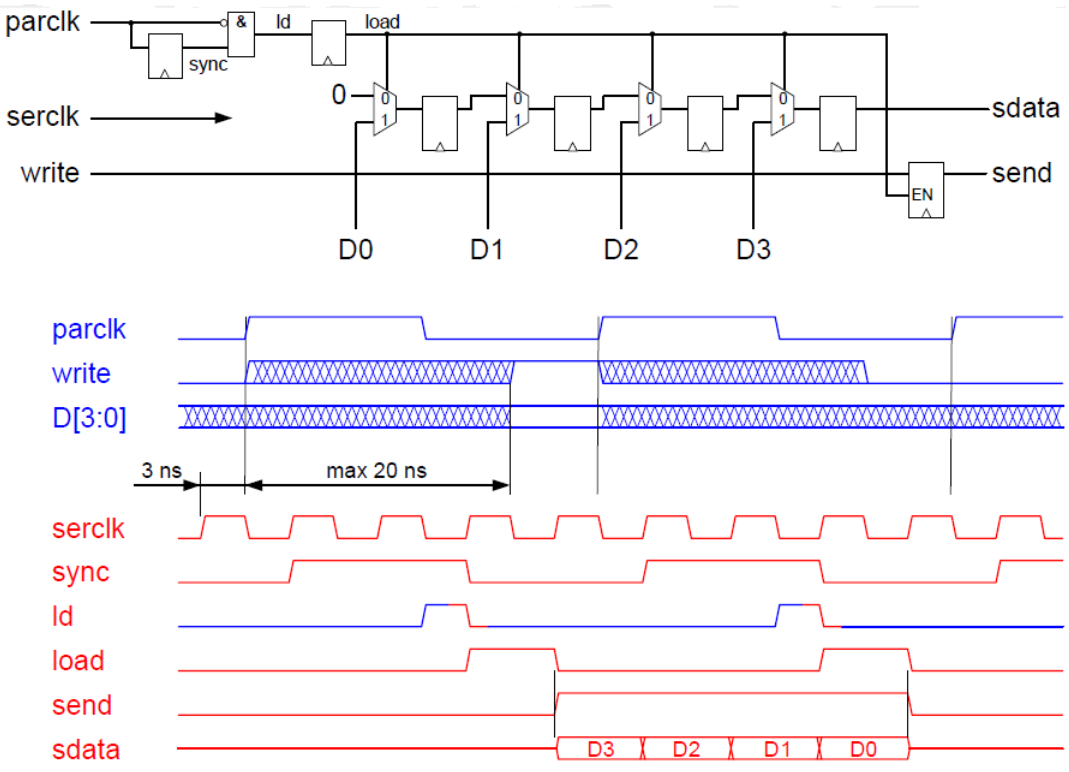

Figure 5–14: Diagram of the serializer and signal involved in its performance.

These studies were done by doing simulations of the performance of the complete serializer for different values of the input signal parameters. The results of the study of the relative timing between the parclk and the serclk are shown in Figure 5–15. For every timing value simulated it was determined whether the serializer output the correct data bit or not. The base synchronization of these two signals occurs when their falling edges coincide (Case 1). The serializer works correctly for that case. The graphs in Figure 5–15 show different cases depicting the relative delay of the parclk with respect to the serclk but equivalent graphs could have been done depicting the relative delay of the serclk with respect to the parclk. The check marks are meant to convey the fact that correct performance is obtained when the parclk is delayed up to 2.69 ns (Case 2) or advanced up to 3.50 ns (Case 4). Any further advance or delay within windows of 60 ps of instability results in a loss of data. If the delay is larger than 2.75 ns the serializer reads the wrong bit (that of the next clock cycle). Advances larger than 3.56 ns fall in an area of stable operation where the correct bit is read.

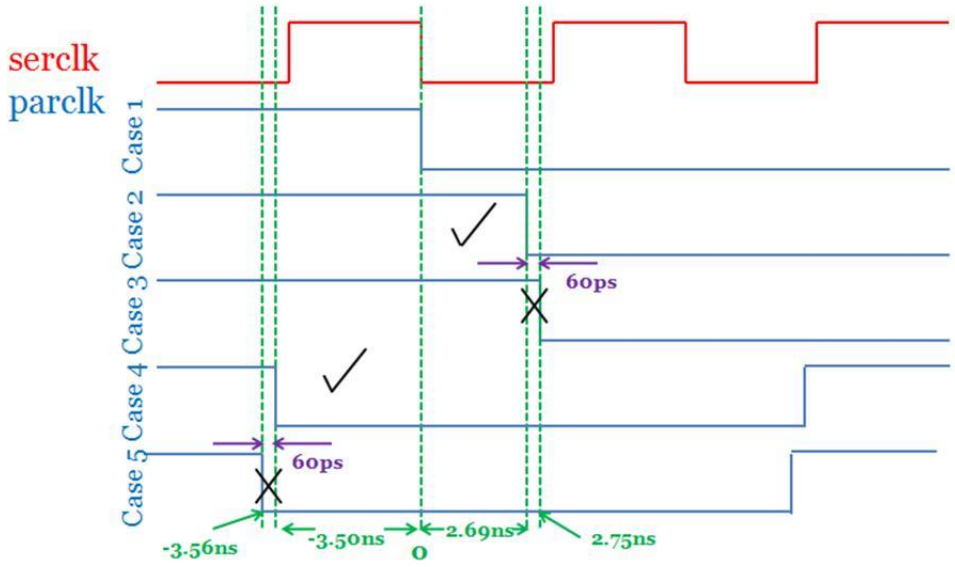

Figure 5–15: Intervals of the operation time for parclk signal in relation to serclk signal for their falling edge.

Figure 5–16 defines the write signal parameters that determine the timing of this signal with respect to the parclk rising edge and also determine its width. Using the simulation it was found that the write signal's rising edge can be set from 2.88 ns to 22.12 ns (t_{su}) before the rising edge of the parclk signal. It's falling edge (t_h) can occur from -3.52 ns to 21.44 ns with respect to the parclk rising edge.

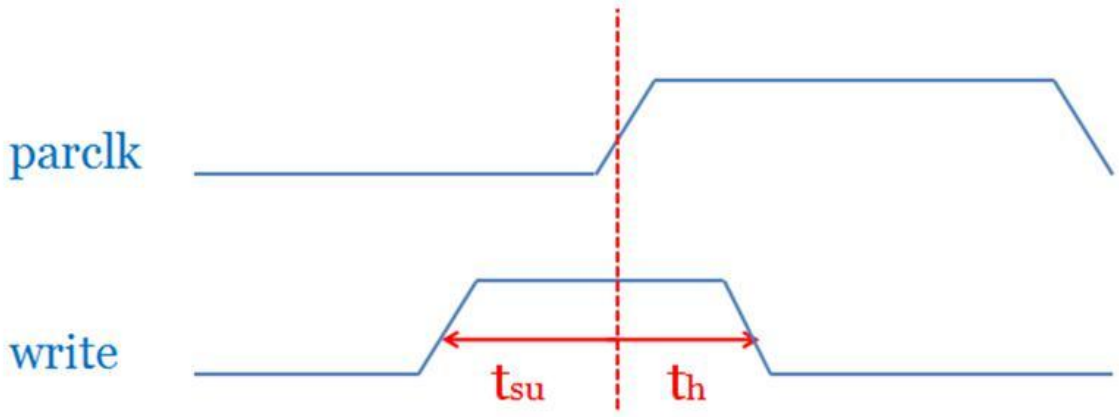

Figure 5–16: Write signal time parameters with respect to the parclk signal rising edge.

CHAPTER 6
CONCLUSIONS AND FUTURE WORK

This work presented the detailed design of two new components for the CMS pixel detector readout system. These components are important for the change to a digital readout at a much higher frequency. The Voltage Control Oscillator (VCO) design was based on a basic structure called a Ring Oscillator while the Serializer circuit design used a number of digital logic circuits and transmission gates. The designs were studied and found to be viable through computer simulations. The VCO design was built as an integrated circuit and tested experimentally. In addition, three VCO test chips were submitted to high levels of radiation to determine their resistance and how long they will be able to perform in the radiation environment of the upgraded LHC accelerator.

The Voltage Control Oscillator was an array of NAND gates and transmission gates in five stages. It was simulated with SIMETRIX software changing the control voltages (Vcom and Vdiff) between 0 V and 2 V while the VDD voltage was set to 2 V. The simulations showed that the desired operating frequency of 160 MHz could be obtained by a judicious choice of control voltages and this was, in fact, confirmed when the design was implemented on an integrated circuit. The test chips were subjected to 10 doses (5 Mrad each) from a ^{60}Co source and were tested after each dose. The chips worked even after 50 Mrad with a small drop in the operating frequency to 147 MHz.

Detailed simulation of the serializer circuit components as separate units and as an integrated circuit not only confirmed the viability of the design but also provided information on the relative timing requirements on the input signals in order for the designs to work properly. These requirements were found to give a large operating range.

This version of the serializer has as its ideal the situation where the serclk and parclk signals are synchronized in their falling edges. In practice it may be easier to produce signals that are synchronized in their rising edges. A continuation to this work could be adjustments to this design so that it may work with signals that are synchronized in their rising edges. The next step in the development of the serializer would be to build it and test its performance in conjunction with the VCO and the new digital ROC.

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