DESIGN OF SINGLE-INDUCTOR MULTIPLE-OUTPUT CONVERTER FOR LOW POWER & HIGH EFFICIENCY APPLICATIONS

By

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May 2015

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This work presents a control architecture for Single Inductor Multiple Output (SIMO) converters applied to low power applications. A functional Power Management Integrated Circuit (PMIC) was designed, simulated, and fabricated, using a 0.8µm BiCMOS technology, to provide three totally independent output voltages by using only one external inductor. The proposed hybrid operation mode, along with the stable non-invasive inductor current controller, allows the system to achieve high efficiencies even under low load conditions. The system's architecture exhibits maximum efficiency of 85% with nominal loads of 25µA, 25µA, and 10µA; with less than 1µA of controller current consumption.

Resumen de Tesis Presentado a Escuela Graduada
de la Universidad de Puerto Rico como requisito parcial de los
Requerimientos para el grado de Maestría en Ciencias

DISEÑO DE CONVERTIDOR SINGLE-INDUCTOR MULTIPLE-OUTPUT PARA APLICACIONES DE BAJA POTENCIA Y ALTA EFICIENCIA

Por

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Mayo 2015

Consejero: Dr. Guillermo Serrano
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Este trabajo presenta una arquitectura de control para convertidores "Single Inductor Multiple Output" (SIMO) aplicada a aplicaciones de baja potencia. Se diseñó, simuló, y probó experimentalmente un Circuito Integrado de Manejo de Potencia (PMIC por sus siglas en inglés) usando una tecnología BiCMOS de 0.8µm, para proveer tres voltajes de salida totalmente independientes mediante el uso de un solo inductor externo. Bajo condiciones nominales, se alcanzó una eficiencia de 85% mediante la implementación de un controlador que consume menos de 1µA durante su estado inactivo. El modo híbrido de operación, junto con el controlador estable de corriente de inductor, permite al sistema alcanzar altas eficiencias aún bajo condiciones de baja potencia.

To my father, my mother, my brother, and my fiancée Rosedanny who always makes me feel loved.

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Finally, but not less important, to all my friends who contributed a sand grain to be who I am today. Thanks to all the people that directly or indirectly contributed to this experience. Blessings for everyone!

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Chapter 1 : Introduction

All electronic devices are powered from a source of energy, typically in the form of batteries. The unregulated power obtained from batteries requires proper regulation through the use of power management integrated circuits (PMICs). PMICs play an essential role on the device life as its efficiency will have a direct effect on the energy delivered to the device. Additionally, the use of external component is a key design parameter, particularly in portable and wearable applications where the device area reduction is one of the design priorities. The quantity and size of the external components will affect the production cost of the integrated circuit (IC) along with its size [1].

This research presents the design, simulation, and experimental validation of a PMIC for wearable devices applications. Design techniques like dynamic powering, low quiescent current, and non-invasive current sensing are used to implement a Single-Inductor Multiple-Output (SIMO) DC-DC converter that works in a proposed Sequential-Distributive hybrid operation mode. The implementation of an 85% efficient PMIC which minimizes the use of external components is discussed in detail, which is one of the main contributions of this research to the field of low power DC-DC converters.

1.1 Objectives

Figure 1-1 shows a block diagram of the power management system of a typical digital wrist watch. The PMIC module, labeled as “Display PMIC”, supplies three different and independent output voltages to a digital display. A lithium battery provides the unregulated power to the PMIC. This work presents the design, simulation and experimental evaluation of a PMIC with the following specifications:

- Three independent and regulated output voltages.
  - 3.2 V @ 25µA of nominal load
  - 4.5 V @ 25µA of nominal load
  - 6.5 V @ 10µA of nominal load
- An input voltage range of (2.5 – 5.5) V
- A 85% efficiency at nominal load
- Minimization of external components
- Less than 10uW of power consumption at no load

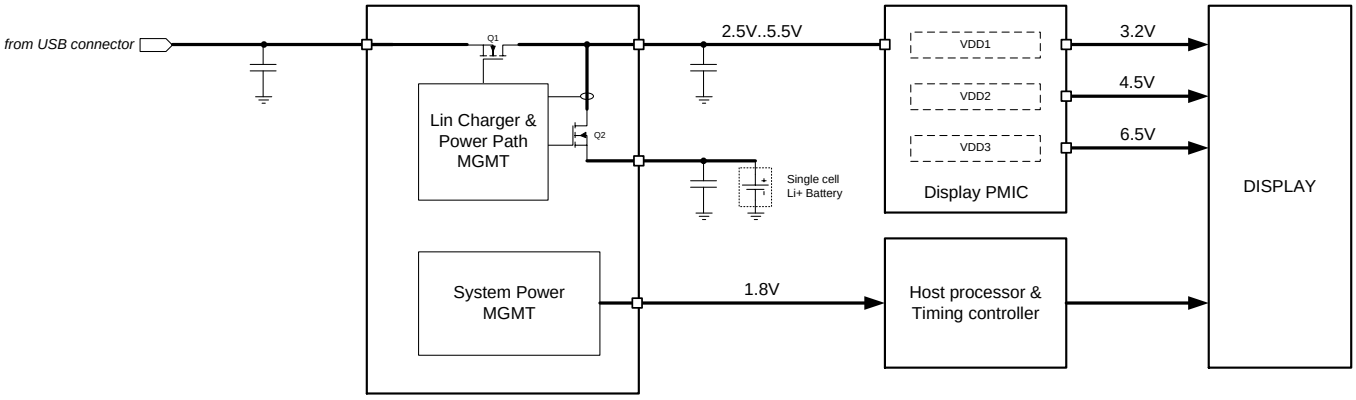

Figure 1-1 Application Block Diagram

The objectives of this research project were the following:

1. Design a Power Management Integrated Circuit (PMIC) that satisfies the specifications presented above using a 0.8µm BiCMOS process.
2. Proceed with the fabrication process of the IC.
3. Apply a validation procedure to the IC. The goal is to provide data about the obtained performance and compare it with the simulator results.

1.2 Content Organization

The research discussion is divided into five chapters. Chapter 2 discusses a literature overview in which the different topologies used for this application are explained. In addition, the system architecture is proposed after researching the literature. The system design stage is discussed in detail in Chapter 3; in which each system component's circuits are explained either from the schematic and layout perspectives. The simulation and experimental data is presented in Chapter 4 with the purpose of comparing them and generating conclusions about the system's functionality. The conclusions are presented in Chapter 5 after analyzing all the simulation and experimental collected data.

Chapter 2 : Previous Works & Architecture Selection

This research's topic will be the design and optimization of voltage regulators for low power applications. With the purpose of selecting the proper circuit architecture to achieve the specifications presented in section 1.1, the literature in DC/DC converters for low power applications was reviewed. The review findings are summarized in section 2.1 along with the additional analysis done for this research's objectives. Section 2.2 offers the analysis and discussion of the selected architecture to implement the PMIC proposed in this research.

2.1 Literature Review & Topologies Overview

Voltage regulators can be classified in three fundamental topologies: linear regulators, switching regulators (inductive), and charge pumps (capacitive). Linear regulators are limited to step-down conversion and exhibit poor efficiencies, hence are not suitable for the target application. An analysis of inductive and capacitive converter will follow, with the objective of selecting the topology that best suits the outlined specifications.

Capacitive voltage regulators have been studied by decades, but they aren't as common as the inductive ones. This is due to the fact that the capacitive regulators are used mostly in low power applications, usually microwatts. They can be designed as step up or step down. For example, a capacitive step up regulator was designed for 697µA nominal load with 95% of efficiency [2]. Also other capacitive regulators where designed as step up for loads of 111µA [3] and 10µA [4] and efficiencies of 78% and 97% respectively. Step down capacitive regulators has been also designed, like the ones designed for nominal loads of 11µA [4] and 18mA [5].

The fundamental topology of the capacitive regulator is the "Dickson Charge Pump", shown in Figure 2-1. The output voltage V_{OUT} is regulated by sending charge packages between stages. The digital signals Φ, which has a logic high greater than the threshold voltage V_T of the diodes, are alternated each stage to provided current path between capacitors. The output voltage is controlled by the frequency at which this charge transitions between capacitors occurs. Equation (1) describes the efficiency n of this topology, where N is the quantity of stages, V_T is the forward voltage of the diodes, f is the frequency of operation, C is the stage capacitance, α is the rate of the parasitic capacitances with respect to C, V_{IN} is the input voltage and I_{OUT} is the load current [6].

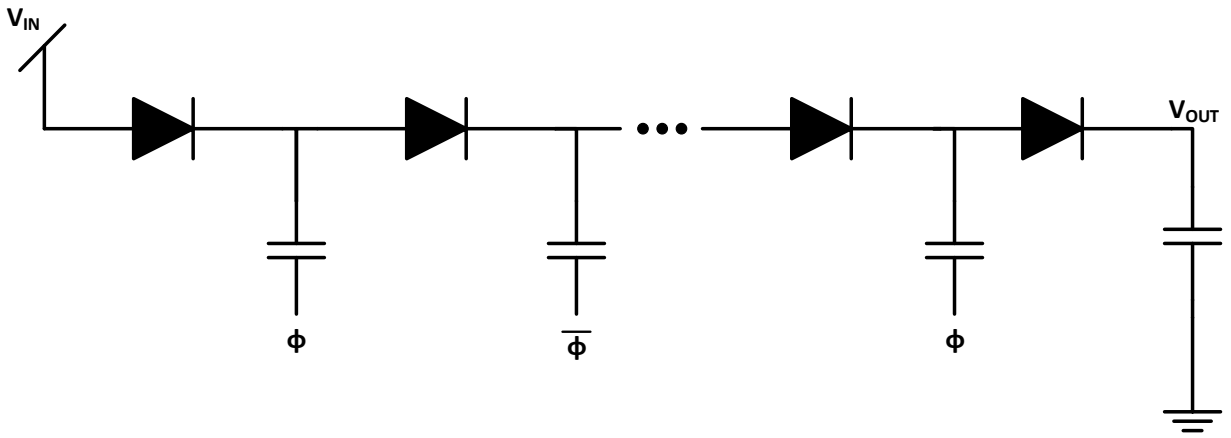

Figure 2-1 Dickson Charge Pump

$$n = \frac{(N+1) - \frac{(N+1)V_T}{V_{IN}} - \frac{NI_{OUT}}{fCV_{IN}}}{(N+1) + \frac{f\alpha CV_{IN}}{I_{OUT}}N} \qquad \textbf{(1)}$$

The efficiency is influenced by many parameters, some of them physical like V_T and α; and others by design like V_{IN}, C, N, and f. One of the disadvantages of this topology is that the efficiency depends on the load and the input voltage; which are two variable parameters in the specifications. Also, to minimize the effect of V_{IN} and load in the efficiency very large stage capacitances are needed, therefore increasing the area of the device.

Inductive Converters

There are different topologies of inductive converters. Like the capacitive converters, they can be used as step up or step down. The fundamental topologies of this type of converter are the "Buck Converter" and the "Boost Converter". There are other topologies, but usually they are based on these two fundamental topologies. The diagrams of these two fundamental topologies are shown in Figure 2-2 and Figure 2-3. Their operation consists on managing the stored energy in the inductor magnetic field allowing a fix output voltage independently of the output load.

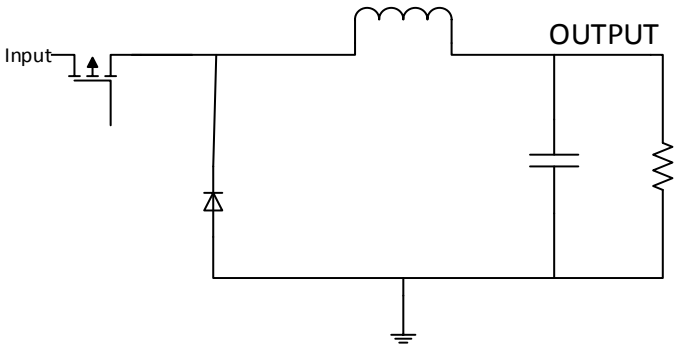

Figure 2-2 Buck Converter

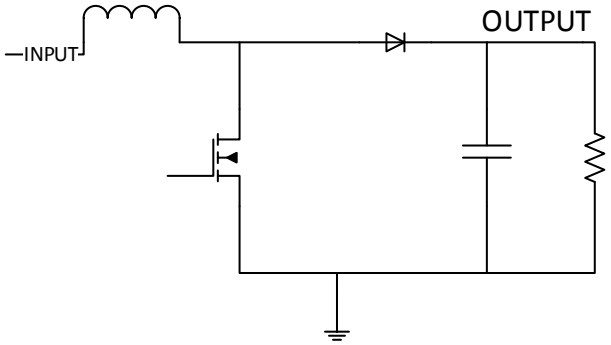

Figure 2-3 Boost Converter

The inductive converter's operation modes could be classified in two when considering the behavior of the inductor current. These two modes are: continuous and discontinuous conduction modes (CCM and DCM respectively). In CCM the inductor current is always positive and greater than zero; while in DCM the inductor current reaches zero. This system will be forced to operate in DCM due to the very low load currents in the specifications. This could be proven with Equation (2) [7], because the K value of this converter will be so small that there won't be any possible value of D to satisfy the CCM criterion. This is important to be known when designing the system controller. Working in DCM has the advantage of simplifying the implementation of a digital control; therefore avoiding the use of oscillators and decreasing the quiescent losses.

$$K > K_{crit} \quad for\ CCM \tag{2}$$

$$K = \frac{2Lf_s I_L}{V_{out}} \quad \& \quad K_{crit} = 1 - D$$

In Equation (2), D is the "duty cycle" or the fraction of time that the inductor is being charged assuming CCM, L is the inductance, I_L is the load current, V is the output voltage, and f_s is the frequency of operation. If the value of K is less than the value of K_{crit} the converter will be forced to operate in DCM; otherwise it will be operating in CCM. It can be noticed that when the output current increases, the converter is nearer to CCM operation. Although this K_{crit} changes for some topologies, the criterion for DCM is always the same. The only difference between topologies will be the definition of K_{crit}. Table 1 shows the CCM-Gain, DCM-Gain, and K_{crit} expressions for each basic topology.

Table 1 Switching Converters Gain Equations

Converter	K_{crit}	CCM-Gain	DCM-Gain
Buck	1 - D	D	$\frac{2}{1+\sqrt{1+4\frac{K}{D^2}}}$
Boost	$D\,(1-D)^2$	$\frac{1}{1-D}$	$\frac{1+\sqrt{1+4\frac{D^2}{K}}}{2}$
Buck-Boost	$(1-D)^2$	$-\frac{D}{1-D}$	$-\frac{D}{\sqrt{K}}$

Single-Inductor-Multiple-Output (SIMO) Converters

The main objective of this research is to develop a solution that minimizes the quantity of external components. This makes the "Single-Inductor-Multiple-Output" (SIMO) topology the best option. A SIMO Buck-Boost serves as both, step-up and step-down converters, [8] therefore being the viable alternative. A circuit schematic of the SIMO Buck-Boost is shown in Figure 2-4. Its operation is the same of a single buck-boost converter, which consist on managing the stored energy in the inductor magnetic field. Its three outputs switches M_{P1}, M_{P2}, and M_{P3} provides current path to all the outputs; therefore enabling it to manage all of them.

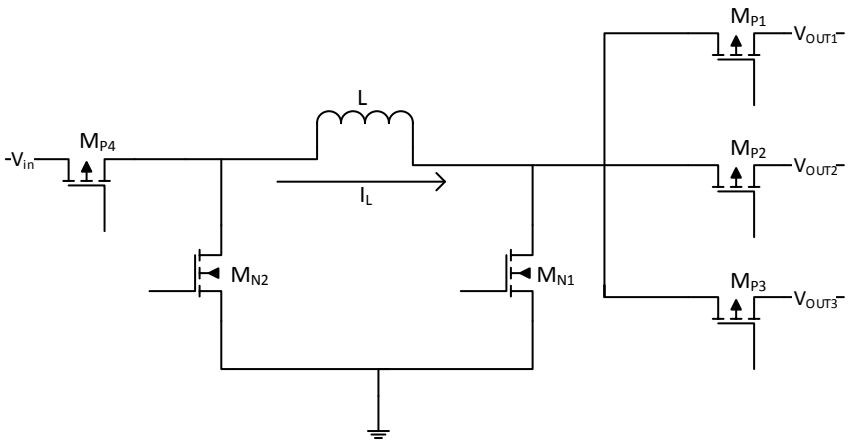

Figure 2-4 SIMO Buck-Boost Converter

Although SIMO converters have been studied extensively, most of them focus on designs targeting loads in the milliamps or higher. SIMO converters with efficiencies of 80% [9] and 93% [10] were designed, although in the milliamps range. By using the equations presented in [10] and [11] (shown in Table 2), and transforming them assuming a one output SIMO, it is possible to derive an expression for the efficiency assuming typical values of parasitic resistances and capacitances. In Table 2 I_{PK} is the inductor peak current, D_1 and D_2 are the energization and denergization fraction of time, respectively, with respect to the frequency of operation f, t_{trans} is the switching time, V_{IN} is the input voltage of the converter, I_{load} is the load current of the stage; and R_L, R_C, R_{se}, R_{sde} are the internal resistances of inductor, output capacitor, energization switches, and denergization switches respectively. The resulting equations showed that it is possible to design a SIMO converter with efficiency between 85% and 95% (Figure 2-5), being the 95% the maximum efficiency point (MEP) in the frequency domain. The optimal point is the inflection point in which the switching and conduction losses are equalized due to the operation frequency. The $P_{control}$ plot is shown also in Figure 2-5 having 10µW, its maximum, at the MEP. This $P_{control}$ plot was calculated assuming target efficiency (η_{target}) of 85%.

Table 2 SIMO Converter Efficiency Equations

	Name	Expression
η	Maximum Efficiency	$\frac{P_{OUT}}{P_{OUT} + P_{COND} + P_{SWITCH} + P_{Control}}$
$P_{control}$	Controller Power Available	$P_{OUT}\left(\frac{1-\eta_{target}}{\eta_{target}}\right) - P_{COND} - P_{SWITCH}$
P_{COND}	Conduction Losses	$P_L + P_C + P_{SW,COND}$
P_{SWITCH}	Switching Losses	$I_{PK} t_{trans} f (V_{IN} + V_{OUT})$
P_L	Inductor Losses	$R_L I_{L,RMS}^2$
P_C	Output Capacitor Losses	$R_C I_{C,RMS}^2$
$P_{SW,COND}$	Switches Conduction Loss	$2R_{se} I_{se,RMS}^2 + 2R_{sde} I_{sde,RMS}^2$
$I_{L,RMS}$	Inductor RMS Current	$\frac{I_{PK}\sqrt{D_1 + D_2}}{\sqrt{3}}$
$I_{se,RMS}$	Energization Switches RMS Current	$\frac{I_{PK}\sqrt{D_1}}{\sqrt{3}}$
$I_{sde,RMS}$	Denergization Switches RMS Current	$\frac{I_{PK}\sqrt{D_2}}{\sqrt{3}}$
$I_{C,RMS}$	Output Capacitor RMS Current	$\frac{I_{PK}\sqrt{D_2}}{\sqrt{3}} + I_{LOAD}\sqrt{1 - D_2}$
f	Frequency of operation	$\frac{V_{IN} D_1}{L I_{PK}}$

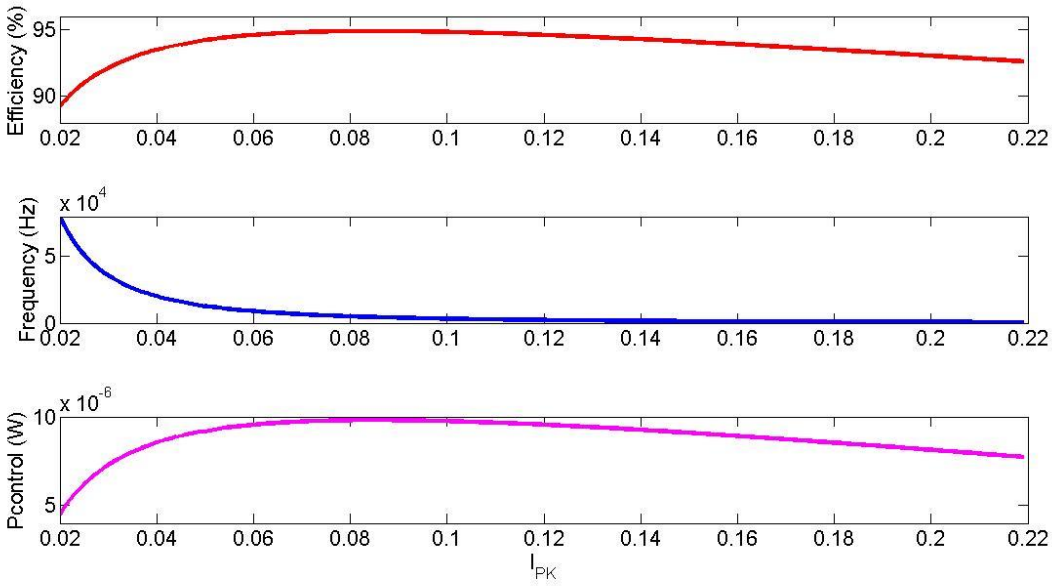

Figure 2-5 SIMO Converter Efficiency Equations Plot

From the literature and theoretical review, the SIMO Buck-Boost converter predominated due to the good output regulation and external components minimization. But such DC-DC converter needs a controller to keep its functionality as discussed previously. A controller architecture is proposed in section 2.2 for the SIMO Buck-Boost converter operating in DCM.

2.2 Proposed Architecture

As discussed in the previous section, SIMO converters offer high efficiency while minimizing the external components, hence are best suited for the target application. Voltage regulation of the SIMO converter for the intended loads (~25µA) will inevitably be in discontinuous mode, as explained in section 2.1.

When operating the SIMO converter in DCM, the stored energy can be delivered to the load in two modes: sequential and distributive. In the Sequential Mode all the energy stored in the inductor during a switching cycle is sent to a single output. Opposed to this, in the Distributive Mode the energy stored in the inductor is sent to every output whenever a switching cycle occurs. It has been shown that Sequential mode has less cross-regulation problems than the Distributive Mode due to its good isolation between the outputs. The advantage of the Distributive Mode is that it has less switching losses than the Sequential mode, because its frequency of operation is usually slower than in the other mode; hence increasing the efficiency [8][12].

Figure 2-6 shows a time diagram of the Distributive mode of operation, assuming the SIMO Buck-Boost of Figure 2-4 is been used. Every time that the inductor reaches a peak value, energy is sent to all the outputs, in this case V_{OUT1} to V_{OUT3}. The inductor current increases when the transistors M_{P4} and M_{N1} are turned on while all the other transistors remain off, this being the energization stage. Right after the inductor reaches its peak current, energy is sent to the outputs by turning off M_{P4} and M_{N1}, and turning on M_{N2} and the transistors M_{P1} to M_{P3}, depending on which output is receiving the inductor energy. As mentioned before, this operation modes results in less switching cycles, therefore reducing the conduction losses; this with the price of having less isolation between outputs.

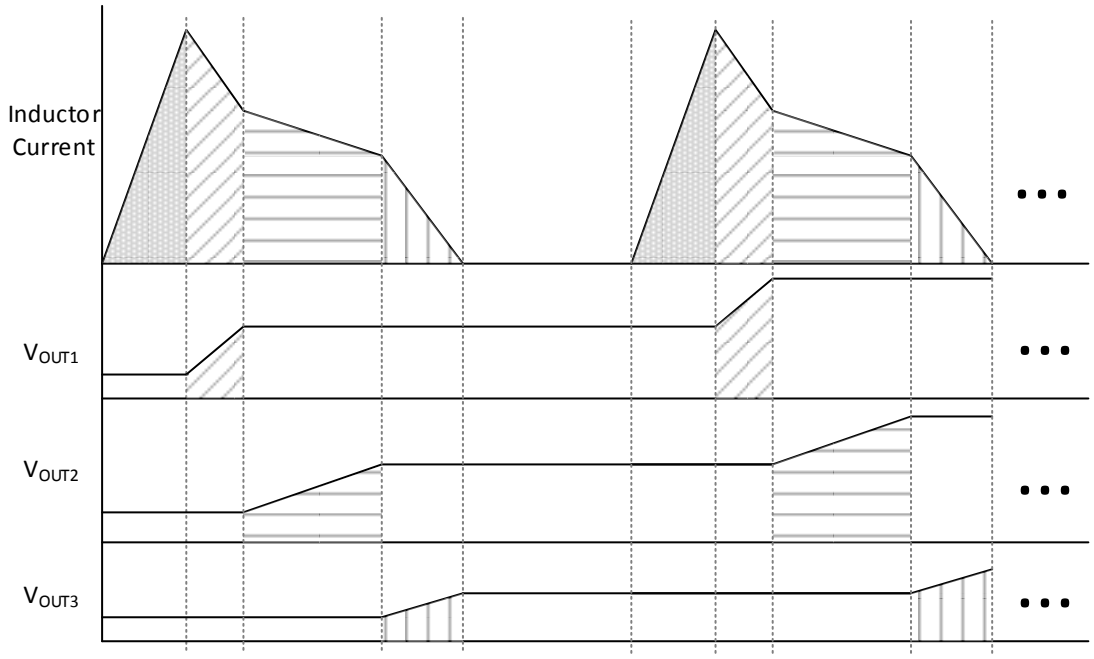

Figure 2-6 SIMO Distributive Mode Time Diagram

In the sequential mode the inductor is charged until its current reaches a peak current value, like in the distributive mode, but in this mode all the energy is sent only to one output. This is shown in Figure 2-7, which is a time diagram of this operation mode. It could be noticed that three switching cycles are needed to send energy to every output. This increases the switching losses with respect to the distributive mode previously discussed, but more output isolation is achieved; which is an important design specification of this device. The output isolation is achieved due to the fact that whenever an output is disabled, the system just ignores it and focus in the other two outputs; while in the distributive mode every output needs to receive energy every switching cycle.

Due to the specifications of high efficiency, it's convenient to use the Distributive Mode to reduce the switching losses. But the Distributive Mode requires every output to receive a portion of charge each switching cycle, and the system could have some of the outputs disabled. This fact makes impossible the use of a pure Distributive operation. For this reason it was decided to use a hybrid between Distributive and Sequential modes; therefore having the benefits of both of them, good outputs isolation and less switching losses.

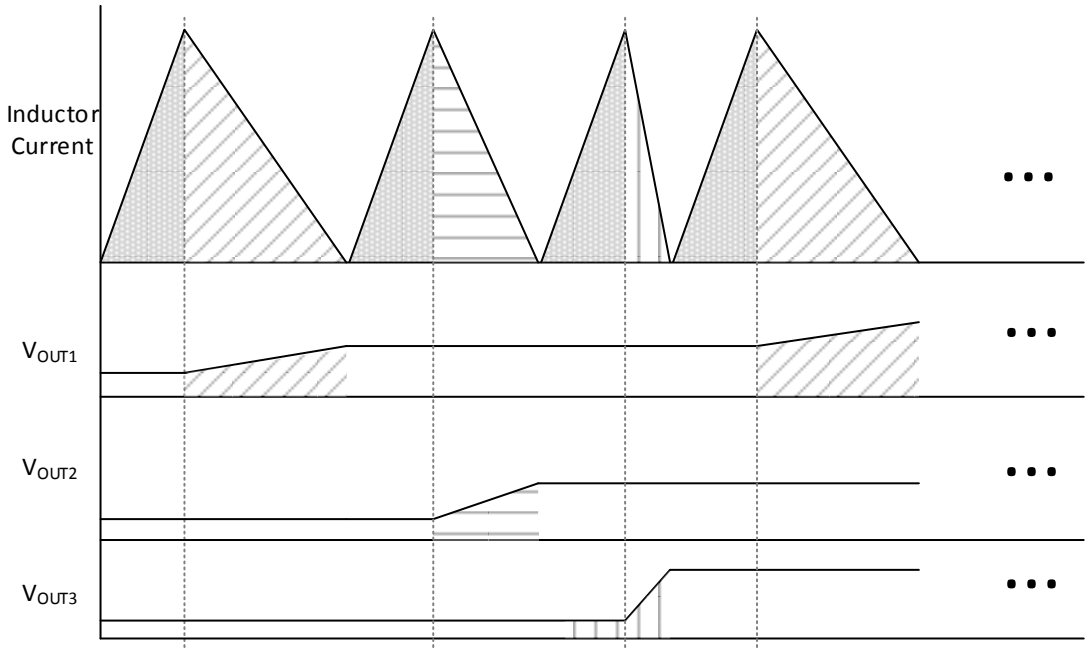

Figure 2-7 SIMO Sequential Mode Time Diagram

The hybrid operating mode will take from the sequential mode the characteristic of ignoring an output whenever it is disabled, or energy isn't needed there. This will give the device the output isolation that is required by the specifications. From the distributive mode, the ability of sending energy to more than one output during the same switching cycle is adopted; but being optional. This means that the converter don't have to send charge to all the outputs every switching cycle, the converter just has to do it when it's required. As shown in Figure 2-8, which is the time diagram for the hybrid mode, there is a priority order for the outputs. The highest priority output is V_{OUT3}, followed by V_{OUT1}, and being the last one V_{OUT2}. In the time diagram, the first three switching cycles are dedicated to V_{OUT3}, until it crosses with its reference voltage, which is the value to which V_{OUT3} have to be regulated. After this crossing occurs, the second priority output V_{OUT1} receives energy. Before the switching cycle is finished V_{OUT1} crosses its reference voltage, therefore immediately passing the priority to V_{OUT2}; which receives energy during the same switching cycle. This is the characteristic adopted from the distributive mode. When no energy is needed in any output the system passes to the freewheeling stage, hence forcing the inductor current to zero. This stage will be active until energy is needed again in an output.

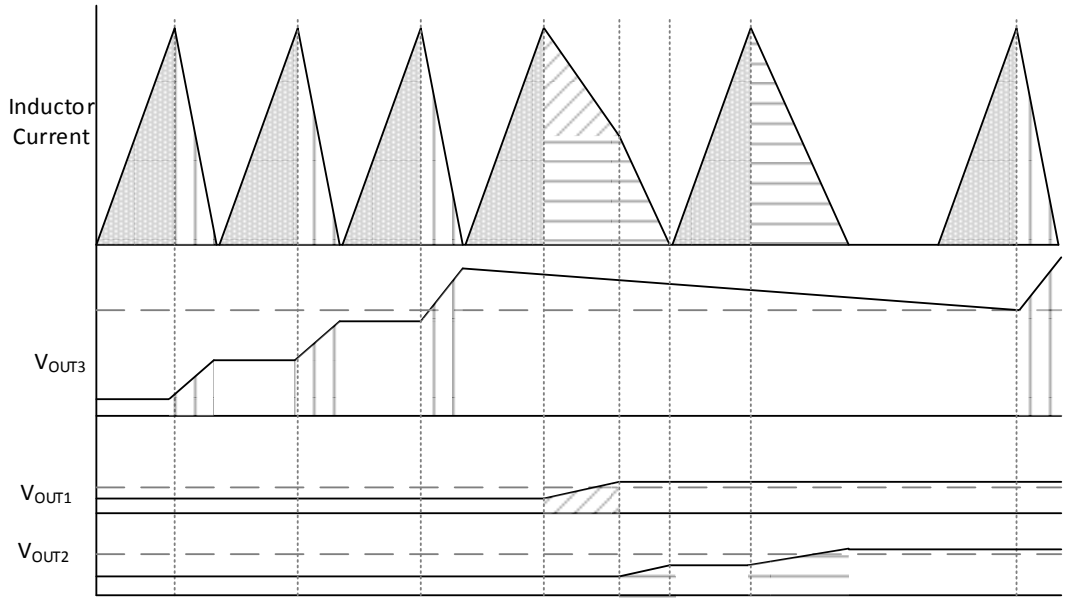

Figure 2-8 Hybrid Mode Time Diagram

As shown in Figure 2-8, the operation of the hybrid mode consists on charging and discharging an inductor. The inductor current is increased to a value called Inductor Peak Current (IPK) and decreased to ideally zero. For this reason an inductor current sensing circuit is needed to detect such current values, and therefore be able to implement a controller. The inductor current could be measure by invasive and non-invasive ways. The invasive current sensing circuit requires being in series along the current path, in this case the inductor. The disadvantage of this approach is that there are conduction losses due to the internal resistance of the sensor. On the other side, the non-invasive current sensing circuits can measure a current without interfering with the current path. This method is a research topic since it is the most efficient manner to sense a current and there are many ways to implement it. In this design the inductor current needs to be measured to detect two instants, the instant when the inductor current reaches IPK and the instant when the inductor current reaches zero (ZCD).

A non-invasive topology is proposed for detecting the IPK and ZCD instants based on [12] and [13]. Current-voltage converters, dynamic voltage reference generators, and hysteretic comparators are used for the implementation of such current sensors; and they are discussed in detail in Chapter 3.

A digital controller was implemented to control the system due to its very DCM operation. If the system is operated with conventional PWM (Pulse Width Modulation) the resulting t_{ON} (energizing time) would be very small and very difficult to be implemented. For this reason a fixed peak inductor current controller was selected. Although this type of controller can be implemented using an oscillator, the use of an Asynchronous State Machine was selected to avoid the use of a high frequency oscillator, and the DC losses generated by using it. A similar controller was implemented in [14], but for milliamps loads. The state machine uses the IPK and ZCD current sensing modules to control the energizing and de-energizing times of the inductor; and distributes the energy stored in the inductor to the system's outputs. Figure 2-9 shows the state diagram of the proposed state machine controlling the inductor switching cycles. When the system is turned on, it immediately goes to the "Inductor Energization" stage, in which only switches M_{P4} and M_{N1} are turned on. This stage will remain active until IPK signal is activated meaning that the inductor peak current was reached. After this occurs, the "Inductor De-energization" stage is started by turning on only the M_{P1}, or M_{P2}, or M_{P3} and M_{N2} switches. This stage is when the energy stored in the inductor is delivered to the output terminals. When the ZCD signal is activated, meaning that zero inductor current was reached, this phase is terminated and the "FW stage" is started. In this stage the M_{P5} transistor, or freewheeling (FW) switch, is turned on to short the inductor terminals and avoid oscillations after ZCD is reached. This stage will remain active until any of the output comparators signals is activated; meaning inductor energy is needed in an output. During this stage all the components of the controller are put in standby mode to reduce DC losses.

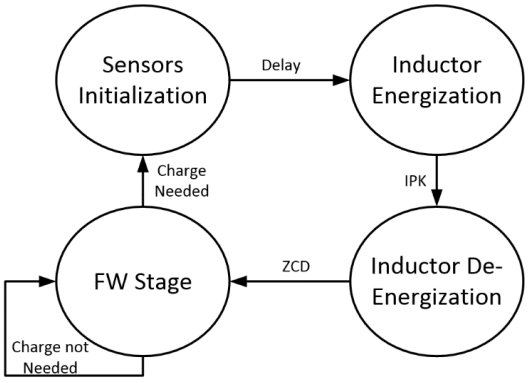

Figure 2-9 State Machine's State Diagram

Figure 2-10 shows the SIMO converter presented in Figure 2-4 but including the proposed controller block diagram with its components. Further information of device design process is discussed in Chapter 3.

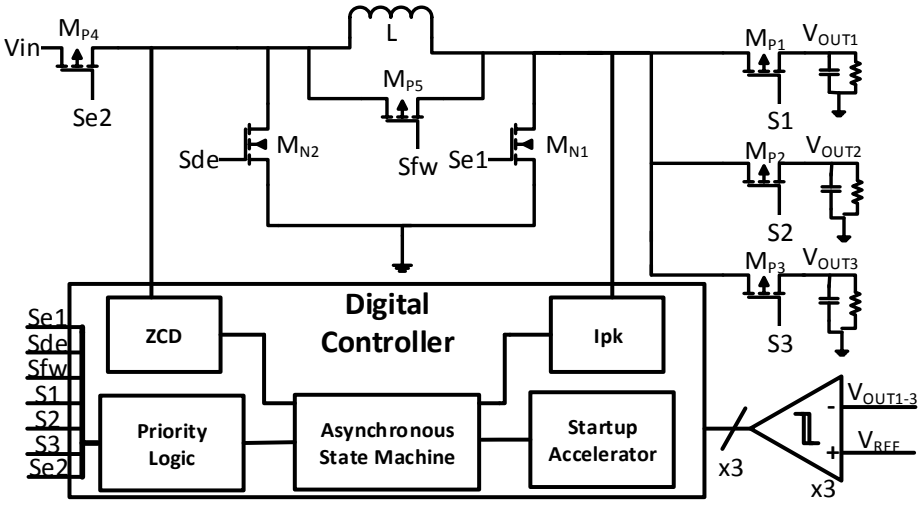

Figure 2-10 SIMO Converter Topology and Controller

Design Challenges

Some of the challenges of this design involve the implementation of very low power consumption components. Current Sensing, Comparators, and Reference System components need to be designed for a global power consumption of less than 10µW to keep the target efficiency of 85%. To implement these very low power consumption components techniques like very high resistances and dynamic powering should be used. Very high resistances are used in the Reference System; and all the current sensing and comparators components are implemented using the dynamic powering technique.

Chapter 3 : System's Design & Components Overview

A PMIC was designed to supply three totally individual outputs. To do this the architecture presented in Figure 2-10 was used. As discussed previously, it is a complex architecture due to its novel components. This chapter discusses in detail the circuit schematics, design process, and circuit layouts of the different sub-circuits inside the proposed PMIC. The system’s design was done using Computer Aided Design (CAD) and a 0.8µm BiCMOS process. Since the device is very complex, its design was divided in modules. This chapter shows all the modules and components designed along with their layout design.

3.1 System's Components Overview

Due to the system complexity, the design stage was implemented modularly. There are two main modules, which are the Power Module and the Controller Module. The Power Module includes the power transistors and their gate drivers. From Figure 2-10, those power transistors are M_{N1}, M_{N2}, M_{P1}, M_{P2}, M_{P3}, M_{P4}, and M_{P5}. All the other components of the system are included inside the Controller Module. Figure 3-1 shows the module map of the device.

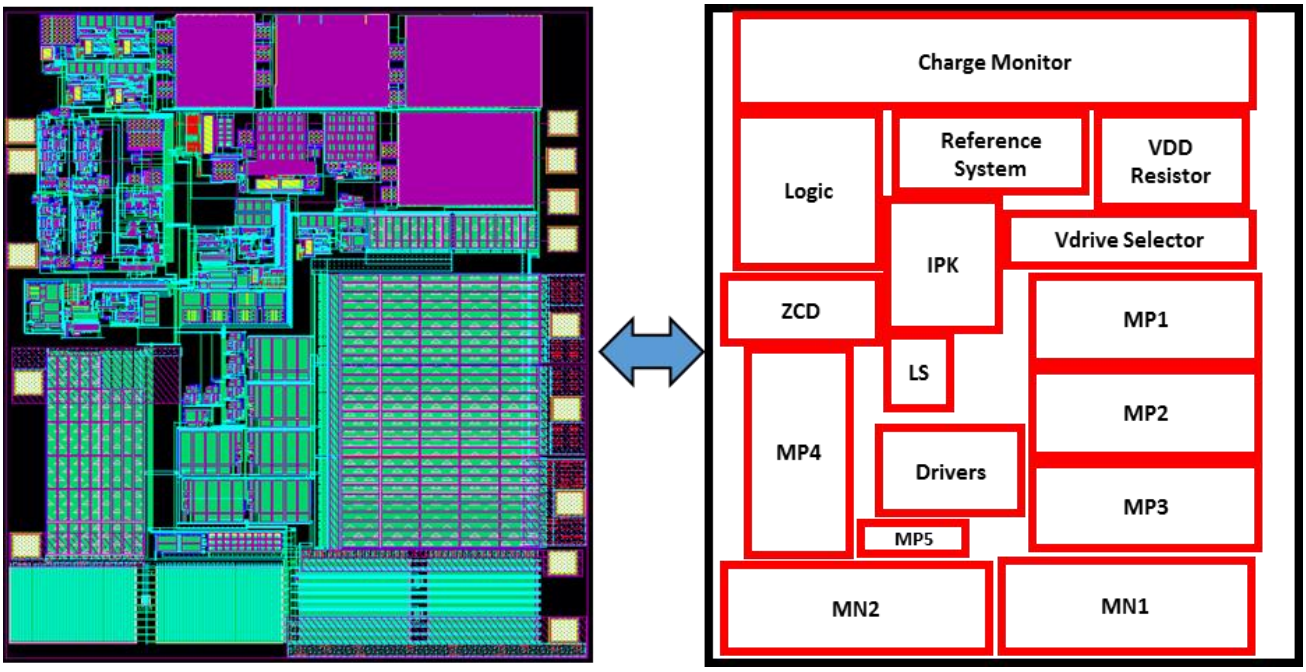

Figure 3-1 Device's Map of Modules

Each component of the device is discussed in detail on this chapter. The list of modules and sub-modules is shown in Table 3, along with their accomplished specifications. If the power consumption of each controller module is added, a total of 10.28µW is obtained; which is exactly the power budget for the controller calculated in Figure 2-5. The design procedure done to get those accomplished specifications is discussed in detail in the next sections, which discusses it one module per section. Although schematics are shown in this chapter, they are to illustrate the design. Therefore simplified schematics are shown in this section; and the real CAD schematics are shown along with their respective layouts in Appendix A – Cellviews and Layouts.

Table 3 Module Design Specifications

Module	Accomplished Specs	Value	Module's Purpose
Reference System	*VREF*	1.22V +/- 7%	Generates the voltage and current references needed by the system
	Iref	70nA	
	*PC**	0.840µW	
Inductor Peak Current Sensor	IPK	FAST Mode → 800mA Steady State → 400mA	Provides the system with an inductor current value detector that sends a signal when the IPK value is reached during the energization stage
	PC*	2.95µW	
Zero Current Detector	ZCD	0A +/- 100mA	Detects the point when the current decreases near to zero during the de-energization stage
	PC*	2.80µW	
Logic	PC*	0.23µW	Contains the Asynchronous state machine and the priority logic
Charge Monitor	PC*	2.76µW	Monitors the 3 outputs to determine if they need more energy to raise its voltage
VDRIVE Selector	PC*	0.70µW	Provides the highest voltage of the system from the supply or either from the 6.5V output
Level Shifters	PC*	0.18µW	Transform a digital signal with a logic level "A" into a signal with a logic level "B"
Drivers	Rise-Fall Times	2 ns	Provide isolation between controller and power stage, and the enough current to change the voltage in the power transistors' gates
	PC*	0.55µW	
Switches	$R_{internal}$	[200 - 550] mΩ	Contains all the power transistors along with the protective diodes

* PC: Power Consumption at nominal corner

3.2 Reference System (Refsys)

The purpose of this component is to generate the voltage and current references needed by the system. It generates a 1.22V band-gap voltage reference and a 70nA constant-to-temperature current that is mirrored to serve as 12 current sinks for the system's components. A totally independent amplifier is used as buffering for the reference voltage to an external pin. This module has the ability to change the system's reference from the internal band-gap voltage reference or either an external reference; and it's selected through a digital enable pin.

The 1.22V reference voltage directly influences the output regulation of the system because it is used as reference by the output comparators. Due to this fact, it should have a very low error percentage at every corner to accomplish with the output regulation specifications. To implement this voltage reference a double-cascode PTAT current generator was used along with BJT transistors. Figure 3-2 shows the simplified schematic of the band-gap voltage reference generator.

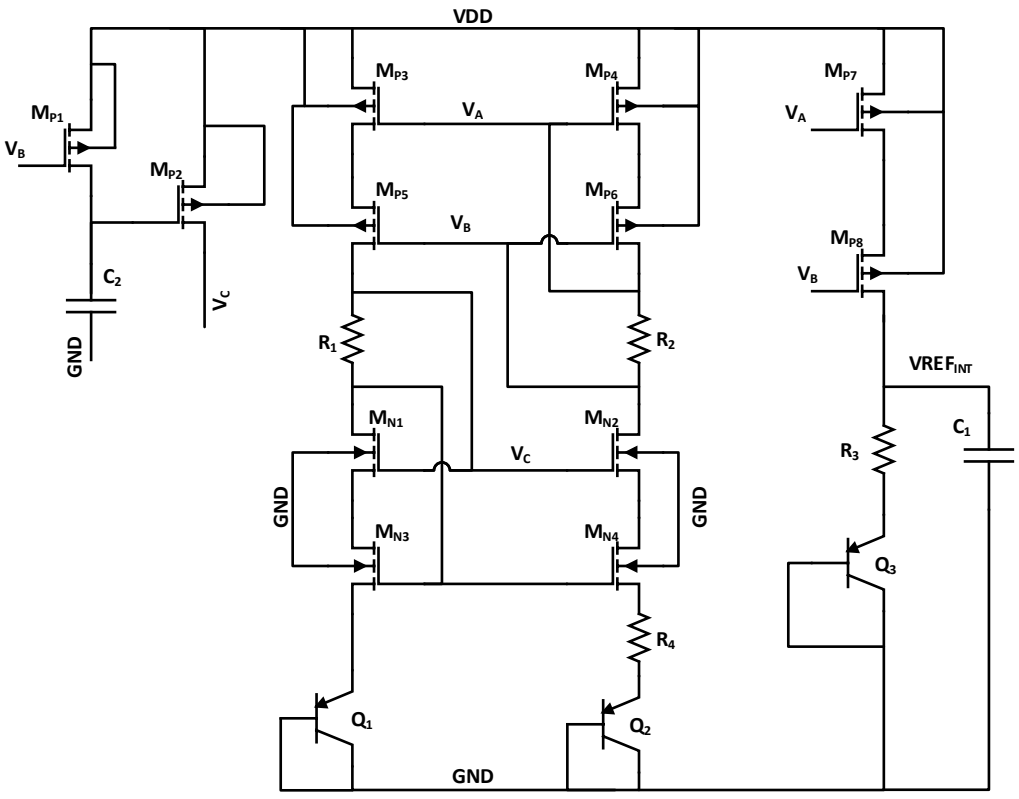

Figure 3-2 Internal Reference Voltage Schematic

$VREF_{INT}$ is the band-gap reference voltage; and it is generated by adding negative and positive Temperature Coefficients (TC). The positive TC is provided by the thermal voltage (V_T) and the negative TC is generated by the base-emitter voltage V_{be} of transistor Q_3. The equation of the current flowing through transistor M_{P7} is shown in Equation (3). It can be shown that the same current passes through resistor R_3 [15], assuming that transistors $M_{P3} = M_{P4}$, $M_{P5} = M_{P6}$, $M_{N1} = M_{N2}$, and $M_{N3} = M_{N4}$; and all of them are operating in saturation region. In Equation (3), A_{Q1} and A_{Q2} are the respective transistors Q_1 and Q_2 areas; and V_T is the thermal voltage. The voltage $VREF_{INT}$ is equal to the addition of the voltage drops V_{beQ3} in transistor Q_3 and in R_3, which is equal to I_{MP7} multiplied by the value of resistor R_3; as shown in Equation (4).

$$I_{MP7} = V_T \frac{1}{R4} \ln\left(\frac{A_{Q2}}{A_{Q1}}\right) \quad \textbf{(3)}$$

$$\mathrm{VREF_{INT}} = \mathrm{V_T} \frac{\mathrm{R_3}}{\mathrm{R_4}} \ln\left(\frac{\mathrm{A_{Q2}}}{\mathrm{A_{Q1}}}\right) + \mathrm{V_{beQ3}} \quad \textbf{(4)}$$

If the partial derivative over temperature is taken to Equation (4), the relation shown in Equation (5) is obtained. To achieve TC cancellation the rate between resistors R_3 and R_4 should be set, along with the natural logarithm of $N= A_{Q2}/A_{Q1}$, equal to the value shown in Equation (6).

$$\frac{\partial VREF_{int}}{\partial T} = \frac{\partial V_{be}}{\partial T} + \frac{R_3}{R_4} ln(N) \frac{\partial V_T}{\partial T} \quad \textbf{(5)}$$

$$\frac{R_3}{R_4} ln(N) = \frac{-\frac{\partial V_{be}}{\partial T}}{\frac{\partial V_T}{\partial T}} \quad \textbf{(6)}$$

M_{P1}, M_{P2}, and C_2 form the startup circuit of the PTAT current generator. When the circuit is turned on, meaning VDD goes from zero to the supply voltage, V_C node will be charged through M_{P2}. This will force the NMOS transistors M_{N1}, M_{N2}, M_{N3}, and M_{N4} to conduct current and find and stable operation point. When capacitor C_2 is completely charged to VDD through transistor M_{P1}, M_{P2} will remain off while VDD remains high. The capacitor C_2 is designed to allow enough time to M_{P2} to start the circuit. The resistors R_1 and R_2 are designed to set the appropriate bias voltages for the PTAT current generator cascode-stages.

This reference system has the feature of switching between two different references, the internal one discussed above and an external one. The reference to be used is controlled by an

external pin called VREF_EXT_EN. When this pin is high, connected to VDD, the external reference is used by the system. If the external reference enable pin is connected to GND then the internal reference will be used by the system. This was implemented by using CMOS transmission gates.

With the objective of monitoring the internal reference voltage externally, a buffer was used to replicate it to the output pin VREF_OUT. This was done because the rail current flowing through M_{P7} is in the nano-amperes range being this not enough to charge the enormous pin capacitance. A simple two stage amplifier was designed to be connected as buffer. The bias current for the amplifier is provided by a second PTAT current generator dedicated only to this purpose. It has very low rail currents and it's almost the same first PTAT circuit of Figure 3-2.

Simulations were done to the reference system to check its performance in quiescent current and error percentage. DC sweeps were done to verify the error percentage of the internal reference voltage varying the supply voltage (VDD), the temperature, and the process. The supply voltage was varied in 3 discrete steps, which are 2.5V, 3.6V, and 5.5V. The two opposite corners of process, which are weak and strong inversions, were used with each VDD corner. A Temperature-DC sweep was simulated to verify the reference voltage error percentage at every corner. Figure 3-3 shows the temperature sweep of the reference voltage. The error percentage value of VREF is (-6.65, +1.73) %. The weak process is the principal responsible of the negative error percentage.

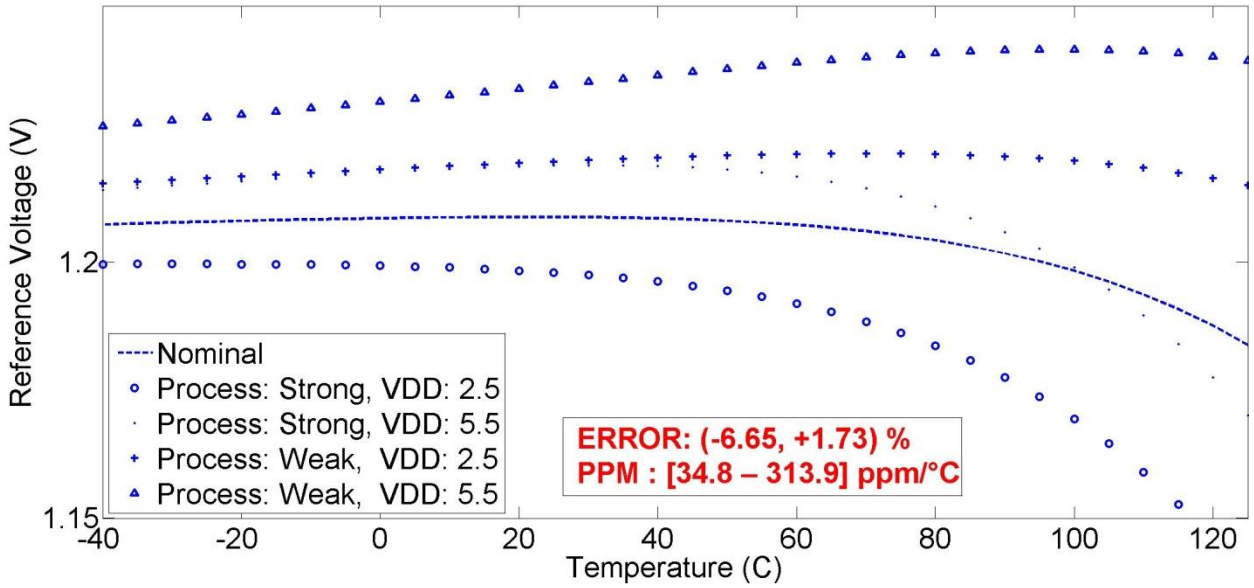

Figure 3-3 Reference Voltage Temperature-DC Sweep

Reference currents are provided by this module to different components. Some of them as the Charge Monitor module don't need a very precise reference; but others like the current sensing modules need a very precise current reference to be accurate. If the current reference varies with temperature, a proportional variation will be seen in the inductor peak current and zero current values; therefore degrading the optimal inductor current control and the systems efficiency. To avoid that variation, a constant-to-temperature current reference needed to be designed. This was implemented by adding a Complementary-to-Temperature (CTAT) current reference to the PTAT current reference generated in the internal reference circuit of Figure 3-2. The CTAT generator used in this design is shown in Figure 3-4 along with the CTAT and PTAT current adder and the current sinks.

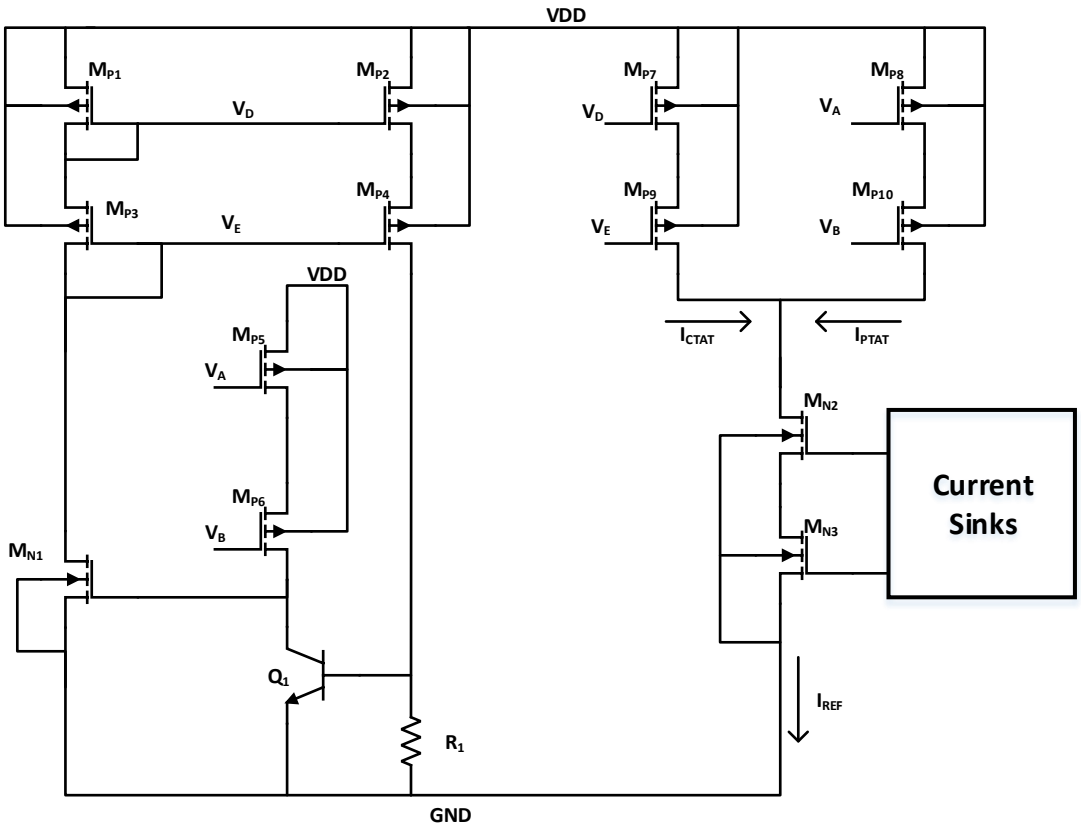

Figure 3-4 Current Reference Generator Schematic

This schematic assumes that M_{P1}=M_{P2}=M_{P7}/1.5, M_{P3}=M_{P4}=M_{P9}/1.5, M_{P8}=M_{P5} and M_{P10}=M_{P6}; from which M_{P8} and M_{P10} also are equal to M_{P4} and M_{P6} of Figure 3-2 respectively. Transistor M_{P5} is a mirror of the PTAT current that forces a multiplier of the PTAT current to flow through transistor Q_1. The V_{ce} voltage of Q_1 turns on the transistor M_{N1}; and with it the cascaded-mirror formed by M_{P1}, M_{P2}, M_{P3}, and M_{P4} starts flowing current. That current flowing through transistors M_{P2} and M_{P4} is described by Equation (7), where $V_{be,Q1}$ is the base-emitter voltage of transistor Q_1. Due to this direct proportionality of I_{MP4} to a base-emitter voltage, which has a negative TC, it's called a Complementary-to-Temperature (CTAT) current.

$$I_{MP4} = \frac{V_{be,Q1}}{R_1} \qquad \textbf{(7)}$$

The value of this current is settled by R_1 to achieve I_{REF} TC cancellation, described by Equation (8), which is the addition of I_{PTAT} and I_{CTAT} currents. This differential equation is valid only assuming that $\frac{\partial R_1}{\partial T} = 0$, which could be very small depending the process. R_1 value is

calculated by Equation (9), where TC_{PTAT} is the chosen value when $VREF_{INT}$ was designed in Equation (5); which is obtained by setting the I_{REF} TC to zero and solving Equation (8) for R_1.

$$\frac{\partial I_{REF}}{\partial T} = \frac{\partial I_{PTAT}}{\partial T} + \frac{\partial I_{CTAT}}{\partial T} = \frac{\partial I_{PTAT}}{\partial T} + \frac{1}{R_1}\frac{\partial V_{be,Q1}}{\partial T} \quad \textbf{(8)}$$

$$R_1 = \frac{1}{-\frac{\partial I_{PTAT}}{\partial T}}\frac{\partial V_{be,Q1}}{\partial T} \quad \textbf{(9)}$$

Temperature sweeps were done to verify reference and supply currents performance. Figure 3-5 shows the temperature sweep for the reference current I_{REF}. At the nominal corner the I_{REF} is hold near 70nA over the entire temperature window. But two groups of current data are with positive and negative offset over the nominal corner; and these variations are due to process variations. I_{REF} variation would have been much larger if the TC cancellation hasn't been implemented. That could be noticed in the parabolic shapes of the plot, which shows that the changes in current aren't proportional to temperature changes.

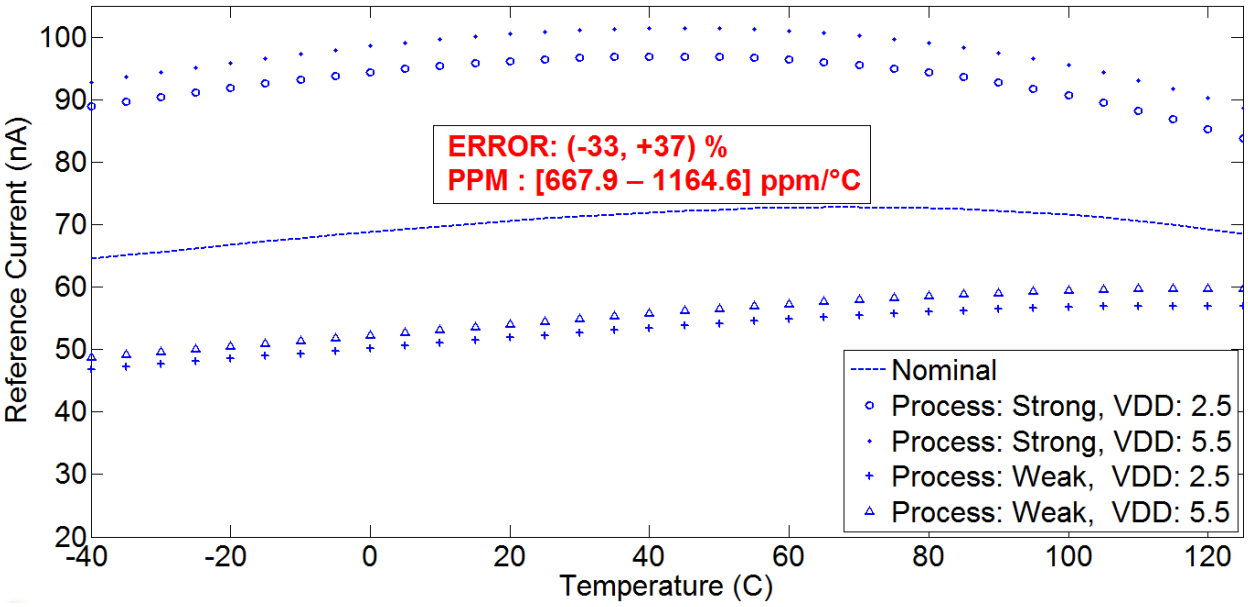

Figure 3-5 Reference Current Temperature-DC Sweep

In order to implement an efficient reference system, its current consumption should be the minimum. To corroborate this fact, temperature sweeps were done in different supply voltages and processes corners; and the results are shown in Figure 3-6. Assuming from the plot 300nA maximum current at nominal temperature, the maximum power loss due to the reference system operation could be calculated. If the maximum supply voltage (5.5V) is multiplied by

300nA, a maximum power of 2µW is needed to operate the reference system at nominal temperature. Since the power budget for the controller of 10µW hasn't been overpassed even at the worst case scenario of VDD, it could be concluded that power consumption accomplishes the specifications. In addition, the average reference system power consumption at nominal corner was verified using transient simulations, an as shown in Table 3, the result was 840nW; which leaves enough power budget for the rest of the modules.

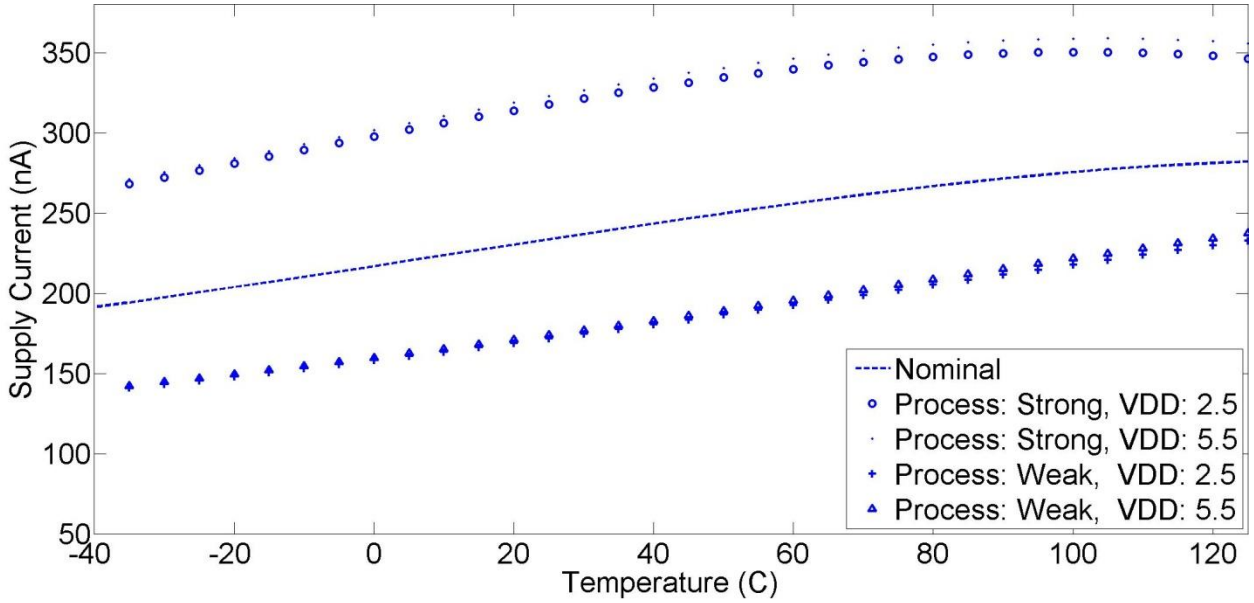

Figure 3-6 Supply Current Temperature-DC Sweep

This module's layout is located almost in the center of the device. This was done to avoid product fabrication damage to it. Its layout is shown in Figure 3-7 along with its three main components identified. As explained above, those main components are the internal reference voltage generator, the CTAT current generator, and the reference voltage buffer. The layout design was emphasized in symmetry between components with rates; like the transistors Q_1 and Q_2, and resistors R_3 and R_4 of Figure 3-2. These components has directly influence on the bandgap-voltage, or reference voltage, as shown previously in Equation (4). To achieve perfect symmetry, dummy transistor, resistors, and capacitors were used. Figure 3-8 shows the distribution used for resistors R_3 and R_4. The values of R_4 and R_3 are 3.2MΩ and 17.5MΩ respectively. They were distributed as serpentine by dividing R_4 in 15 fingers of 213.333kΩ; and R_3 in 80 fingers of 218.750kΩ. To achieve a 1 to 4 correspondence between the resistors, 5 dummy fingers of R_4 were added.

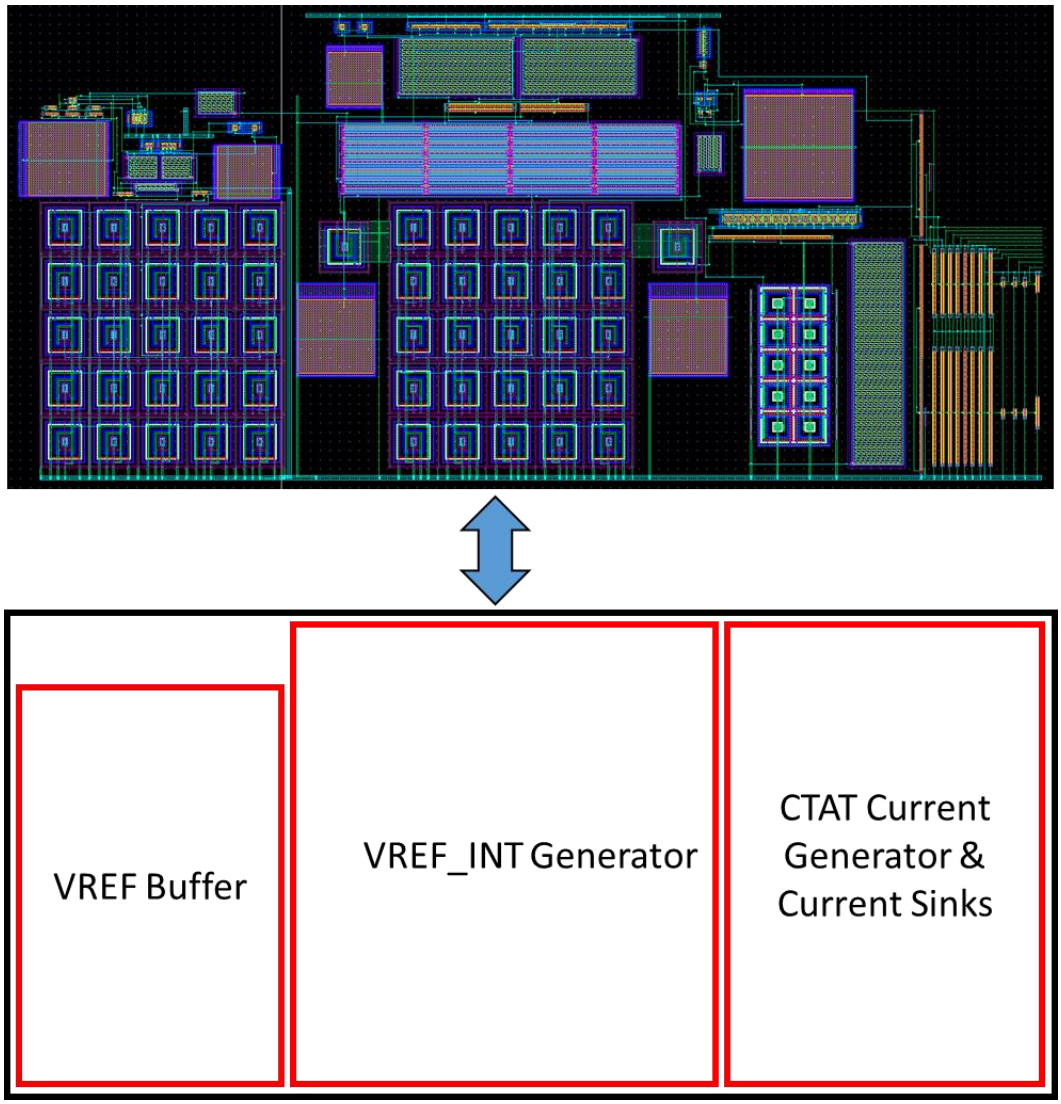

Figure 3-7 Reference System's Layout

R4	R4	R4	R4
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R4	R4	R4	R4
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R4	R4	R4	R4
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R4	R4	R4	Dummy
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
Dummy	Dummy	Dummy	Dummy
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3
R3	R3	R3	R3

Figure 3-8 R3 and R4 Resistors Matching Distribution for Internal Reference Voltage

In Figure 3-2, transistor Q_2 has 10 times the emitter area of Q_1. For every BJT transistor in the reference system the unit area is 7.03 μm^2. The area of Q_1 and Q_2 is 7.03 and 10*7.03 um^2 respectively. To have a completely symmetric distribution 14 unit area BJT transistors were added to the layout as dummies. Figure 3-9 shows the Q_1 & Q_2 distribution for the internal reference voltage.

Dummy	Dummy	Dummy	Dummy	Dummy
Dummy	Q2	Q2	Q2	Dummy
Q2	Q2	Q1	Q2	Q2
Dummy	Q2	Q2	Q2	Dummy
Dummy	Dummy	Dummy	Dummy	Dummy

Figure 3-9 BJT Transistors Q1 & Q2 Distribution for Internal Reference Voltage

For the Q_1 BJT transistor in the CTAT current generator no distribution is needed because there is no rate with another transistor in the CTAT current equation (Equation (7)). The same BJT transistor distribution used for the internal reference generator's PTAT was used for the reference buffer's PTAT. All the PMOS and NMOS current mirrors were distributed using interdigitation [16]. More detailed layout vs schematic components identification is shown in Appendix A – Cellviews and Layouts

3.3 Inductor Peak Current Sensor (IPK)

Since the operating mode of the SIMO converter, in DCM, consist on charging and discharging an inductor, meaning increasing the inductor current to an IPK value and decreasing it to ideally zero, an inductor current sensing circuit is needed to be able to implement a controller. This module provides the system with an inductor current value detector that sends a signal when the IPK value is reached during the energization stage of Figure 2-8. It consists of a non-invasive current sensor, therefore doesn't affecting the efficiency of the system's power stage. In addition, less than 50nA of quiescent current is achieved during standby mode, therefore decreasing the expected controller DC losses.

The Inductor Peak Current Sensor's block diagram is shown in Figure 3-10. It consists of six main components which are: Starter, Current Reference Amplifier, IPK Reference Voltage Generator, Current-Voltage Converter, Hysteretic Comparator, and Output Stage. Each component is discussed in detail below.

The Starter is the responsible of initializing every component when the ENABLE signal is received. This signal is turned on/off by the Logic Module in Figure 3-1, discussed in section 3.5; and it will be turned on every time a switching cycle is started. This component provides the IPK sensors with the VDD_B and VDD_C supply nodes; and raises the signal READY when the initialization stage is done. The Current Reference Amplifier converts a reference current of 50nA, provided by the Reference System module shown in Figure 3-1, and generates a new reference of 5µA. The 5µA are created only when the system isn't idle. This allows the system to have a low quiescent current. These 5µA serves as reference to the Current-Voltage Converter, IPK Reference Voltage generator, and Hysteretic Comparator components. Inductor current sensing is implemented by the Current-Voltage Converter. This component generates a voltage, the sensing voltage V_{SENSE}, which changes linearly with respect to the inductor current. The V_{SENSE} voltage is compared with the V_{REF} voltage generated by IPK Reference Voltage Generator. The reason of using a reference voltage different from the one generated by the Reference System module of section 3.2 will be discussed below when the components' schematics are shown. A hysteretic comparator was implemented using active latches to achieve fast response when V_{SENSE} approaches to V_{REF}. The comparator's output $COMP_{OUT}$ passes

through an output stage before moving the output pin voltage IPK. The Output Stage is responsible of filtering possible spikes at IPK during the initialization stage.

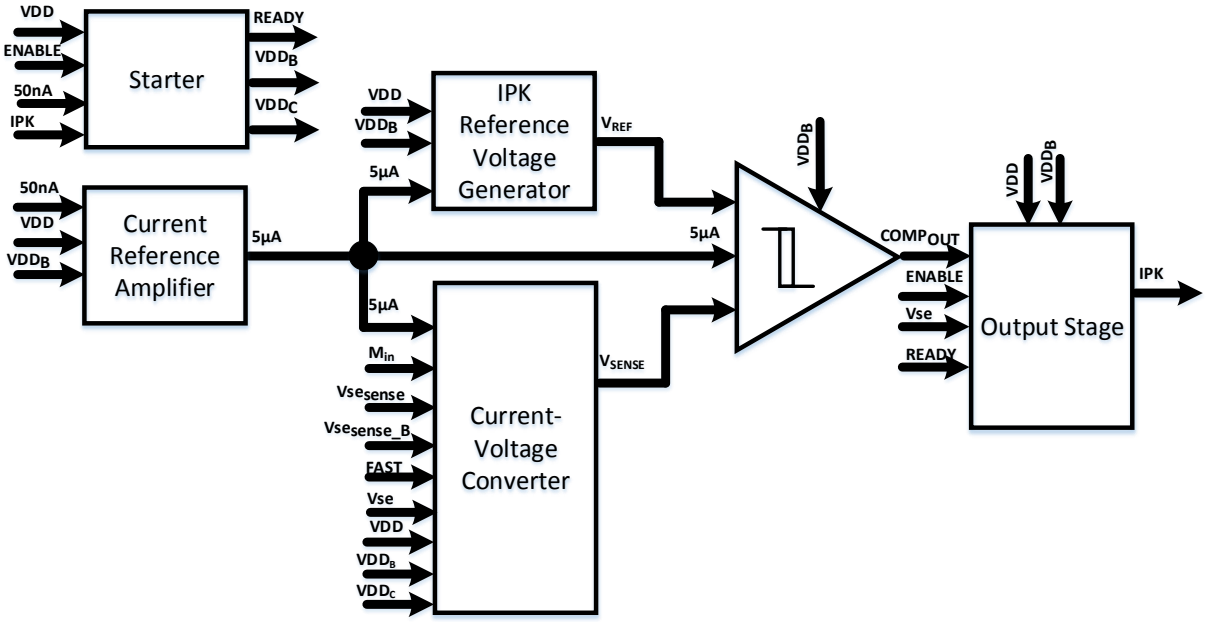

Figure 3-10 Inductor Peak Current Sensor Block Diagram

When the ENABLE signal is turned on by the Logic module, the first IPK component to work is the Starter. The Starter gives some delay time between the IPK sensor initialization and energization stage's start time. The energization stage will begin when the IPK sensor's output READY is turned on. In all the modules of this design, every delay is generated using current-limited CMOS inverters and Hysteretic CMOS inverters. A schematic of the delay circuit is shown in Figure 3-11.When a rising edge occurs at the input signal the Delayed signal node changes slowly, therefore holding the output node to GND until the delay time occurs. Figure 3-12 illustrates this scenario, in which the input, delayed, and output signals are the magenta, red, and blue plots respectively. In this case the delay time is almost 10µs, but it can be controlled with the capacitor value in the delayed signal node and with the limited current value.

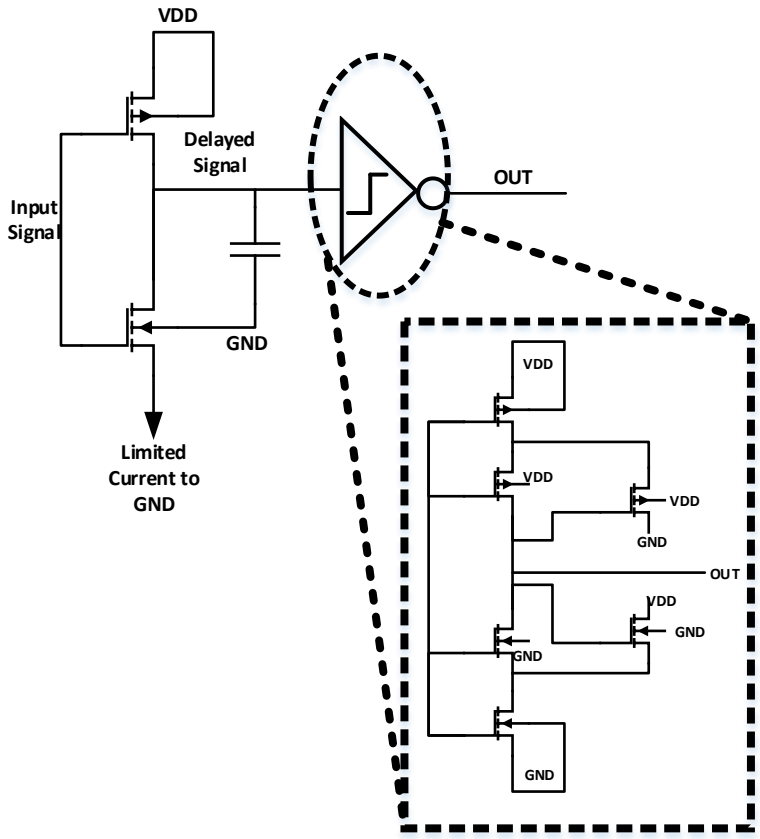

Figure 3-11 Delay Circuit Low-to-High Edge

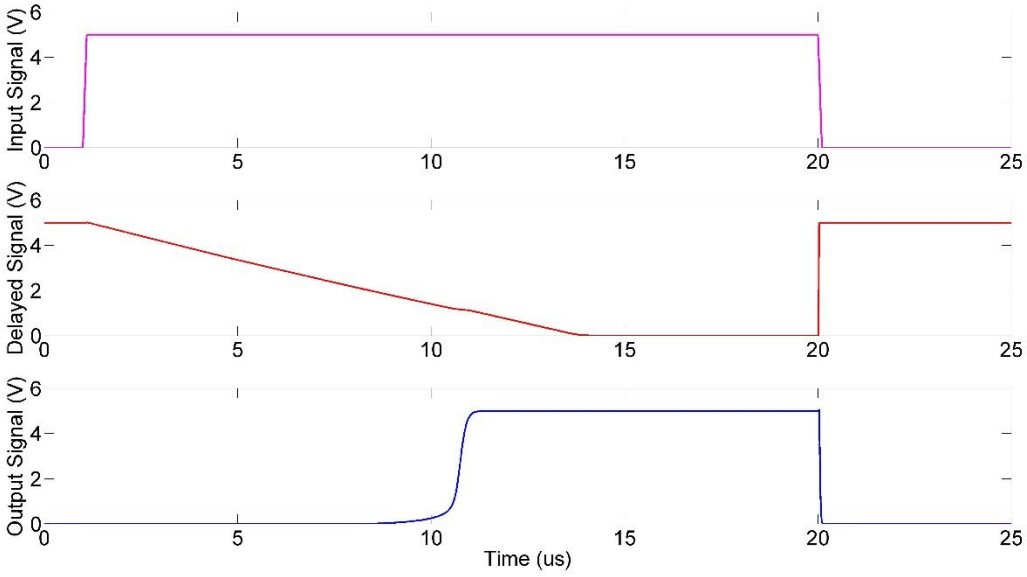

Figure 3-12 Delay Circuit Example Plot

In addition to adding a delay between the ENABLE and READY signals, the Starter manages the supply nodes VDD_B and VDD_C. Figure 3-13 shows the schematic of this component. The VDD_B power comes from VDD through a PMOS switch; and VDD_C power comes from VDD_B also through a PMOS switch. Immediately after ENABLE changes to high, the signal ENABLE_Z goes to low and VDD_B rises to the VDD voltage. This will initialize all the parts supplied by this node. Due to the fact that READY is low at the beginning, ENABLE_VDD_C_Z will remain high, therefore keeping VDD_C disconnected from VDD_B. Immediately after READY goes to high, ENABLE_VDD_C_Z will be low and VDD_C will be connected to VDD_B, therefore supplying the components connected to this supply node. During this time the energization starts and current sensing is running. When IPK is reached, the IPK signal will raise forcing the Q output of the Starter's latch to high, therefore blocking the supply on VDD_C. This is done to avoid current spikes during high current paths inside the Current-Voltage Converter Component. The process will be repeated each time energization is required.

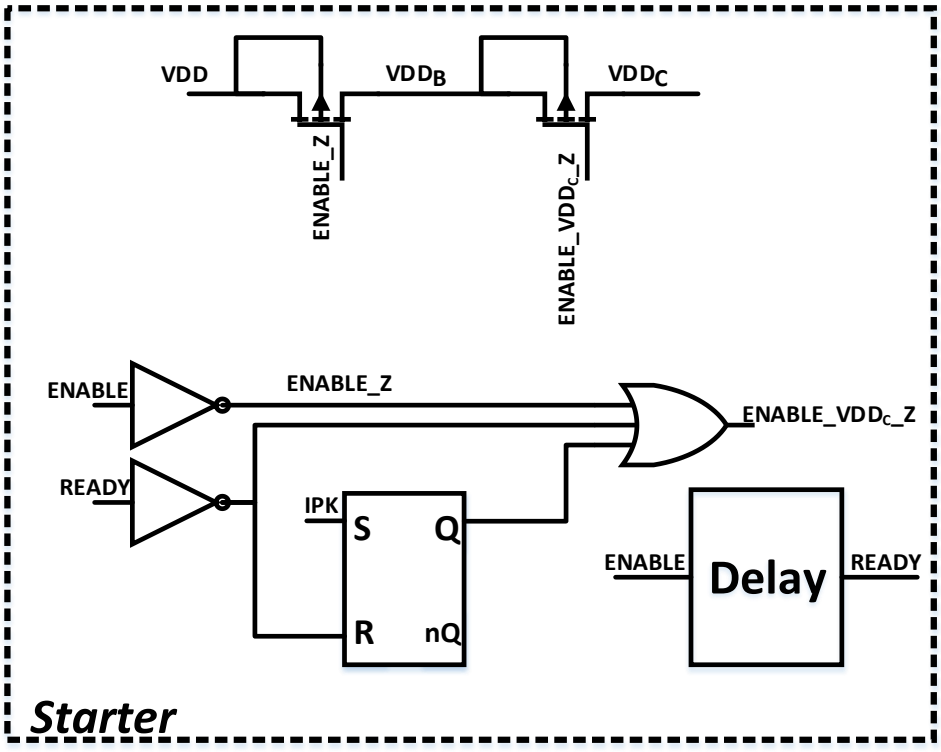

Figure 3-13 IPK Starter Component Schematic

The IPK sensor module needs to have a very fast response due to the very high inductor current slope. For this reason currents in the micro-amperes range are needed to increase the slew rate of the Comparator and the Current-Voltage Converter. But using for example 5µA of DC reference current will make the system exceed the controller's power budget of 10 µW (Figure 2-5). This current converter (Figure 3-14), or current mirror, converts the 50nA of reference current to 5µA when the supply VDD_B is available. This supply voltage is provided by the Starter and it is available immediately after the ENABLE signal is turned on by the Logic module. The current is increased by a factor of hundred using two stages of cascoded-current mirrors with gain of 10. This occurs if the transistors sizes relations shown in the schematics are implemented. The 5µA current is copied to other modules by mirroring the PMOS transistors MP_3 and MP_4.

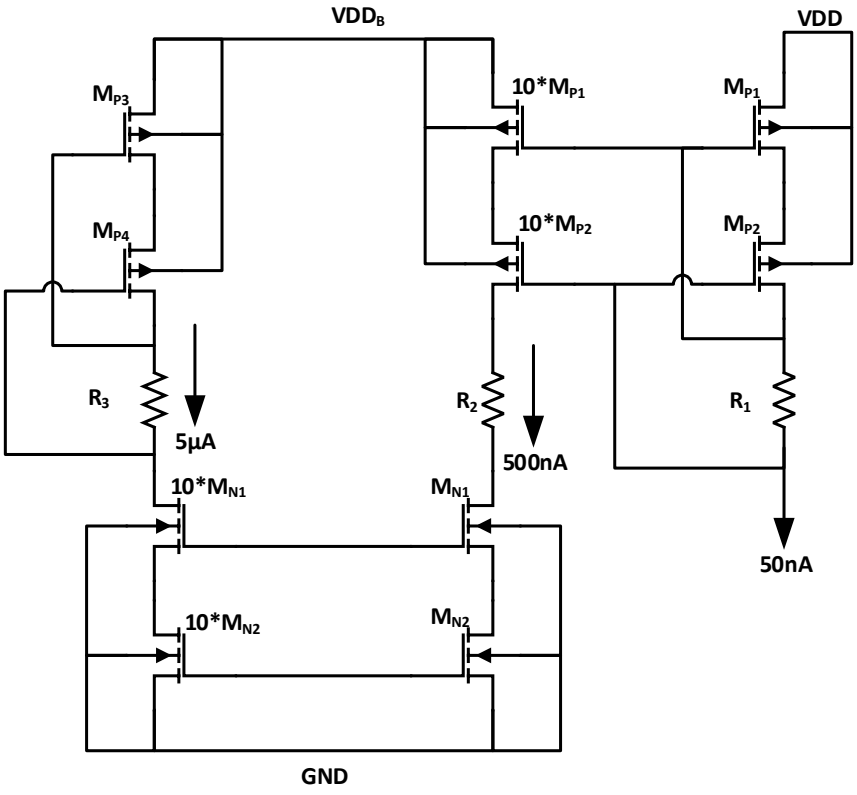

Figure 3-14 IPK Current Reference Amplifier

A more detailed diagram, than the one shown in Figure 3-10, of how the components of the IPK sensor interact is shown in Figure 3-15. There the supply nodes VDD_B and VDD_C, which are provided by the Starter, can be identified. When active time begins, S2 switch is turned on and the current amplifier starts to force the drain voltages of M_{SENSE1} and M_{N1} to the

same potential. This occurs because both NMOS transistors, M_{N1S} and M_{N2S}, are operating in the saturation region while having the same drain current I_{mirror}. Since M_{SENSE1} is K times smaller than M_{N1}, and both have the same potentials, its current will be smaller than I_L by the same amount, as shown in Equation (10). This equation is derived from the MOSFET drain-current equation for the triode region; resulting that the ratio between I_{MN1} and $I_{MSENSE1}$ is only influenced by their transistors' size. The $I_{MSENSE1}$ current is the addition of I_{SENSE} and the I_{mirror} current flowing through M_{N2S}; and I_{SENSE} is provided by the negative feedback loop formed by M_{P1S} and M_{N2S}. The sensing current is converted to the voltage V_{SENSE} by passing it through the diode-connected PMOS $M_{P2S;}$ and also M_{P3S} when the FAST signal is on. This sensing voltage is compared with a reference voltage (V_{REF}) generated by M_{P5S} and the 5µA current reference generated by the IPK Current Reference Amplifier. This novel V_{SENSE} and V_{REF} generation allows a constant peak inductor current at every supply voltage. V_{SENSE} and V_{REF} are compared with an active-latch comparator to allow high speed comparison. The inductor current at which V_{SENSE} and V_{REF} crosses will be the inductor peak current detected by the sensor; as shown in Figure 3-16 where the red, blue, and magenta graphs are the IPK current, the V_{SENSE}, and the V_{REF} voltages respectively. This peak current can be settled by K and the ratio between M_{P2S} and M_{P5S}, as indicated in Equation (11); where I_{mirror} is the current flowing through M_{N1S} and M_{N2S}, and I_{REF} is the 5µA current reference flowing through M_{P5S} in Figure 3-15.

$$\frac{I_{MN1}}{I_{MSENSE1}} = \frac{\left(\frac{W}{L}\right)_{MN1}}{\left(\frac{W}{L}\right)_{MSENSE1}} = K \qquad \textbf{(10)}$$

$$I_{peak} = \left(\left(\frac{M_{P2S}}{M_{P5S}} I_{REF}\right) + I_{mirror}\right) K \qquad \textbf{(11)}$$

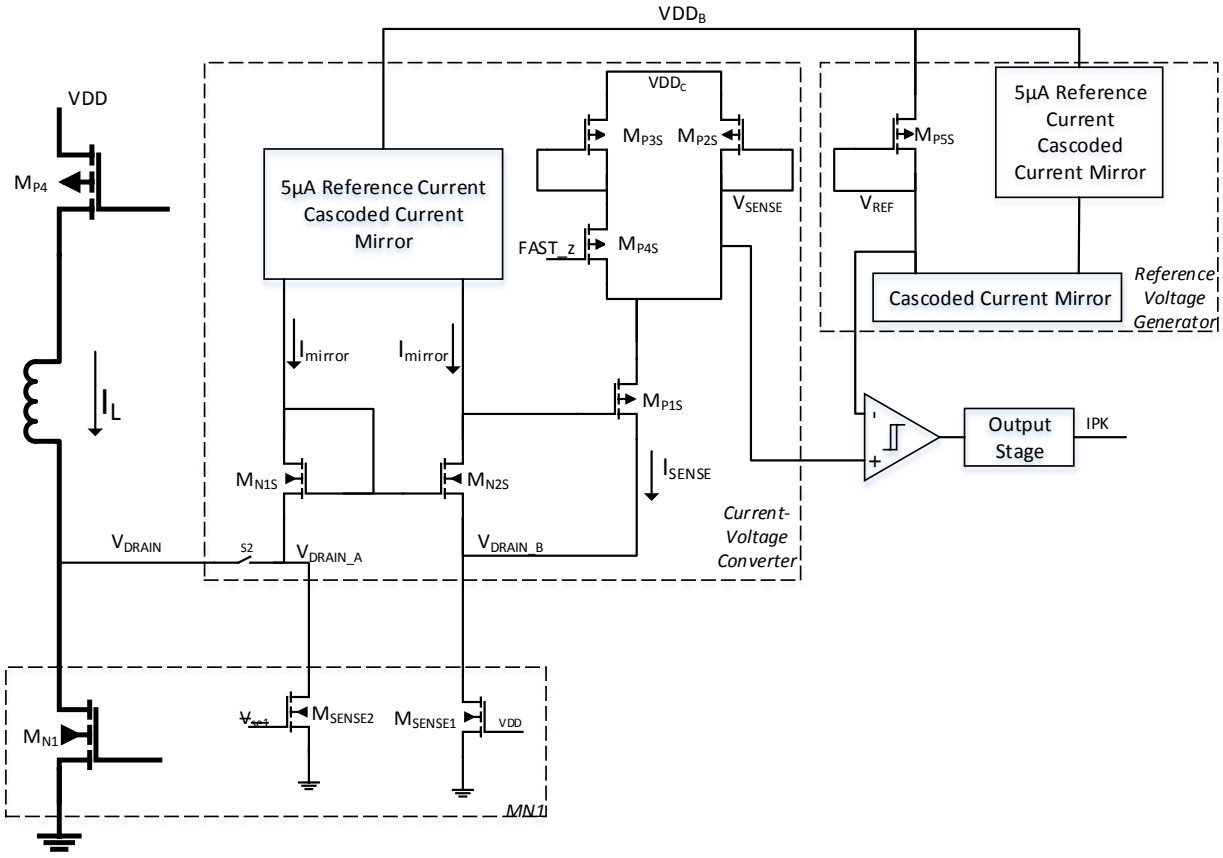

Figure 3-15 IPK Current Sensor Topology Diagram

The FAST mode is activated when the system is during the startup stage. This occurs whenever any of the output voltages is below the reference voltage by more than 0.5V. During this stage the PMOS transistor M_{P4S} is active and part of the current I_{SENSE} will flow through M_{P3S}, therefore increasing the rate between M_{P2S} and M_{P5S} in Equation (11). A higher peak inductor current will be settled in this mode, therefore increasing the regulation speed of the output nodes.

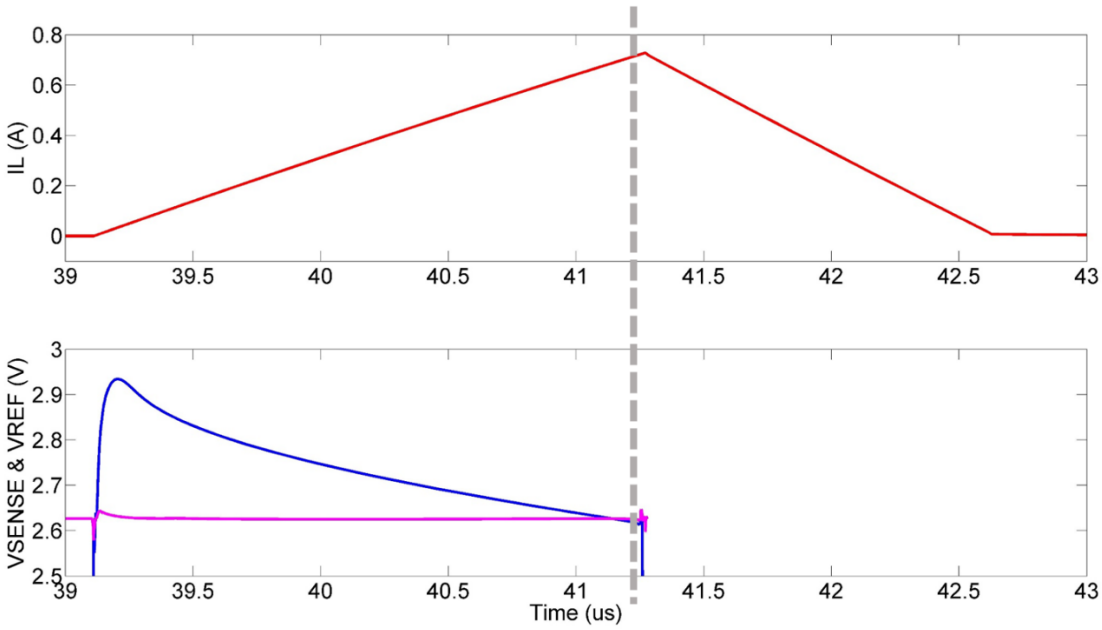

Figure 3-16 Inductor Peak Current Control, VSENSE & VREF

A latched hysteretic comparator, like the preamplifier presented in[17], was used to compare the V_{SENSE} and V_{REF} voltages inside the IPK current sensor. It consists of a NMOS input differential pair with active load, an active latch stage, and the Hysteretic CMOS Inverter used in the delay circuit shown in Figure 3-11. The schematic of the Hysteretic comparator is shown in Figure 3-17 along with a plot describing its operation in Figure 3-18. As shown in the plot, the comparator's response is very fast, under the 200 nano-seconds range. A minimum difference between V+ and V- signals is amplified in signals V_1 and V_2. As the two input signals are near crossing, V_1 and V_2 nodes approaches the DC equilibrium point in which both of them have the same voltage; which is almost one volt over GND. When this point is reached, the NMOS transistor M_{N11} will be turned on and it will pull down the V_3 voltage; therefore pulling up the output node V_{OUT}.

The output stage consist of an AND gate with the objective of masking any noise during the initialization stage. It will keep the IPK output low until a Min_{ton} time, for minimum turn on time, has passed. This time is settled by a delay circuit like the one shown in Figure 3-11 but with a current source instead of a current sink.

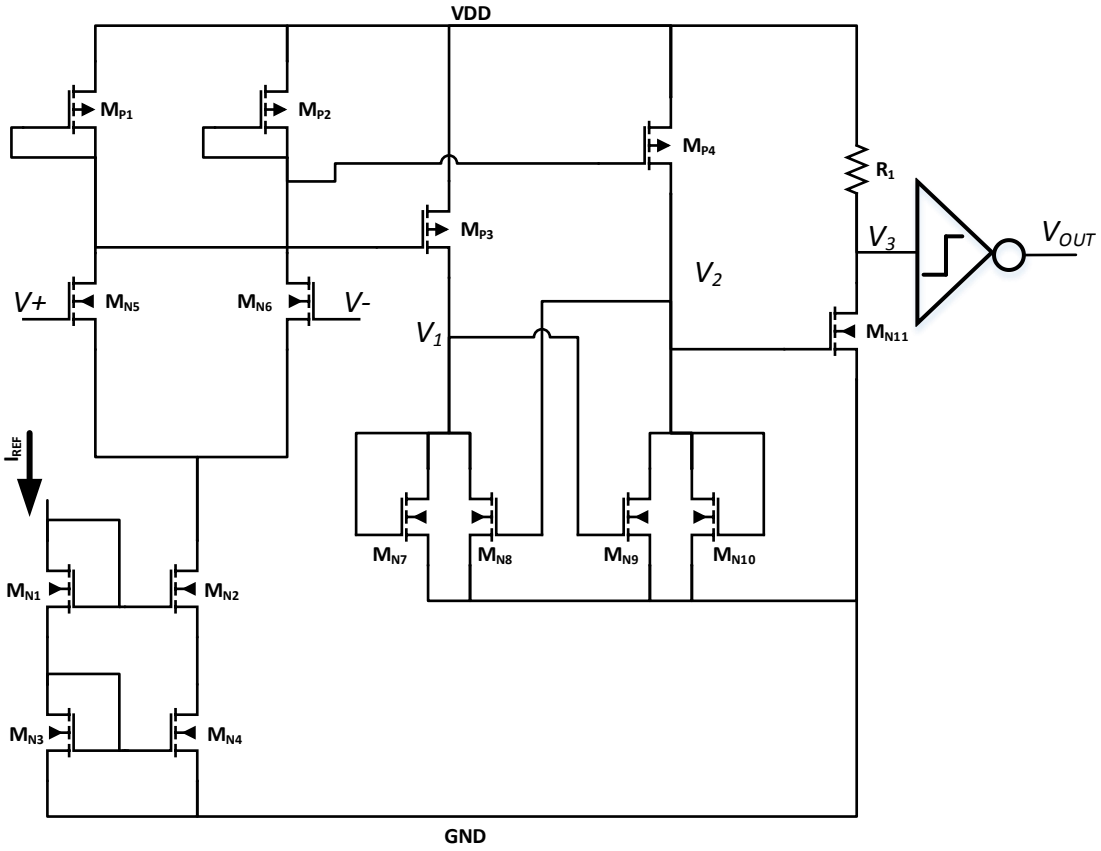

Figure 3-17 Inductor Peak Current Sensor's Hysteretic Comparator

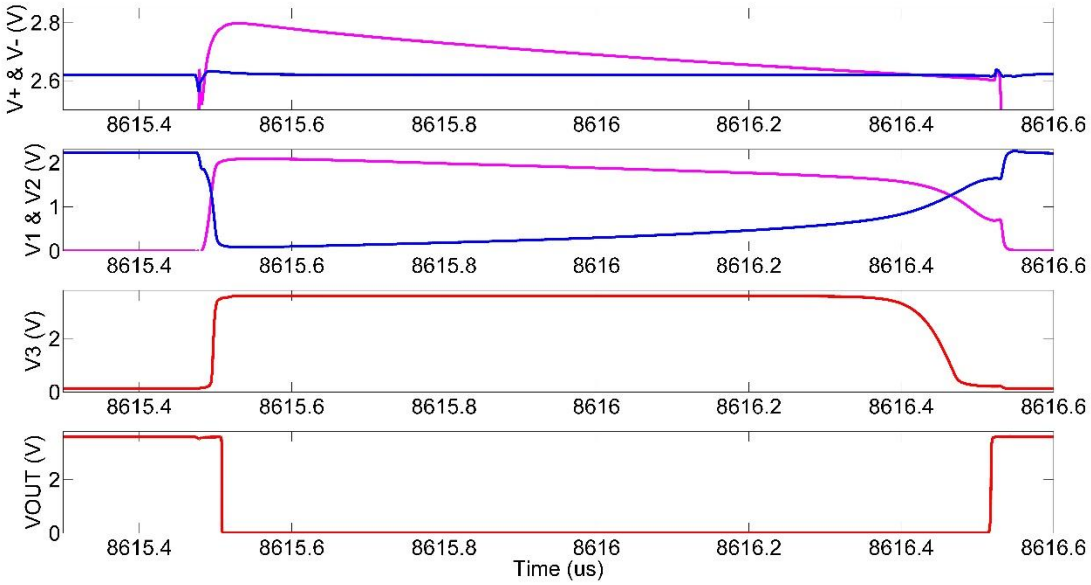

Figure 3-18 Hysteretic Comparator Operation Plot

To prove the functionality and performance of the IPK current sensor, transient simulations were done at supply voltage and process corners. The supply voltage was settled to discrete steps of 2.5V and 5.5V. The two opposite corners of processes, which are weak and strong, were combined with each VDD corner. Figure 3-19 shows the performance for the 4 different corners obtained when combining the process and supply voltage variations mentioned. The plot shows the inductor current behavior during a switching cycle (solid lines), along with the expected IPK value at each corner (dashed lines), which is calculated using Equation (11) and the simulation data presented in Table 4.

As shown in this equation, the IPK value is proportional to I_{REF} and I_{mirror} therefore inducing dependence from the reference current of section 3.2; which have variation due to process as shown in Figure 3-5. This is the reason why different expected IPK values are defined for each corner. Due to this reference current variation, different IPK values results from Equation (11). The I_{mirror} and I_{REF} values for each corner are summarized in Table 4 along with the corners specifications.

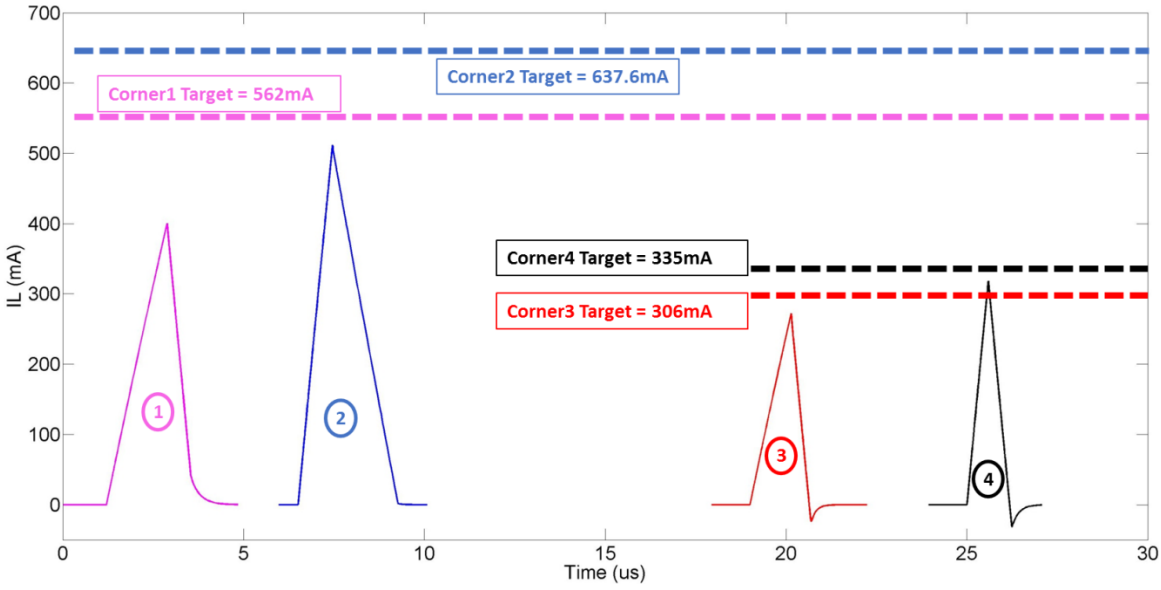

Figure 3-19 IPK Module Performance Plot

But in addition to the expected IPK value variation, a negative offset from that value could be noticed in Figure 3-19, meaning that the actual IPK value is less than the expected value. From the IPK Current Sensor Topology Diagram shown in Figure 3-15, the switch S2 isn't an

ideal switch; and a parasitic resistance $R_{PAR,S2}$ exists on it. This $R_{PAR,S2}$ creates and offset in $V_{DRAIN\_A} = V_{DRAIN\_B}$ over V_{DRAIN} as described in Equation (12).

$$V_{DRAIN\_A} = V_{DRAIN} + R_{PAR,S2} I_{mirror} \quad \textbf{(12)}$$

This offset is applied to the sense transistor M_{SENSE1} drain, and the assumption of exactly same terminal voltages between M_{SENSE1} and M_{N1} isn't entirely true. Of course, the error doesn't affect the functionality for generating the sense current I_{SENSE}, but a different value of K in Equation (11) will be obtained. This K value is the ratio between M_{N1} and M_{SENSE1} transistors, as shown in Equation (10), and its value will be less than the 1000 times ratio designed. The value of K's reduction is dynamic, and it is inversely proportional to the inductor current, or V_{DRAIN} voltage; meaning that the larger the V_{DRAIN} voltage is, the smaller the error's effect would be.

The inductor peak current IPK value, including the effect of S2 switch parasitic resistance, could be calculated by Equation (13); in which K_{ERROR} is the error percentage of the K value.

$$I_{peak} = \left(\left(\frac{M_{P2S}}{M_{P5S}} I_{REF} \right) + I_{mirror} \right) K * (1 - K_{ERROR}) \quad \textbf{(13)}$$

Table 4 contains the simulation data for the inductor current when the V_{SENSE} and V_{REF} voltages of Figure 3-15 are equal, "I_L-Sim" column, and the results of Equation (13) for each corner. As could be noticed, these two values are very near for each corner, therefore proving the I_{peak} value equation accuracy. The K_{ERROR} is calculated using Equation (14), which depends on the ratio between the actual values of I_L and the addition of I_{SENSE} and I_{mirror}.

$$\frac{\left(1000 - \left(\frac{I_L}{I_{SENSE} + I_{mirror}}\right)\right)}{1000} = K_{ERROR} \quad \textbf{(14)}$$

Table 4 IPK Simulation Data

Corner	Process	VDD	I_{mirror}	I_{ref}	I_{sense}	I_L-Sim	K_{ERROR}	I_L-EQ	IPK-EQ	IPK-Sim
Units		VDD	µA			mA		mA		
1	Strong	2.5	48.02	4.8	506.51	373.57	33%	378.70	562.15	400.4
2		5.5	52.03	5.5	588.61	467.64	27%	465.44	637.63	510.37
3	Weak	2.5	26.313	2.6	277.27	226.718	25%	228.75	306.31	273.03
4		5.5	27.5	2.9	312.93	259.856	24%	256.30	335.77	318

The columns IPK-EQ and IPK-Sim in Table 4 show the data of the IPK calculation using Equation (11) and the IPK data from the simulations. The simulation data for IPK value shows that it is greater than the current when V_{SENSE} and V_{REF} are the same; being the delay of the Comparator response the responsible one.

Although the real IPK value is less than the expected one, it doesn't affect the functionality of the device. This is because the error is negative and no excessive inductor current, that could damage the device, is reached. On each corner, the error in the IPK value is less than 100µA, which represents 0.016% of the IPK value.

This module's layout is located right down of the Reference System's layout, as shown in Figure 3-1. It was intentionally located near the reference system, far from the power stage, to avoid noise due to power paths. Matching was considered between the Current-Voltage Converter and the Reference Voltage Generator; specifically between PMOS transistors M_{P2S}, M_{P3S}, and M_{P5S} of Figure 3-15. These three transistors were symmetrically distributed as shown in Figure 3-21. As in all the modules, every transistor current mirror was matched using the interdigitation method[16]. The NMOS transistors M_{SENSE1} and M_{SENSE2} in Figure 3-15, which are K times smaller than power transistor M_{N1}, are located in the M_{N1} module in Figure 3-1 to achieve good matching between them. The location of the IPK sensor's components in the layout is shown in Figure 3-20. More detailed layout vs schematic components identification is shown in Appendix A – Cellviews and Layouts.

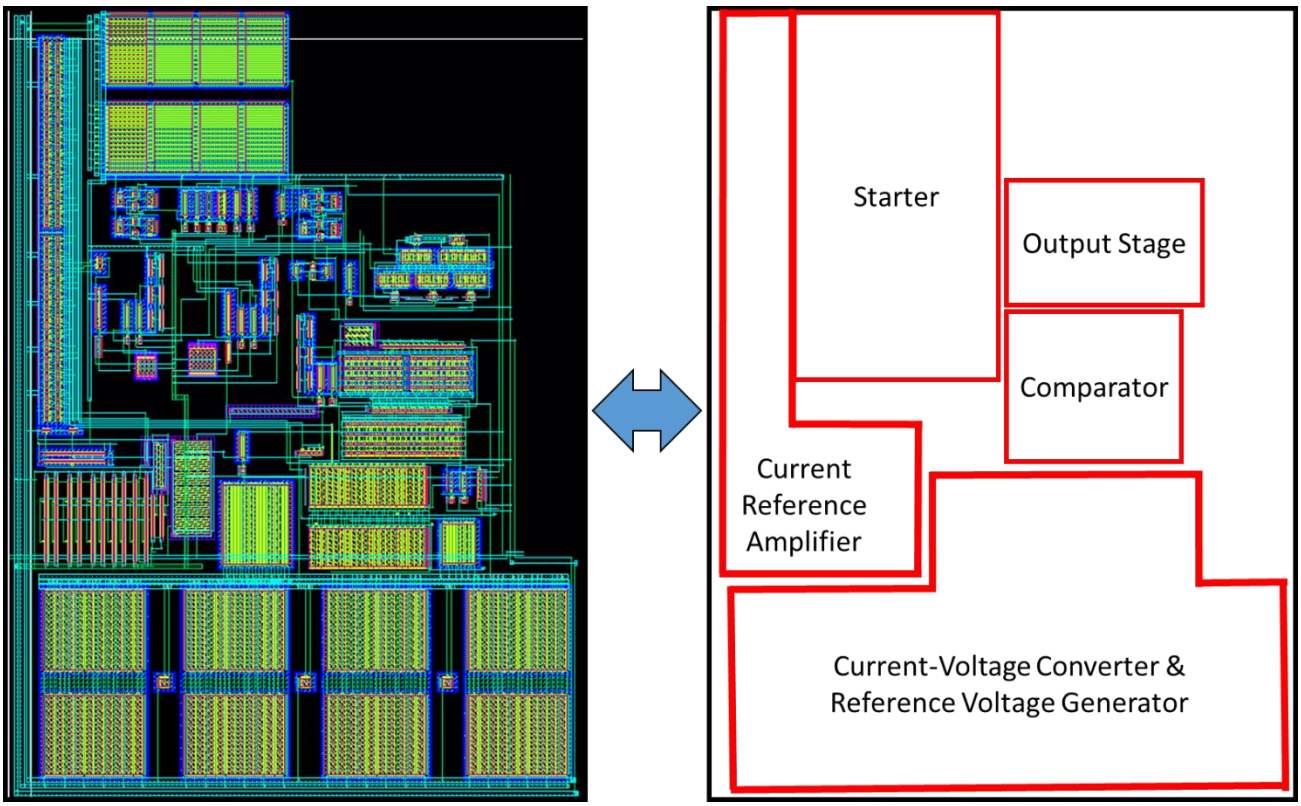

Figure 3-20 Inductor Peak Current Sensor's Layout

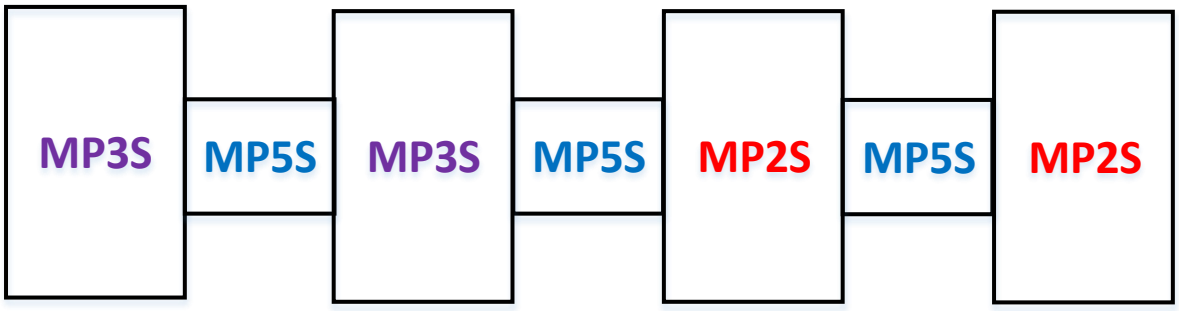

Figure 3-21 IPK Current-Voltage Converter & Reference Voltage Generator Matching

3.4 Zero Current Detector (ZCD)

After inductor peak current value is reached, de-energization stage will begin and inductor current will start decreasing. If it overpasses much below zero then efficiency will be degraded because the negative inductor current will be provided by the output capacitors. For this reason a very precise zero current detector (ZCD) is needed to avoid negative inductor currents. A similar IPK topology was implemented to detect the point when the current decreases near to zero; but using the approach presented in [13]. The same standby zero current loss of IPK is required for this module to maintain a very low quiescent current, and therefore not exceed the controller power budget in Figure 2-5.

The same block diagram of Figure 3-10 could be used to describe the ZCD module, but without the Starter module. It‘s not needed because this module is initialized with the same ENABLE signal provided to the IPK sensor, therefore being initialized at the same instant that the IPK sensor initializes. Then when the de-energization stage is started, the ZCD module is already initialized.

The Current Reference Amplifier is exactly the same used in the IPK sensor. It receives a current sink of 50nA, and amplifies it a hundred times to get a 5µA current reference during the time ENABLE stays high. Its schematic is shown in Figure 3-14. The same occurs with the Voltage Reference Generator; since it is exactly the same used in IPK sensor (Figure 3-15). It generates, from the 5µA current reference, a reference voltage V_{REF} to be compared with the V_{SENSE} voltage generated by the Current-Voltage Converter.

The largest difference between the current sensors is their Current-Voltage Converter component, as shown in Figure 3-23. As difference from IPK, the current amplifier forces the voltage V_1 to GND instead of forcing it to the power NMOS’s drain voltage, as occurs in IPK. This occurs due to the fact that the NMOS transistors M_{N1S} and M_{N2S} are operating in saturation with the same drain current I_{mirror}. Since the sense transistor M_{SENSE1} is K times smaller than M_{N2} its current (I_{SENSE} + I_{mirror}) will be K times smaller than the inductor current because both have the same terminal voltages. This sensing current is provided by the negative feedback network formed by the PMOS transistor M_{P1S}, and by M_{N2S}. The sensing voltage V_{SENSE} will be the gate

to source voltage of the diode connected transistor M_{P2S}. V_{SENSE} is compared with the reference voltage V_{REF} generated by the Reference Voltage Generator. They are compared by the same hysteretic comparator used in the IPK sensor, shown in Figure 3-17. When V_{REF} and V_{SENSE} crosses, while in the de-energization stage, the ZCD output signal V_{OUT} will be turned on indicating to the controller that the inductor current has reached the ZCD value; as shown in Figure 3-22. This ZCD can be settled by K and the ratio between M_{P2S} and M_{P5S}, as indicated in Equation (15); where $I_{mirrror}$ is the current flowing through M_{N1S} and M_{N2S}, and I_{REF} is the 5µA current reference flowing through M_{P5S} in Figure 3-23.

$$I_{ZCD} = \left(\frac{M_{p2S}}{M_{p5S}} I_{REF} + I_{mirror}\right)K \qquad \textbf{(15)}$$

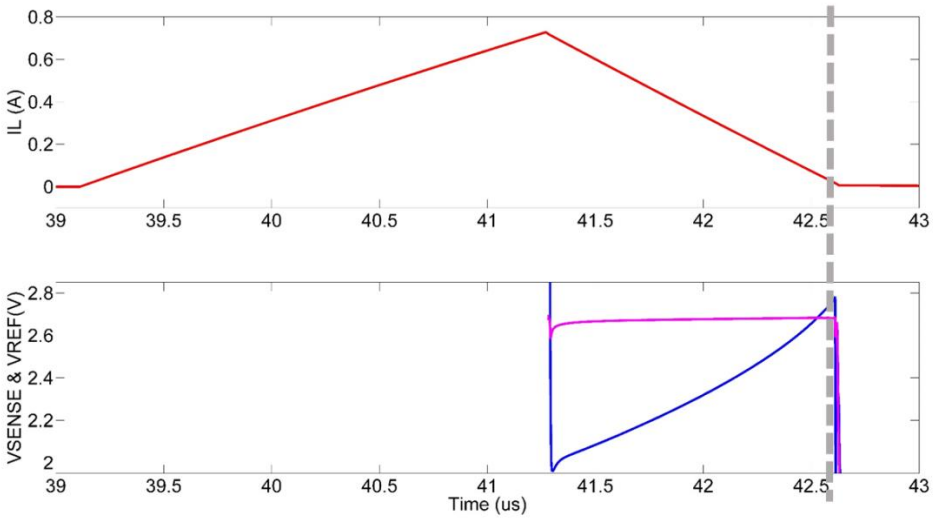

Figure 3-22 Inductor ZCD Current Control, VSENSE & VREF

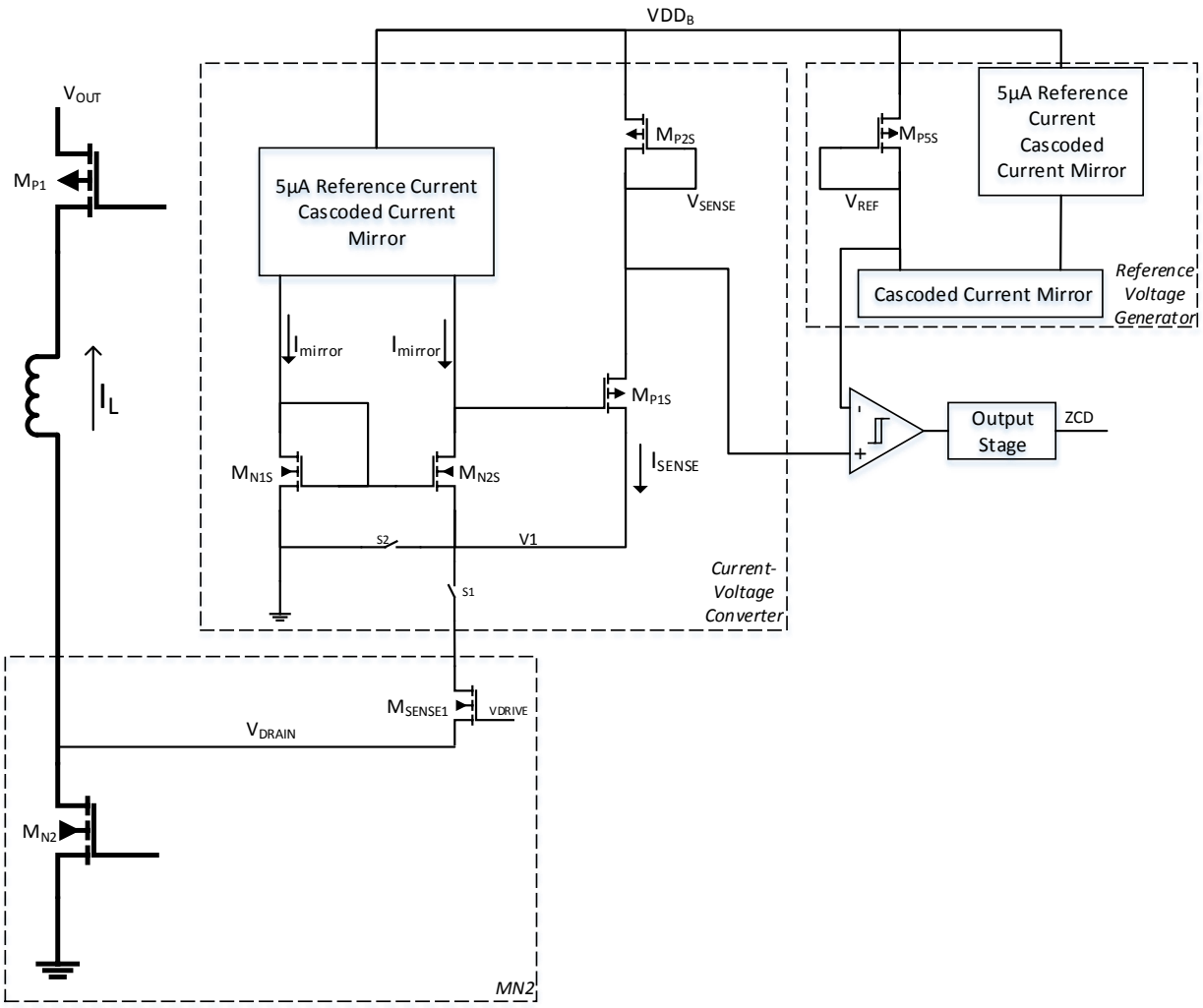

Figure 3-23 ZCD Topology Diagram

To prove the functionality and performance of the ZCD current sensor, transient simulations were done at different supply voltage and process corners; as they were done to corroborate the IPK sensor performance in Figure 3-19. The supply voltage was varied in 2 discrete steps of 2.5V and 5.5V. The two opposite corners of process, which are weak and strong inversions, were combined with each VDD corner.

Similar to the IPK sensor, parasitic resistances affects the accuracy of this component. The value of K in Equation (15) is changed due to these parasitic resistances, therefore changing the value of I_{ZCD}. This new I_{ZCD} value could be calculated using Equation (16), in which K_{ERROR} value is calculated using Equation (17). The I_L, I_{mirror}, and I_{SENSE} values are simulation data, which are shown in Table 5.

$$I_{ZCD} = \left(\left(\frac{M_{P2S}}{M_{P5S}} I_{REF}\right) + I_{mirror}\right) K * (1 - K_{ERROR}) \quad \textbf{(16)}$$

$$\frac{\left(500 - \left(\frac{I_L}{I_{SENSE} + I_{mirror}}\right)\right)}{500} = K_{ERROR} \quad \textbf{(17)}$$

The same data collected for the IPK sensor performance, but applied to the de-energization stage, was taken for this component. Information like the I_{mirror}, I_{ref}, I_{SENSE}, and I_L where measured at the moment when the V_{REF} & V_{SENSE} voltages intersects. The objective of using that instant of time is to prove the accuracy of the equations presented in this section. I_L-Sim shows the simulation data for I_L when that instant occurs, and I_L-EQ shows the result of Equation (16), but using the data obtained from the simulations. As could be noticed, these columns have very similar values for each corner; hence proving the accuracy of Equation (16). The different values at different corners are due to the variation in I_{ref}, which is proportional to the system's reference current, discussed in section 3.2.

Table 5 ZCD Simulation Data

Corner	Process	VDD	Imirror	Iref	Isense	I_L-Sim	K_{ERROR}	I_L-EQ	ZCD-EQ	ZCD-Sim
Units		VDD	uA			mA		mA		
1	Strong	2.5	48.05	4.8	144.2	103.84	-8%	104.31	96.57	41
2		5.5	50.1479	5.3	160	22.209	79%	22.16	104.82	42
3	Weak	2.5	25.7434	2.6	75.197	59.199	-17%	60.49	51.57	-15
4		5.5	26.9516	2.9	84.3	10.9712	80%	11.09	56.24	-26

The column ZCD-Sim contains the ZCD values obtained from the simulations. They are below the I_L-EQ column values due to the delay provoked by the comparator's response delay; which also occurs in the IPK sensor. The sense transistors' size was designed to provide the optimum performance inside the entire process and supply voltage window. ZCD-EQ shows the result of Equation (15), which doesn't consider the effect of parasitic resistances; therefore resulting deviated from the I_L-EQ values.

Although non-ideal ZCD value is reached, which is I_{ZCD}=0, system's functionality is maintained with the optimum values that the process allows. The necessary sensing and comparisons are implemented successfully keeping the component's functionality at every process and supply voltage corners. This converts this circuit in a universal current sensor that

could be used whenever a transistor's drain current needs to be measured. In addition, the 50nA quiescent current, achieved by the VDD_B supply switch, reduces the power consumption of this component inversely proportional to its frequency of operation.

This module's layout is located to the left of the Inductor Peak current sensor IPK, as shown in Figure 3-1. It was intentionally located near the reference system, far from the power stage, to avoid noise due to power paths. The same matching issues in the IPK module were considered in the ZCD sensor; therefore considering the matching between the Current-Voltage Converter and the Reference Voltage Generator; specifically between PMOS transistors M_{P2S}, and M_{P5S} of Figure 3-23. These two transistors were symmetrically distributed as shown in Figure 3-25. As in the IPK sensor, and all the other modules using current mirrors, they were matched using the interdigitation method[16]. The NMOS transistor M_{SENSE1}; which is K times smaller than power transistor M_{N2}, in Figure 3-23 are located in the M_{N2} module in Figure 3-1 to achieve good matching between them. The location of the ZCD sensor's components in the layout is shown in Figure 3-24. More detailed layout vs schematic components identification is shown in Appendix A – Cellviews and Layouts.

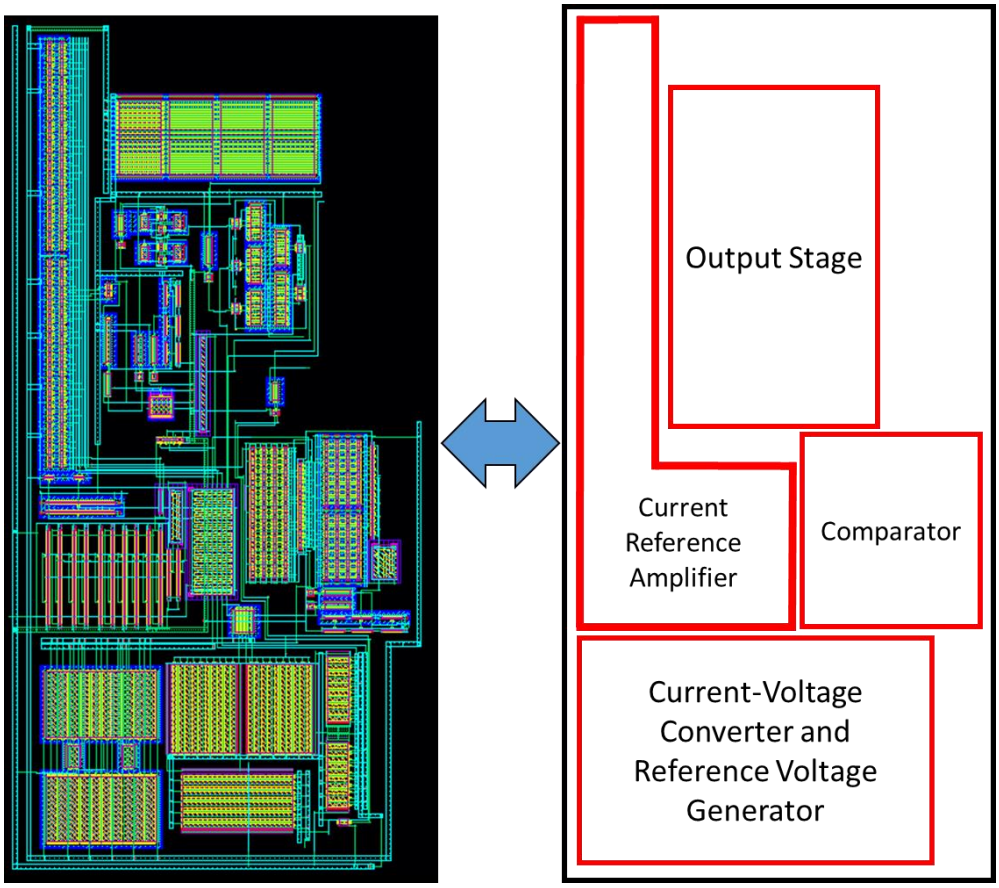

Figure 3-24 ZCD Sensor's Layout

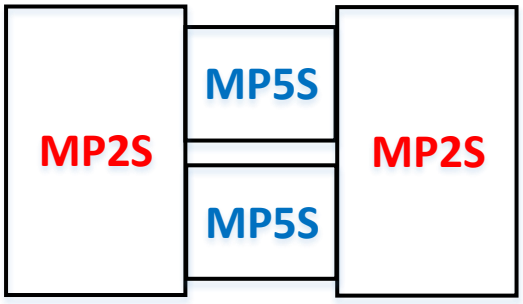

Figure 3-25 IPK Current-Voltage Converter & Reference Voltage Generator PMOS Distribution

3.5 Logic

As mentioned in section 2.2, a digital controller is needed to control the SIMO converter due to its DCM operation. It needs to be completely asynchronous, since a very fast oscillator will require more power than the controller power budget obtained in Figure 2-5. This module contains the circuits implementing such digital controller that work together with the current sensors IPK and ZCD already discussed, and all the other modules.

The Logic module can be divided into three main components. The first one being the Asynchronous State Machine to define the energization/de-energization stages timing, the second one being the combinational logic circuit controlling the State Machine, and the third one being the combinational logic circuit to control the power switches depending on the active SIMO converter's stage. A block diagram of the Logic module is shown in Figure 3-26. The blocks "Initalization & Next Cycle Pulse Generator" and "Cycle Terminator" contains all the combinational logic required to control the block "Asynchronous State Machine"; which contains the asynchronous sequential logic circuits required to control the SIMO converter stages' timing. The block "Power Switches Control Output Stage" controls the signals moving the system's power transistors, through the Level Shifters and Drivers, depending on the active stage settled by the state machine.

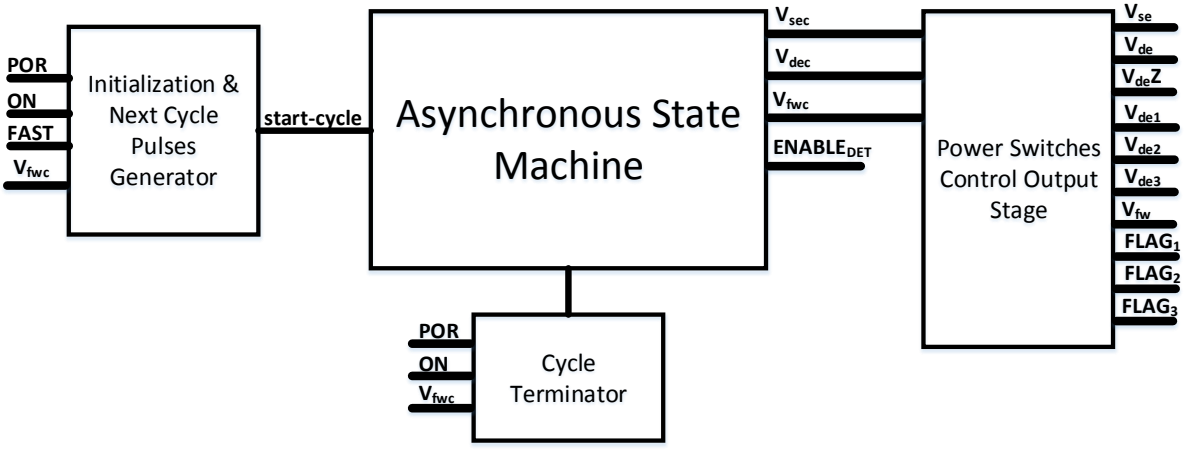

Figure 3-26 Logic Module's Block Diagram

The "Initialization & Next Cycle Pulses Generator" generates the rising edges of the signal start-cycle required to start the first state of the state machine, Figure 3-27. The decision of

when to send the pulse signal start-cycle depends on the values of POR, ON, FAST, and V_{fwc} signals. It has two sub blocks which are the pulse generator for the system initialization and the pulse generator for the consecutive cycles. When the system supply is connected, the device will turn on with the consequence of turning on the Power-on-Reset signal POR. When this occurs, a delayed pulse that will contain the rising edge needed to start the state machine, will occur; therefore starting the first energization stage. This part of the circuit will operate only when the entire system is turned on. The "Rising Edge Pulse Generator" block shown in Figure 3-27 consists of a two input AND gate with two time-offset signals; and its circuit is shown in Figure 3-28. When the input signal goes high, both AND gates' input voltages will be different for a time defined by the capacitor, therefore producing a rising edge when the delay time has passed.

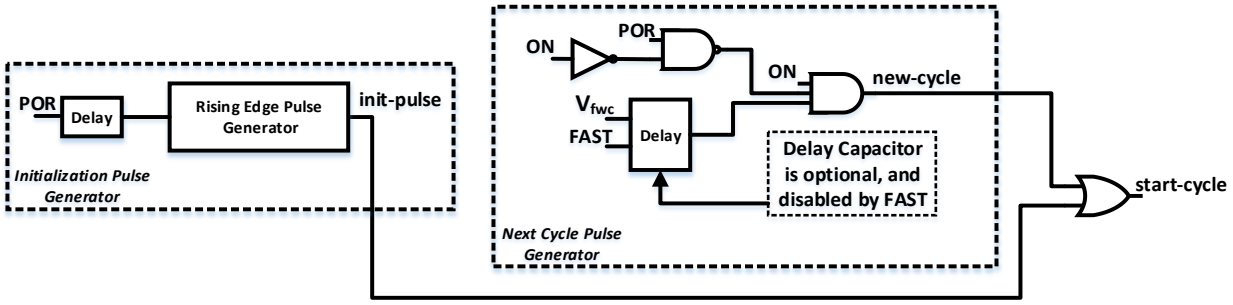

Figure 3-27 Initialization & Next Cycle Pulses Generator Schematic

The rest of the pulses needed to start switching cycles will be managed by the "Next Cycle Pulse Generator" component. Each time a switching cycle is finished, the signal V_{fwc} will be turned high by the state machine; therefore forcing the Delay block's output to high. After this, whenever a switching cycle is needed ON and POR signals will be high, and the new-cycle signal will rise to high, and with it the start-cycle signal; therefore starting the new switching cycle. The signal V_{fwc} will be low when the switching cycle is started; and it will force the new-cycle and start-cycle signals back to low. The reason of having a delay block in this circuit is to provide a wait time between each switching cycle, with the objective of providing enough stabilization time to the output comparators. Not having the delay will result in bad load regulation due to the slow response of the system's feedback loop to fast changes in the output voltages. But when fast output voltage changes are required, like during the startup stage, the FAST signal is activated, and with it the delay block's capacitor is disconnected to reduce the wait time. The "Cycle Terminator" block only consists of a three-input AND gate that sends a logic high whenever the ON signal is turned off, indicating that no switching cycle is needed.

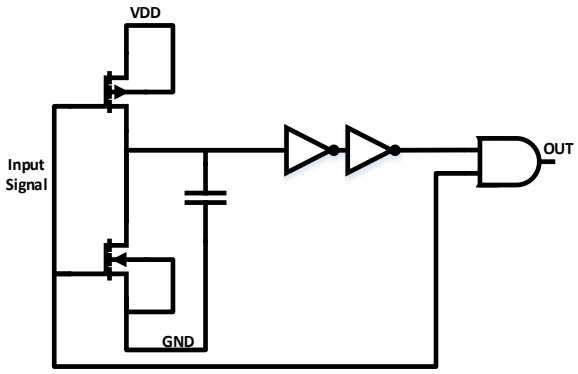

Figure 3-28 Rising Edge Pulse Generator Schematic

The state machine have 4 different states; from which the first one is for the current sensors initialization and stabilization, the second one is for the energization stage, the third one is for the de-energization stage, and leaving the fourth one for the freewheeling stage. Its schematic is shown in Figure 3-29. Every flip-flop has a logic high in its D input; meaning that every time a rising edge occurs in its triggered input, its Q output will be changed to a logic high. The same occurs with the R (Reset) input but instead of the Q output resulting in a logic high, a logic low will be obtained in it.

When a rising edge occurs in the start-cycle signal, provided by the Initialization & Next Cycle Pulses Generator component previously discussed, the $ENABLE_{DET}$ signal will be a logic high; and the inductor current sensors IPK and ZCD will start their initialization and stabilization procedures. The Delay block in the FF2 flip-flop's edge triggered input provides the necessary wait time until the inductor current sensors finishes the initialization and stabilization process. This delay is settled by choosing the Delay module's correct capacitor value. This state of current sensor initialization will end when the wait time ends; therefore beginning the energization state.

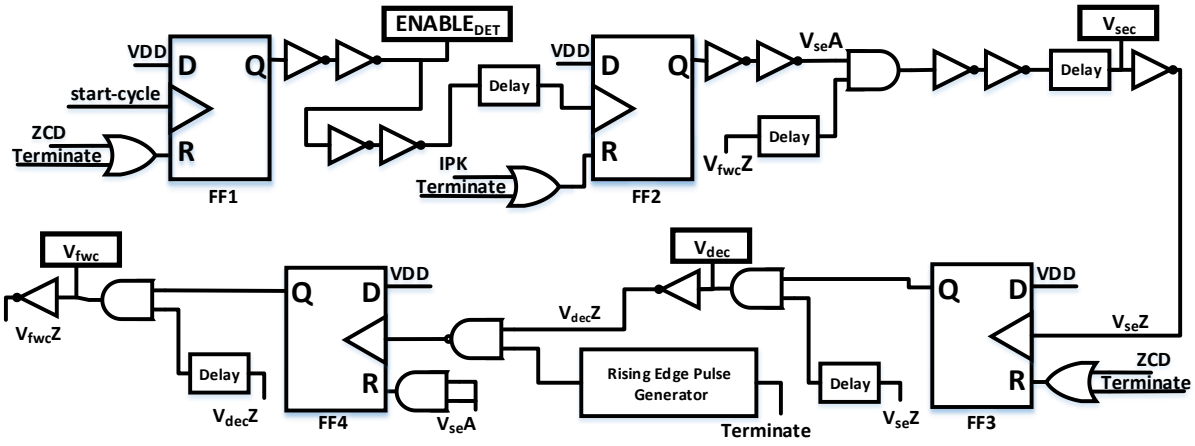

Figure 3-29 Logic Module's Asynchronous State Machine

The energization state starts when the signal V_{sec} is a logic high. This occurs a wait time after $V_{se}A$ turns to high, which happens when the FF2 flip-flop edge triggered input receives the rising edge of $ENABLE_{DET}$; and a wait time after $V_{fwc}Z$ turns to a logic high. During this stage the inductor current will start to increase until the IPK signal turns to high due to the detection of the inductor's peak current value (Section 3.3). This will reset the FF2 flip-flop's Q output to a logic low, therefore forcing V_{sec} to a logic low and finishing the energization state. Right after V_{sec} turns to low, the Q output of FF3 flip-flop will be turned to high; and also the signal V_{dec} after a delay time has passed. During this state the inductor current will be decreasing while the active output voltage will be increasing due to the inductor energy being sent to it. When the inductor current reaches zero the ZCD is activated; therefore resetting the FF3 flip-flop Q output to zero. This will start the Freewheling stage, by turning to high the FF4 flip-flop Q output due to the rising edge provoked by the V_{dec} signal falling edge. During this stage the $ENABLE_{DET}$ signal is reset to logic low, and with it the inductor current sensors IPK and ZCD are turned off. In addition, during this state the inductor terminals are shorted by turning on the freewheeling transistor M_{P5} (Figure 2-10); with the purpose of reducing the voltage oscillations in its terminals. This state will remain active until another switching cycle is required by putting a rising edge in the start-cycle signal. The simplified state diagram illustrating the state machine's functionality is shown in Figure 2-9 of section 2.2.

As explained above, the Asynchronous State Machine only controls the timing of the four stages of a switching cycle no matter which output is receiving charge. The "Power Switches

Control Output" component controls the decision of which output will receive the inductor energy each switching cycle. It is decided by priority; in which the priority order, from the highest to the lowest one is: V_{OUT3}, V_{OUT1}, and V_{OUT2}, in Figure 2-10. This component's schematic is shown in Figure 3-30; where V_{COMP_OUT3}, V_{COMP_OUT1}, and V_{COMP_OUT2} are the signals requiring switching cycles for the V_{OUT3}, V_{OUT1}, and V_{OUT2} outputs respectively. Priority is implemented by the $FLAG_1$, $FLAG_2$, and $FLAG_3$ signals; since to activate the V_{OUT2} output for receiving charge, $FLAG_1$ and $FLAG_3$ need to be already low indicating that the other two outputs, of higher priority, don't need charge. The same occurs for output V_{OUT1}, which needs $FLAG_3$ to be low in order to receive charge. $ENABLE_{SW}$ and $ENABLE_{OUT\_1\_2}$ pins, are provided externally for testing purposes. $ENABLE_{SW}$ enables the power switches; while $ENABLE_{OUT1\_2}$ enables only V_{OUT1} and V_{OUT2} but has no effect on V_{OUT3}.

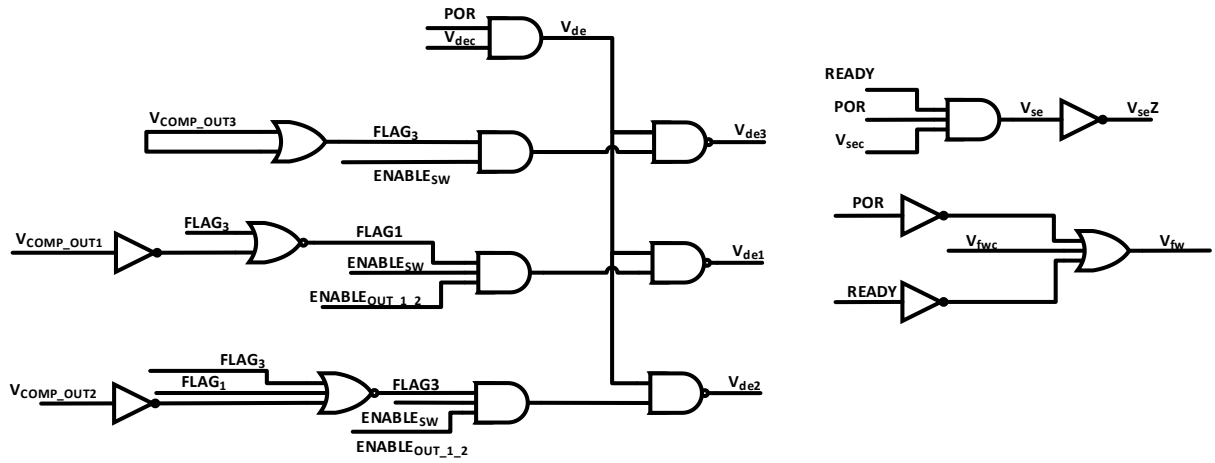

Figure 3-30 Logic Module's Power Switches Control Output

The IPK and ZCD current sensors performance also proves the performance of the Logic module, since otherwise malfunction would have been detected. Figure 3-31 shows the Asynchronous State Machine's signals timing. As shown in it, when the start-cycle pulse happens $ENABLE_{DET}$ rises to a logic high to turn on the current sensors; and after a wait time V_{se} and V_{fw} turns on and off respectively. Then when the IPK occurs, V_{de} turns on after V_{se} is turned off; and with it the de-energizing stage starts. Immediately after the ZCD pulse occurs, the de-energizing stage is finished by turning off V_{de}; and the freewheeling stage is started by turning on the V_{fw} signal. This process will be repeated each time a switching cycle is required.

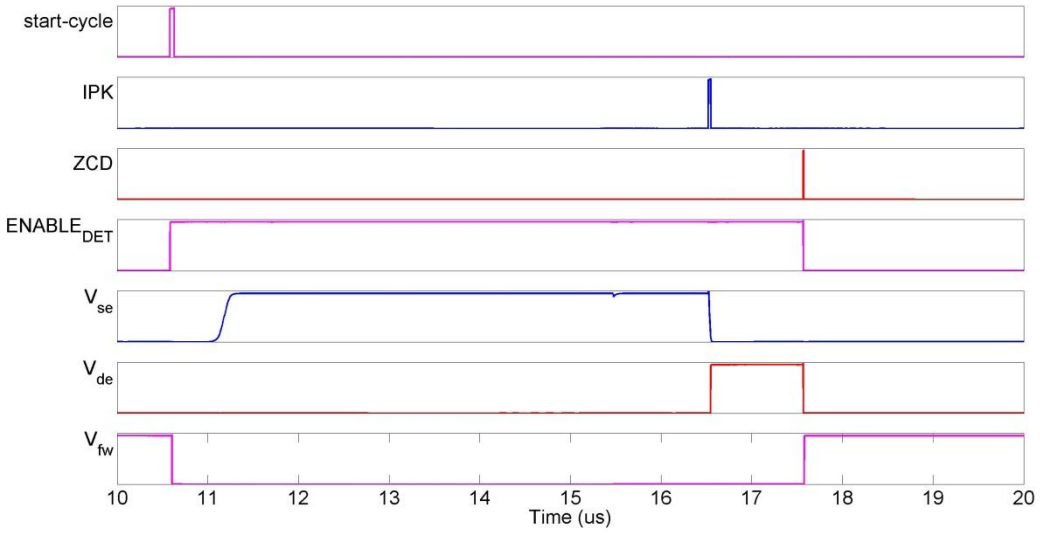

Figure 3-31 Logic Module's State Machine Performance

All the circuits in this module are digital, hence not requiring any symmetrical distribution for layout matching, like in the previously discussed components Reference System, IPK and ZCD. Due to this fact, the main goal when designing the layout was to reduce the module's area as much as possible. Figure 3-32 shows the layout of the Logic module along with the layout map. It is divided into two main parts; which are the Asynchronous State Machine and the Combinational Logic Circuits. As discussed in Figure 3-29 the Asynchronous State Machine contains all the sequential logic circuits (D-latched Rising Edge-triggered Flip Flops) that control the switching cycle's timing. The Initialization & Next Cycle Pulses Generator are included inside the Combinational logic block.

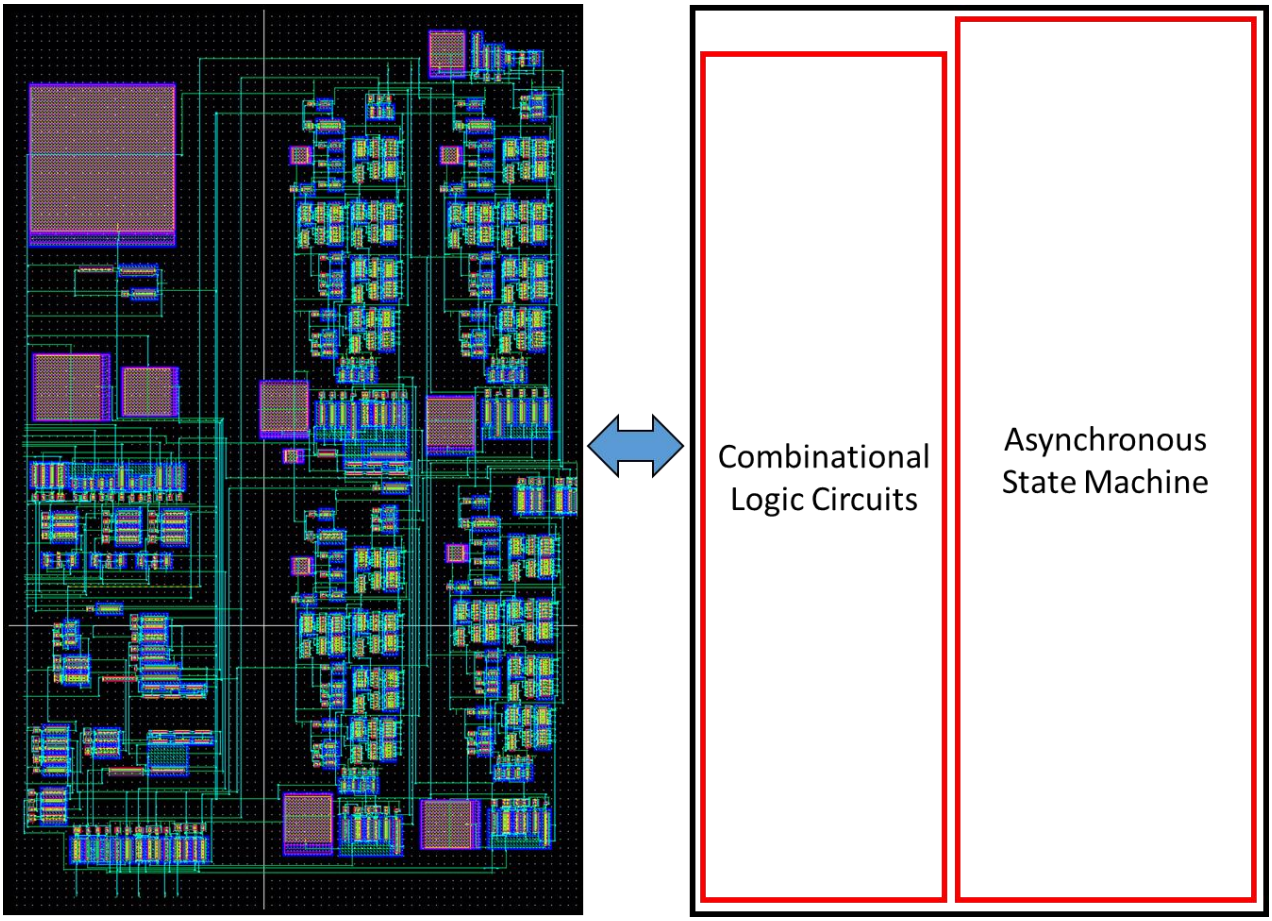

Figure 3-32 Logic Module's Layout

3.6 Charge Monitor (CharMon)

This system's objective is to automatically regulate three output voltages to some specific values without the intervention of external calibration. This means that it needs to have a closed-loop controller to constantly monitor the three output voltages and request switching cycles when it's required. That's the purpose of this Charge Monitor module; its mission is to monitor the three output voltages and notify the Logic module whenever charge is needed to be sent to any of them.

The Charge Monitor could be divided into two main components, which are the Voltage Dividers and Comparators blocks. Its block diagram is shown in Figure 3-33. The Voltage Dividers block receives as input the three output voltages of the system, and outputs three different proportions of them for each output node. This component contains three voltage divider circuits, one per each output node, which is shown in Figure 3-34.

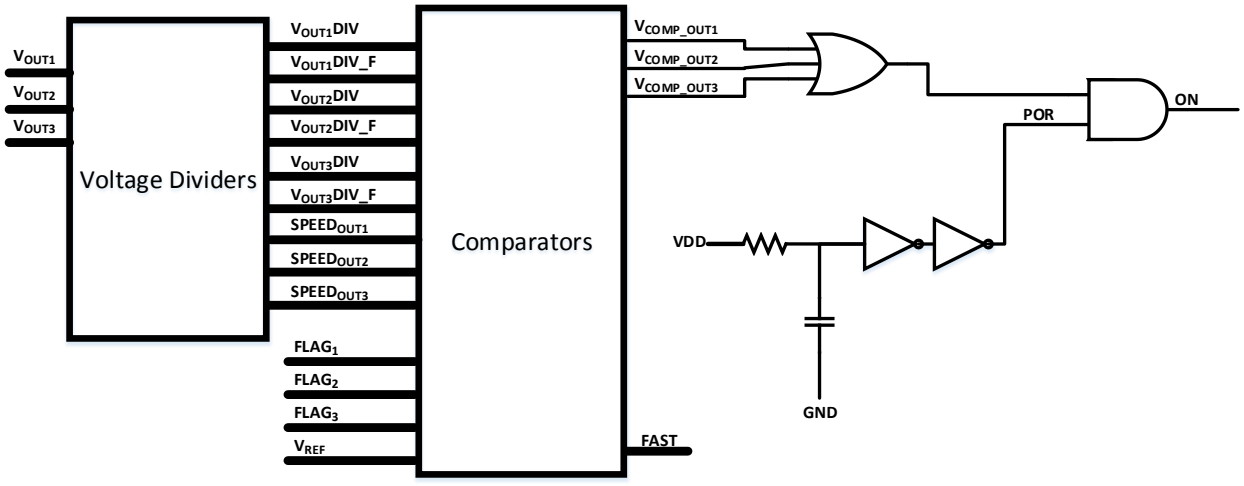

Figure 3-33 Charge Monitor Block Diagram

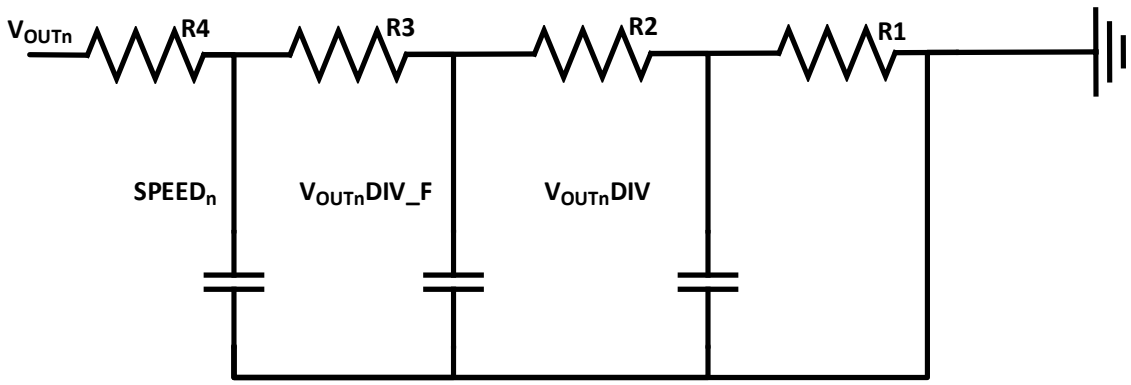

Figure 3-34 Voltage Divider Circuit

Each voltage divider circuit is designed to have a constant DC current of 150nA flowing through it. This very low current was chose to reduce losses and increase efficiency. At nominal corners the lowest output current will be 10µA, therefore having a maximum output voltage divider current rate of 1.5%; which is acceptable. The disadvantage of having such a low current in these circuits is that a slow response will be achieved. To counter this disadvantage, two components were added; being the first one the three capacitors of Figure 3-34, added to filter noise coming from the comparators input pins. When comparators internal nodes changes very fast, noise could appear at its input nodes due to the parasitic capacitances; and these capacitors serves as low pass filters to reject the noise. Not filtering that noise could result in voltage changes in the sensing network nodes that could take much time to stabilize again due to its very low response. The second thing done to counter the effect of the low current in the voltage dividers was to add a wait time between each switching cycle, as explained in the Logic module discussion in section 3.5. The wait time between switching cycles was designed to provide enough time to the voltage dividers to stabilize after fast changes occurs in the output voltages at the end of each switching cycle.

The bottom resistor R_4 was designed to have a voltage drop of 1.22V, which is the reference voltage, when the output voltage is at its expected value. The next resistor, R_2 was settled to the right value to get a 5mV drop over the 1.22V of R_1; and that drop is used by the comparators when the reference voltage is reached. This is done to add hysteresis to the feed-back loop with the objective of avoiding oscillations. Resistor R_3 has the objective of generating the voltage $SPEED_n$ for each one of the output sensing networks. This voltage reaches the 1.22V reference voltage when the output reaches its expected value minuss 0.5V, for example when V_{OUT1}

voltage is at 2.7V $SPEED_1$ node will reach the reference voltage of 1.22V. These $SPEED_n$ signals go to a comparator that determines when to accelerate the switching cycles speed to reach higher charge rate sent to the output nodes. When this fast speed is needed, the output signal FAST will have a logic high value indicating the Logic module that the wait time between switching cycles needs to be reduced.

The Comparators block is composed of four comparators, three to monitor the output voltages and one to monitor if the FAST mode is needed. Like the comparators used in the IPK and ZCD current sensors (Figure 3-17), these comparators have 50nA DC current loss when standby mode is active; but these ones have differences in the input and output stages. For the output monitoring, the comparator shown in Figure 3-35 was used. Differently from the IPK and ZCD comparators, this one has a PMOS input stage; intentionally selected because its input voltages are never going to be near the minimum supply voltage of 2.5V. Due to this fact, now the latch is form by PMOS transistors M_{P3} to M_{P6} instead of using NMOS transistors like in Figure 3-17. Other difference is that the output stage is formed by a current comparison between the drain currents of the NMOS transistors M_{N3} and M_{N4}. Differently from the previously discussed comparator, in which a simple common source stage was added in cascade with V_2, this output stage was selected because no high speed is needed in this comparison.

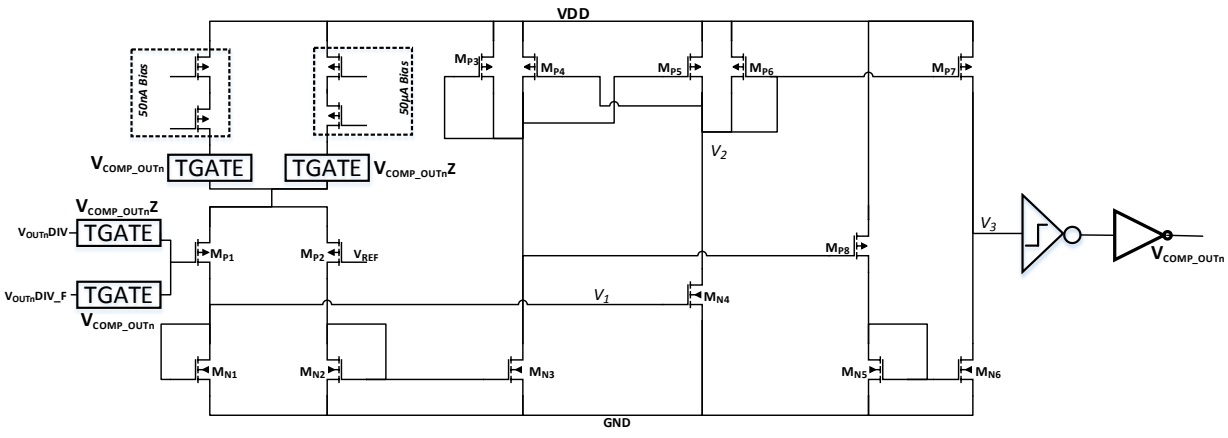

Figure 3-35 Charge Monitor Output Monitoring Comparators

The hysteresis created by the two sensing nodes in the voltage resistors is provided to the differential pair input by CMOS transmission gates (TGATE). Depending on the actual state of

the digital output V_{COMP_OUTn}, $V_{OUTn}DIV$ or $V_{OUTn}DIV\_F$ will be provided to the gate of M_{P1}. Similarly the bias current of the PMOS differential pair is provided; where two different bias current values could be provided, which are 50nA and 5µA. When V_{COMP_OUTn} is logic high, meaning that the output voltage has passed over the reference, the 50nA current is used as bias current; therefore having very low power losses during this stage, which is the longest one. When V_{COMP_OUTn} changes to low, indicating that the output voltage is below its reference and charge needs to be sent, 5µA will be provided as bias current instead of the 50nA of the standby stage. This gives the comparator a very high speed comparison, which is needed due to the very fast changes of the output voltages when charge is sent to it at the end of the switching cycle. The same hysteretic inverter used in the IPK sensor (Figure 3-11) is used as output stage to avoid non-digital voltages at the output V_{COMP_OUTn}. To provide the two different bias currents, the same Current Reference Amplifier used in the IPK and ZCD current sensors (Figure 3-14) is used in this component. Also, the same VDD switch used in the current sensors is used in this component to turn off the 5µA current reference when standby stage is active.

The comparator used to obtain the FAST signal has the same output stage of the comparators used in the current sensors; but its input stage is PMOS type like the output monitoring comparators. The $SPEED_n$ sensing signal provided to the differential pair input is the one corresponding to the active output during the switching cycle; which is known by the $FLAG_n$ signals provided by the Logic module. Depending on which FLAG signal is high, the input gate of the differential amplifier receives $SPEED_1$, $SPEED_2$, or $SPEED_3$. If the output voltage is below the expected voltage minus 0.5V, then the FAST output signal will turn to logic high and with it the FAST input of the Logic module. The output node is masked with and AND gate to avoid digital noise when the ENABLE signal changes and the entire comparator is turned on. This enable signal is turned on directly with the ON signal, which indicates to the Logic module that one of the outputs needs charge to raise its voltage. The same Current Reference Amplifier used in every discussed comparator is also used in this component to generate the 5µA current reference. This comparator's schematic is shown in Figure 3-36.

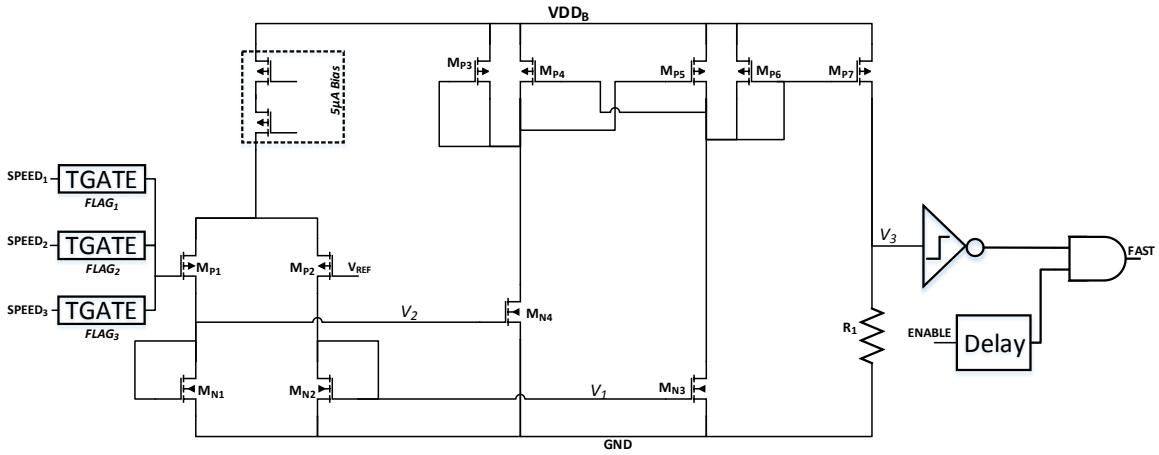

Figure 3-36 Charge Monitor SPEED Comparator

The Power on Reset is implemented by a RC low pass filter in series with a CMOS digital buffer, formed by two cascaded CMOS inverters. The ON signal will be high only when any of the output monitoring outputs is high and POR is high, therefore indicating to the Logic module that charge is needed in an output node.

Every component of this module was tested in simulations to prove their functionality. The POR circuit and the output monitoring and speed comparators were simulated under different supply and temperature corners. Figure 3-37 shows the performance of the output monitoring comparators; where the magenta graph is the V_{OUT3} voltage at steady state, the bottom red graph is the comparator output, and the graph in the middle shows how the two sense voltages of the voltage divider for V_{OUT3} oscillates around the reference voltage (blue). When the red sense voltage (V_{OUT3}Div_F) crosses the reference voltage when falling, the switching cycles start and the output voltage starts to rise. This occurs until the magenta sense voltage (V_{OUT3}Div) crosses the reference voltage and the output V_{OUT3} is un-active.

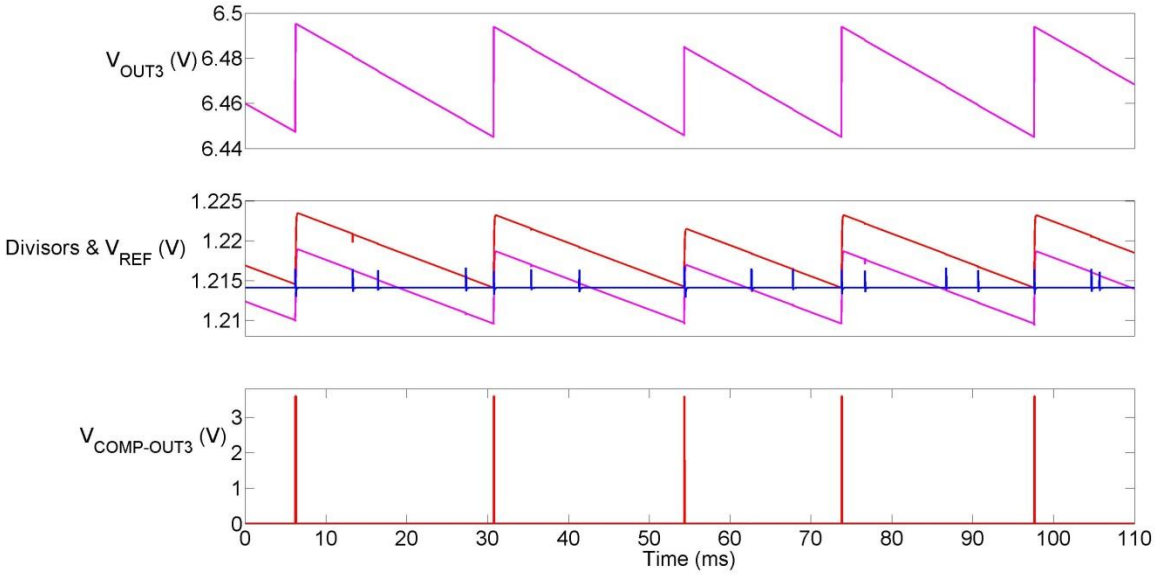

Figure 3-37 Charge Monitor Output Comparators Performance Plot

During the startup stage, when the voltage has to rise from zero to its expected value, FAST mode is activated to reach the steady state faster. To prove the functionality of this mode, a startup simulation was done monitoring the $SPEED_n$ sense voltage for V_{OUTn}, the reference voltage V_{REF}, the inductor current I_L, and the output voltage V_{OUTn}. Figure 3-38 shows the performance plot of the $SPEED_n$ comparator during the startup stage. As shown in the plot, when V_{REF} is greater than $SPEED_n$ the signal FAST is high. During this time the peak inductor current value will be the double of its value during steady state. When V_{OUTn} almost reaches its expected voltage, the speed comparator detects it and turns to low the FAST signal, therefore terminating the FAST mode and reducing to half the inductor peak current value. Although there are switching cycles occurring in the plot, the $SPEED_n$ sense signal looks smooth. This is due to the low pass filters added to the voltage dividers previously discussed in Figure 3-34.

As mentioned before, the POR signal is necessary to start the digital controller, specially the Asynchronous State Machine discussed in section 3.5. The system was tested under different supply, temperature, and process corners and its functionality wasn't affected. Figure 3-39 shows the POR signal rising time, which happens around 4µs after the supply voltage rises.

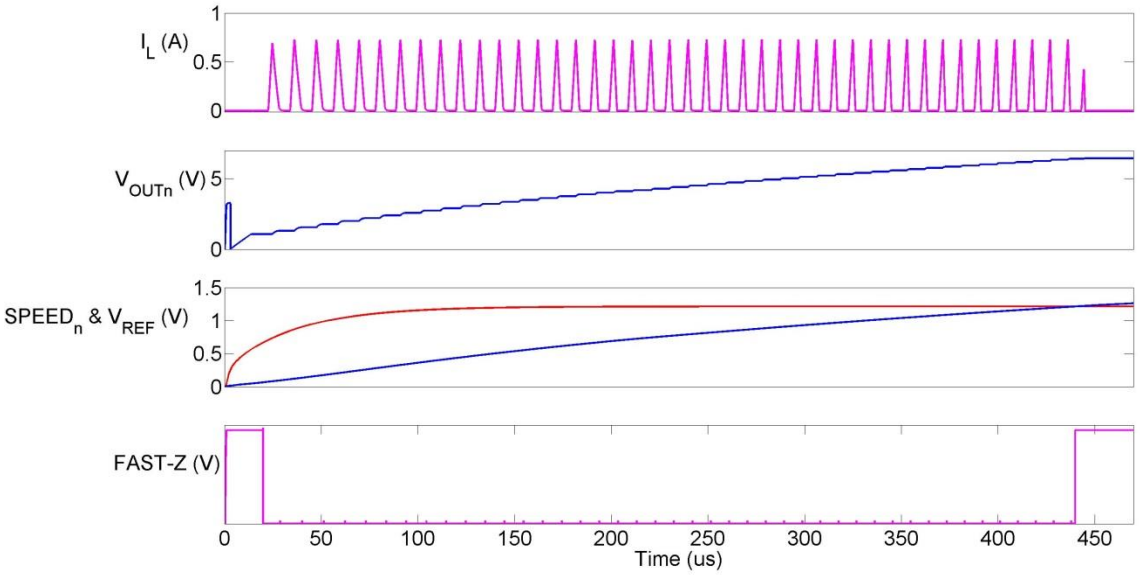

Figure 3-38 Charge Monitor SPEED Comparator Performance Plot

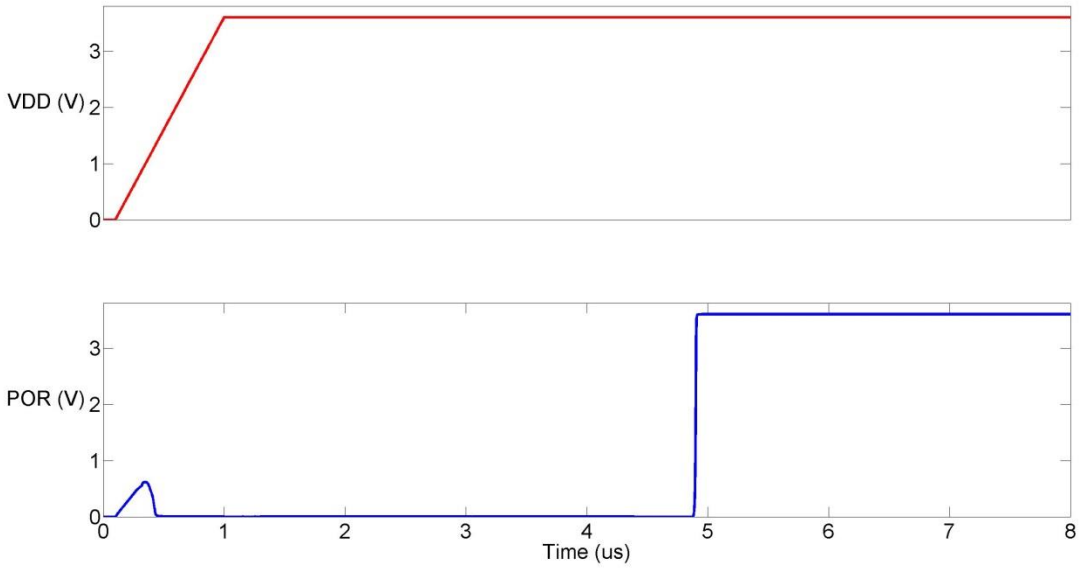

Figure 3-39 Charge Monitor POR Performance

As shown in Figure 3-1, this module's layout is at the top corner of the device. It can be placed in that corner without any problem because it doesn't have any circuit that could stop working if fabrication and package damage occurs, different from the Reference System and current sensors modules which are more delicate to this type of damage. Figure 3-40 shows the

layout map of this module, in which the two main components of the Charge Monitor are identified.

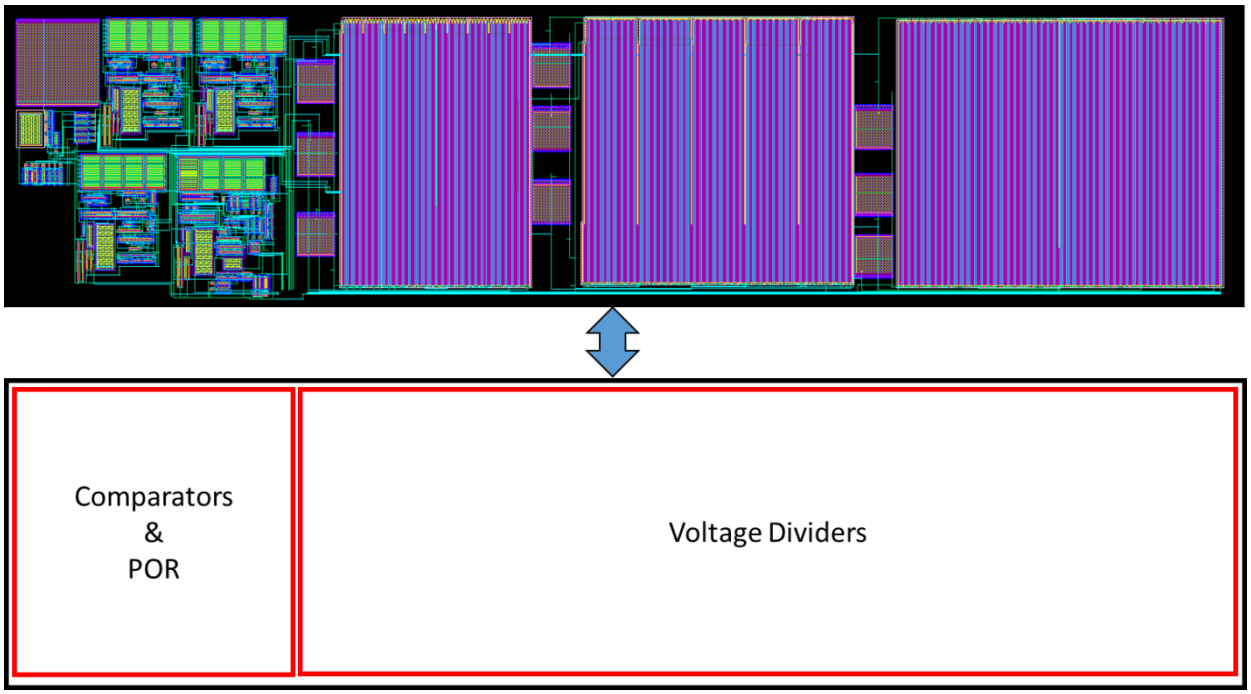

Figure 3-40 Charge Monitor Layout Map

For the comparators layout, like in the Logic modules layout, the priority was to reduce the occupied area of the module as much as possible. This is due to the fact that there is no matching need other than the small transistors of the input stages of the differential pairs; which were satisfied by using the interdigitazion technique in [16].

Differently, for the Resistor Dividers, layout matching was the priority during the layout design. The reason of this matching requirement is that any non-symmetrical change in resistances could affect the output voltage regulation. The mega-ohms order resistors were symmetrically distributed as much as possible for each one of the three different resistive networks. The resistor divider network layout for the V_{OUT2} output is shown in Figure 3-41; in which the resistor names correspond to Figure 3-34. In this case, R_1, R_2, R_3, and R_4 were divided in 120, 5, 5, and 40 segments respectively, including the dummy resistors. To achieve a symmetrical distribution, resistors R_4 and R_1 were intercalated with a rate of 4 to 1 in five groups; which in between have 1 segment of R_2 and R_3. Dummies were used to achieve an integer correspondence between the resistors inside the network. A similar distribution was used

for the other two resistor divider circuits, as could be seen in Figure 3-42, which shows the distribution for the V_{OUT1} output.

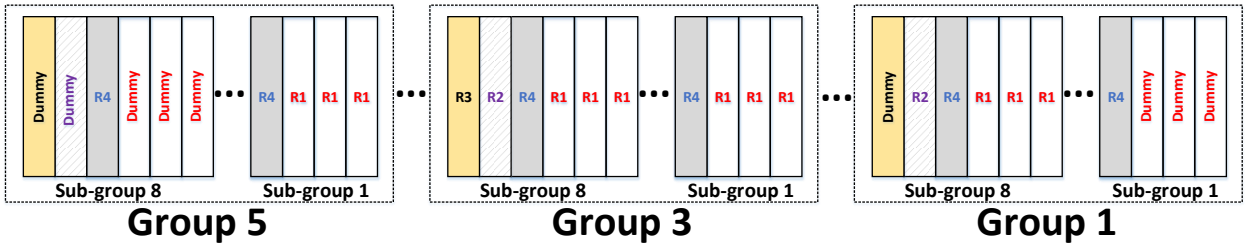

Figure 3-41 Charge Module V_{OUT2} Resistor Divider

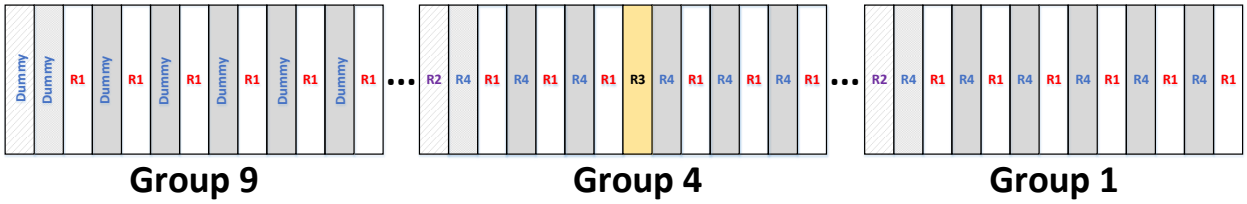

Figure 3-42 Charge Module V_{OUT1} Resistor Divider

3.7 V_{DRIVE} Selector

This device objective is the voltage regulation of three independent outputs; and to achieve such regulation a SIMO Buck-Boost was used, as explained in section 2.2. That topology needs to have at least six power switches, seven in this case; from which four of them will be implemented by using PMOS transistors, as shown in Figure 2-10. These switches implemented with PMOS transistors are M_{P1}, M_{P2}, M_{P3}, M_{P4}, and M_{P5}; and to avoid current flowing through their bulk terminal, the maximum system's voltage (V_{DRIVE}) is connected in it. The maximum system's voltage could be the supply voltage VDD, or the V_{OUT3} terminal of 6.5V. In addition, this V_{DRIVE} voltage is used as logic high for the power transistors' gate; this with the objective of achieving minimum possible drain-to-source resistance $R_{ds,on}$.

When the system is started, all outputs voltages are zero, the active V_{DRIVE} voltage will be VDD; but when V_{OUT3} has overpassed the VDD voltage value then it becomes the new active V_{DRIVE} voltage. At steady state V_{OUT3} will be constantly the active V_{DRIVE} voltage because it's the maximum system voltage in such state.

This module's objective of sensing the VDD and V_{OUT3} voltages, and supplying V_{DRIVE}, requires a voltage divisor to sense the VDD voltage and provided such sense voltage to a comparator. The sense voltage of V_{OUT3} is provided by the resistor divider included inside the Charge Monitor module discussed in section 3.6; which is also the same resistor divider used for VDD sensing. Based on the output of the comparator, the decision of which voltage will supply the V_{DRIVE} voltage is taken. The schematic of the V_{DRIVE} Selector module is shown below in Figure 3-43. The VDD sense voltage is compared with the sensing nodes of V_{OUT3}, and its output goes to a Level Shifter. The level shifter is a circuit that transforms an input logic level to another output logic level. In this case the input logic level is VDD, which is the supply voltage of the comparator, and the output logic level is the V_{DRIVE} voltage. The reason for using a level shifter is to achieve PMOS turn off when necessary, specifically at steady state where the VDD voltage will be less than V_{OUT3} voltage. The Level Shifter circuit is discussed in detail in section 3.8.

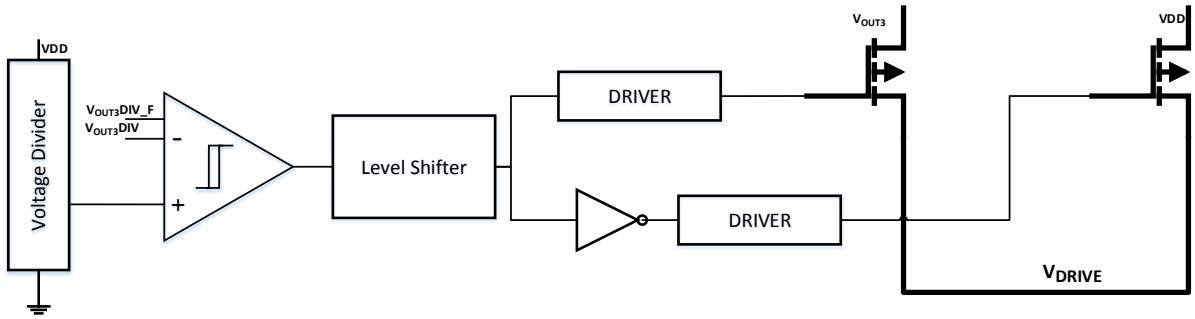

Figure 3-43 VDRIVE Selector Schematic

The Level Shifter output is the input of the Driver circuits that controls the PMOS switches connecting the VDD and V_{OUT3} voltages to the V_{DRIVE} output. Since these PMOS transistors are very large, but smaller than the power transistors of Figure 2-10, driver circuits are required to provide enough current to move their gates nodes to the desired voltage level. These Driver circuits, along with the Driver circuits used for the power switches, are discussed in detail in section 3.9.

A bad functionality of the V_{DRIVE} Selector will cause bulk current paths inside the power PMOS transistors, and with that efficiency degradation. In addition, the power PMOS transistors could remain turned on when they are supposed to be turned off therefore causing regulation degradation. For this reason a good performance review should be completed in order to avoid these problems.

Transient simulations were done to verify the module's performance during startup, which is the instant requiring more precision due to the very fast voltage rise of V_{OUT3}. Figure 3-44 shows the transient performance plot for the nominal corner. As discussed above, when V_{OUT3} is below VDD, V_{DRIVE} is equal to VDD; but when V_{OUT3} crosses VDD, V_{DRIVE} will follow the V_{OUT3} voltage. This test was done at different corners, and its behavior was good.

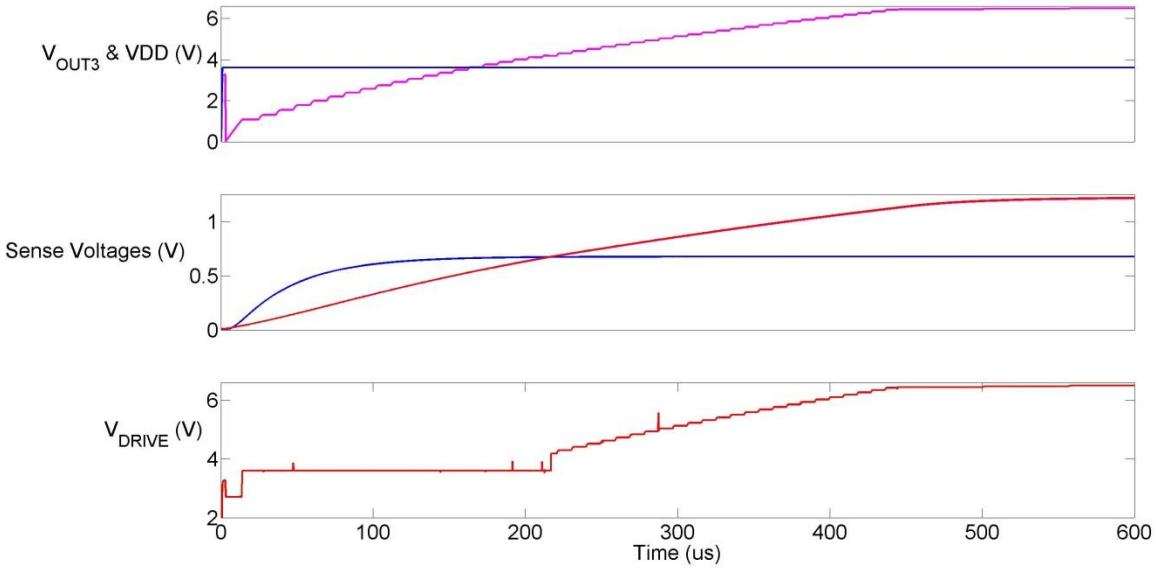

Figure 3-44 VDRIVE Selector Performance Transient

During the switching cycles, specifically during the power PMOS gate's transitions, very high currents could appear due to the large gate drivers used. Because of this, high internal resistance on the power paths of the module should be avoided; specifically in the PMOS switches. For this reason the PMOS transistors of this module have a huge size. A Temperature-DC sweep was simulated (Figure 3-45) to select the right size value to obtain an internal resistance of less than 1.2Ω. If the PMOS switches has this resistance value there will be almost 0.6V of dropout in it, assuming 500 mA passes through it; which won't cause any problem. In case of mal-function, or bad model estimates of internal resistance, an external pin access was created for the V_{DRIVE} node to add the necessary capacitance to filter these voltage dropouts.

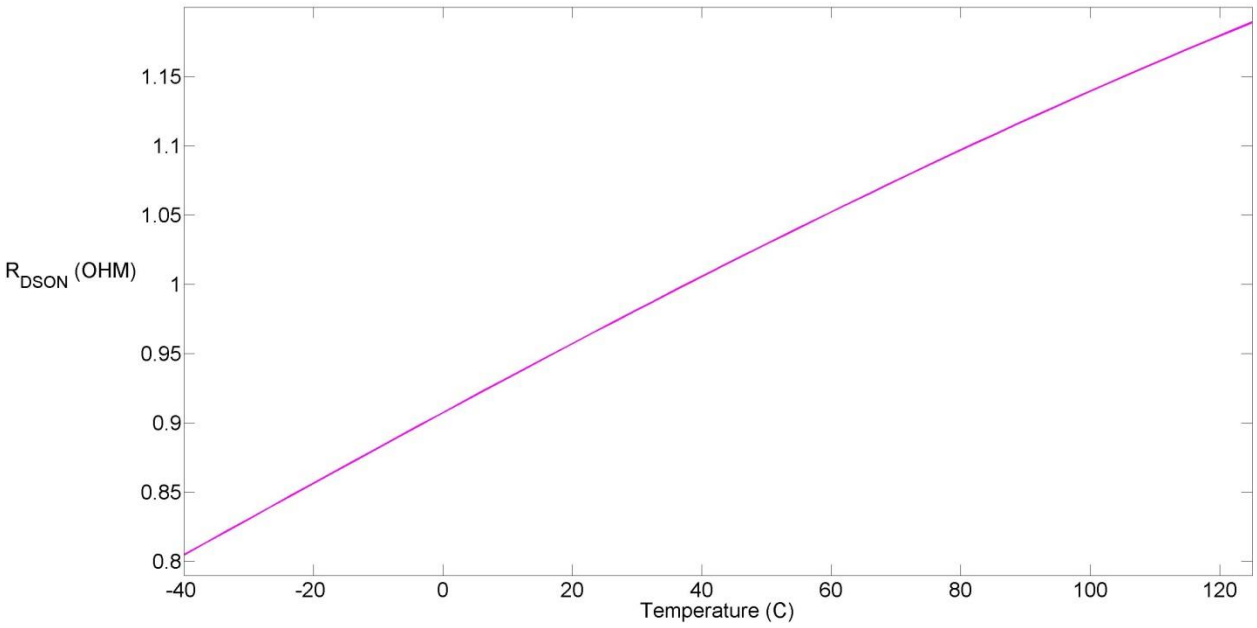

Figure 3-45 VDRIVE Selector Switches Resistance

The V_{DRIVE} Selector layout and its map are shown in Figure 3-46. The resistor divider component in Figure 3-43 is a copy of the resistor divider used in the Charge Monitor for output V_{OUT3} in section 3.6. For this reason the layout of this component is the same used in the Charge Monitor; in which the resistors where symmetrically distributed by intercalation. The same happens with the comparator, which is the same used for the Charge Monitor output monitoring comparators. The Level Shifters and Drivers modules are discussed in the sections 3.8 and 3.9 respectively.

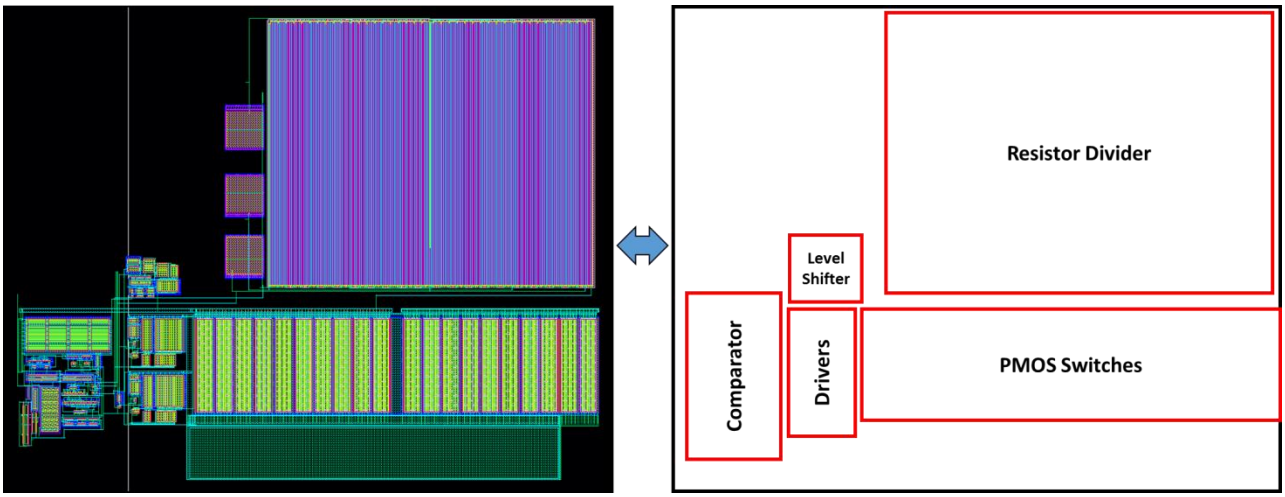

Figure 3-46 VDRIVE Selector Layout Map

3.8 Level Shifters (LS)

This system is composed of two main modules, as discussed in section 3.1; which are the Controller and the Power Stage. Under some scenarios, these two modules could have two different logic high level values. For this reason a coupling circuit between their digital parts needs to exist to avoid bad functionality. This module can transform a digital signal with a logic level A into a signal with a logic level B, where A ≠ B. This section discusses the fundamental level shifter circuit, but inside the system there is a bank of six level shifters; one for each Power Switch except for M_{P4} in Figure 2-10.

The conventional level shifter circuit, presented in, [18] , was used in this device. It is a six transistor topology and its schematic is shown in Figure 3-47. A latch is formed by PMOS transistors M_{P1} and M_{P2}, therefore forcing the source terminal with less sinking current to a logic high level of V_{new}. If V_{in} is a logic high, meaning V_{old}, then M_{N1} will be turned on while M_{N3} is turned off; therefore pulling M_{P2}'s gate to GND, and V_{out} to V_{new}. The oppose occurs with V_{in} changing from logic high to logic low; when V_{out} is forced to GND by turning on M_{N3} instead of M_{N1}.

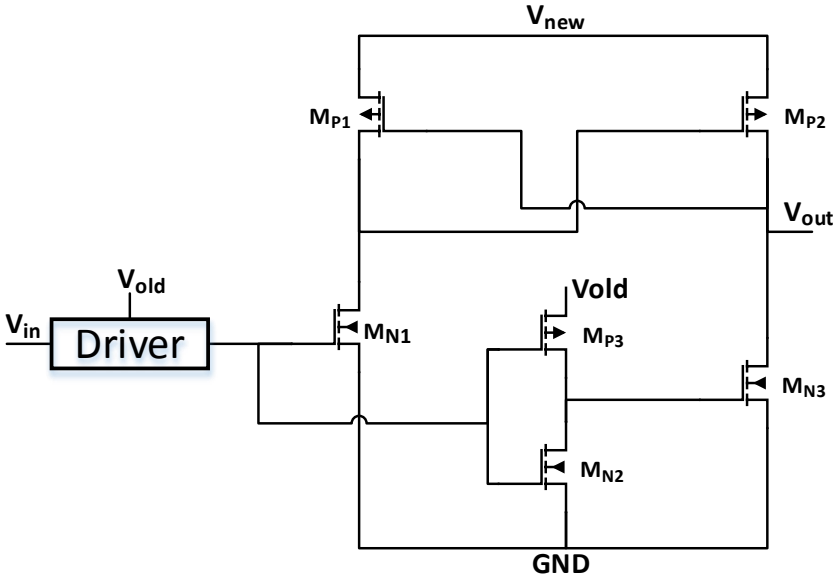

Figure 3-47 Level Shifter Schematic

M_{N1} and M_{N3} have to be larger than M_{P1} and M_{P2} to be able to change the PMOS latch operating point. Due to this fact, a large size Driver had to be added to keep acceptable rise and fall times. Its topology is the same used for the Power Switches Drivers, as discussed in section 3.9.

Since the Level Shifter is a digital circuit, no much performance review is necessary to be done other than its functionality at least in nominal corner. Figure 3-48 shows how when the input signal changes from low to high, which has a logic level of 3.6V, the output signal also changes to a logic high, but with a logic high level of 6.5V. In addition to this, the current consumption of the module was verified. Every time a transition occurs in the input signal the current consumption of the level shifters has its peak. This peak current only occurs during around 20ns (I_{LOSS}), resulting in a nano-ampere-range average current consumption at the system's frequency of operation.

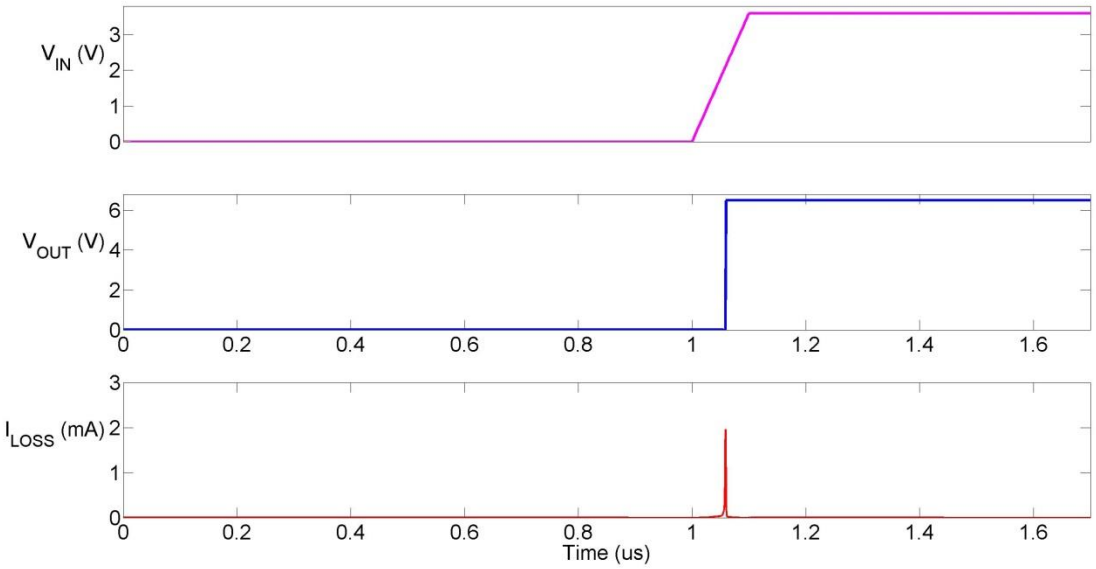

Figure 3-48 Level Shifter Performance Plot

3.9 Drivers (DRIVERS)

This system's objective is to regulate the voltage of three different outputs; and to achieve such regulation a SIMO switching converter topology was selected, as discussed in section 2.2. Since this is a switching converter topology, power switches are contained inside the system; which needs to be constantly activated and deactivated. In this design, CMOS transistors are used to implement the power switches; and their gate terminal voltage is used to control them. To keep acceptable rise and fall times of their gate voltage, due to the huge size of the transistors, gate-voltage drivers are needed between the controller and the power switches. This module contains the needed drivers to couple the Controller and the Power Stage.

The Driver module is implemented with six cascade-connected CMOS inverters, as shown in Figure 3-49. The input inverter is the smallest inverter; this with the objective of having ideally zero input parasitic capacitance. The output inverter is the largest one because it provides enough current to move the output voltage with good timing. The other four inverters connect the input and output inverters, and they increase its size each stage by a factor of three.

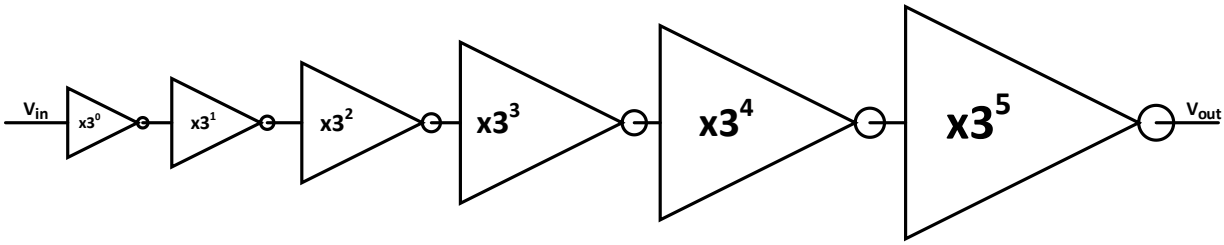

Figure 3-49 Driver Module Schematic

There are two types of Drivers inside the device; which are the Large and Small Drivers. The Large Driver has exactly the same schematic shown in Figure 3-49; and the difference with the Small Driver is the number of stages. The Small Driver only has four stages because the capacitance at its output pin is lesser than the capacitance at the output pin of the Large Drivers. The Small Driver is used for the freewheeling switch, M_{P5} in Figure 2-10, because this switch is smaller than the other Power switches. All the other Power Switches are gate-supplied by the Large Drivers.

The $t_{trans,}$ value in Table 2 refers to the rise and falling times of the power switches; and the value used during the efficiency analysis of Figure 2-5 was 1ns. Therefore the drivers need to be designed to match that parameter, and with that keep the parameters matched as much as possible with the reality. For this reason the drivers were tested to prove that at the maximum capacitance corner the rise time value is at least near that value. Figure 3-50 shows the results of that scenario simulation; in which the rise time of the output signal is less than 3ns, being close enough to 1ns.

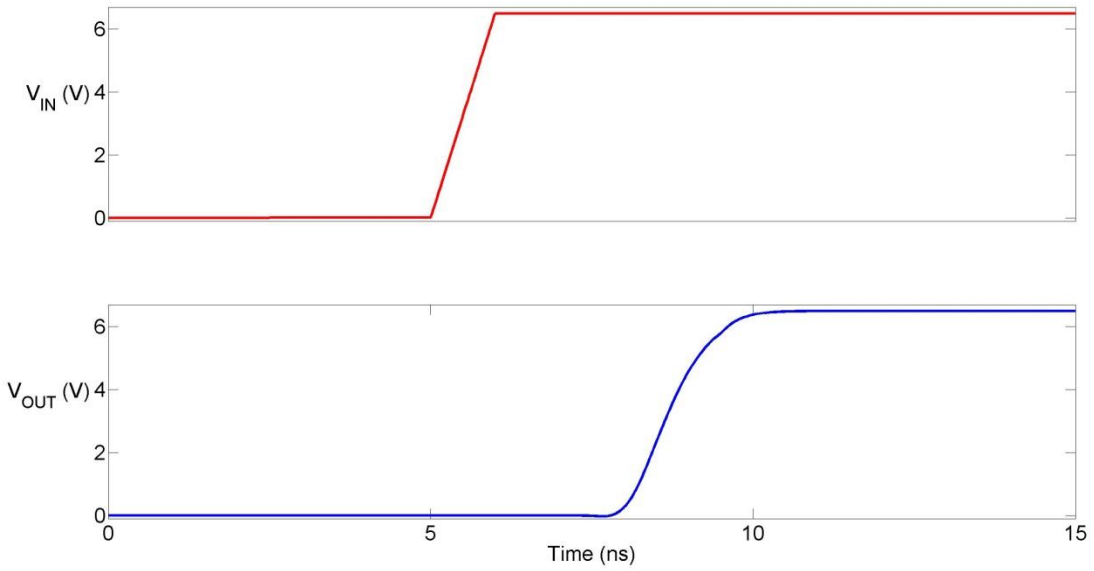

Figure 3-50 Driver Performance Plot

For this module's layout the priority was the area minimization because it is a digital circuit, and there is not matching need. This module is located right into the power stage (Figure 3-1) of the device due to the facts that it is a completely digital circuit and it needs to be near the power switches. Its layout is shown in Figure 3-51.

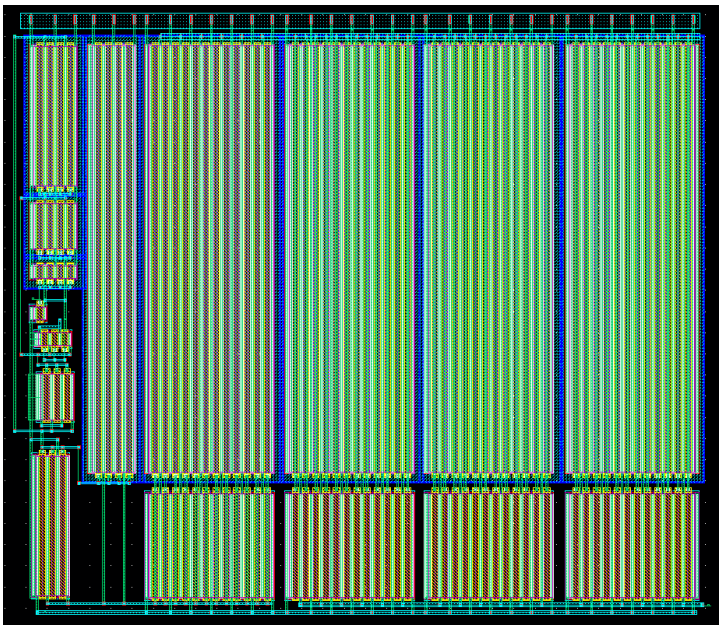

Figure 3-51 Driver Module's Layout

3.10 Switches

All the Controller modules identified in section 3.1 have been already discussed; but the power Switches haven't been explained. The power switches overviewed in this section implements the SIMO Buck-Boost converter, shown in Figure 2-4, used in this architecture.

This module consists of seven power NMOS and PMOS transistors to form the topology presented in Figure 2-4 with six switches. In addition to this, smaller portions of two switches were designed to serve as sense transistors for the IPK and ZCD current sensors. Figure 3-52 shows the Switches module's schematic, which is divided in three main components: VA-Switches, VB-Switches, and FW. This division was implemented to make easier the layout design as will be discussed further.

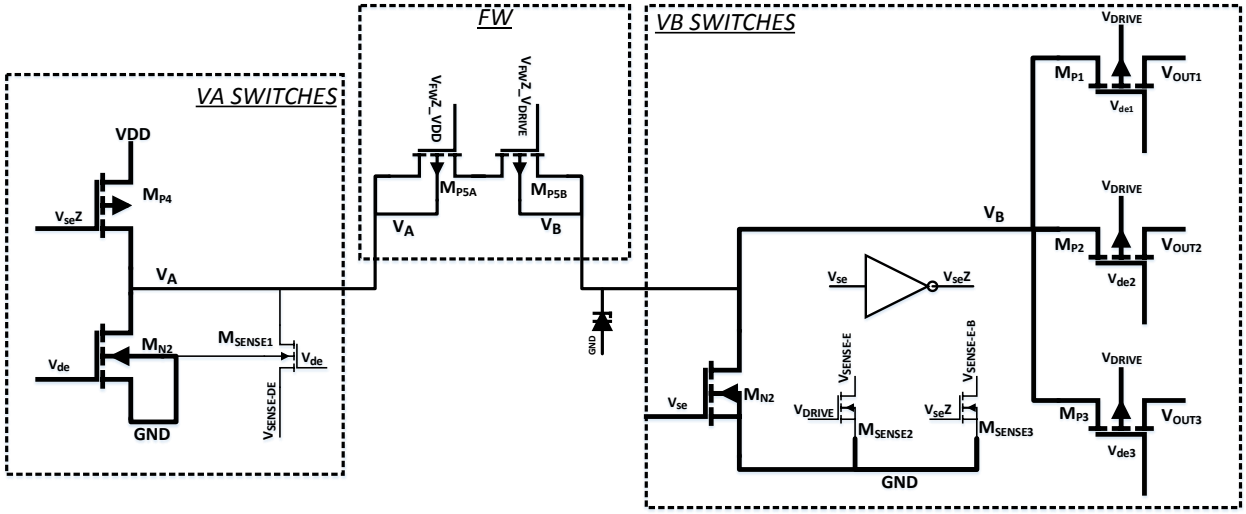

Figure 3-52 Switches Module's Schematic

For the power switches, the design variable is its size, since it will determine the internal resistance of the switch; which in fact is the dominant factor in the conduction losses equations of Table 1. Besides, the internal resistance doesn't affect only the efficiency, it could affect also the functionality of the device if its value is too high. For example, consider the energization stage shown in Figure 3-53; if the transistor M_{P4} internal resistance is too high such that V_A decays to GND, then no energization will occur in the inductor because voltage isn't applied to the inductor terminals. Therefore the internal resistance should be design such that at every inductor current and supply voltage corners the energization occurs. For this reason the

resistance at which the voltage drop in the transistor M_{P4} is half of the supply voltage VDD, is set as maximum as shown in Equation (18); which could be used for the maximum internal resistance value allowed for the other switches.

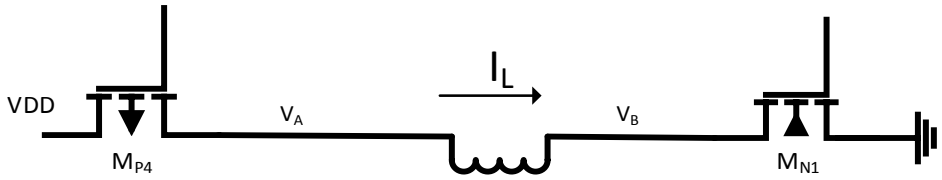

Figure 3-53 Switches Energization Stage

$$R_{internal} < \frac{VDD_{MIN}}{2IPK_{MAX}} \qquad \textbf{(18)}$$

Assuming a maximum inductor peak current of 1.5A, which assumes a very large IPK current error, and the minimum supply voltage of 2.5V then the maximum allowed internal resistance $R_{internal}$ value results in 833mΩ. To check that the design accomplishes this maximum internal resistance criteria DC simulations were done over temperature to measure the internal resistance at every process corner. The results of these simulations are shown in Figure 3-54, and the maximum resistance resulted to be under 600mΩ; therefore accomplishing the maximum $R_{internal}$ criteria.

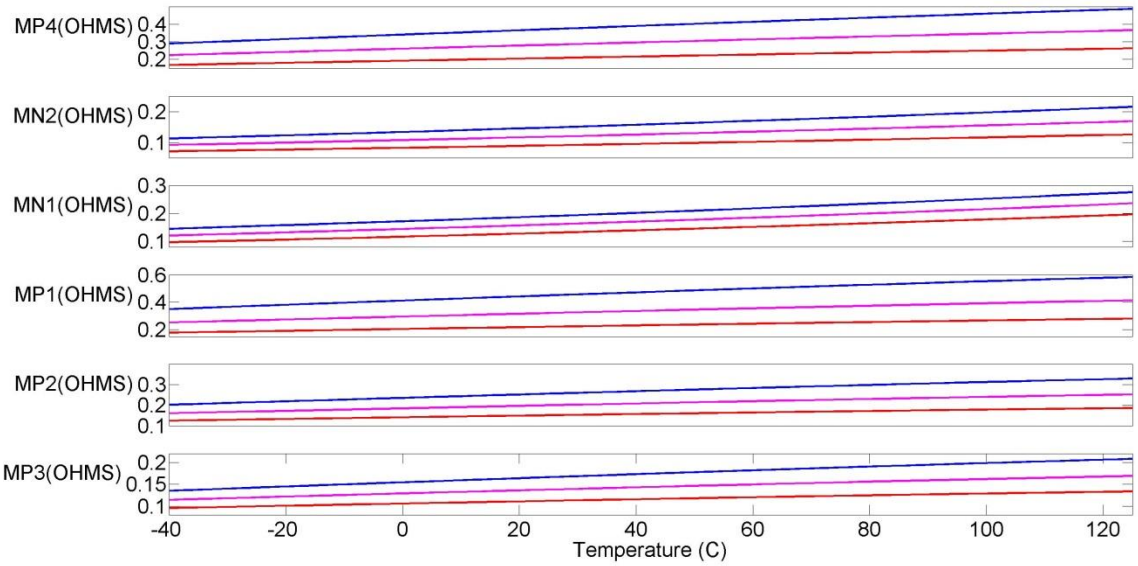

Figure 3-54 Switches Internal Resistance Plot

The second design parameter for the power switches is efficiency, due to the direct effect of $R_{internal}$ in the conduction losses equations of Table 1. To check this parameter, transient simulations were done to the total system efficiency at steady state, and the efficiency specification at nominal corner of 85% was accomplished. The designed size for each power transistor is shown in Table 6.

Table 6 Switches Module Power Transistors Size

Switch	M_{N1}	M_{N2}	M_{P1}	M_{P2}	M_{P3}	M_{P4}	M_{P5A}	M_{P5B}
Size $\left(\frac{W}{L}\right)$ (µm)	(21.8/0.9)k	(20.6/0.8)k	(70/0.8)k	(70/0.8)k	(70/0.8)k	(70/0.8)k	(1/1.3)k	(1/1.3)k

The sensing transistor M_{SENSE1} is 500 times smaller than M_{N2}, meaning that the sensing current of the ZCD current sensor will be 500 times smaller than the actual inductor current. Similarly to this, the sensing transistors M_{SENSE2} and M_{SENSE3} are 1000 times smaller than M_{N1}. This makes the IPK sensing current smaller than the sensing current inside the ZCD current sensor; done this way because the IPK current sensor needs to be precise at high inductor current, near the IPK value, contrary to the ZCD current sensor which needs precision in inductor currents near zero.

The freewheeling PMOS M_{P5} was divided into two different transistors M_{P5A} and M_{P5B}, as shown in Figure 3-52. This was done to avoid current leakages through the freewheeling path when noise is present in the V_{DRIVE} voltage. When switches' gate-voltages are moved, there could appear noise in the V_{DRIVE} node; therefore accidentally turning on the freewheeling path if it is controlled only with the V_{DRIVE} voltage logic high value. For this reason a PMOS transistor M_{P5A} was added in series to the V_{DRIVE} controlled M_{P5B} transistor, but controlled with a logic high level of VDD, therefore keeping the freewheeling path turned off even when noise appears in the V_{DRIVE} voltage.

A Zener-diode is connected to V_B node to avoid over-voltage in it; which could occur during the dead-time between the energization and de-energization stages. Although this dead-time occurs only during around 16ns it could raise the V_B voltage very high due to the charged inductor. As shown in Figure 3-55, the Zener diode limits the voltage raise to a voltage under 7.7V; which is the maximum voltage limit the utilized process could handle.

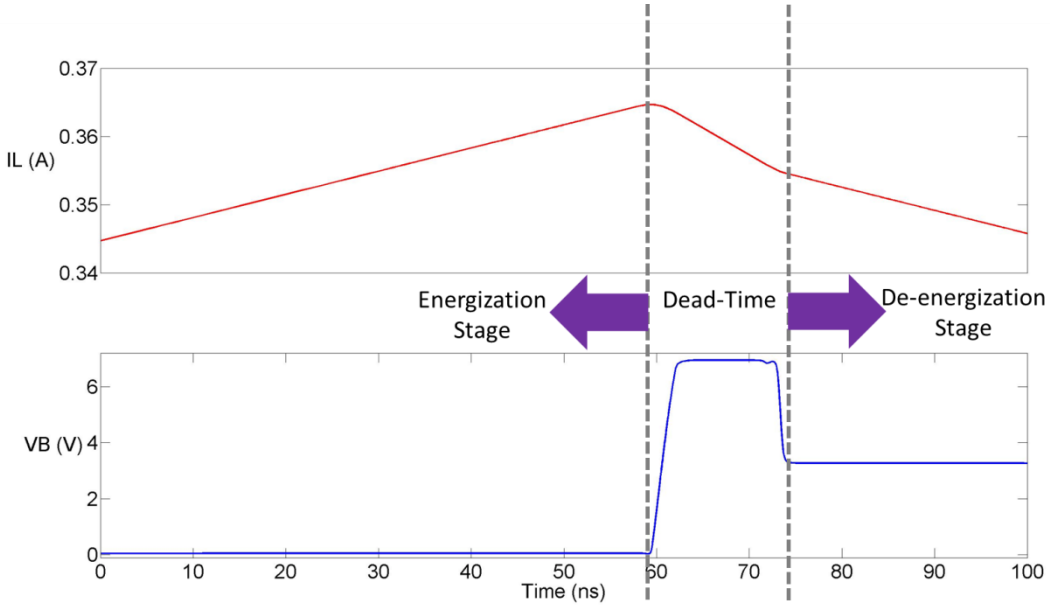

Figure 3-55 Dead Time & V_B Node Voltage Raise Protection

Two priorities existed when doing the Switches module layout. They were the matching between the sensing transistors $M_{SENSE1,2,3}$ and the power NMOS $M_{N1,2}$, and the area minimization as much as possible. Since the size of the power transistors is fixed by the design parameters already discussed, the area minimization priority is limited to the concentration of the

components to leave as less as possible empty area. Doing this also helps to reduce the metal resistance in the power transistors connections to the power nodes V_A and V_B; therefore reducing the conduction losses. Figure 3-56 shows the layout map of the Switches module; and it could be noticed the very high components condensation in the utilized area by this module.

To achieve good matching between the sense transistor M_{SENSE1} and the power transistor M_{N2}, M_{SENSE1} was symmetrically distributed along all the area occupied by M_{N2}. This is shown in Figure 3-57, in which the two components of M_{SENSE1} are identified. The same was intended for the M_{N1} and its sensing transistors matching, but there was limitation due to process implementation of the LDMOS transistors used for this power switch. A distribution as symmetrical as the one achieved in M_{N2} wasn't possible due to this limitation. To see the effect of this non symmetrical distribution, DC simulations were done using the layout-extracted model of this part's layout; which contains the effect of parasitic components.

As mentioned before, the module was divided into three main components: VA-Switches, VB-Switches, and FW. This was done to facilitate the layout design procedure by doing its integration module by module; and therefore make easier the debugging procedure when problems occur.

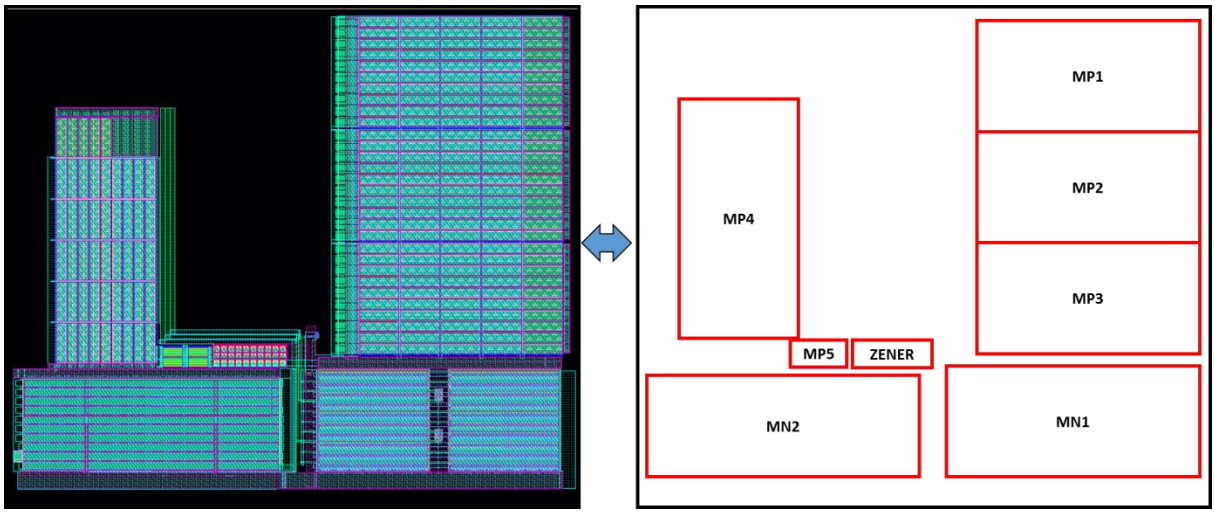

Figure 3-56 Switches Module Layout

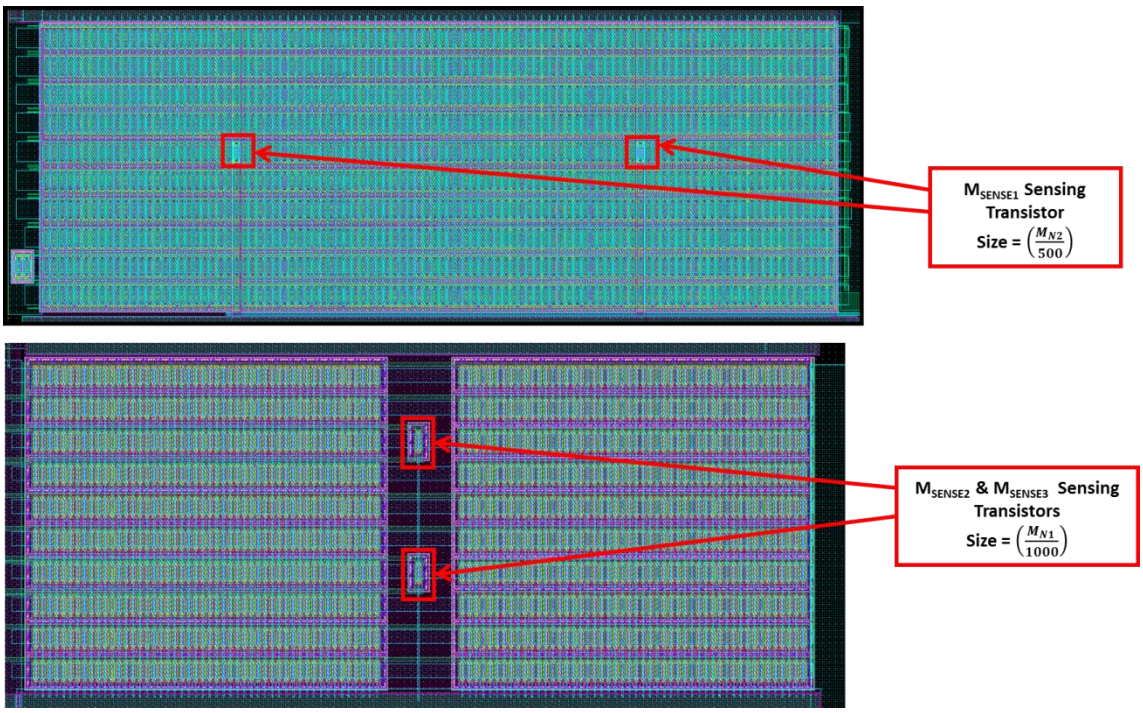

Figure 3-57 Sensing Transistors Layout Distribution Map

Chapter 4 : System Simulations & Experimental Results

A Power Management Integrated Circuit (PMIC) was designed and fabricated to achieve the objectives presented in section 1.1. During the design stage, discussed in Chapter 3, simulations were done to corroborate the specifications accomplished and the functionality of the device. All the collected data from the simulations is compared in this chapter with the experimental data obtained from the physical device testing stage.

This chapter contains an overview of the experimental stage; including done tests, testing setup and results. In addition, experimental results are compared with the simulation results to be able to quantify the effect of internal and external parasitic components against the CAD models.

4.1 Experimental Overview

Inductor current control, system's startup, output regulation, efficiency, and quiescent current data are enough to prove the functionality of the device. By doing these tests all the specifications in section 1.1 could be determined by measuring the proper signals. The measured signals and calculations done to determine each specification are discussed below within each test section.

The PMIC was packaged inside a Dual in-line Package (DIP) of 14 pins. The pin diagram of the device is shown in Appendix B – Testing Setup. To reduce the external parasitic components as much as possible, a Printed Circuit Board (PCB) was built. To achieve such parasitic components reduction every component, except the PMIC, were soldered to the PCB board. The PMIC wasn’t soldered because it is the Device under Test (DUT), and not soldering it allows to change it without the necessity of unsoldering it. In addition, the highest possible width value of the board’s paths was used to reduce in such a way the parasitic resistances. The PCB board picture and layout, along with the pin diagram of the PMIC, are shown in Appendix B – Testing Setup.

Although many simulations were done during the design stage in order to ensure the functionality of the device in different corners, during the testing stage only the essential tests to determine the specifications accomplishment at nominal corner were implemented. These tests are summarized in Table 7 along with their objective and the measured signals. All these tests, along with their comparison to the simulation results, are discussed in the following sections.

Table 7 Simulation and Experimental Tests Description

Test	Objective	Signals
Switching Cycle	To prove the functionality of the inductor current controller.	1. Inductor Current 2. Inductor Terminal Voltages 3. Output Voltages
System's Startup	To test the functionality of the startup accelerator circuit	1. Inductor Current 2. Output Voltages
Line Regulation*	To characterize the output voltages at every input voltage	1. VDD 2. Output Voltages
Load Regulation*	To test the response of the controller to load steps	1. Output Load 2. Output Voltages
Efficiency	To quantify the efficiency of the device	1. Input Current 2. Output Voltages

*Belongs to the Output Regulation Tests

4.2 Switching Cycle

Inductor current control is an essential component of this device; because any bad functionality with it could deviate the operation mode of the SIMO converter away from the Hybrid mode discussed in section 2.2. For this reason the discussion of this test is done in detail in this section.

From the simulations, Figure 4-1 shows the inductor terminals' voltage, and its current, during a switching cycle. When the switching cycle starts the inductor terminals separate to a voltage difference of almost V_{DD}; therefore increasing the inductor current with a slope of $\frac{V_{DD}}{L}$. When the IPK current value is reached the inductor terminal turns their separation to a voltage almost equal to $-V_{OUTn}$; therefore reducing the inductor current with a slope of $-\frac{V_{OUTn}}{L}$. This is the stage when all the energy stored in the inductor is sent to the capacitor of the active output. This stage ends when zero-current value is detected by the ZCD; and the inductor terminals are shorted.

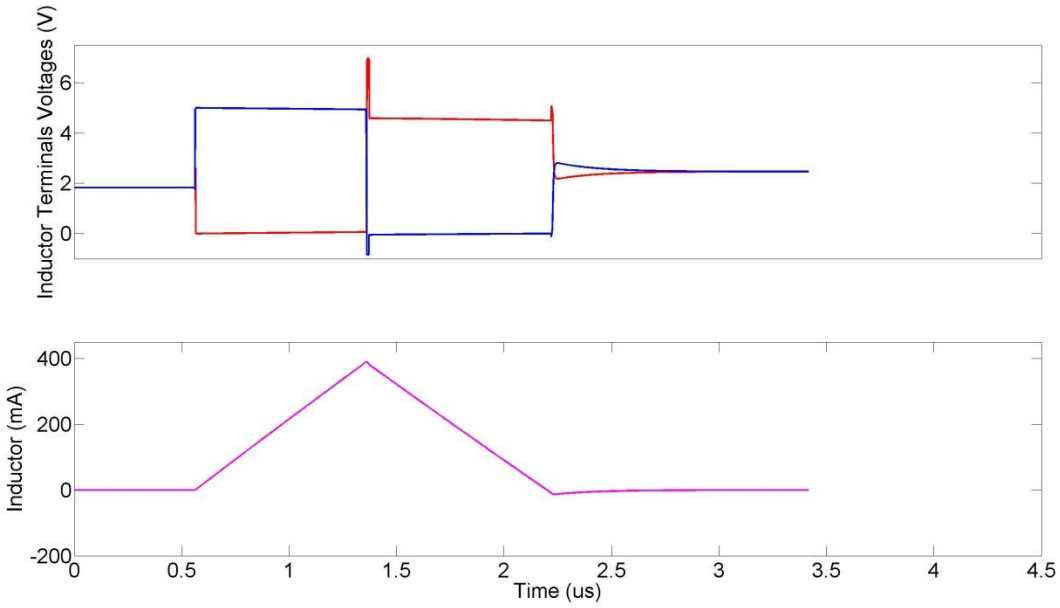

Figure 4-1 Switching Cycle Inductor Current Simulation Data

Figure 4-2 shows the switching cycle experimental data; and the behavior of every signal is as expected. The inductor terminals voltages are as expected during the energization, de-energization and freewheeling stages. The only difference is the small oscillations during the

stages transitions. Such oscillations could occur due to the parasitic inductances of the board; but they aren't large enough to damage the functionality of the device. The inductor current waveform during the energization time is almost identical for both data sets, simulation and experimental, where it reaches the IPK value in almost a micro-second. During the de-energization stage the slope is the same but the ZCD sensor response is different between both data sets. The experimental data shows an error in the ZCD response of around 100mA below zero. Although this error degrades the efficiency of the device, it doesn't damage the functionality of the device, neither makes it unstable.

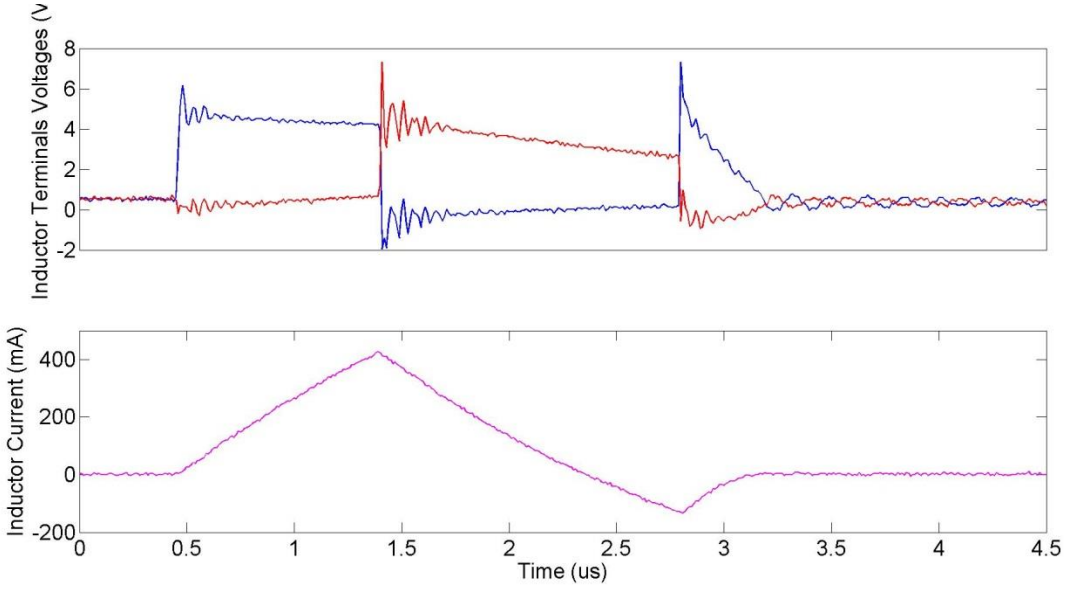

Figure 4-2 Switching Cycle Inductor Current Experimental Data

The system's controller should be able to send the remaining inductor energy if there's another output needing charge. The experimental data shown in Figure 4-3 describes how the system is able to implement this behavior. When the de-energization stage starts the inductor energy is sent to V_{OUT3}; but when it's already satisfied the remaining energy in the inductor goes to V_{OUT2}. Due to the experimental error in the ZCD response, V_{OUT2} receives only the negative portion of the inductor current before it reaches the -100mA value; therefore reducing the efficiency of the device.

The inductor current control is working properly, along with the parasitic components effect and the error in the ZCD response. Although these two issues affect the efficiency of the system, the presented data proves that a functional inductor current controller was implemented.

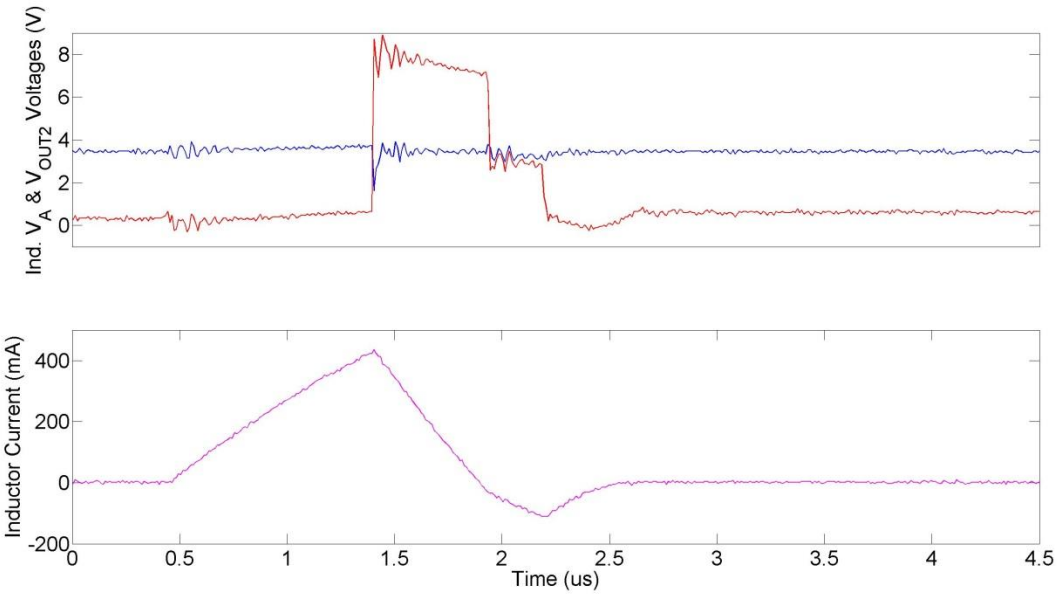

Figure 4-3 Switching Cycle Dual De-Energization Experimental Data

4.3 System's Startup

When the system is turned on, all the output voltages are zero, the controller doubles the IPK value to reach steady state faster than using just the IPK value. How this is implemented was discussed in sections 3.3, 3.5, and 3.6. From Figure 4-4, which contains the startup simulation data, it could be noticed how IPK is doubled until the output voltages reaches a voltage near the reference. The inductor current peaks observed between the biggest ones are to avoid overshoot due to the very high inductor current charging the output capacitors. In addition to this, the output priority circuit discussed in section 3.5 proves its functionality. Such functionality is proven because the output voltage raise order observed in Figure 4-4 correspond to the priority order discussed in the Logic component design section; which is V_{OUT3}, V_{OUT1}, and V_{OUT2}, from highest to lowest priority.

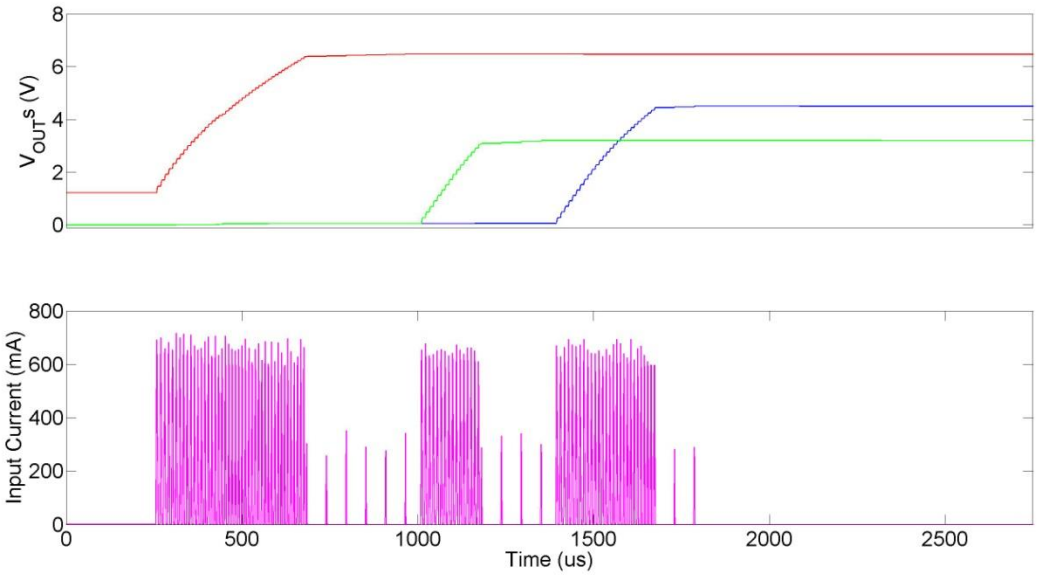

Figure 4-4 Startup Simulation Data

Figure 4-5 shows the experimental data for the startup test; which is very similar to the simulation results. The simulation data shows a startup time of almost 2ms, while the experimental data shows 1.8ms; therefore having the same startup time. The double of IPK of 800mA in the simulation data is replied in the experimental data. This proves experimentally the functionality of the startup accelerator circuit. In the simulation data the input current peaks appear to be more organized and condensed than in the experimental data. The reason for this is

the averaging of the oscilloscope used to collect the experimental data. Since every switching cycle occurs in a time range of 2µs and the plot range is almost 2ms, the oscilloscope doesn't have the required precision to collect the data without averaging it. In addition, the same output voltage priority observed in the simulation data is observed in the experimental data; therefore proving the functionality of the priority circuit inside the Logic component.

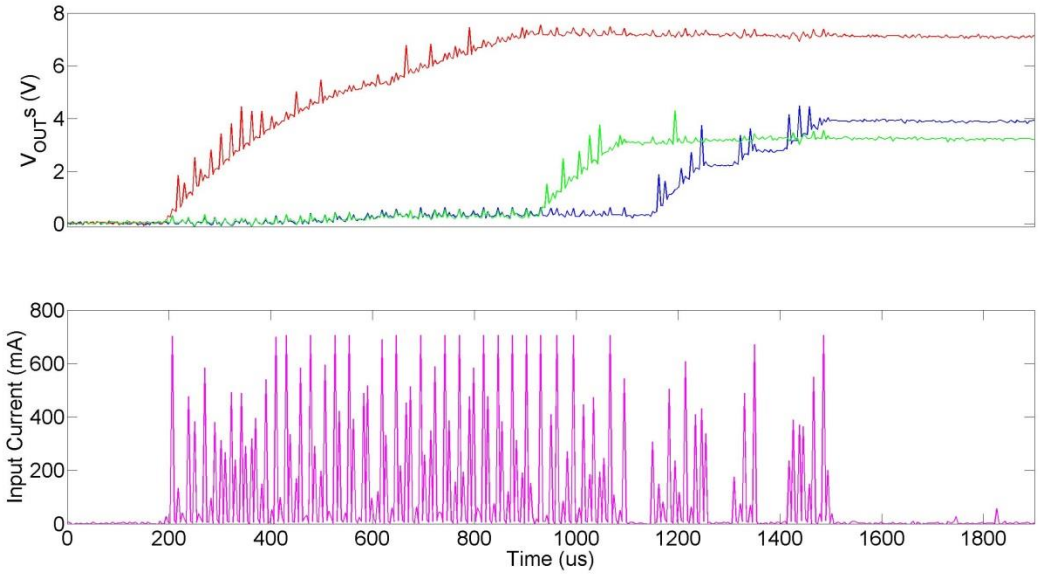

Figure 4-5 Startup Experimental Data

4.4 Output Regulation

The main objective of this device is to regulate three DC output voltages to three different values. For this reason regulation tests are essential to determine the PMIC's functionality. The first regulation test to be discussed is the nominal load regulation. In this test the system is turned on at nominal load, and its output voltages are measured. The mean value of the voltage data is calculated to be compared with the specifications. The simulation data for this test is presented in Figure 4-6; from which constant voltages could be appreciated at the three outputs. The mean voltages were calculated, and they resulted to be 3.17 V, 4.46 V, and 6.46 V for V_{OUT1}, V_{OUT2}, and V_{OUT3} respectively. These values resulted to be near the experimental data values; which are shown in Figure 4-7.

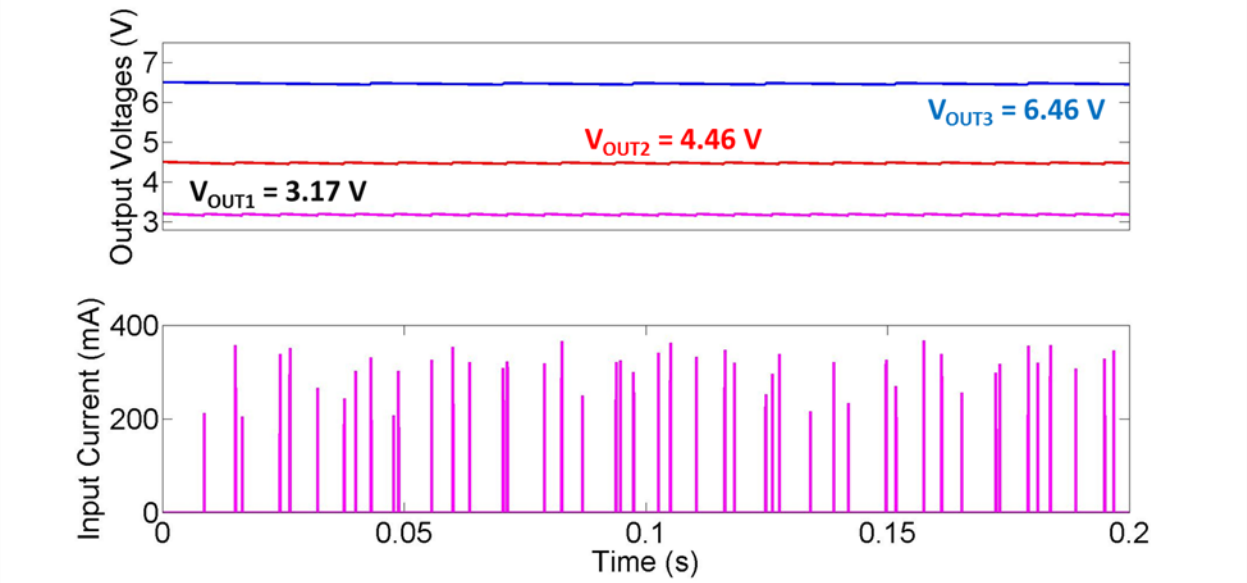

Figure 4-6 Nominal Load Regulation Simulation Data

The experimental data shown in Figure 4-7 contains the output voltages of the PMIC for 5 seconds. This proves the stability of the system during nominal load conditions. The mean voltages for the outputs resulted to be 3.21V, 4.66V, and 6.67V for V_{OUT1}, V_{OUT2}, and V_{OUT3} respectively. Although there is a 200mV error in two of the outputs, when compared with the simulation results, a constant voltage is maintained at the output nodes of the device; which proves that the device is able to keep output regulation. This 200mV error is due to the reference

voltage variation when compared with the simulations. The reference voltage during this test resulted to be 1.256V, which is higher than the 1.22V of the simulations.

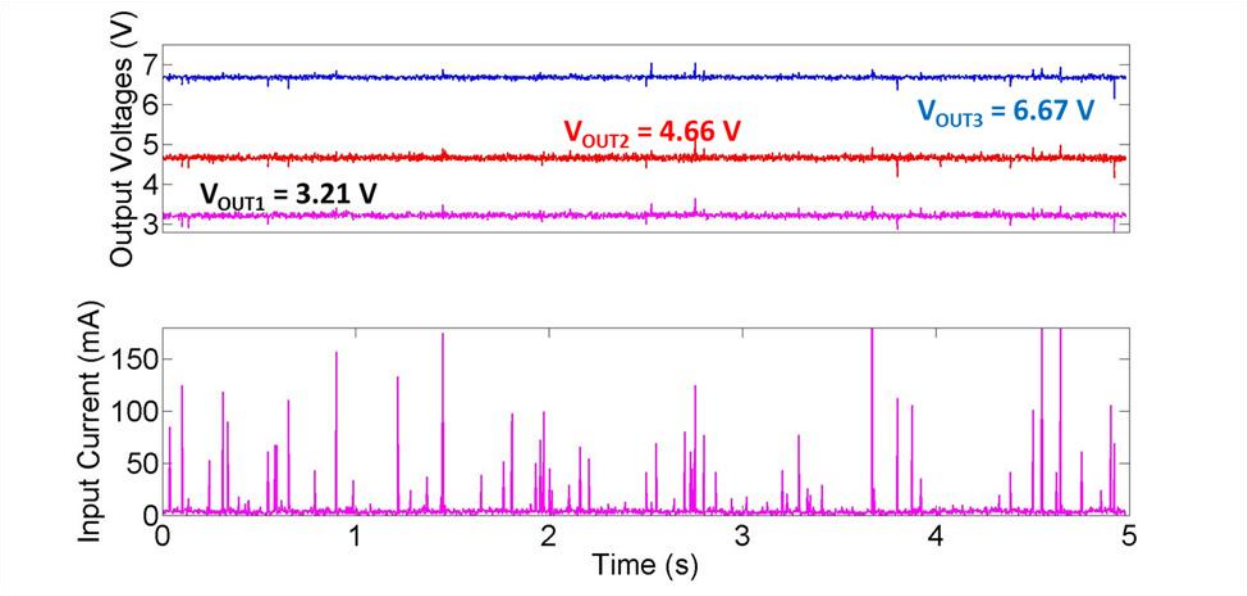

Figure 4-7 Nominal Load Regulation Experimental Data

Since proper operation of the device was proven under nominal load conditions, its functionality under different load corners should be tested. For this reason different loads were tested to see their effect on regulation. Figure 4-8 shows the V_{OUT1} load regulation data; which proves the good output regulation of the device. The V_{OUT1} load is varied from the nominal 25µA to a maximum of 1.5mA, and V_{OUT3} is the only affected output. Almost 500mV of error range, from nominal corner, is obtained in V_{OUT3}. The same pattern could be observed in Figure 4-9, which shows the V_{OUT2} load regulation data; since it follows the same V_{OUT3} variation of the V_{OUT1} load regulation data. V_{OUT3} voltage is not affected by varying its load within the design range (10 - 250µA), as shown in Figure 4-10. The V_{OUT3} variation is due to the leakage in PMOS bulks each time a switching cycle occurs.

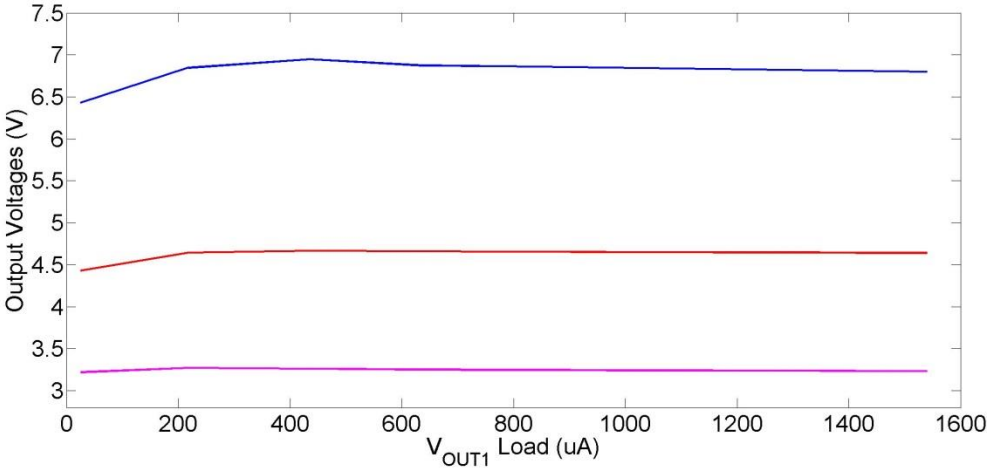

Figure 4-8 V_{OUT1} Load Regulation Experimental Data

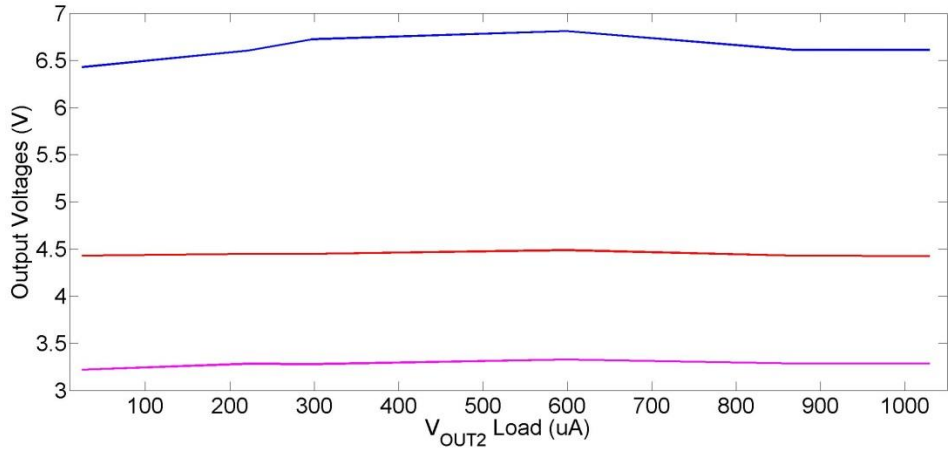

Figure 4-9 V_{OUT2} Load Regulation Experimental Data

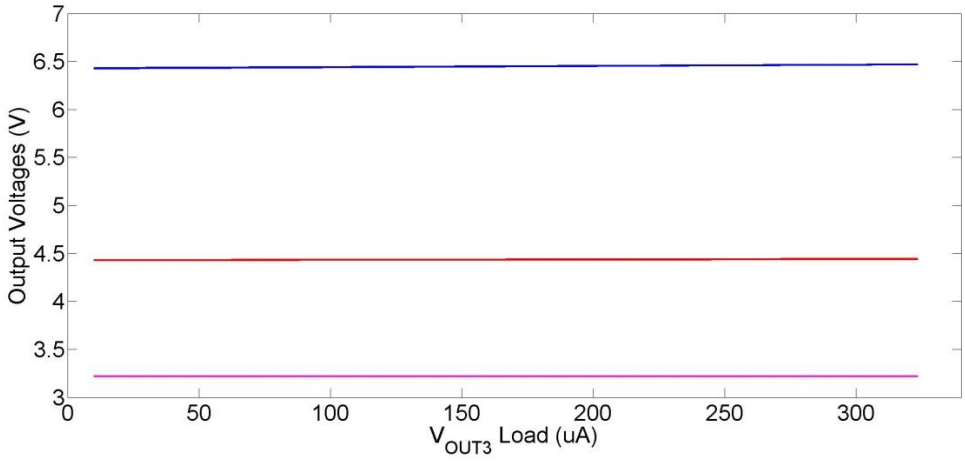

Figure 4-10 V_{OUT3} Load Regulation Experimental Data

The system should be able to regulate its three output voltages over an entire supply voltage range; which is 2.5-5.5V as shown in section 1.1. For this reason a line regulation test was done to quantify the output voltage regulation over the supply voltage range. Figure 4-11 shows the output voltage at different supply voltages. When the supply voltage is greater than 3.3V, output voltage regulation is achieved; but when the supply voltage is below that value, no regulation is achieved and the output voltages are zero. This may be due to the internal and external parasitic resistances; which doesn't appear in the simulation models.

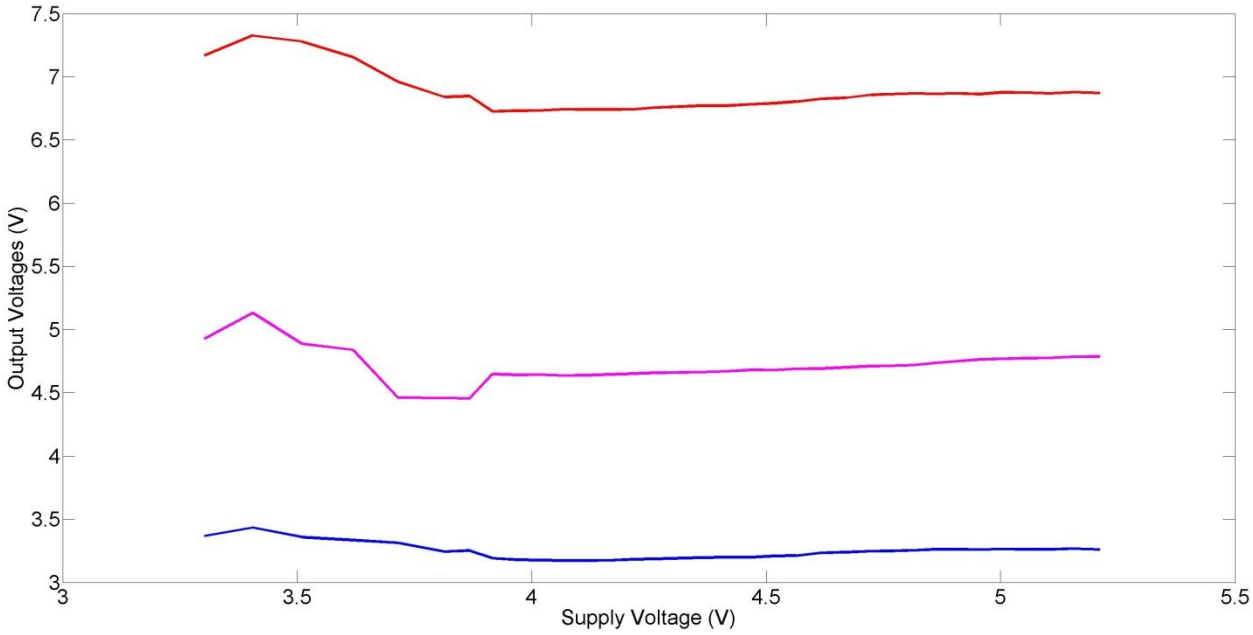

Figure 4-11 Line Regulation Experimental Data

All the tests performed and discussed in this section coincide in the good functionality of the output regulation parameter. Output regulation isn't as ideal as it appears in the simulations; but the system's controller is able to keep its functionality at many corners.

4.5 System's Efficiency and Results Overview

One of the main specifications presented in section 1.1 is the system's efficiency. 85% target efficiency was settled as the design goal. For this reason the power budget $P_{control}$ of Table 2 was considered during the design stage. As mentioned in the design discussion of Chapter 3, almost every controller components were design to have the smallest possible quiescent current; and therefore achieve a controller power dissipation lesser than the $P_{control}$ value.

Simulation data was collected to measure the system's efficiency under nominal corner conditions; which resulted to be 85.58%. Figure 4-12 shows the simulation data, containing all the output voltages and the input current. The mean output voltages were calculated using the simulation data to obtain the output power P_{OUT}. The same was done with the input current data, by calculating its mean value and therefore the input power P_{IN}. The system efficiency was obtained by calculating the ratio between P_{OUT} and P_{IN}.

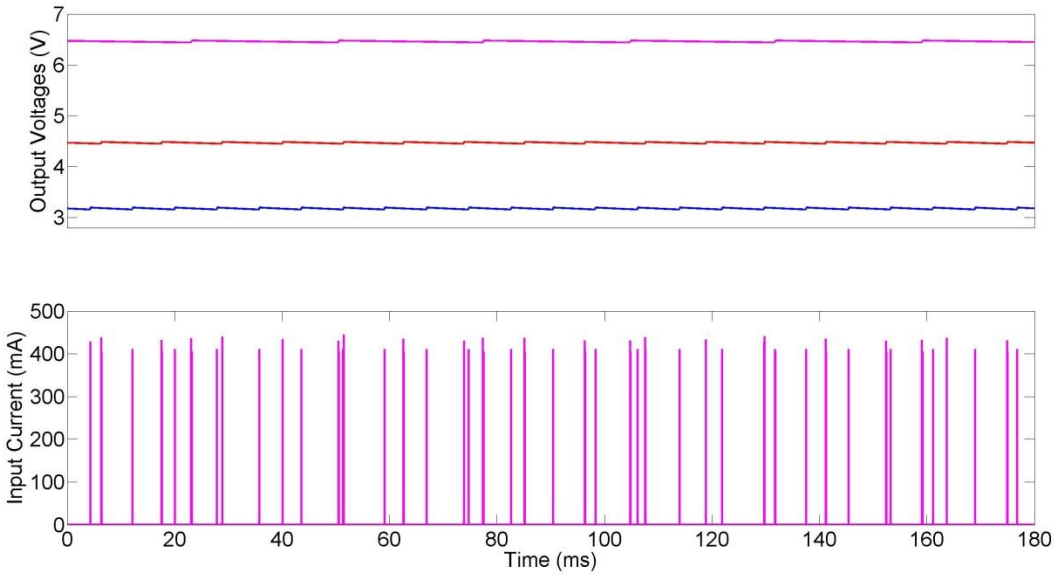

Figure 4-12 Efficiency Calculation Simulation Data

Due to the fact that this device was designed for low power applications, its quiescent (stand-by) current is a very important specification. In fact, the very low quiescent current of this device is one of the great contributions of this research to the field. From the simulations, the quiescent current resulted to be between 659.9nA and 867.4nA**;** but it wasn't possible to be

measured experimentally. Although, the current consumed by the reference buffer through the VDD_B pin was measured, and it resulted to be around 800nA. Since it was designed to consume more than the controller in stand-by mode, it could be concluded that the controller quiescent current is below that value. This proves the functionality of the low current and dynamic powering techniques used during the design process.

Experimental steady state data was collected for the output voltages and input current; this with the purpose of doing the same efficiency calculation done for the simulation data. Since the test bench is limited to a minimum of 10mA current measure, by the ETC laboratory current probe, data processing was required to obtain an accurate experimental efficiency estimate. By using MatLab, the current probe error was fixed by superimposing it with the quiescent current measured in the VDD_B pin, which resulted to be less than 800nA. The processed data showed an efficiency of around 40%, which is far from the 85% obtained in the simulations. Such efficiency reduction is justified by the chip's test bench internal and external parasitic components. The first efficiency simulation, which resulted in an efficiency of 85%, was done without considering parasitic resistances.

The research liaison, which fabricated the PMIC, provided optimal package parasitic values of 100mΩ series resistance and 5.5nH inductance in series with each package pin. The main source of these parasitic components, called internal parasitic components, are the bond wires connecting the die with the package pins. An efficiency simulation was done considering these internal parasitic components and an efficiency of 73.9% was obtained, which is almost 12% less than in the ideal simulation. This proves the effect of optimal internal package parasitic components, which in this case could be greater due to the non-optimal package used for the PMIC fabrication.

In addition to internal parasitic, external parasitic also exists in the test bench. These parasitic refer to the parasitic values of the external components, like the inductor and output capacitors. Tantalum capacitors with about 2Ω of ESR resistance were used for the output capacitors, and a 220µH inductor with 200mΩ of series resistance as the SIMO inductor. Other external parasitic resistances exist in the test bench, like the board connections resistances and inductances, but their value wasn't possible to be estimated. To see the effect of the external components parasitic resistances on the efficiency, a simulation was done considering only such

parasitic components. The effect of the external parasitic resistances was the reduction of the efficiency from the ideal 85.5% to 57.7%, almost a 28% reduction. This proves that the main responsible of the efficiency reduction are the external parasitic resistances. Using optimal external components, as used in the industry, will allow an efficiency near the 85.5% optimal value. When combining the internal and external parasitic estimates in a single simulation, the efficiency resulted to be 55.6%, which is almost the same 57.7% efficiency obtained in the only external parasitic simulation. The difference of the 40% efficiency obtained experimentally, with respect to the 55.6% of the parasitic simulation, could be justified by underestimated internal parasitic values, and the already mentioned not considered test bench parasitic resistances.

With the purpose of summarizing all the simulation and experimental data already processed, Table 8 shows a comparison of both data sets; along with other references. The startup time is almost the same for the simulation and experimental data sets. The efficiency target was achieved when avoiding the high internal and external parasitic resistances. Although such efficiency target wasn't reached experimentally in the test bench, its value could be clearly increased near its target value if optimal external components are used. The experimental data reflects functionality of the device, although with some minor effects due to parasitic components. Stable inductor current control was reached, and good output regulation was measured. Almost any SIMO converter reference applied to microwatts loads was found during the literature review. As shown in Table 8, the loads supplied by the references' SIMO converters are in the hundreds of milliamps range. This converts the no efficiency degradation at light loads (under the 1mA) one of the greatest contributions of this research to the field.

Table 8 System's Performance Summary

	References				This Work	
	[22]	[21]	[20]	[19]	Simulation	Experimental
Supply Voltage	1.2-2.2 V	5 V	1.2-2.2	3.6-5 V	2.5-5.5	2.5-5.5
Process	0.5-µm CMOS	0.35-µm BCD	0.25-µm CMOS	0.25-µm CMOS	0.8-µm BiCMOS	0.8-µm BiCMOS
Maximum Efficiency	81.00%	88.70%	75.00%	90.00%	85.58%	40%
Quiescent Current	-	-	-	-	Less than 867.45nA	Less than 800nA
Inductor	1µH	10µH	2.2µH	4.7µH	10µH	10µH
Output Capacitors	10µF	10µF	22µF	4.7µF	5µF	4.7µF
Output Voltage	V_{OUT1}	V_{OUT2}	V_{OUT1}	V_{OUT1}	V_{OUT1}	V_{OUT1}
				V_{OUT2}	V_{OUT2}	V_{OUT2}
				V_{OUT3}	V_{OUT3}	V_{OUT3}
				V_{OUT4}	V_{OUT4}	
Nominal Load	3.0 V	2.5 V	3.3 V	1.2 V	3.17 V	3.22 V
				1.8 V	4.46 V	4.43 V
				2.5 V	6.46 V	6.43V
				3.3 V		
Nominal Load	140 mW		5mA	24mA	25µA	25µA
				2mA	25µA	25µA
				5.6mA	10µA	10µA
				Total Load ≈ 650mA		
Total Startup Time	-	-	-	-	1.2ms	1.3ms

Chapter 5 : Conclusions & Future Work

A functional Power Management Integrated Circuit (PMIC) was designed to provide three independent regulated output voltages. Differently from the literature, this PMIC was designed for a very low load range; therefore making complex its high efficiency operation. A novel hybrid operation mode, a combination between sequential and distributive modes, was defined and implemented to reach such efficiency levels. To implement the hybrid operating mode, different low quiescent current control techniques were used from different literature articles; being the Asynchronous State Machine, and the Inductor Peak Current (IPK) and Zero Current (ZCD) detectors the most essential components of the system.

The design was implemented using a 0.8µm BiCMOS technology, and simulations were done to ensure its functionality over different supply voltage and load corners. In addition to the validation by simulation results, the device was fabricated and tested experimentally. Both data sets, simulation and experimental data, shows a functional system. Good output regulation was observed in both data sets and almost identical inductor current control and output voltages startup were found. The simulation data shows an efficiency of 85.58% which accomplishes the efficiency specifications, while the experimental data shows 40% efficiency due to the test-bench's high parasitic resistances. Such efficiency was reached thanks to the design of a very low quiescent current controller, which resulted in less than 1µA.

All the collected data indicates that a functional and efficient Single Inductor Multiple Output (SIMO) converter was designed for very low power applications. In addition, external components minimization was achieved by using only one external inductor.

The following could be considered as contributions of this project to the field:

1. A new hybrid operation mode was proposed, implemented, and tested for SIMO converter operating in the DCM region
2. The design of functional non-invasive inductor current sensors applicable to many DC/DC converters applications
3. Design of a low quiescent current, less than 1µA, asynchronous digital controller to control SIMO converters

4. The design of dynamic powered comparators that could operate under nano-ampere current consumption conditions
5. An 85% efficient SIMO converter, which was designed, implemented, and tested for micro-watts loads applications

The following were identified as work that could improve this research's results and contributions:

1. To reduce the quantity of external pins, different solutions could be explored to block the Power PMOS transistors' bulk terminals without using the V_{DRIVE} module. This module requires an external nano-faradays capacitor to keep its functionality over every temperature and process corners. The use of back-to-back connections was explored, but more than the double of the area will be needed for such transistors.
2. The research of voltage sensing circuit topologies could improve the efficiency under even lower loads, since 150nA are consumed at each output node for sensing purposes. The use of capacitive sensing networks could improve such current consumption, and hence the systems efficiency.
3. The enormous size of this device's database makes impossible to run extracted simulations over the entire layout-extracted model and be able to see the effects of parasitic in its functionality. For this reason a deep study of the system's layout should be done to detect and fix such parasitic components.
4. The test bench parasitic components degrade the experimental efficiency data of the PMIC. The improvement of the PCB board, and the selection of Surface Mount (SMT) PMIC package and external components, will reduce the system's parasitic resistances and better experimental efficiency results will be achieved.

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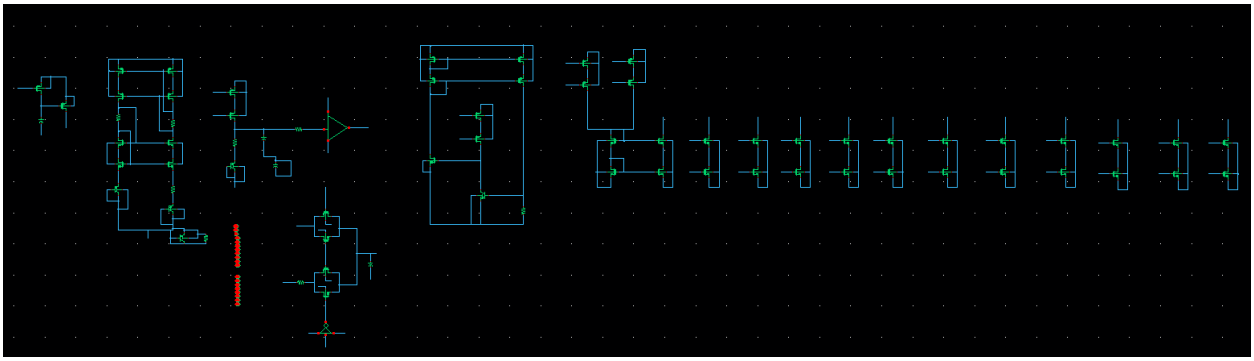
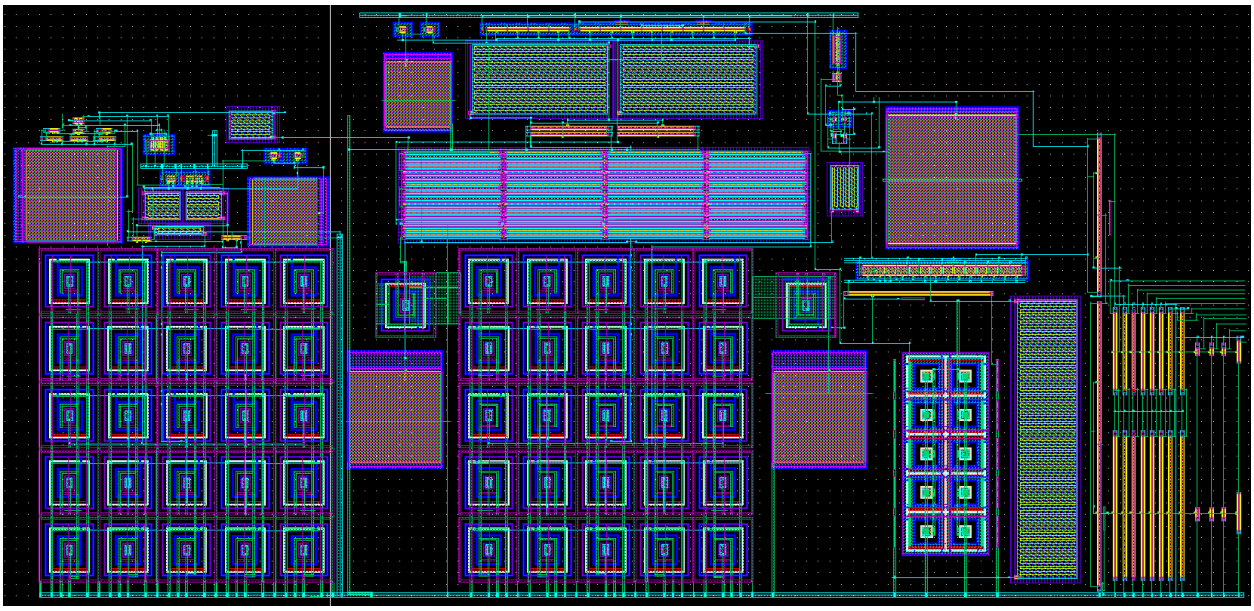
Appendix A – Cellviews and Layouts

A. Reference System (Refsys)

a. This module contains the cellviews:

i. BUFFER – Buffer for the internal reference voltage pad

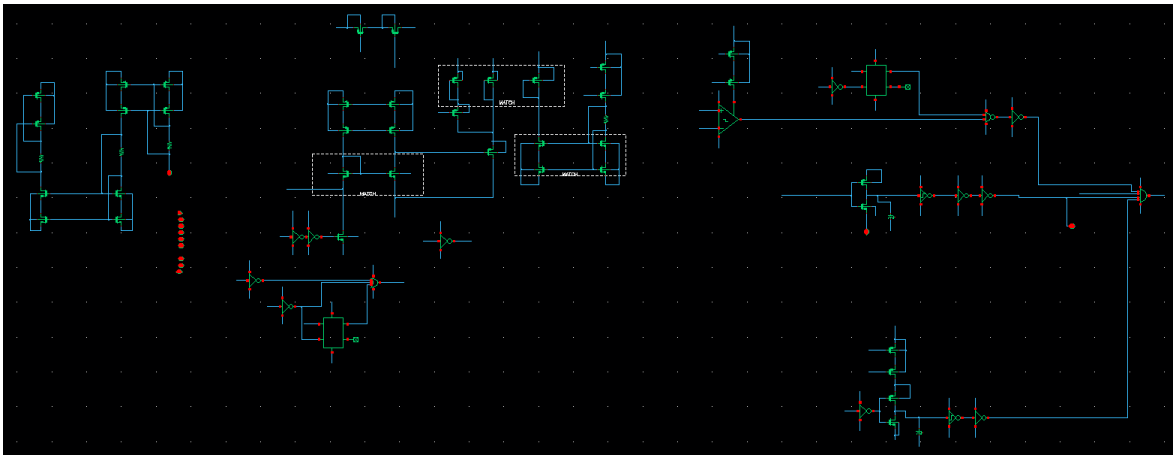


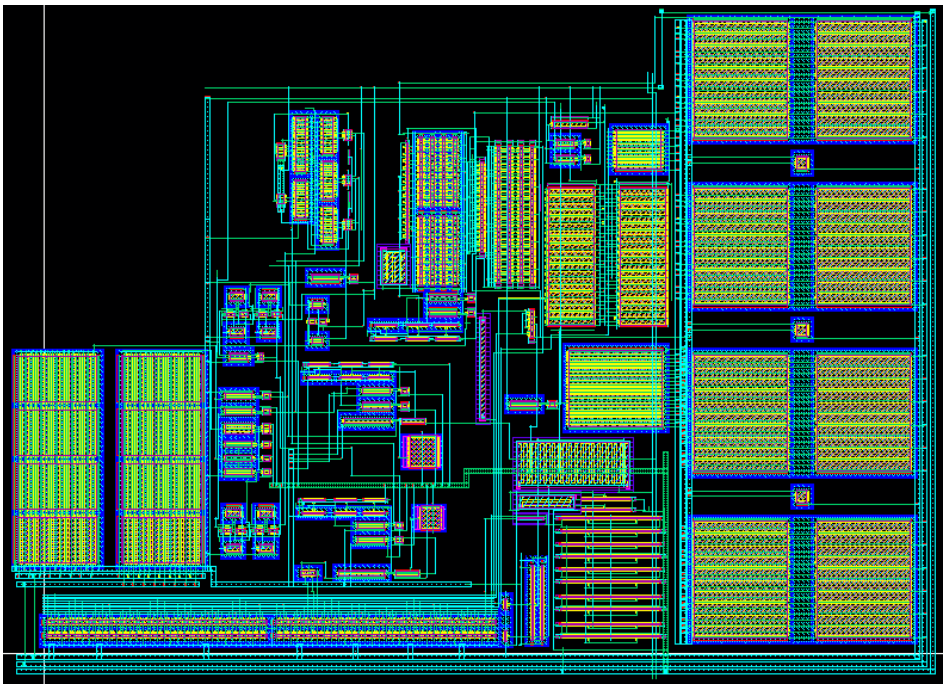


B. Inductor Peak Current Sensor (IPK)

a. This module contains the cellviews:

i. COMPARATOR_LATCH_IPK- Comparator for current sensors

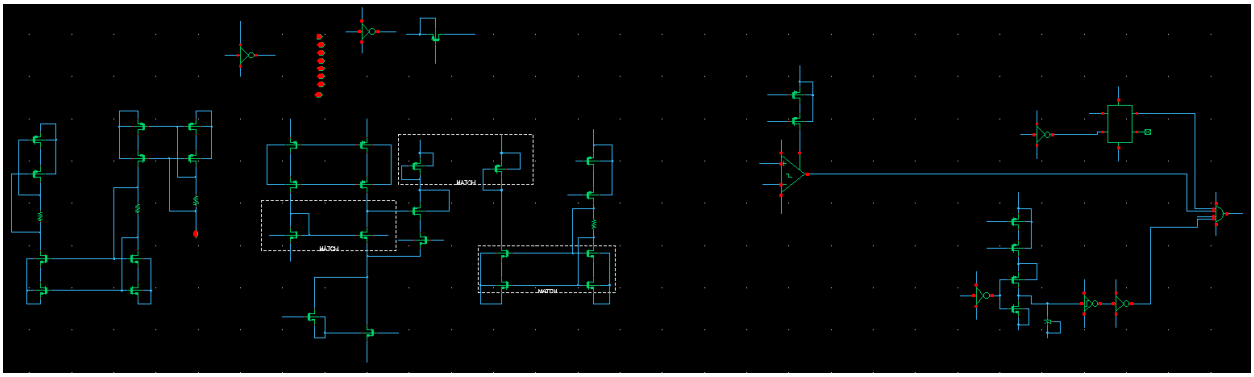


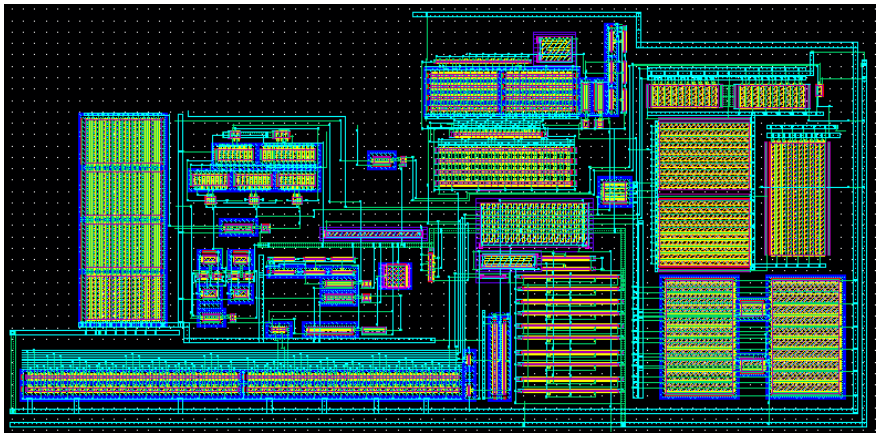


C. Zero Current Detector (ZCD)

a. This module contains the cellviews:

i. COMPARATOR_LATCH_IPK - Comparator for current sensors

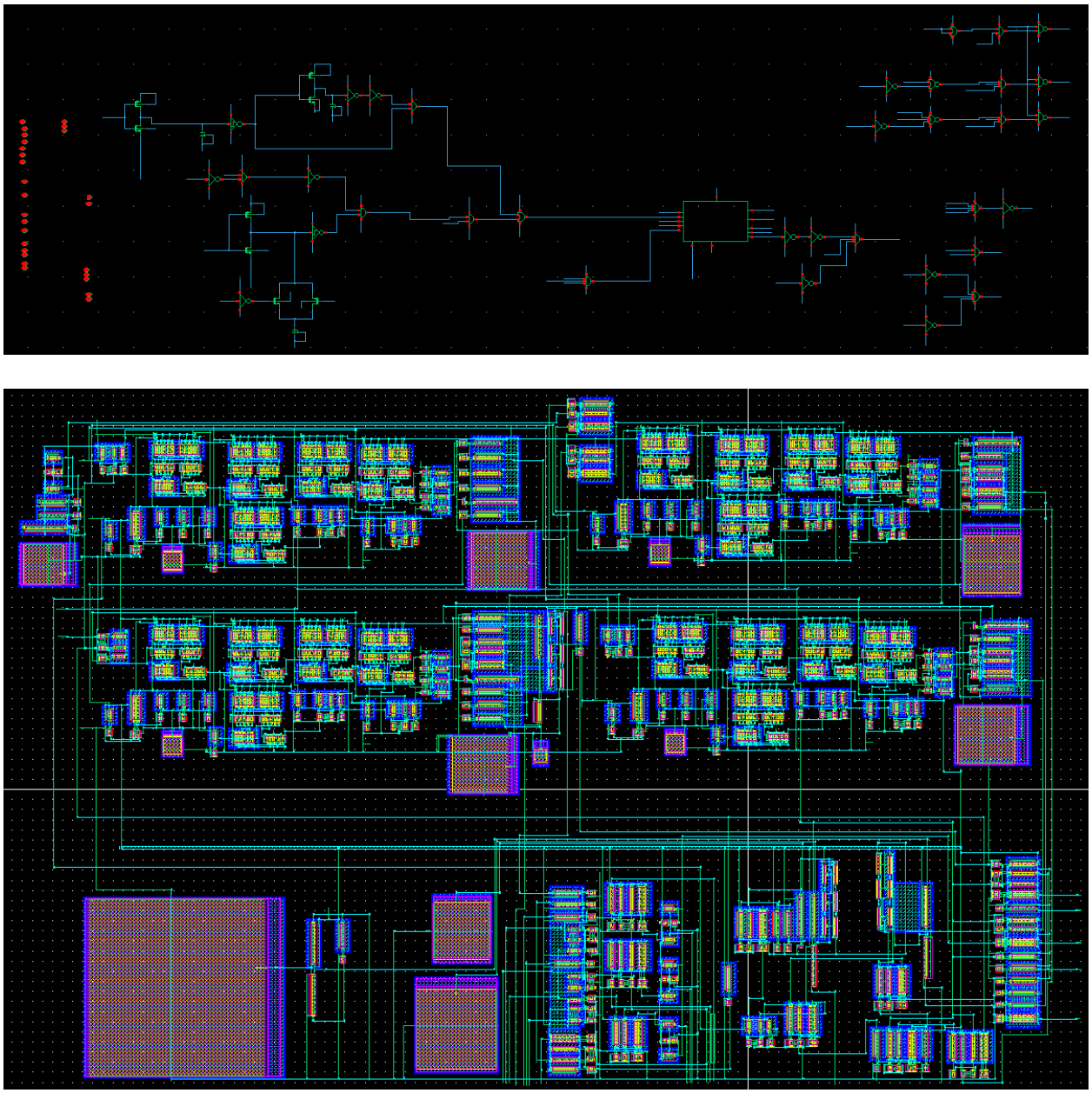




D. Logic

a. This module contains the cellviews:

i. LOGIC_CYCLE – Asynchronous State Machine



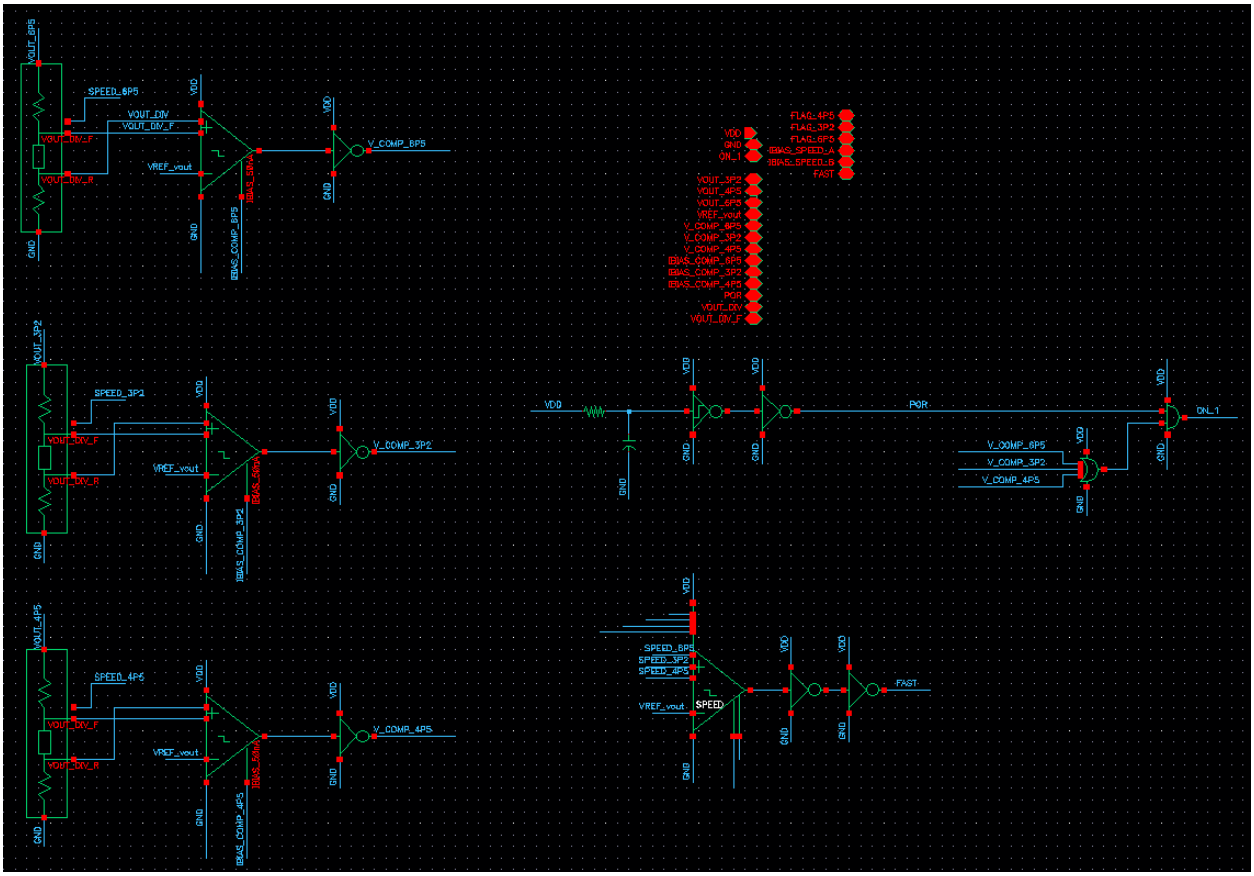
E. Charge Monitor (CharMon)

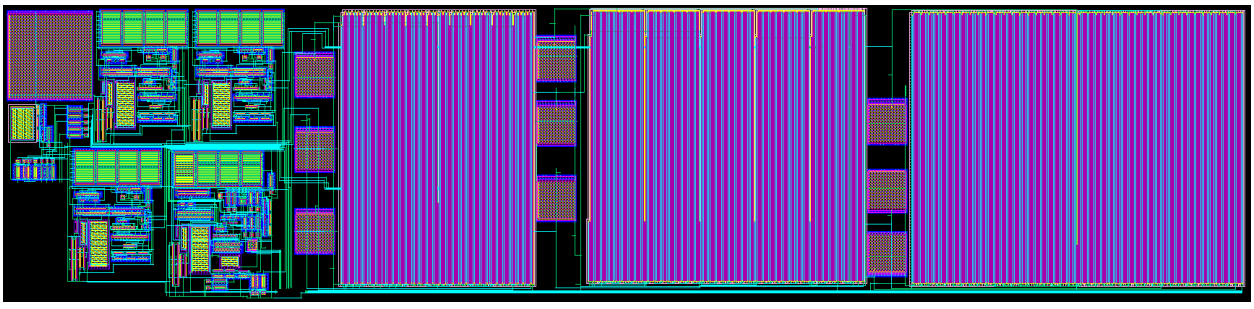
a. This module contains the cellviews:

i. COMPARATOR_LATCH_OUTPUTS – Comparator Monitoring Outputs

ii. COMPARATOR_SPEED – Comparator Monitoring Startup Acceleration

iii. VOUT_..._RESISTOR_DIVIDER_... – Outputs Sensing Networks





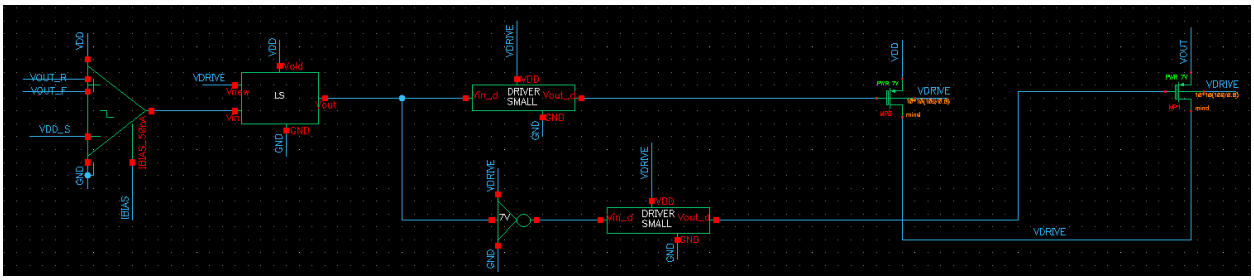
F. VDRIVE Selector

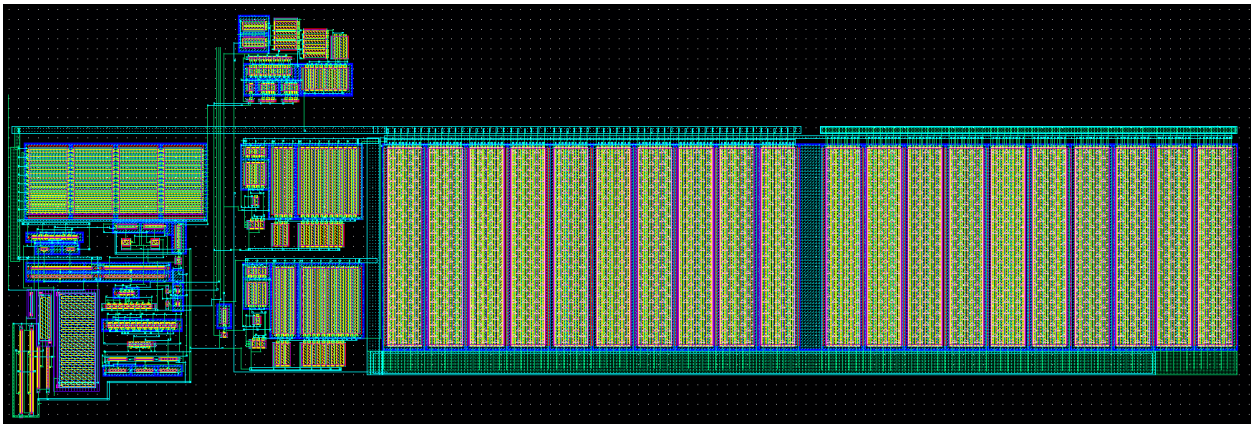
a. This module contains the cellviews:

i. COMPARATOR_VDRIVE – Comparator Monitoring VDD & VOUT3

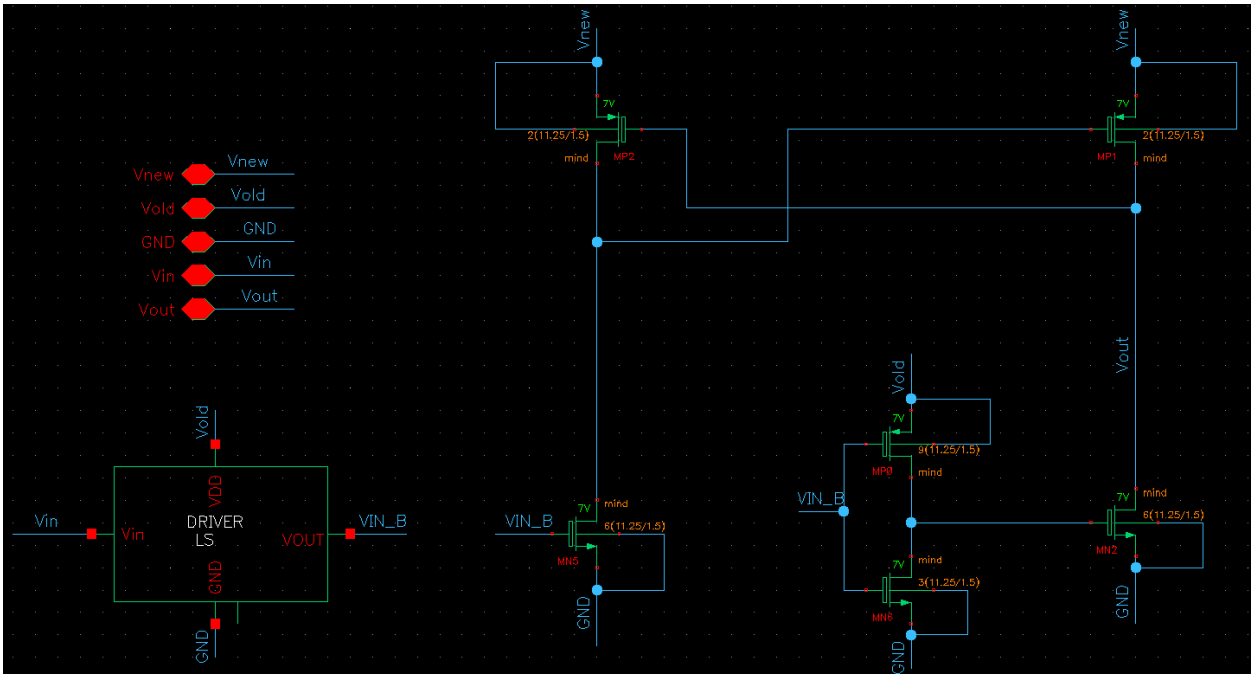
ii. DRIVER_SMALL – Buffer to drive the Power PMOS

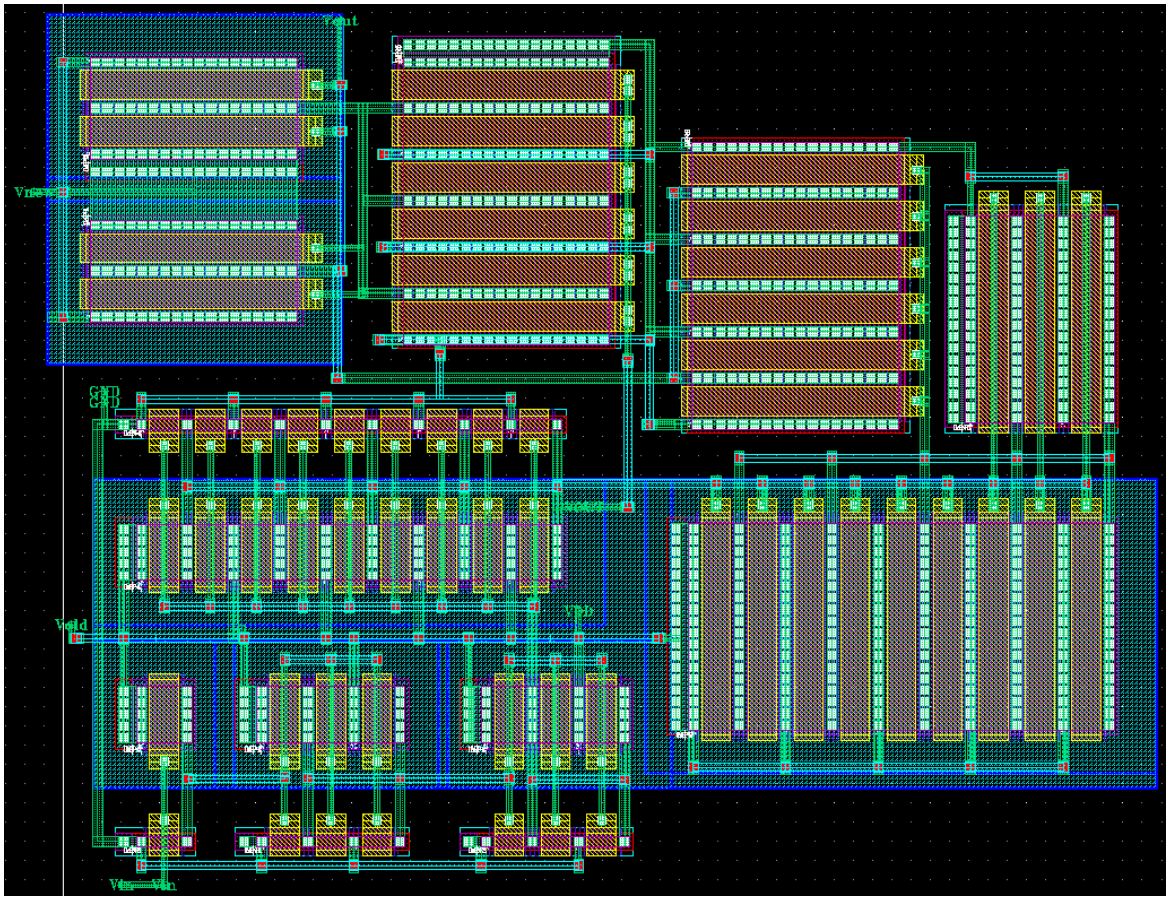
iii. LEVEL_SHIFTER – Level Shifter discussed in section 3.8



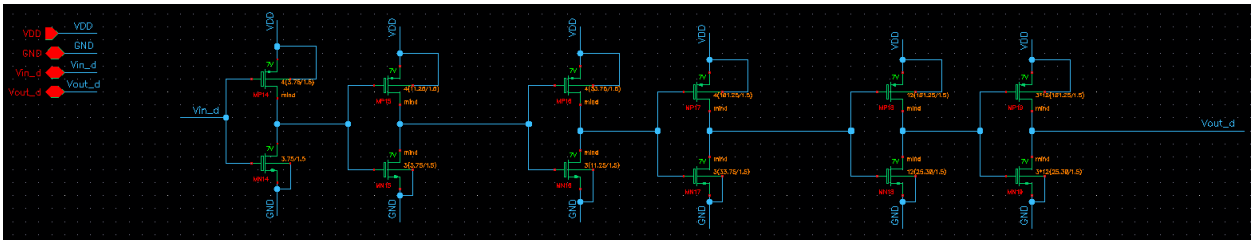


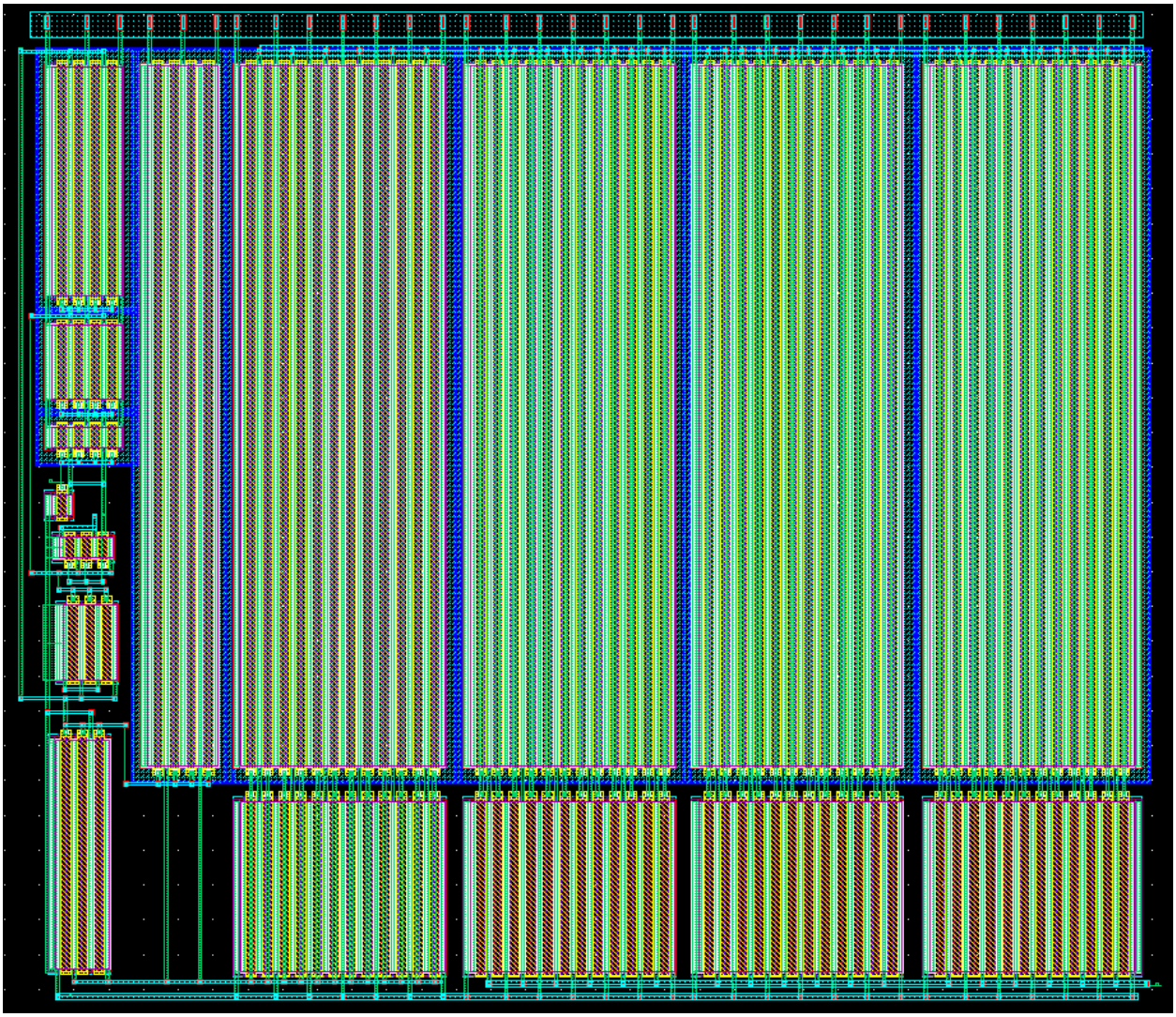
G. Level Shifters (LS)





H. Drivers (DRIVERS)





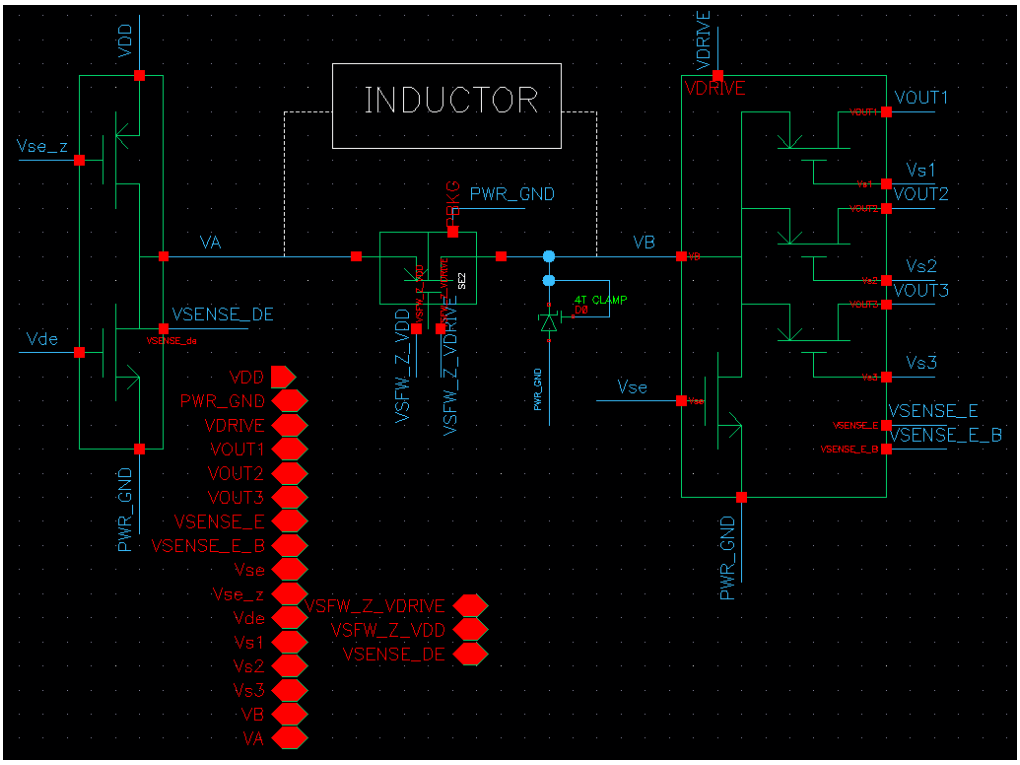
I. Switches

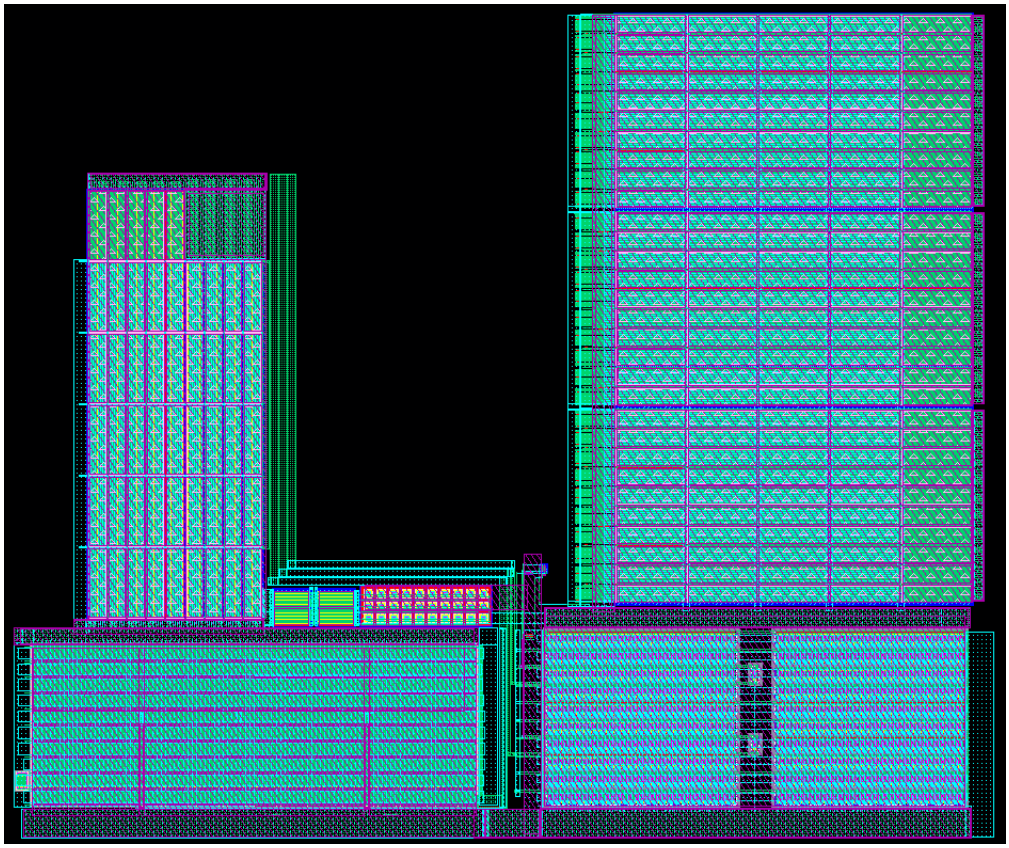
a. This module contains the cellviews:

i. VA_SWITCHES – Contains the MP3 and MN2 Switches of Figure 2-10

ii. VB_SWITCHES – Contains the MP1, MP2, MP3, and MN1 Switches of Figure 2-10

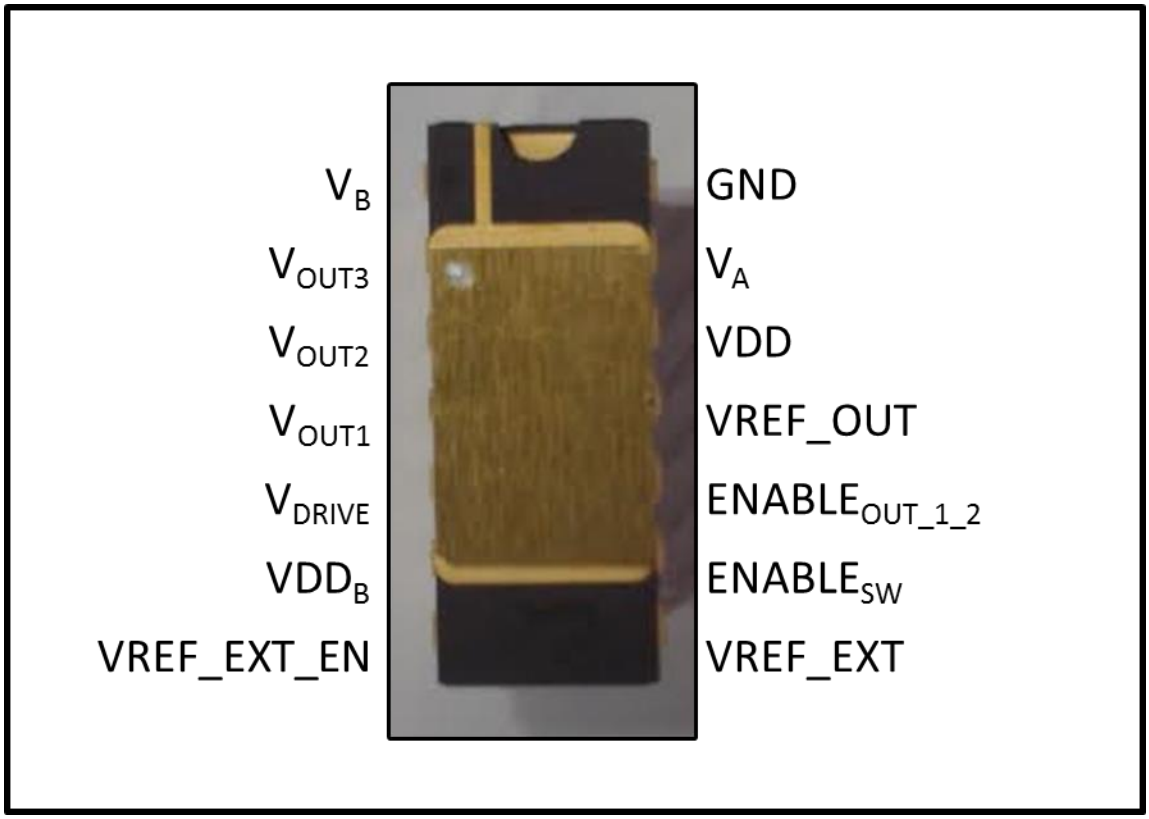
iii. SFW – Contains the MP5 switch of Figure 2-10





Appendix B – Testing Setup

The PMIC was packaged inside a Dual in-line Package (DIP) of 14 pins, which photography is shown below along with the pins identified. The package isn't permanently sealed with the objective of being able of looking it through the microscope.

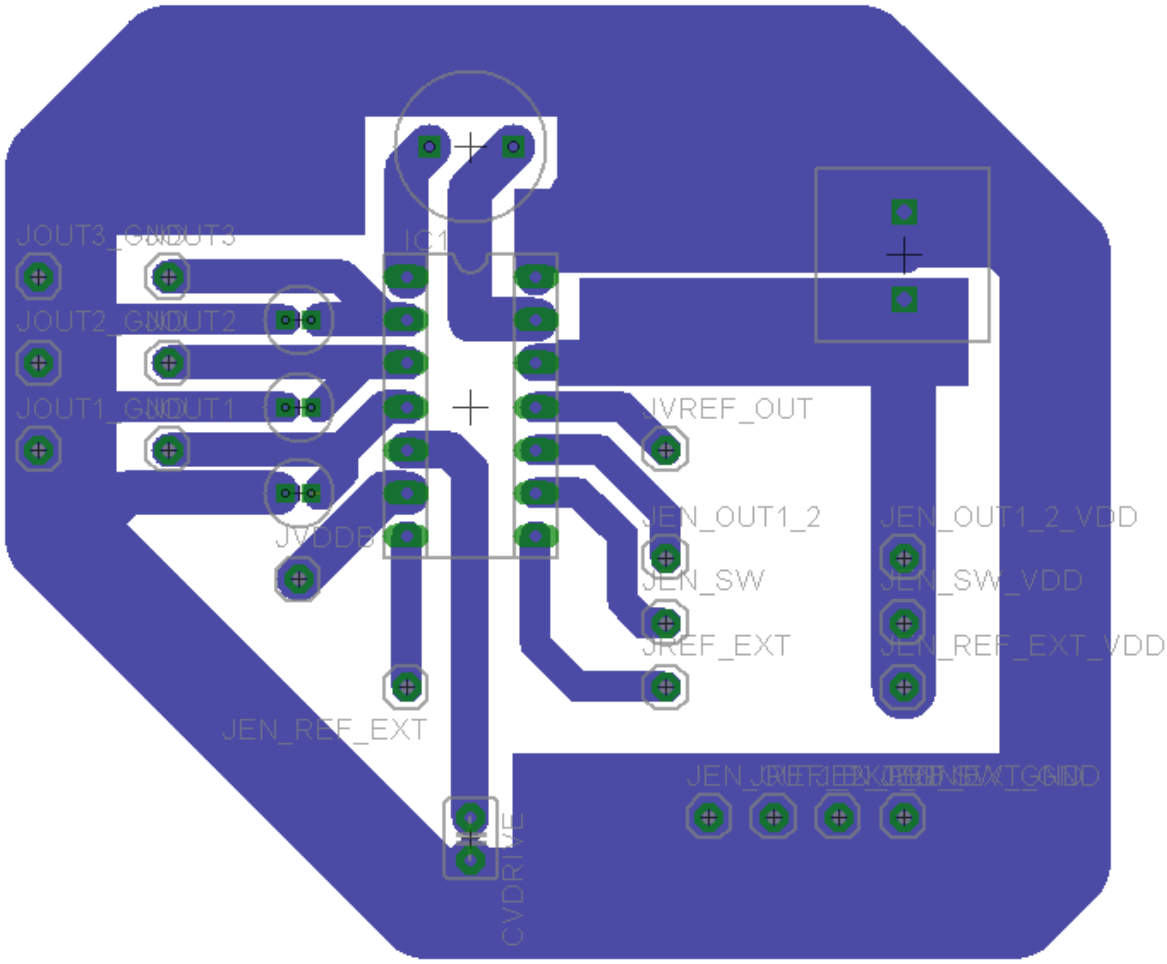


The table below offers a summary of the device's pins, including a brief description of them.

Pin Name	Description
V_B	One of two inductor Terminals
V_{OUT3}	Output 3 Node
V_{OUT2}	Output2 Node
V_{OUT1}	Output 1 Node
V_{DRIVE}	VDRIVE voltage used for Power PMOS Bulk Potential. Provided Internally
VDD_B	Supply voltage for Internal Reference Buffer $VREF_{INT}$
VREF_EXT_EN	Digital enable to use the external reference voltage connected to VREF_EXT
VREF_EXT	External reference voltage input pin.
$ENABLE_{SW}$	Digital enable to regulate all the outputs
$ENABLE_{OUT\_1\_2}$	Digital enable to regulate outputs 1 and 2
VREF_OUT	Internal reference buffer output providing the $VREF_{INT}$ as an output
VDD	Supply Voltage
V_A	One of two inductor Terminals
GND	Neutral Node

The PCB layout used for the testing process is shown below. External inductor, capacitors, and load were included inside the PCB. The components used during the device testing are summarized in the table below.

Component	Value	Part Number
External Capacitors	4.7 µF	USR1V4R7MDD
External Inductor	10 µH	RFB0807-100L


JOUT3_GND
JOUT2_GND
JOUT1_GND
IC1
IVREF_OUT
JEN_OUT1_2
JEN_OUT1_2_VDD
JEN_SW
JEN_SW_VDD
JREF_EXT
JEN_REF_EXT_VDD
JEN_REF_EXT