AUTOMATED CHARACTERIZATION OF THE DYNAMIC ON-RESISTANCE (R_{DSON}) IN A POWER MOSFET

By

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The technological community is highly focused in the area of power electronics. Specifically, these efforts can be observed in the design of efficient power transistors that can handle known and unknown applications to come. Part of the design process is to obtain accurate characterization data from a device under test.

This thesis presents the automation of extracting of the dynamic on-resistance (R_{DSon}) of power MOSFETS using low cost equipment. The automation procedure is presented in a replicable and systematic environment. This work also presents the execution of two different measurements, single pulse and multiple pulse (stress test) measurements. The current setup is implemented for measuring dynamic on-resistance in a three terminal packaged devices.

R_{DSon} measurements were taken under several conditions that verified the accuracy and precision of the extracted value. The results show that the implementation is capable of extracting the R_{DSon} in an automated setup with minimal intervention from a user.

Resumen de tesis presentado a la Escuela Graduada
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CARACTERIZACIÓN AUTOMATIZADA DE LA RESISTENCIA DINÁMICA (R_{DSON}) EN UN TRANSISTOR DE POTENCIA MOSFET

Por

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Julio 2015

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Departamento: Ingeniería Eléctrica y Computadoras

La comunidad tecnológica está altamente enfocada en el ámbito de la electrónica de potencia, particularmente en el diseño de transistores de potencia eficientes que puedan manejar futuras aplicaciones ya sean conocidas o desconocidas. Parte del proceso de diseño es obtener datos de caracterización de manera rápida y precisa de un dispositivo bajo prueba.

Esta tesis presenta la automatización de la extracción del valor de la resistencia dinámica (R_{DSon}) de transistores de potencia MOSFET con instrumentación de bajo costo. El procedimiento de automatización se ejecuta en un ambiente replicable y sistemático. La ejecución de la medición es realizada por dos métodos, la extracción en un solo pulso y la extracción en pulsos múltiples (prueba de esfuerzo). La configuración actual permite la medición en dispositivos empaquetados de tres terminales.

Las medidas de la resistencia dinámica se hicieron bajo varias condiciones que verifican la exactitud y precisión del valor obtenido. Los resultados muestran que la aplicación es capaz de extraer el valor de R_{DSon} en un sistema automatizado con intervención mínima del usuario.

To my family and friends...

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List of Abbreviations

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
DC	Direct Current
AC	Alternating Current
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOS	Vertically Diffused Metal Oxide Semiconductor
VI	Virtual Instrument

Chapter 1
Introduction

Dynamic On-Resistance (R_{DSon}) is a key factor in power MOSFET design, and usage. MOSFET is an acronym for Metal-Oxide-Semiconductor Field Effect Transistor. These transistors are designed to be majority carrier devices that are controlled through the presence of an electric field. Power MOSFETS are transistors specifically designed to handle large voltage and current across the device channel. A vast amount of effort has been placed into designing power MOSFETS that excel in having the aforementioned characteristics. This has led to the design of new structures for power MOSFETS and exploiting their limits. [1]. The need for better, more efficient power MOSFET structures still continues to this day. For example, in the late 1990's the superjunction power MOSFET structure was introduced [2]. Also a lot of effort has gone into developing materials and structures that have better intrinsic behavior than the traditional silicon devices such as: GaAs,Ge and GaN. [3]

An important need in this design process has been to accurately characterize data in the shortest possible time frame. This allows the engineer for rapidly assessing the behavior of the device and for correcting evident flaws that may showup in the design of the transistor. For power MOSFETS, the dynamic on-resistance is the observed voltage-to-current ratio from the drain to the source of the device when the device is fully turned on. The measurement of dynamic on-resistance for the several families of transistors (BJT, MOS, IGBT, ect) is a well known key characterization test.

Obtaining characterization data through an automated environment gives the end user faster access to desired data. For example, efforts have been dedicated to

automating the extraction of switching losses for IGBT devices [4]. Additionally, there is always a strong push in developing circuital topologies that reduce non desirable effects (such as ringing, self heating) during testing for switching losses [5]. There are different circuit topologies that have been used to provide the voltage to current ratios of a transistor with reduced loss of information. [4, 6, 7]

Rapid access to accurate dynamic R_{DSon} data for the designer is key in reducing development and production time. Automating the dynamic R_{DSon} test allows for the rapid data capture. For the purpose of this automation has two main criteria. One, is automation with respect to data capture. Secondly, the automation of the movement and post processing of the obtained data with no user intervention.

This work presents an automated procedure to extract the dynamic on-resistance of a power MOSFET. The extraction procedure is fully automated using LabVIEW software as a platform with the use of commercial accessible hardware. This setup allows the user to execute the test under minimal supervision.

This document is organized as follows: Chapters 2 and 3 present the theoretical foundations of the proposed and previous work in the field. Chapter 4 provides a more formal discussion of the problem and the hypotheses which this work was based on. Chapter 5 gives an overview of specific objectives and the methodology followed to obtained them. Chapter 6 examines the circuit used for the R_{DSon} test. Chapter 7 discusses the specifics of automation used for the implementation of the R_{DSon} test. Finally Chapters 8 and 9 exhibit the results obtained, a detailed discussion and a summary and conclusion of the work rendered.

Chapter 2
Theoretical Background

This chapter reviews fundamental concepts necessary to understand the R_{DSon} test, its execution and automation.

2.1 Power Transistors

Power transistors such as: Power MOSFETS, IGBT's, and BJT's are devices specifically designed to sustain large breakdown voltages and high current densities through their channels. They are used throughout a wide range of applications such as in: power and energy, automotive, home appliances (HVAC and motor control), and others. The inherent qualities of power transistors require a series of specific characterizations tests to determine how well a device performs. These devices are normally operated in a switching mode, meaning they are either fully turned on or off [8]. Some key parameters include [9]:

- Dynamic On-resistance(R_{DSon})
- Breakdown voltage(V_{BSS})
- Reverse Recovery Charge(Q_{rr}, t_{rr})
- Intrinsic Capacitances(C_{iss}, C_{oss})
- Gate Charge(Q_g)

Since R_{DSon} is the focus of this work, a more thorough discussion will be presented in the following sections and the upcoming chapters. For the remaining tests, concise definitions will be offered in this section [10–12].

The breakdown voltage (V_{BSS}) is the largest voltage that the transistor can sustain across the device channel with no inversion layer present for conduction. Once the breakdown voltage is reached, conduction will take place regardless of the signal present at the gate of the device.

Powers MOSFET have a body diode parallel to its channel. The body diode is an intrinsic by-product of a MOSFET formed by the PN junction in its physical construction. They are common instruments in switching application used as free-wheeling diodes at no additional component cost. Once a power MOSFET is choosen for an application, the behavioral characteristics of its body diode are also well defined. The reverse recovery charge is a characterization test for diodes. Reverse recovery takes place when a diode carrying a positive forward current is switched off instantaneously. After turn-off the current changes direction (negative current) and the amount of time for charge recombination to take place is known as the reverse recovery.

The intrinsic capacitances are the capacitances that are formed during device fabrication. Some capacitance dominate the input behavior of the device (C_{iss}) other the output behavior (C_{oss}) during device switching. Manufacturers give information of the behavioral dynamics of these capacitances in the device datasheet as part of the characterization data.

Finally, the gate charge (Q_g) refers to the amount of charge that needs to be accumulated in the gate of a power MOSFET for the device to turn-on. This allows a user to determine the current required to turn on the transistor in a desired amount of time.

2.2 Dynamic On-Resistance

R_{DSon} is ratio of the drain to source voltage V_{DS} to the drain to source current I_{DS}, when the transistor is fully turned on under switching conditions.

$$R_{DSon} = \frac{V_{DS}}{I_{DS}} \tag{2.1}$$

The switching behavior of a transistor is difficult to model. It has a non linear behavior and it is laborious to express analytically due to the device intrinsic capacitances [9] [13] [14]. This switching behavior foreshadows the definition of dynamic in R_{DSon}. The channel resistance varies ideally from infinity (no-channel present) to a minimum value, hence dynamic on-resistance.

In a power transistors, a key parameter in the validation of transistor fabrication processes is the calculation of the dynamic on-resistance. Its measurement helps to determine the losses to be incurred in the switching action of the transistor. Specially since power transistor by their nature operate under high voltages and/or high current conditions, the losses can be significantly higher than voltage or current operation. The measurement also plays a vital role in the performance of power converter circuits such DC-DC and AC-DC [15].

A way to clarify the losses seen by R_{DSon} in a power transistor is to calculate the power loss in a known condition. Since R_{DSon} is a linear model describing a power MOSFET under specific conditions, the power consumption can be described by the following equation [16]:

$$P_{DS} = R_{DSon} x I_{DS}^2 \tag{2.2}$$

As mentioned in the previous section, R_{DSon} is a critical parameter but it is not the only one for power MOSFETS. During operation the gate charge of a power MOSFET increases as dynamic on-resistance decreases, a definitive trade-off during the device design. Such trade-off has brought forth discussion of a figure of merit

for power MOSFETS. Examples of this discussion include the gate charge-dynamic on-resistance product(Q_g x R_{DSon}), the discharge rate of the input capacitance and discharge rate of the output capacitance, among others. [11]

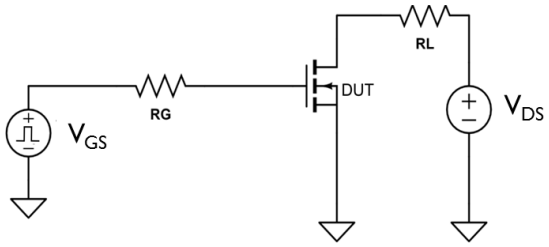
2.3 Dynamic On-Resistance Test Condition

In the dynamic on-resistance characterization test, a power MOSFET is taken through all its regions of operation from fully turned-off to fully turned-on very rapidly and very abruptly. Figure 2.1 illustrates the general circuit model of the test. Conditions for the dynamic on-resistance test include the following:

- $V_G >> V_t$ when the transistor is fully turned on
- Duty Cycle of Gate Pulse has a maximum of 10 %.
- $V_D >> V_G - V_t$ (i.e. Saturation)

V_G is the gate potential, V_t is the threshold voltage and, V_D is the drain potential.

Figure 2.1 : Fundamental Test Circuit for R_{DSon}



A pulsed voltage source connected to the device gate turns the DUT on and off. The load connected to the DUT drain is monitored by measuring its voltage and current waveform, allowing for the R_{DSon} value to be calculated. Variants of the test execution may also include a switching source in the load voltage [7].

2.3.1 JEDEC Standards

The Joint Electron Device Engineering Council (JEDEC) is an independent semiconductor engineering trade organization and standardization body. They offer a

library of standard procedures and expected metrics for the testing and characterization of semiconductor devices. For dynamic on-resistance, JEDEC does not offer a direct standard like it does for diode reverse recovery charge. But their standard JESD24-1 : "Method for Measurement of Power Device Turn-Off Switching Loss" [17] gives an overview for switching test conditions. Some conditions can be adopted in the R_{DSon} test since it is a characterization test of switching nature. The standard recommends:

- Sampling Time must be at least twice as fast as the fastest signal in the circuit
- On-State Current must be known (I_{DSon})
- Off-State Output Voltage must also be known (I_{DSoff})
- Input Drive (Pulse Signal): Any appropriate method that ensures a strong delivery is favored. It should not raise the junction temperature (T_j)
- Output Load: Should have the same considerations as the input drive with respect to T_j
- Circuit Layout is critical; the ground path, minimizing stray capacitances are examples of key layout items.

2.3.2 Single Pulse and Stress Test

It is important to consider that besides capturing a single set of voltage and current waveforms from the device, it is also necessary to observe the transistor behavior when subjected to a load voltage for an extended period of time. This is the premise of the R_{DSon} Stress Test, simulating an everyday use of the power MOSFET. Does the device sustain its expected behavior over a determined time frame? When does it being to degrade? How does the degrading behavior happen? General characteristics of the stress test include the following:

- Ability of providing the switching voltage and current waveforms
- Ability of running test a long period of time (i.e. 10 hours for example)

- Ability of capturing waveform data sets (voltage and current) in a defined period of time during the test run. (i.e. capturing data every 5 minutes during the an hour long test)

2.4 Use of R_{DSon}

As established previously, the dynamic on-resistance is used to quantify switching losses of a power device. But also, the unwanted fluctuations of R_{DSon} can serve as a precursor of other fabrication or usage failures. Celaya et al. [18] applied the field of prognostics to power MOSFETS. Since R_{DSon} has dependencies on junction temperature (switching losses due to resistive behavior and thermal dissipation), it has been used as a precursor to failure indicator for die attachment.

Chapter 3
Previous Work

This chapter presents relevant work dedicated to characterizing the R_{DSon} behavior in power transistors. Main items to be discussed are the following: power MOSFET structure and the origins of R_{DSon}, efforts devoted to measure R_{DSon}, the work dedicated to elucidating the physical mechanisms that describe the R_{DSon}, and attempts to partially automate the extraction of R_{DSon}. The following section introduces the theoretical aspects and basic concepts related with the R_{DSon}. The chapter concludes with a summary of the ideas discussed here.

3.1 Power MOSFET Structure

This work focuses on the extraction of R_{DSon} of a power MOSFET. Yet, before extracting R_{DSon}, understanding its origins and subsequent importance is fundamental and of explanatory nature for the purpose of this work. Power MOSFETS are designed in several structures that allow for substantial increases in breakdown voltages and sustaining higher currents through its channel. Examples of power MOSFET structures include: DMOS, VDMOS, LDMOS, Trench and superjunction. All structures have their advantages and disadvantages regarding design and fabrication [10, 19]. Additionally, there are structures based on materials such Silicon Carbide or GaN [3,20]. For example, a GaN power MOSFET requires a negative pulse voltage in order to turn-off the device because of the intrinsic channel formation in its structure.

3.2 Dynamic On-Resistance

Temple et al. performed an experimental design for a 600 volt power MOSFET with a vertical source-drain geometry [21]. Their work highlighted not only the relationship between R_{DSon} and breakdown voltage but also the trade-off between switching frequency and R_{DSon}. Although showing great promise by increasing the breakdown voltage from 50 to 100 volts this work did not pursue alternate junction structures for the power MOSFET device. It was limited by not reducing the dynamic on-resistance present in the intrinsic structure of the device.

Sun and Plummer gave analytical expressions to the dynamic on-resistance of three structures proposed at that time for power MOSFETS: VMOS, VDMOS and LDMOS. They used the technique of ion implantation and separating the channel from the drift region of the device through a lightly doped region to improve the performance of the device. The novel structures at the time showed increases in breakdown voltage and minimize R_{DSon} [22]. Furthermore, by this new physical device design, analytical expressions that describe the dynamic on-resistance were determined by showing that the resistance is dominated by drift region bulk resistance, and that it reduces until it saturates as $V_{GS} - V_{TH}$ increases. One of the main aspects of this work that is not important to forget is the fact that these analytical equations are dependent on the device process and technology used to create it.

Gelagaev et al. discussed current circuits used for capturing R_{DSon} data and provide optimization to a known circuit [23]. His work provides a more formal discussion on the implementation of clamping circuits for the improvement of resolution. It also provides for an analytical discussion quantifying the accuracy of the test circuit.

3.3 Characterization Test Automation

Next is a discussion of the efforts performed to automate the R_{DSon} characterization test.

Shen, et al. designed in LabVIEW a semi automated test environment to extract switching losses from IBGTs. Using a DSP and an oscilloscope combined with their test bench they extracted the switching voltage, current waveforms and calculated the power and energy waveforms for an IGBT [4]. Most of the post processing work on the extracted data was done in MATLAB. The test environment was controlled with the use of the LabVIEW software which provided minimal human intervention when the test was executed. There is minimal discussion to any considerations to be taken when executing the test with respect to timing. Also, little attention is given to how the device is turned on and off (pulse delivery).

Joh et al., provided insight into present-day automation efforts for current collapse measurements in GaN devices. One of the reason to highlight this work is because of their use of the semiconductor device parameter analyzer [24]. These instruments provide an on suite solution for several characterization tests but the costs begin in the $\$30,000$ to $\$40,000$ dollar range making them more expensive for the contemporary working environment where streamlining and reduction costs is the main order of the day.

Jin et al. also used these instruments to measure GaN R_{DSon} over a span of eleven decades (gate voltage signal periods from ns to ms). To achieve this they combine the response of two semiconductor device analyzer the Agilent B1500 and Auriga AU4750. They used the Auriga to measure R_{DSon} from 200ns to 3ms periods and the B1500 for greater than 3ms. One of the distinct condition of the R_{DSon} extraction in this paper was that both the gate and drain voltage signal were switching synchronously. This effort is mostly dedicated to elucidate the mechanisms responsible for R_{DSon} in terms of observing the release of trapped electrons in the AlGaN/GaN barrier [7]. The authors found that border traps dominated the R_{DSon} behavior in short time scale and thermal effects in the surface traps dominate in the larger time scales. Again the semiconductor device analyzer was a limiting factor for test replication.

In [7] there was neither a stress test being performed in the device,just single pulse measurements captured from the device. It is important to note the method of extraction of the actual R_{DSon}. The condition for extraction was when the device is fully turned on, sample and average R_{DSon} value. Once the point in time where the sampling would take place was selected, 300 samples spaced at $5ns$ each are taken from the voltage and current waveforms respectively. An average of the 300 points for each waveform was the value used for the R_{DSon} calculation. Yet the criteria of selecting the extraction moment was not discussed.

Lu et.al [25] presented a methodology for extracting R_{DSon} under soft and hard switching conditions. Hard switching refers to having a load voltage present (V_{DS} ¿ 0) when the device is turned on. Soft switching refers to having no load voltage ($V_{DS} = 0$) when the device is turned on. The authors presented the need of a circuit topology that improves the resolution of the measured drain voltage. Typically, the drain voltage in power transistor switches from a high voltage (600V) to low voltages (millivolts) from turn off to turn on. This is a five order magnitude drop in the range of the measured value. This implies a loss of resolution in the instrument used to measure the signal. Lu et.al depicted the use of a clamping circuit to act as a voltage follower limited up to 5.1 volts by the use of a zener diode bridge in the source of the clamping transistor. This arrangements reduced the change by three orders of magnitude and increased the available resolution to be more precise in the millivolt range. The authors tested this circuit topology under both hard and soft switching condition with specific circuit designs for each switching condition. No attempts at automation were done for this proposed setup. There were no discussions of when is it appropriate to sample the voltage and current signals, only the condition of the device being fully turned on for the R_{DSon} extraction.

Gelagaev et al. [15] presented the use of a another clamping circuit with a zener diode in it. Discussing the criteria of when to sample and how to process the samples

taken, Gelagaev, et al. also chose a point in time where the device is fully turned on to extract the waveforms. For the calculation, the R_{DSon} waveform was obtained by dividing the voltage and current waveforms and extracting the R_{DSon} is a post-processing exercise. Afterwards, the power waveform was calculated by multiplying the R_{DSon} waveform by the square of instantaneous current signal. This work did not reflect on the criteria for sampling and waveform extraction, it presumes the condition of fully turned-on to begin sampling.

Table 3.1 summarizes the relevant aspects of the previous work

Table 3.1 : Dynamic R_{DSon} Test Review

Device Family	R_{DSon} Test	Automated Test	LabView	Stress Test
MOS	Yes [15]	No	No	Yes [18]
IGBT	Yes [26]	Yes [4]	Yes [4]	Yes [27]
BJT	Yes [28]	No	No	Yes [29]
GaN	Yes [25]	No	No	Yes [30]

Chapter 4
Problem Statement and Hypothesis

4.1 Problem Statement

The problem addressed is the implementation of an automated extraction for R_{DSon} in power MOSFETS through the use of low cost equipment. Recall from previous discussion in Chapter of the high cost of semiconductor device analyzers as limiting factor for test replication. Some of these instruments cost in the high thousands of dollars or greater. It is critical of this work achieve this automation using low cost, commercially available equipment.

Low-Cost is relative term. The end user of the R_{DSon} test would be a test or characterization engineer that works in a lab in an industrial or research and development setting. In such settings, there is equipment whose value can range from the tens of dollars to millions. Typically, reliable testing equipment will start in the thousands of dollars range. At any company, industrial or not, minimizing operational expenditures is always a high priority item. It is always highly desired to have low cost solutions implemented that save the company additional expenses or reduce current ones.

Additionally, test execution should be in a minimally supervised environment. This relates to lower costs from an operational stand point. as it required less man-power to execute the test.

From an implementation standpoint, to obtain exact measurements of R_{DSon}, it is important to understand what factors are significant for its implementation.

Factors that could affect the R_{DSon} measurement in a power MOSFET include: circuit topology for curve extraction, suitable instrumentation for test execution, and software considerations taken for the automation process.

Also, there are several topologies that can be used to extract the V_{DS} and I_{DS} curves to calculate the R_{DSon}. These include direct measurement on the DUT or indirect measurements from the DUT. Examples of these setups are: setting up a current probe in series with the DUT in order to extract the I_{DS}. An indirect measurement is measuring the voltage across a resistance and determining the current through Ohm's Law instead.

Another major factor for R_{DSon} measurement is the use of proper instrumentation. Recall that the fundamental idea of R_{DSon} is to provide a load voltage and pulse the DUT on and off in order measure the current and voltage through the channel. An example of required instrument behavior is the delivery the load voltage and the current required by the circuit (e.g. a high slew rate for the load voltage supply).

An additional critical consideration is the physical setup of both the circuit and instrumentation. A compact setup that reduces the introduction of unwanted effects is essential (minimal ringing, for example). By definition, a power MOSFET may use high voltage, high current or both conditions.

4.2 Hypothesis

This work is presented under the following hypothesis:

An automated solution for R_{DSon} measurement in power MOSFETS can be implemented using accesible low cost equipment in a minimally supervised environment.

There additional key items that highlight the steps necessary to achieve the desired goal:

- Improvements on the known existing methods and solution for R_{DSon} testing can be performed. This included reduction of undesired effects in the hardware side, and use of low cost of-the-shelf equipment for test execution.

- An automated extraction procedure for the R_{DSon} can be developed using experimental data.
- An automated procedure used to quantify R_{DSon} can be developed with a circuital setup aided by a virtual instrument platform.
- Both the automated extraction and automated calculation procedure will permit a minimally supervised test environment for theR_{DSon} test.

Chapter 5
Objectives and Methodology

5.1 Objectives

The objective of this work was to develop an automated extraction and calculation method for R_{DSon} in power MOSFETS using low cost equipement. This was aimed at allowing the user to distinguish a measurement from reliable R_{DSon} from that of a faulty device. Also there were particular objectives necessary for the completion of the main objective:

a) Development of a test architecture and excitation circuit that is proper for R_{DSon} measurement.

b) Development of an automated procedure that extracts voltage and current curves required for R_{DSon} measurement.

c) Development of an algorithm that determines the R_{DSon} value by processing the extracted data curves.

d) Development of single pulse and stress test measurement tests.

e) Implementation of the test using low cost equipment.

f) The validation the model and the extracted R_{DSon} value of the DUT.

5.2 Methodology

With the objectives identified, a methodology was devised and followed to achieve these objectives. Figure 5.1 shows a cognitive map for the methodology.

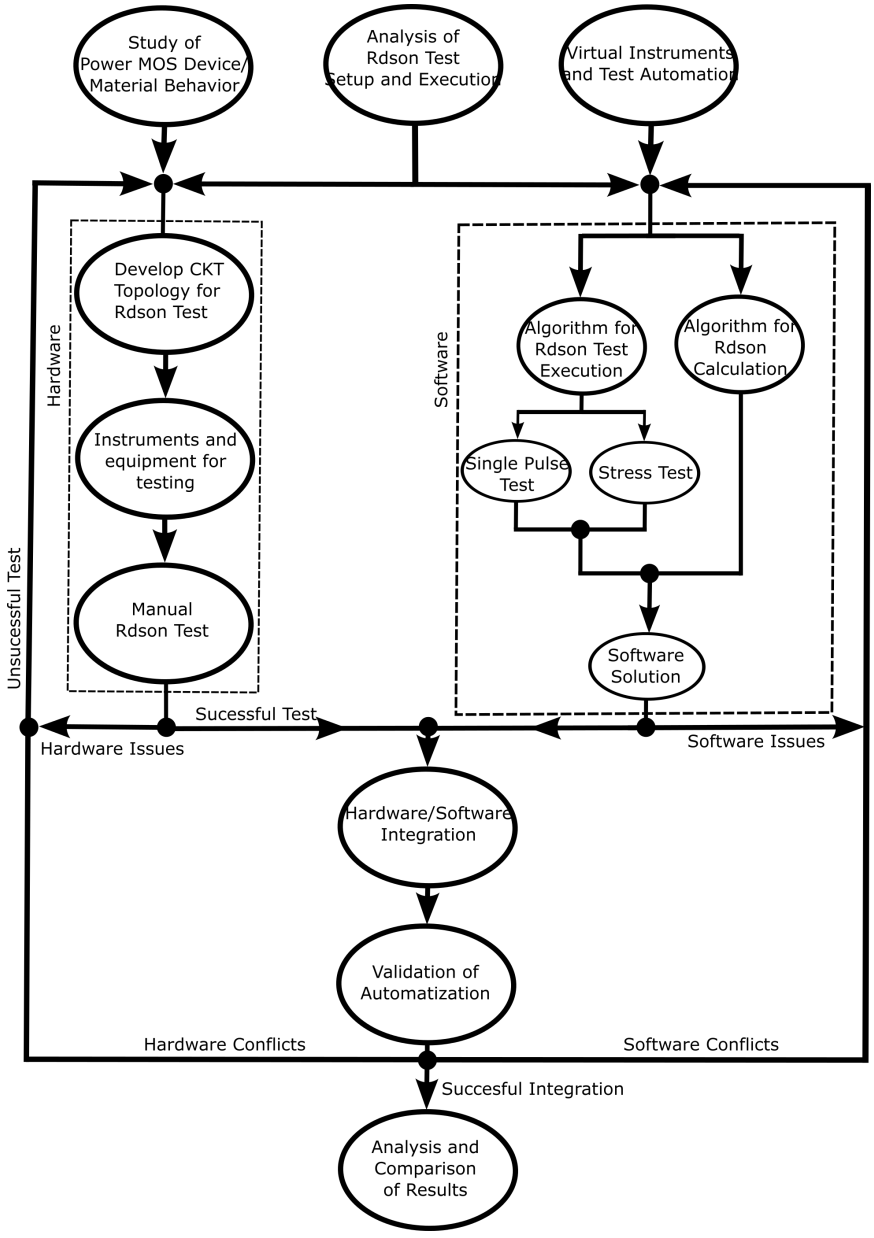


Figure 5.1 : Diagram of methodology flow

The methodology is implemented by first integrating the past work dedicated to power MOSFET behavior, R_{DSon} extraction, and the virutal instrumentation/automation. Integrating knowledge of all three areas allowed to select a suitable R_{DSon} circuit, proper instrumentation and to devise an algorithm to calculate the R_{DSon} value for the power MOSFET.

Next, the major tasks of the methodology to reach each particular objective are discussed:

5.2.1 R_{DSon} Test Circuit

A revision of the circuit topologies used to measure R_{DSon} was required to determine the topology used to execute the test. The R_{DSon} test circuit must provide the information required to obtain the voltage and current curves for the R_{DSon} calculation. There are fundamental circuit implementations based of industrial notes. [2,31] Most of them suggest to use the circuit shown in Fig 2.1 . The major steps taken to obtain the test circuit were the following:

1. *R_{DSon} background*

   This stage consists in throughly understanding of what is dynamic on-resistance, how it is defined, and its importance to device development.

2. *Previous R_{DSon} Test Circuits*

   A literary revision of previous work dedicated to obtaining the R_{DSon} value in power MOSFETS. Suitable topologies for R_{DSon} test execution were identified in this step.

3. *Validation*

   R_{DSon} test circuit was validated using experimental data behavior.

5.2.2 Automated Procedure for Data Extraction

Once a circuit topology was chosen, an automated procedure for extraction was developed. Advancing this stage required the following:

1. *Automation of Characterization Tests*

   Characterization tests are specifically designed to extract a particular or several parameters of a DUT. The previous work dedicated to automated characterization was revised.

2. *Previous Work in R_{DSon} Automation*

   The body work committed to R_{DSon} automation was studied: this included the circuit topology, instrumentation and automation considerations.

5.2.3 R_{DSon} Calculation

R_{DSon} test required the extraction of voltage and current curves that provide the information to calculate the R_{DSon} value. Under the typical test conditions, the subsequent steps were taken:

1. *Nature of the Voltage and Current Curves*

   After the curve extraction through the automated setup, understanding the behavior of voltage and current curves provided insight to the expected R_{DSon} curve.

2. *Signal Filtering*

   Any type of measurement will have noise. R_{DSon} is a dynamic value, therefore the rate of change of the transistor turn-on and turn-off can affect the signal and noise present in the data taken. Available filter techniques suitable for the R_{DSon} test condition where investigated and put to use.

3. *Min R_{DSon} Value Extraction*

   Once extraction and filtering take place, the R_{DSon} curve was calculated and then the minimum R_{DSon} value from the curve was taken from it.

5.2.4 Integration

Once a manual solution has been implemented with appropriate instrumentation, the actions to pursue are the integration of the instrumentation through a software environment. For R_{DSon}, LabVIEW was chosen as the platform for integration [32].

Although LabVIEW offers many device drivers in it library, there are always changes that need to be made in order to make the drivers suitable for the test execution. Examples of such changes include minute ones such as, proper timing in oscilloscope driver. Many oscilloscopes in LabVIEW are formatted to use time stamps (Date/Time). This is not required for the R_{DSon} test, hence modifications for the instrument to capture fractions of second are made.

Additionally, some instrument drivers are not suitable for integration at all and must be completely rebuilt in order to be used in unison with other instruments. Another important aspect for integration is signal flow control in the remote execution environment. What would happen if an instrument received instructions and executed them before it is required? In the case of LabVIEW, it offers an ordered execution flow control (Flat Sequence) that does not allow the test to continue to its next step until all the instruction within that step are executed.

More advanced LabVIEW techniques include data flow control, where the instrument will not execute until all the required parameters for an instruction are present. This would require assessing the speed of the signals that send and receive instrument from all instruments. Furthermore, different instrument use different communication protocols that work at different speeds (examples include: Ethernet, GPIB, and USB). It is better to err in the side of caution and have ordered execution flow control, which also in turn reduces time for it take to implement the integration in the software platform.

5.2.5 Data Validation

The automated R_{DSon} test was compared against the expected value taken from the device data sheet. The following was considered:

1. *Experimental Design* There are three main factor that where considered for the experimental design.

- Test Conditions: Defining test conditions assures a constant expected waveform from the R_{DSon} test circuit. There are test conditions that will be address as constants and others as variables.
  - Bias Conditions: Constants
  - Pulse Amplitude: Constant
  - Test Frequency: Constant
  - Load Resistance: Constant
- Load Voltage: Repeatability of test under different load voltages (Variable).
- Stress Test: Performing a sample stress test (i.e repetitions of R_{DSon} test, while measuring every 5 minutes).

2. *Data Analysis* The R_{DSon} value from experimental measurements was compared with the datasheet value from the DUT.

Chapter 6
R_{DSon} Test

This chapter presents the hardware used to extract the voltage and current waveforms (V_{DS} and I_{DS}) necessary to determine the dynamic R_{DSon} value of the power MOSFET. From this standpoint, the concern is to determine the test circuit and instrumentation for curve extraction. The software will be used to process the extracted curves from the test circuit setup to calculate R_{DSon}. A discussion of the hardware selected, its operation, and realization follows.

6.1 R_{DSon} Test Circuit

Figure 6.1 presents the circuit used for dynamic on-resistance extraction. This circuit is a modified version of the circuit proposed by Lu et al. in their paper [25]. The modifications in this circuit include the use of jumpers that highlight available load variations in the clamping setup. Lu's circuit is the simplest solution for the purpose of automation, since its configuration is confirmed to produced feasible R_{Dson} measurements. Q1 and Q2 are representative of the DUT and Clamping transistor, respectively, and L1 is representative of the current probe used to measure Q1 current.

The instrument setup shown in Fig. 6.2 was used to excite the R_{DSon} circuit and execute the test. The biasing voltages: V_{BIAS}, V_{LOAD}, and V_{GATE} were generated by two source-measurement units (SMU's), model Keithley 2612. The V_{BIAS} and V_{GATE} are constant DC voltage used throughout the test circuit. V_{LOAD} refers to the load voltage conected to the drain of both the DUT and clamping transistor. The V_{PULSE} is generated by the LeCroy ArbStudio waveform generator. The strong delivery of

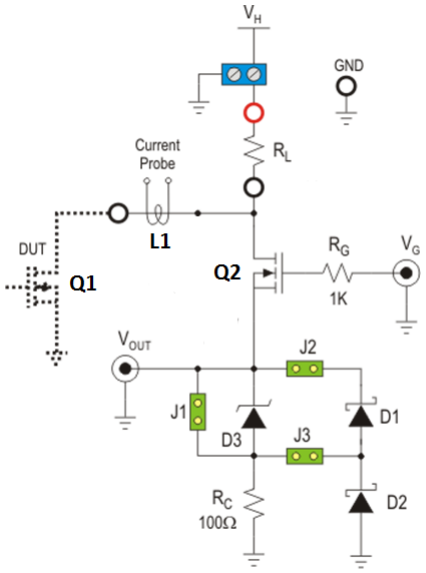


Figure 6.1 : Dynamic R_{DSon} Test Circuit

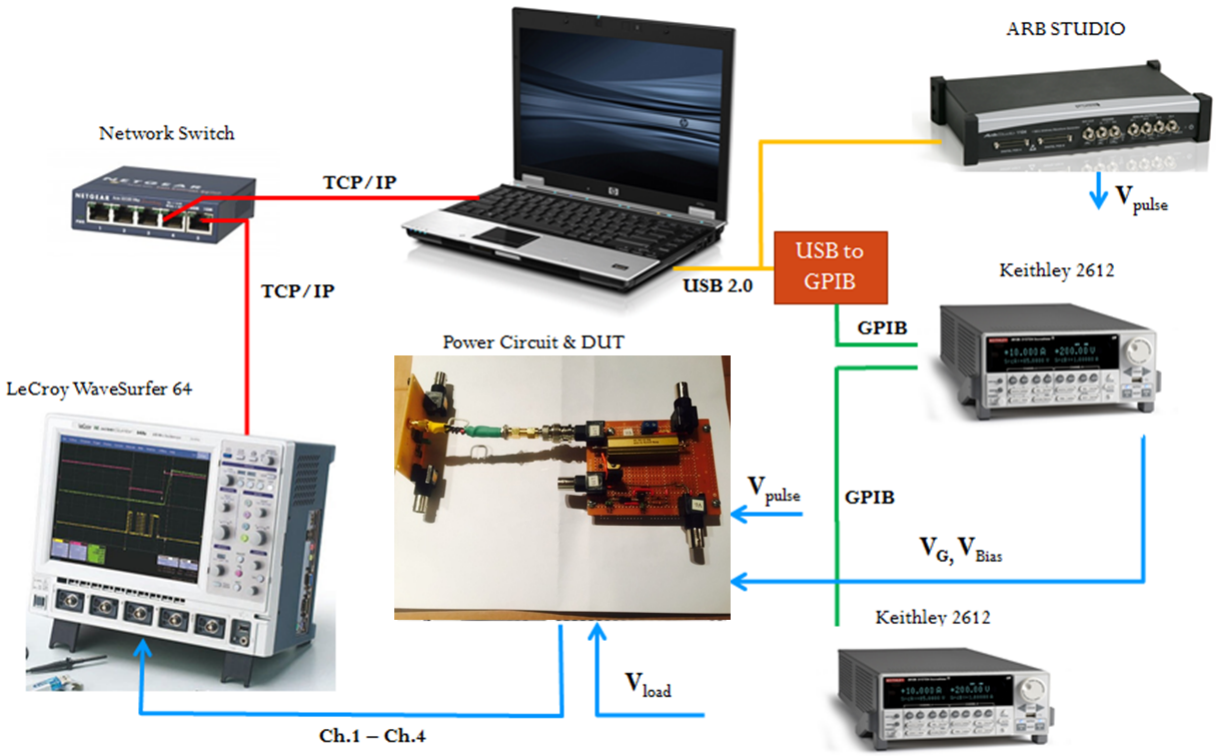


Figure 6.2 : Instrument Setup

the V_{PULSE} is sustained by the driver used between the source of the V_{PULSE} and the gate of the DUT.

6.2 Behavioral Model of R_{DSon} Circuit

Figure 6.3 illustrates an equivalent circuit for the R_{DSon} test setup. Both the clamping transistor and the DUT are treated as resistances. Since the DUT is pulsed on and off, a switch provides that dynamic nature of the circuit.

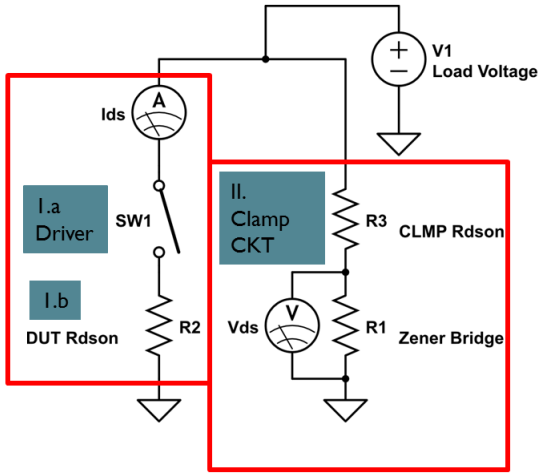


Figure 6.3 : Resistance Model of the Dynamic On-Resistance Circuit

The equivalent element $R1$ is resistance in series with the zener diode, $R2$ is the DUT R_{DSon} and $R3$ is the clamping transistor R_{DSon}. The value of the $R2$ is significantly smaller than that of $R1 + R3$ series combination. The power MOSFET has a sub-ohm resistance, so that the branch with the 100Ω resistor in series with the clamping power MOSFET has a resistance that is several orders of magnitude higher than the DUT itself. Therefore, the $R1 + R3$ combination can be reduced to a 100Ω resistor. When the switch SW1 is closed, current flows through $R2$ and not through the equivalent series resistor of $R1 + R3$. The value of$R1$ was chosen to handle the current that flows through both the DUT transistor and the clamping transistor.

6.3 Curve Extraction

To obtain the dynamic R_{DSon} value of a power MOSFET, the following steps were taken:

i) Extraction of voltage and current waveform from the DUT.

ii) Calculate dynamic R_{DSon} curve of the Power MOSFET.

iii) Obtain the minimum value of the dynamic R_{DSON}.

6.3.1 V_{DS} and I_{DS} Waveforms

From the R_{DSon} circuit, the expected curves for V_{DS} (dashed line) and I_{DS} (bold line) are as shown in Fig. 6.4 :

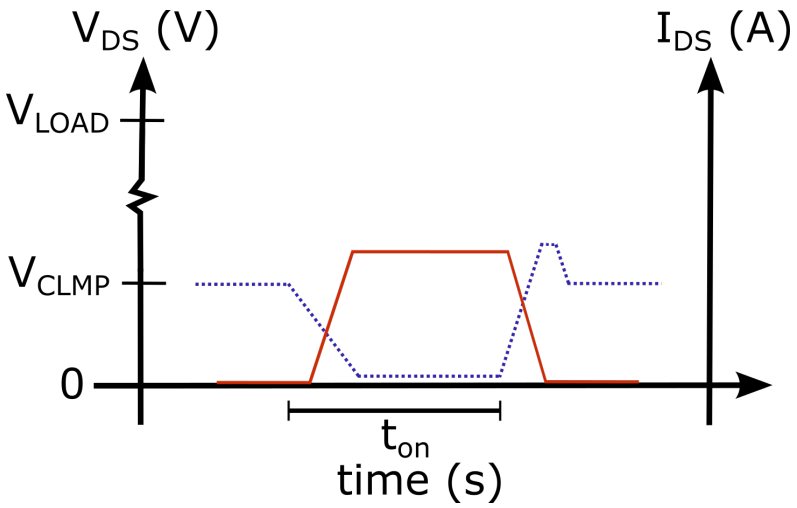


Figure 6.4 : Clamped Voltage and DUT Current Curves

A brief analysis of the behavior of the circuit in Fig. 6.1 illustrates the approximation between the V_{DS} value of the DUT and the curve measurement at the zener diode. The V_{DS} curve begins with the value at the zener diode voltage of 5.1 volts. Once the DUT is turned on and the current flows through the DUT, the V_{DS} value

drops because $R1 + R3 > R2$. Since $R1$ is 100Ω and $R2$ is a sub-ohm value, there is a three orders of magnitude difference in the resistance value. Due to this difference, the current in the clamping transistor branch ideally drops to zero. Therefore setting a current probe directly on the path towards the DUT will provide a direct measurement of the on-state current.

As the DUT is turned on, the behavior of parallel branches indicates that the voltages in both branches will be the voltage across the DUT channel (V_{DS}). From the previous equivalent circuit in Figure 6.3 $R1 + R3$ was reduced to $R1$. Therefore the voltage from the zener diode to ground will reflect the DUT V_{DS}.

As the DUT was turned off, the current flowed through the clamping transistor branch. Since the $R3 < R1$ the largest voltage drop will be present across the zener diode. At this point, the voltage will tend to go to the load voltage, the drop in $R3$ is small so the majority of the load voltage will be seen on the zener diode bridge. At this point the curve tries to reach the load voltage, but it is limited by the intrinsic behavior of the zener diode to 5.1 volts. That is the small peak observed in the V_{DS} curve shown in Fig. 6.4 .

For the I_{DS} curve, the behavior is contrary to V_{DS}. As the channel in the DUT develops, the current flow increases. At the initial point in time when this happens, the capacitance of the power MOSFET is charged. Recall that a capacitance resists instantaneous changes in voltage, so a steep current increase is expected. Afterwards the value settled down to its nominal value given the voltage and load values.

6.3.2 R_{DSon} Curve

Since the dynamic on-resistance is given by the following equation:

$$R_{DSon} = \frac{V_{DS}}{I_D} \tag{6.1}$$

An inspection of the behavioral voltage and current waveforms gives an idea of the expected on-resistance curve by inspection of equation 6.1. The R_{DSon} curve is broken into four sections:

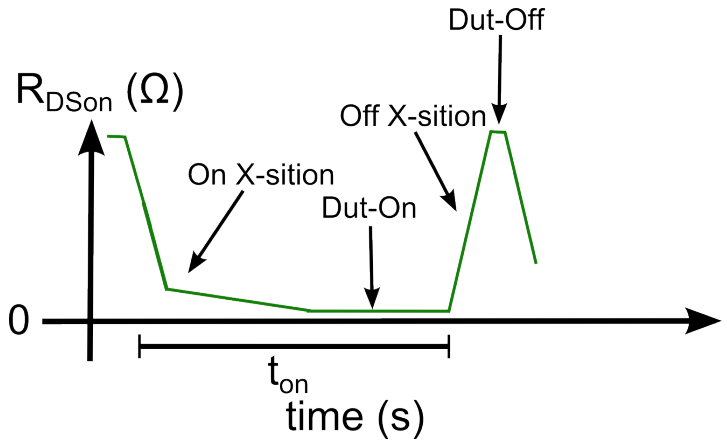


Figure 6.5 : Dynamic On-Resistance Curve

1. DUT-Off Section
2. On-Transition Section
3. DUT-On Section
4. Off-Transistion Section

DUT-Off Section

This section of the R_{DSon} curve has two main conditions: the voltage was clamped at the zener voltage (5.1 Volts) and the current through the DUT was 0 A. (DUT-OFF).

On-Transition Section

At the device turned on, the current going through the DUT increased and the voltage decreased to a minimum. Inspecting this behavior in the R_{DSon} equation, results in a decreasing behavior.

DUT-On Section

Once the DUT is fully on, a fixed current value and a minimal voltage indicated reaching a straight line behavior while the DUT remains on.

Off-Transition Section

Opposite to the On-Transition section, here the current decreases and the voltage increased back to the clamping value.(5.1 Volts). Therefore an increasing behavior should be observed in the R_{DSon} graph. Since the current decreases significantly a steep increase should be observed in the curve.

6.4 Rdson Circuit Implementation

A behavioral discussion of the viability of the proposed circuit was presented in section 6.2. A secondary yet very important aspect of the circuit will be addressed, how to ensure delivery of the pulse signal to the circuit so that it arrives as clean as possible? This is done by using a driver. A driver will require an additional bias. This introduces one final component to the final circuit schematic.

6.4.1 Rdson Final Schematic

Fig. 6.6 show the addition of the driver circuit for the V_{Pulse} delivery. The driver chosen for the task is the LM5101 High/Side Low Side driver. Beside the bias some additional components are required to ensure driver behavior. From a behavioral aspect, nothing changes in the R_{DSon} Circuit.

6.4.2 Components List

A list of major components (devices and IC's) is presented with reasons for their selection.

- DUT Transistor: Infineon C6 CoolMOS Transistor (3) A 600V power MOSFET was chosen as a DUT. A commercial available device well suited for the test.

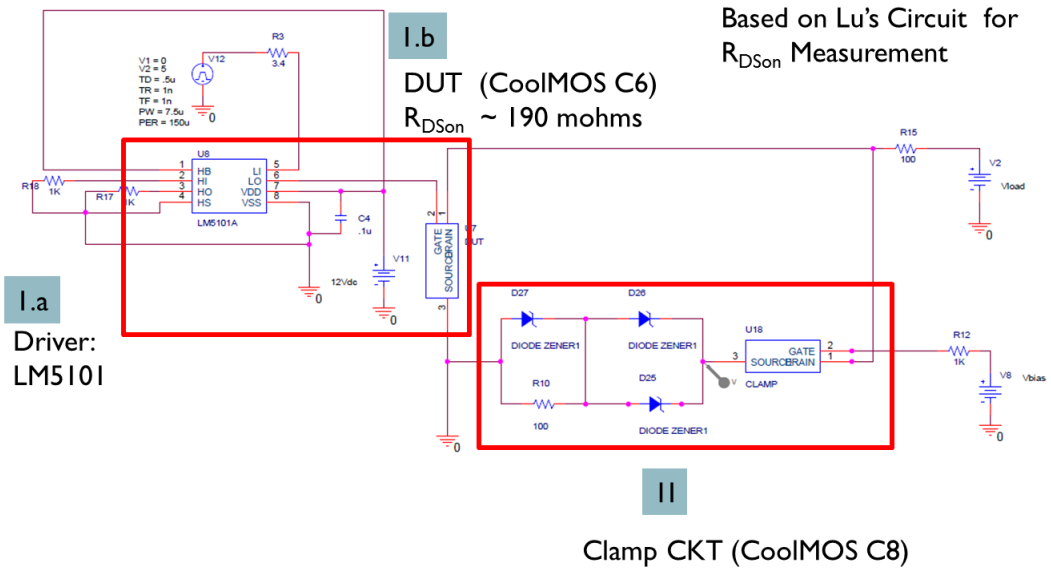


Figure 6.6 : Rdson Test Schematic

- Clamping Transistor: Infineon SPA02N80C3 CoolMOS Transistor (1)A 800V power MOSFET was chosen as a clamping transistor. By definition, as with all test and characterization equipment, the clamping transistor should sustain breakdown voltages than the DUT itself.
- DRIVER:Texas Instruments LM5101 High/Low Side Driver
- High Dissipation Resistor for the Load Current
- Zener Diode 1N4733: 5.1V Zener Diode

6.4.3 Physical Realization of the Circuit

The following images show the realized circuit for the R_{DSon} Test.

Fig. 6.7 Shows the circuit component soldered unto a breadboard for use. The smaller board holds the DUT side of the circuit (Driver and DUT). The larger board hosts the clamping circuit and the high dissipation resistor that sets the load current. All connections to instruments are done through BNC terminals. Finally, the third element is a cable built for measuring the current. It allows the current probe access to the conductor wire. Fig. 6.8 shows the circuit fully realized and connected.

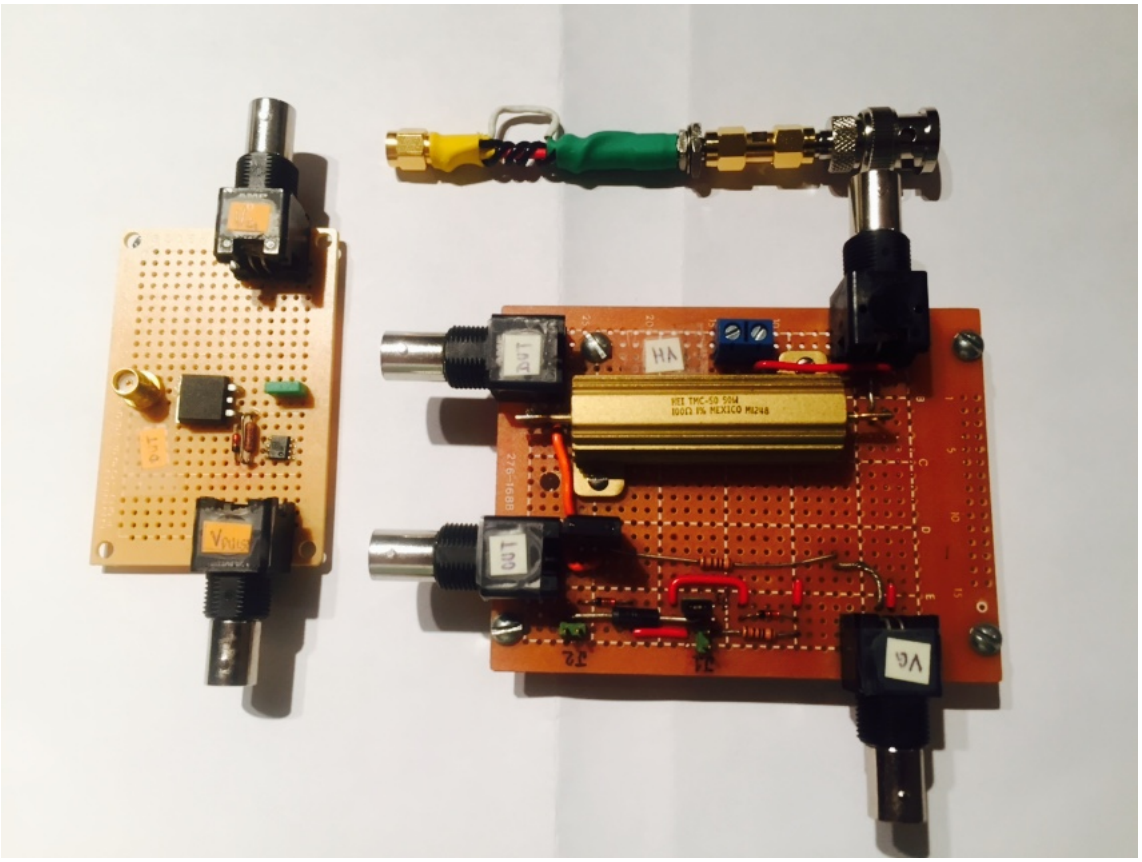


Figure 6.7 : Circuit Components

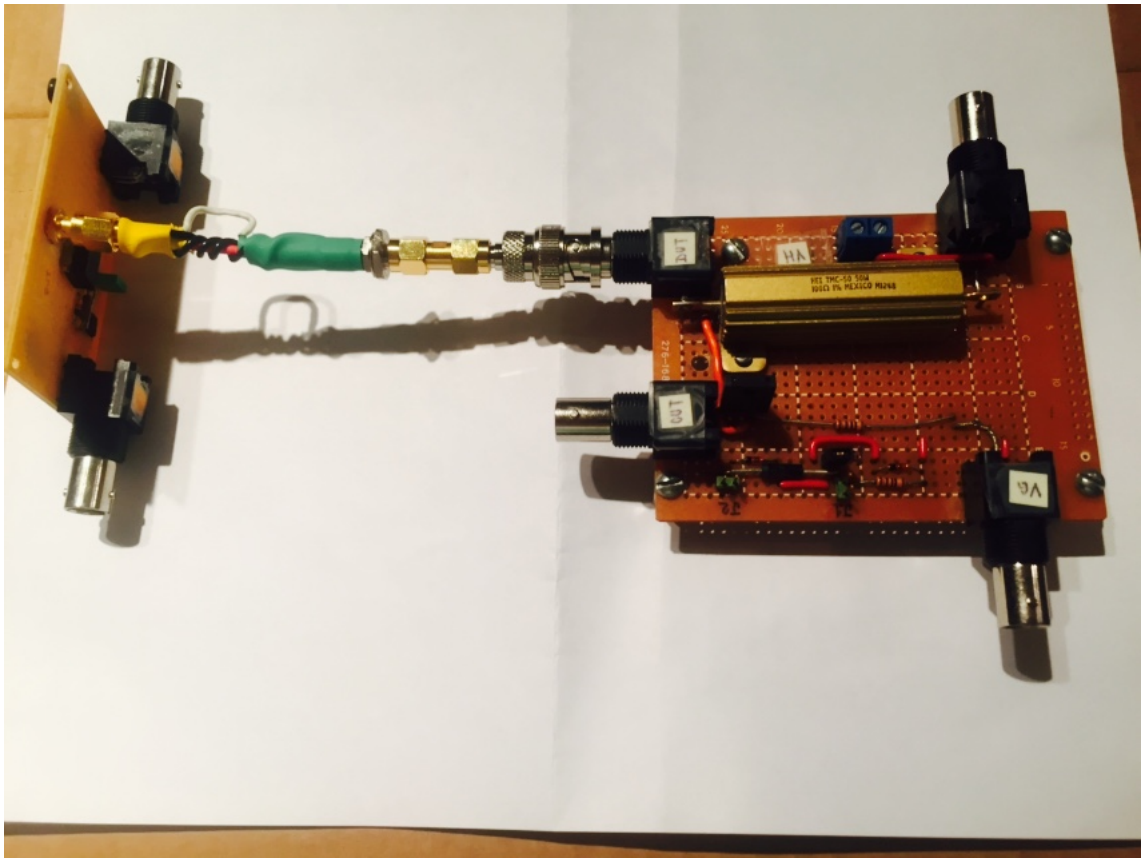


Figure 6.8 : Circuit Realization

Chapter 7
Automation and Experimental Setup

The automated R_{DSon} process was implemented using LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench) software. All measurements were executed with minimal human intervention. The setup for automation and the software design are presented in this chapter.

7.1 Experimental Setup Implementation

7.1.1 Equipment

Keithley 2612

The Keithley 2612 is a source meter unit (SMU). Every 2612 SMU has two channels. Each SMU channel can provide a voltage and limit the current through each available channel. These channels can be configured and used separately. The Keithley SMU's were used to provide biasing conditions for the test circuit and the load voltage for the R_{DSon} test. The communication to the Keithley SMU was performed via the GPIB protocol in LabVIEW. Specifically, the Keithley 2612SMU delivers the following bias conditions:

- DUT Gate Signal Driver Bias
- Clamping Transistor Gate Signal
- Circuit Load Voltage

Lecroy Wave-Surfer 64Xs Oscilloscope

The Lecroy Wave-Surfer Oscilloscope was used to capture the data generated through the R_{DSon} test framework. This instrument does not connect via GPIB

protocol like the rest of the instruments used in the setup but via an ethernet network. The ethernet provides faster connectivity than GPIB which is important for the data collection. In order to use the Oscilloscope, LeCroy has an ethernet protocol specifically designed for LabVIEW, the VICP-Passport. This allows LabVIEW to initialize the communication with the device using an IP address. Afterwards, it sends the instructions to the device like any LabVIEW connected device, using VISA and SCPI protocols.

LeCroy Current Probe

In order to measure I_{DS} a current probe is required. The model used for this purpose is the $CP0030$. It can sustain 30A maximum current. The coupling command for current probes are different than those used for voltage probes. These coupling had to be incorporated into the DSO driver.

PC

The personal computer (PC) was used to run the automated test software. It provides the interface necessary for communication to take place between the devices. The PC used a GPIB-USB adapter in order to communicate with the SMU and the pulse generator. The ethernet port comes already integrated into the PC to communicate to the oscilloscope.

LeCroy ArbStudio 1102 Waveform Generator

The ArbStudio 1102 Waveform Generator administered the gate signal that drives the DUT. This is the most critical signal of test, it causes the change of current flow between the DUT and the clamping transistor. Without this instrument, the procedure for measuring R_{DSon} cannot be executed.

DUT

The test setup was designed for packaged power MOSFETS. The device under test (DUT) is a three terminal device. The biasing conditions for the DUT can be configured using the automation software.

7.1.2 Test Architecture

The test architecture consists of the following three main sections:

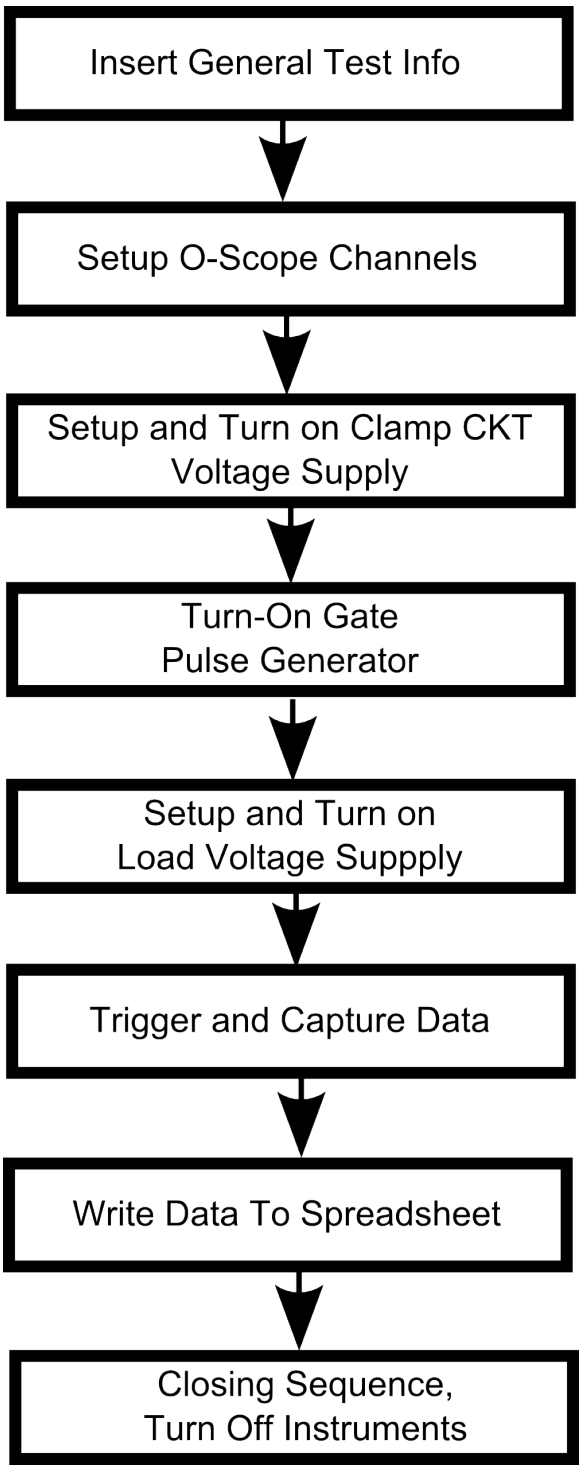
- Curve Extraction
- R_{DSon} Calculation
- Single Measurement/ Stress Test

Curve Extraction

Without a mechanism for curve extraction, there are no effective means to calculate the R_{DSon} value of a power MOSFET. Wasting memory and time capturing the whole signal is not desired due to the duty cycle of 10%. Therefore a software trigger that acknowledges the transition of the curve from an on-state to an off-state was implemented. This allows the 10% to be captured and the 90% of the time that it remains in the off state to be discarded. Since the voltage is known to fluctuate between the zener voltage and the minimum channel voltage, a trigger was implemented to capture when a falling transition takes place in this waveform. This section discusses the results of the curve extraction mechanism; the integration of the circuit setup, instrumentation and software to execute the measurement of the drain to source voltage and current of the DUT.

Figure 7.1 presents the test flow for curve extraction. The first item is a general information setup, any necessary ID information about the test: the user, time, frequency, load resistance, ect. The next four items indicate the sequence of event leading up to the DUT capture. The first instrument configured is the oscilloscope. A minimum of two channels in the oscilloscope are used in the R_{DSon} test (one for

Figure 7.1 : Linear Architecture for Curve Extraction



drain voltage and one for drain current). For the oscilloscope, the time window per division must be set, and individual channel ranges must be set as well.

This required more time than turning on and setting up the source measurement units. After setting up the oscilloscope, the SMU channels dedicated to ensuring the clamping transistor functionality are configured. Finally, the units allocated for the pulse and load voltages were activated. At this point, the conditions for extraction were met. The DUT is being pulsed on and off, the load voltage is present on both the DUT and clamping transistor and, the current is swinging with the turn-on and turn-off of the DUT.

R_{DSon} Calculation

After acquisition, the R_{DSon} value was calculated. This section is described by the following steps:

1. Curve Filtering (V_{DS} and I_{DS})
2. Single Measurement/Multiple Measurements for R_{DSon}
3. Extract R_{DSon} value from curve

Curve Filtering Further discussion from the data in the following chapter will elaborate more on the point being presented here. In the R_{DSon} test, there are two waveforms of primary concern, the voltage waveform and the current waveform. Naturally, both waveforms exhibit random noise when measured. The question is how much and how does it affect the calculation of R_{DSon}.

Of main concern is the I_{DS} waveform. The LeCroy current probe (model CP0030) used in the setup has a minimum sensitivity of 20mA/div and noise floor of +/- 2mA which cannot be controlled. This puts a lower limit on the current that can be established through the DUT during testing. This brings need for filtering the waveform. This ensures that a smoother waveform is used when calculating R_{DSon}. LabVIEW offers a variety of filters to use for such needs. Some examples include:

- Low Pass Filter

- Moving Average
- Smoothing Filter

For the purpose of the test module implemented in LabVIEW, a Savitsky-Golay (SG) smoothing filter function was choosen. SG filters work by creating a polynomial fitting of data. This averages a single point of data with the same amount of data points before and after [33]. The important paramters of the SG filter are the polynomial order and the number of side data points (same amount, either left or right). One important aspect of the SG filter is that from a frequency standpoint, the filter has low pass behavior [34]. LabVIEW can generate a simulated signal with noise under the same condition of the pulse signal from the Arb Studio. Thus the filtering conditions chosen for the R_{DSon} test were: a 15th order polynomial with 7 side points. If the polynomial order is choosen to large, then fluctuations in the waveform could be averaged out. If the polynomial order is to small, then smoothing will not take place and noise is not remove from the waveform.

Single Measurement/Stress Test A Single Measurement of R_{DSon} requires that the linear architecture in Fig. 7.1 be executed once and then post processing can take place. Besides capturing a single set of voltage and current waveforms from the device, observing the transistor behavior when subjected to a long period of excitation is important. This is the premise of the R_{DSon} Stress Test (Multiple Measurements). The data collected in this stage could answer the following sample questions:

- Does the device sustain its expected behavior over a determined time frame?
- When does it being to degrade?
- How does the degrading behavior happen?

To perform the stress test, the Single Pulse Data Capture Time, Delays, Total Stress Time, and the Sampling Interval are key parameters of the test design. The total

amount of data to capture can be estimated as:

$$DataSets = \frac{TotalStressTime}{SamplingInterval} \tag{7.1}$$

For the extent of this work, fixed stress test conditons of 10 mins with measurement every 1 minute were chosen. The fact that the test condition includes a pulse frequency of 10KHz means that the DUT was pulsed during the 10 minutes a total of $10,000Hz$ * $10minutes$ * 60 sec/min = $6,000,000$ times. Out of those six million pulses, only 10 will be captured for observation and processing.

The sampling interval must be larger than the single pulse data capture time, so a delay(ms) must be inserted to adjust the capture. This delay is due to the execution time of capturing and processing the V_{DS} and I_{DS} waveforms. Obviously, for a single pulse it doesn't matter since it is one data capture only.

$$Delay = SamplingInterval - PulseCaptureTime \tag{7.2}$$

This delay allows for the system to correctly index the amount of data to be captured and stopping after completing the collection of data. Futhermore, LabVIEW already has a function for keeping elapsed time while executing the loop at the indicated time. Refer to Fig. A.5 in appendix B to see how the function was implemented in LabVIEW.

7.1.3 Calculate R_{DSon}

This calculation is a software processed solution. For the purpose of the experimental setup, the key item regarding the calculation of R_{DSon} is that the sampling time during stress test is not less than the time it takes for a waveform to be captured and processed. As defined in the previous paragraph, the stress test with 1 minute sampling time can be executed within execution time of the stress test. This will be discussed further in Ch. 8.

7.2 LabVIEW Code

After the setup of main idea regarding the test and instrumentation, the design and implementation was realized in LabVIEW. The code in LabVIEW is divided into five (5) main modules:

- Initialize and Configuration
- Single/Stress Test Implementation
- Data Capture
- Data Processing
- Closure

The following figures feature the critical sections of the modules in the order presented.

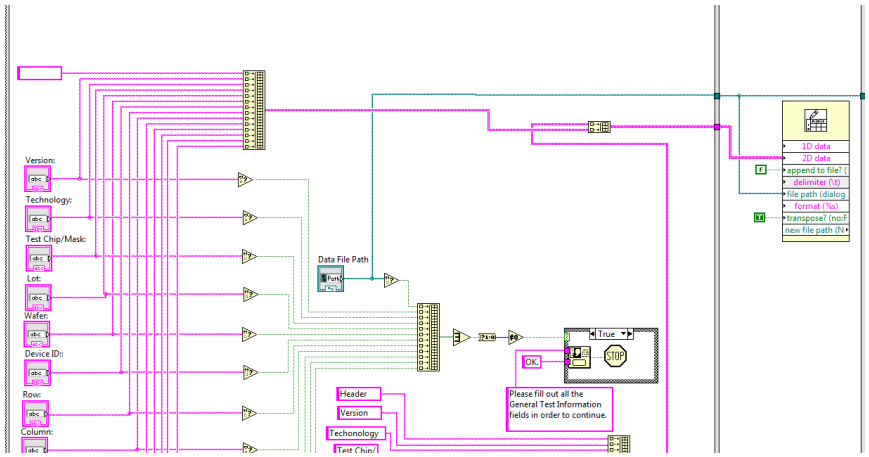


Figure 7.2 : Initialize and Configure

Fig. 7.2 shows how fields where the user can setup up and save test and device information.

Here the elapsed time module is being implemented for stress test execution in Fig. 7.3 . The total time of test is divided by the sample time to obtain the number of measurements to be taken. This is compared to the index of the while loop that controls the stress test execution.

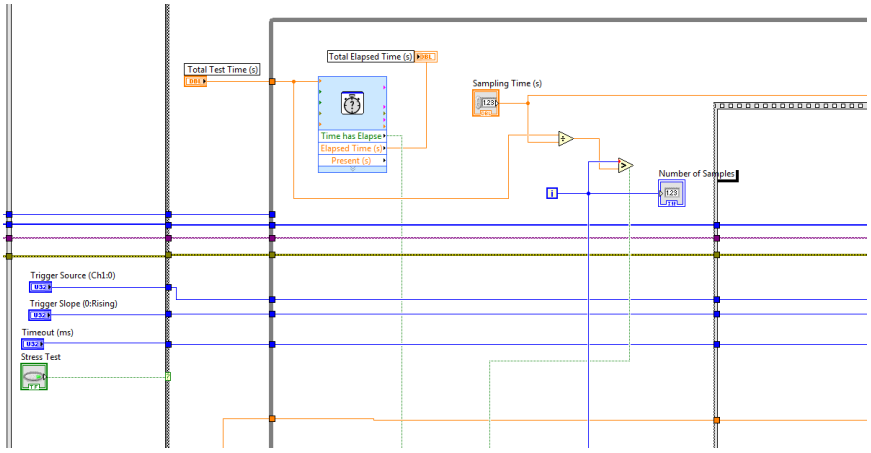


Figure 7.3 : Stress Test Implementation

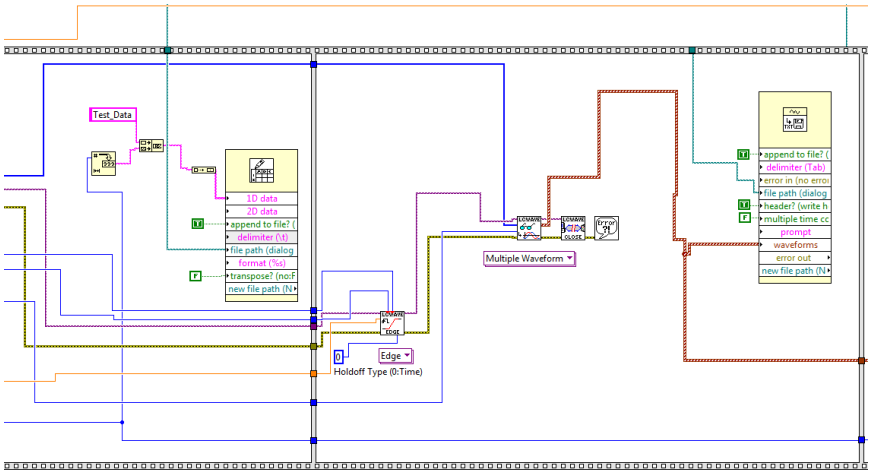


Figure 7.4 : Data Capture in LabVIEW

In Fig. 7.4 , after the data is retrieved from the LeCroy DSO VI, the data is stored in the spreadsheet. This brought up an important limitation in data storage. Excel files have maximum of $2^{20}(1,048,576)$ rows to store data. In the R_{DSon} test, data capture was fixed at $10,000$ sample points per curve measurement. This gives us approximately 100 sampling intervals available at 10,000 points per curve.

Another important detail in testing is the aspect of coherence in sampling data. From a graphical perspective coherence can be described in the following manner: do the transitions (peak, inflections,ect.) present in the sampled data occur at the same time interval within the sampling window. If so, the data is coherent. For R_{DSon},

already there are known factors: the pulse duty cycle time at $10\mu s$ and that the number of samples per waveform is 10,000 and the input frequency is $10KHz$ and there is one capture per single pulse waveform. There is a mathematical relationship between the input frequency, sampling frequency, the number of sampling cycles and the number of points per sample that analytically describe coherence. The following equations presents it:

$$\frac{f_{in}}{f_s} = \frac{N_{window}}{N_{record}} \tag{7.3}$$

Where f_{in} is the input frequency, f_s the sampling frequency, N_{window} is the number of sampling cycles and N_{record} is the number of points per waveform capture. For the R_{DSon} test, this results in a minimum sampling frequency of 1 MHz for data to be coherent. As such this sampling setting was established in the oscilloscope (Le Croy 64Xs) used during testing.

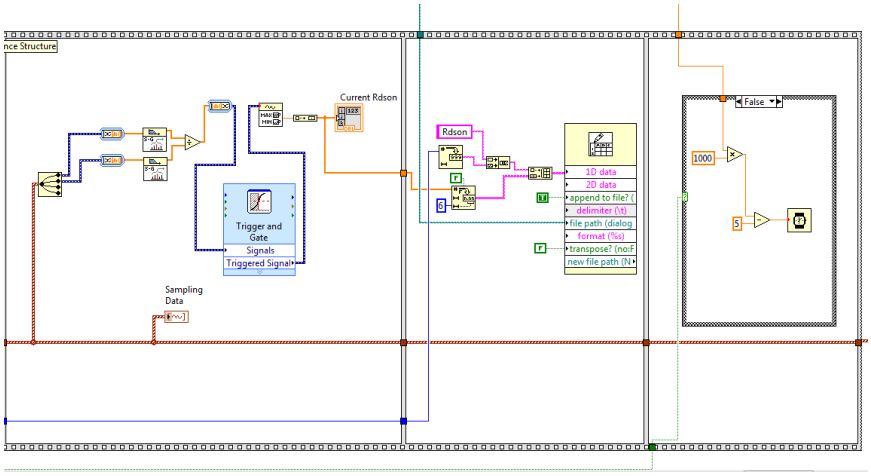


Figure 7.5 : Processing Data in LabVIEW

Fig. 7.5 exhibits the implementation of the SG filter in LabView and subsequent calculation of the R_{DSon} value. The dynamic data type data of the waveform is splited into the individual channels. The channels that correspond to the voltage and current waveforms are then processed through the SG filter. Afterwards, the R_{DSon} curve is

passed through the *Trigger and Gate* VI. This VI allows the user to filter data sets into a known range. In the case of R_{DSon}, the interest is in values that are between 0 and 1 (subohmic, non negative values).

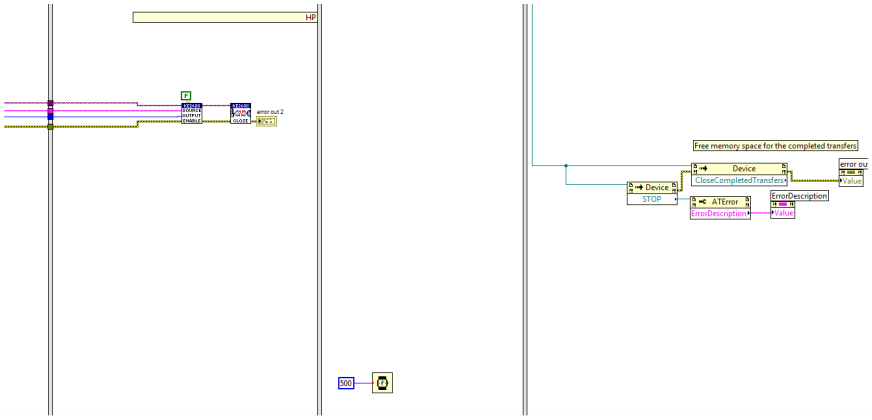


Figure 7.6 : Closing Execution LabVIEW

Finally after test execution, communication with instruments is terminated and the VI execution is finalized. Additional figures of code implementation are presented in Appendix A.

Chapter 8
R_{DSon} Extraction, Validation, and Data Analysis

This chapter discusses the procedure implemented for the R_{DSon} test while validating the extracted data from the automated setup.

8.1 R_{DSon} Curve Extraction

Figure 8.1 : LabVIEW Front Panel Setup

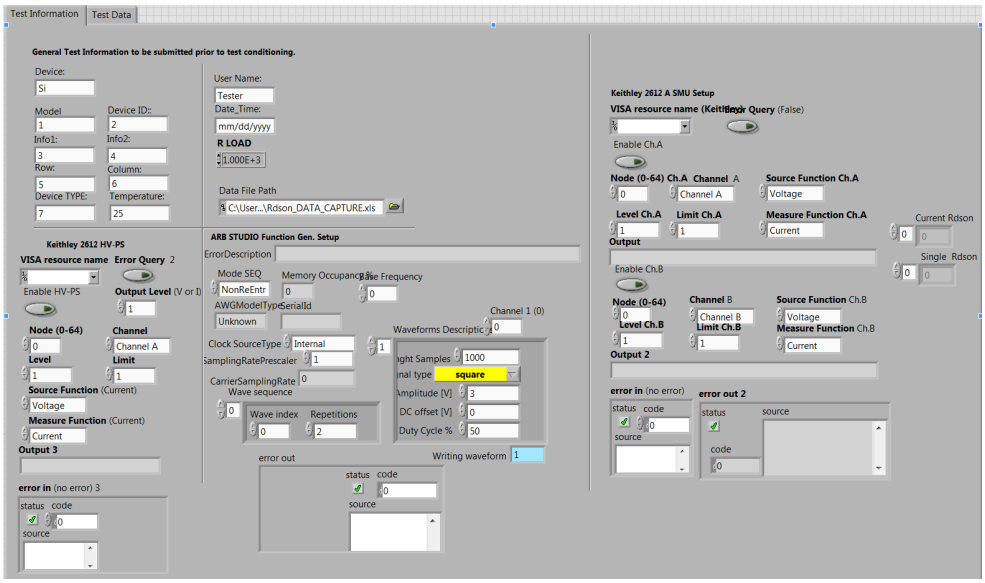


Figure 8.1 shows the execution of the test architecture in LabVIEW. Across the panel, test info, saving capabilities, SMU and pulse generator configurations are displayed. For the saving to take place, the user must create a blank spreadsheet file in the desired location. All the general test information is stored in the indicated spreadsheet file.

Figure 8.2 : LabVIEW Oscilloscope VI

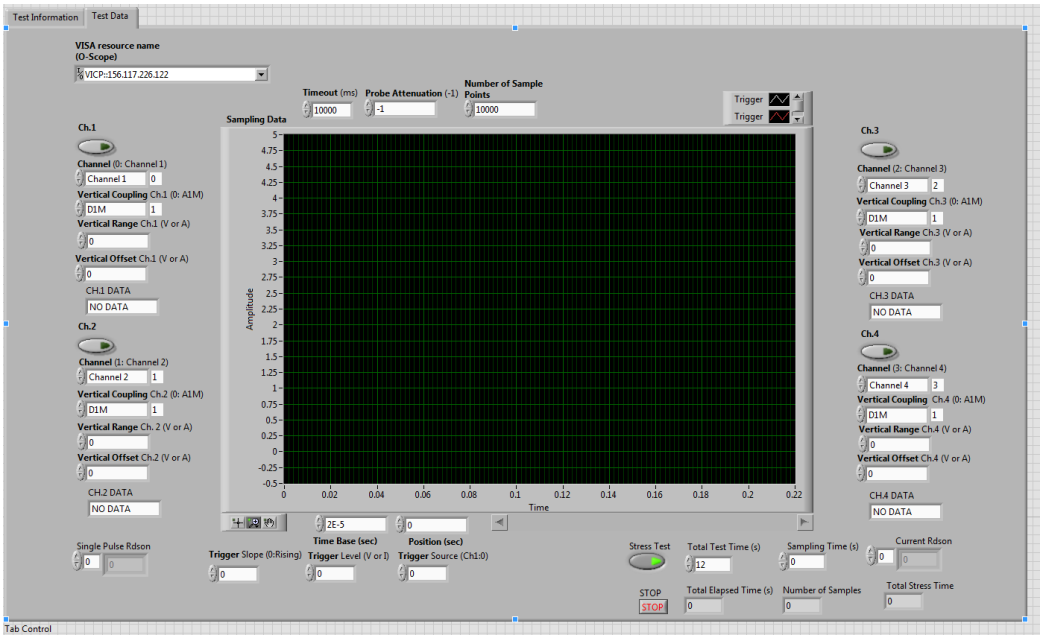


Figure 8.2 show the part of the VI developed for oscilloscope. The user configures the oscilloscope according to the parameters used in the test.

8.1.1 R_{DSon} Curve Extraction

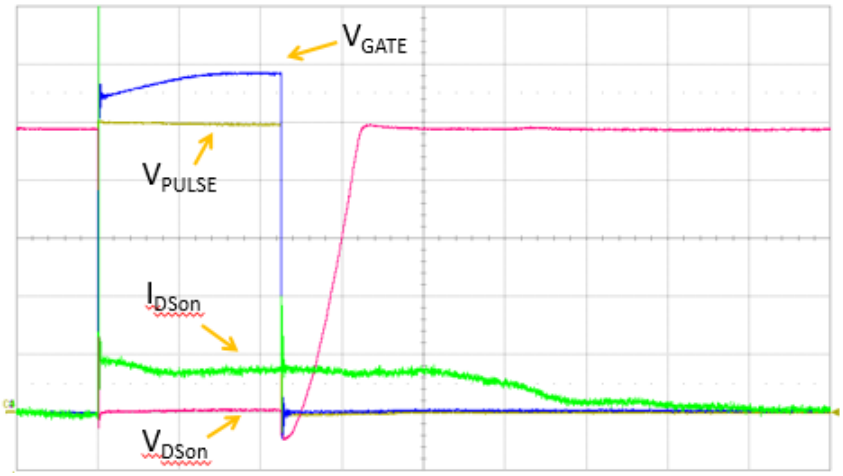


Figure 8.3 : Sample Oscilloscope Capture

Figures 8.3 and 8.4 illustrates a sample capture of the R_{DSon} test curves. Figure 8.3 displays the oscilloscope capture and Fig. 8.4 shows the same capture

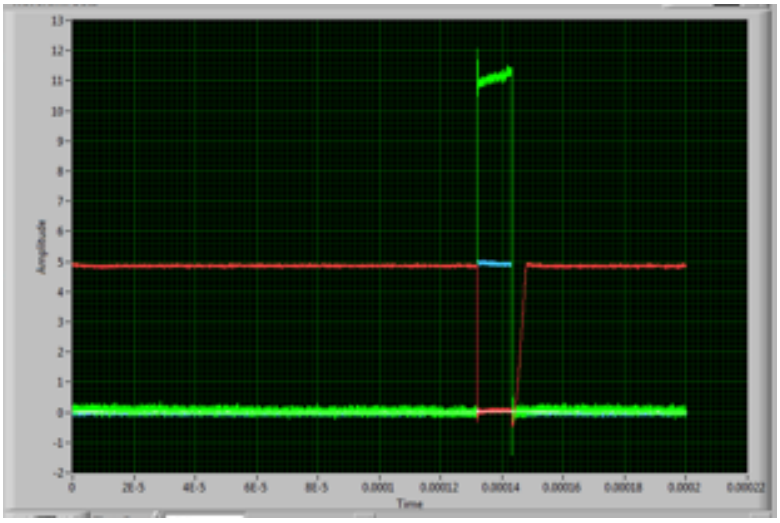


Figure 8.4 : Virtual Oscilloscope Capture

in the virtual instrument developed in LabVIEW. The signals present in the capture are the following:

- Clamped V_{DS} Curve
- Gate Pulse Signal
- I_{DS} Curve

The clamped drain voltage followed what was discussed previously in Ch. 6. Briefly, once the DUT was turned on, the clamp voltage drops to a minimal value. Afterwards, the DUT is turned off and the drain voltage tried to go back the load voltage value. Instead, it was limited by the zener diode bridge of 5.1 volts. This last part was exhibited in the small peak observed in the curve of the red signal.

Furthermore, the current signal (denoted by its green color), displayed its anticipated behavior. As the DUT was energized (gate signal delivered), the current flowed through the device and its measured using the current probe. After the DUT is de-energized, the current comes back down to zero (no channel is present from drain to source).

Additionally, the pulse was completely captured within the window of both the physical oscilloscope and the virtual one. Note that only a segment previous to the

pulse and a segment after the pulse was taken. Capturing only this section of the whole waveform allows memory and processing to be strictly dedicated to the interval of interest of the signal. It reduces time wasted to search for the instance of the pulse. The data was used to calculate the R_{DSon} value of the DUT.

8.2 R_{DSon} Calculation and Validation

8.2.1 Biasing Conditions

The biasing conditions of the test are those that were discussed previously in chapter 7, namely, the pulse, gate, and load voltages.

- V_{pulse}: 10KHz, 10% Duty Cycle, 9V Amplitude
- V_{GATE}: DC Signal 9V
- Load Voltage

8.2.2 Experimental Design

There are two main tests executions to be addressed: single pulse measurement and stress test pulse measurement.

For the single pulse measurement, the following conditions are used:

- Three DUT for testing of same device
- Three Load Voltages: 50, 75, 100
- Ten repetitions per DUT and Condition

For the stress test the DUT used will be the same as those in the single pulse test. The stress test parameters are:

- 10 minutes of stress time
- Capture a data set every 60 seconds
- Repeat 5 times

8.3 R_{DSon} Validation: Single Pulse Measurements

Under the previously mentioned test conditions and experimental design a discussion of the results obtained follows.

First of all, a sample waveform taken from DUT 1 to show the data that is being captured from the system. Fig. 8.5 is data taken from a DUT with V_{Load} at 50 volts. Note the current (blue line) is constant at around 500 mA while the DUT reaches the lowest value in the voltage curve. Then note the clamping behavior, how it peaks and the signal returns down to the clamping voltage of the zener diode. The figures following Fig. 8.5 , 8.6 , 8.7 show the captured waveform from the different load voltages, 75V and 100V.

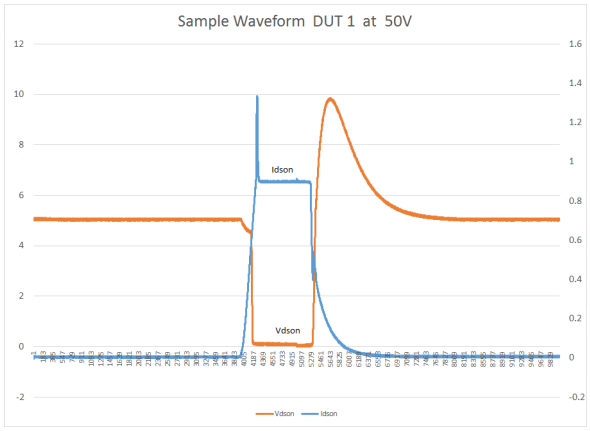


Figure 8.5 : Example of Extracted Waveforms from DUT 1 at 50 Volts

There are two items to observe in the clamping waveform. First, there is the on-transistor bump present in all three curves. Since this occurs in the transition state, a forceful transition may be causing a jerk in the signal that can be observed. It also increases as the magnitude of the load voltage (V_{Load}) increases. Another aspect to observe is the overshoot of the clamping voltage. It goes up to under 10 volts when $V_{Load} = 50$ volts and to a little over 12 volts when $V_{Load} = 100$ volts. Nevertheless, this overshoot or the jerk do not affect the curve in significant manner that might slow down the capture of the V_{DS} and I_{DS} waveforms.

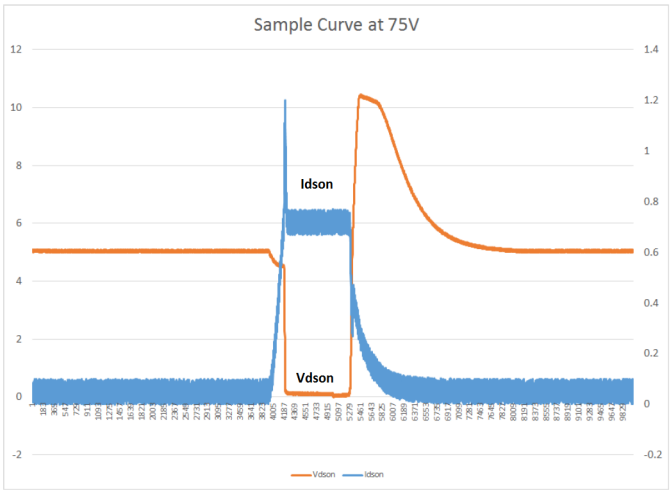


Figure 8.6 : Example of Extracted Waveforms from DUT 1 at 75 Volts

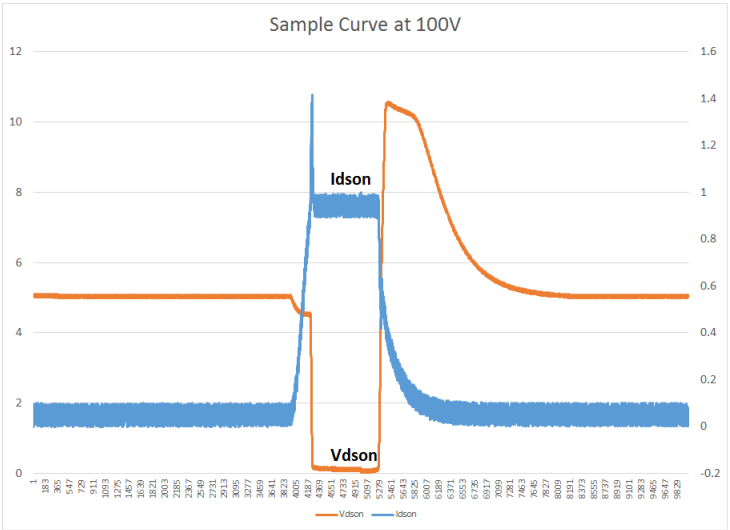


Figure 8.7 : Example of Extracted Waveforms from DUT 1 at 100 Volts

An important standard for switching test is the time for pulse arrival. This refers to time time it takes from fully-off to fully-on once the gate pulse is applied to the DUT. A specific value was not a goal of this work, minimally the pulse arrival should be in the sub-micron time range. The time observed was from 10% to 90% of the on-transition. This measurement was extracted from the current waveform as the transistor becomes conductive. From the sample data curves for 50, 75 and 100 volts the on time was approximately 30 ns.

A general note regarding the data tables with R_{DSon}, current and power data to be presented in the following subsections; the − indicator represents a device under test that was damaged under testing.

8.3.1 R_{DSon} Value

Table 8.1 : Dynamic On-Resistance Value of DUT 1 (Ohms)

	DUT #1		
TEST NUMBER	50V	75V	100V
1	1.931E-01	1.661E-01	1.840E-01
1	2.321E-01	1.523E-01	1.660E-01
3	2.109E-01	1.505E-01	1.316E-01
4	2.025E-01	1.488E-01	1.297E-01
5	1.970E-01	1.473E-01	1.871E-01
6	1.925E-01	1.459E-01	1.279E-01
7	1.885E-01	1.446E-01	1.531E-01
8	1.849E-01	1.434E-01	1.421E-01
9	1.817E-01	1.422E-01	1.844E-01
10	1.787E-01	1.412E-01	1.998E-01
AVG	2.08E-01	1.47E-01	1.621E-01

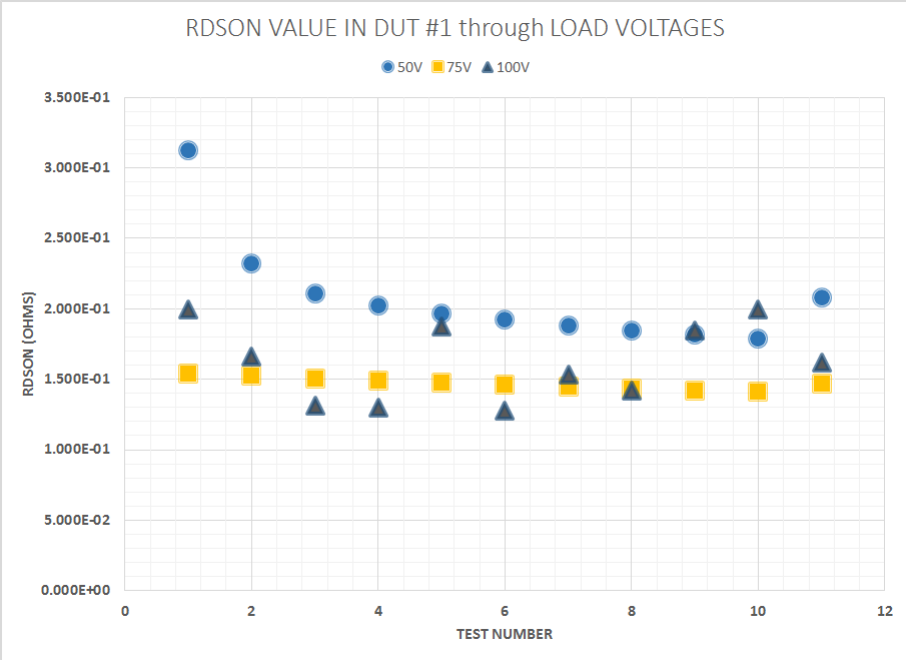


Figure 8.8 : DUT 1 Dynamic On-Resistance

Table 8.1 and Fig. 8.8 shows the extracted R_{DSon} values from the first tested DUT in the system in single pulse measurements. The R_{DSon} value is obtained by filtering the curves and extracting the minimum, greater than 0 value. See A for the code implemented to achieve this.

Note the general subohmic behavior encountered in across all load voltage used for DUT 1. Furthermore in Fig. 8.8 a general decreasing trend can be observed across the load voltage, although at 100 volts the decreasing behavior is observed when compared to the other load voltage conditions. After test number 4, the value increased in comparison to the general decreasing, the same behavior is observed later on in the test.

Table 8.1 shows that the value for R_{DSon} is at near the 200 mohm range. For the 50 V case, the DUT averages a with an R_{DSon} value of .200 ohms. As the load voltage increases, the dynamic on resistance is shown to decrease at 25% as the load voltage increase from 50 to 75 volts. From 75 to 100 volts the change in decreasing R_{DSon} is an additional 12% (.141/.167).

Under the same conditions, observations are noted for the second DUT used for validation. Note the general decreasing trend as well, but anomalies show up along the 50 volt due to the amount of current being carried during testing. Additionally, the DUT 2 ended up failing in its final single pulse measurement run. Possibilities for failure include self heating induced through testing. Compared to DUT 1, DUT 2 exhibits a slightly higher R_{DSon}. Having too low of an R_{DSon} value may indicate that the device is damaged (e.g. shorted out).

Finally, even though DUT 3 died out during the last series of testing at 100 volts, there is enough data to compare behavior from DUT 3. Note that DUT 3 exhibited the highest R_{DSon} value of all three DUT's on average but still the values fall in the subohmic range.

Table 8.2 : Dynamic On-Resistance Value of DUT 2(Ohms)

	DUT #2		
TEST NUMBER	50V	75V	100V
1	3.124E-01	1.543E-01	1.998E-01
1	1.983E-01	1.612E-01	7.874E-02
3	1.902E-01	1.615E-01	1.051E-01
4	1.908E-01	1.513E-01	3.430E-02
5	1.830E-01	1.534E-01	1.089E-01
6	3.175E-01	1.461E-01	2.971E-02
7	2.383E-01	1.494E-01	7.995E-02
8	2.198E-01	1.573E-01	1.283E-01
9	2.043E-01	1.521E-01	1.119E-01
10	2.003E-01	1.551E-01	-
AVG	2.136E-01	1.553E-01	8.609E-02

Table 8.3 : Dynamic On-Resistance Value of DUT 3(Ohms)

	DUT #3		
TEST NUMBER	50V	75V	100V
1	5.174E-01	1.914E-01	2.347E-01
1	4.325E-01	1.785E-01	1.971E-01
3	2.880E-01	2.173E-01	1.874E-01
4	2.570E-01	1.751E-01	1.699E-01
5	3.907E-01	1.608E-01	2.364E-01
6	3.697E-01	2.053E-01	1.594E-01
7	3.557E-01	2.125E-01	1.616E-01
8	2.464E-01	1.864E-01	-
9	3.641E-01	2.094E-01	-
10	2.780E-01	1.949E-01	-
AVG	3.500E-01	1.931E-01	1.924E-01

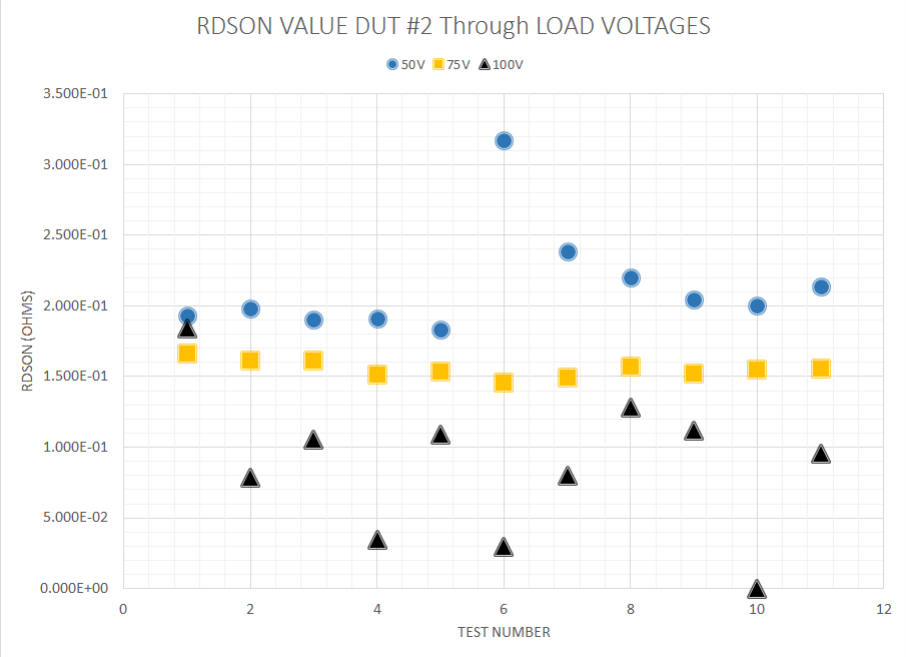


Figure 8.9 : DUT 2 Dynamic On-Resistance

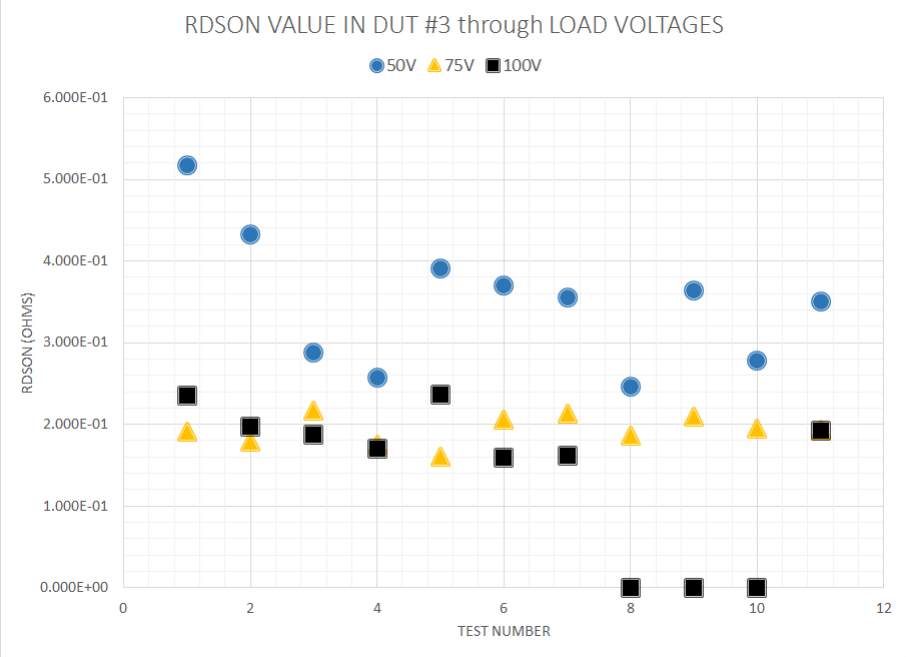


Figure 8.10 : DUT 3 Dynamic On-Resistance

Now a discussion of current and power dissipation across the DUTs during single pulse testing follows.

8.3.2 I_{DSon} Value

Table 8.4 : MAX Current at DUT 1(Amps)

	DUT #1		
TEST NUMBER	50V	75V	100V
1	4.486E-01	7.909E-01	9.624E-01
1	4.466E-01	7.776E-01	1.000E+00
3	4.541E-01	7.657E-01	9.377E-01
4	4.485E-01	7.552E-01	1.065E+00
5	4.534E-01	7.458E-01	9.206E-01
6	4.555E-01	7.374E-01	1.011E+00
7	4.504E-01	7.299E-01	1.056E+00
8	4.522E-01	7.233E-01	9.762E-01
9	4.489E-01	7.173E-01	8.948E-01
10	4.541E-01	7.121E-01	1.030E+00
AVG	4.512E-01	7.455E-01	9.853E-01

Tables 8.4 , 8.5 , 8.6 show the max current average for the extracted R_{DSon} value. Since the load voltages are 50, 75 and 100 volts, it is easy note that the expected current values are 500, 750 and 1000 mA during testing. All current values exhibit noise in their measurement, oscillations compare to their expected value. But the 50 V condition failed to reach the 500 mA value and had an asymptote at around 460 mA. A constant error present across the testing under this load condition. Additionally on the 75V, the outliers move above the current value of 750 mA up too 10 0mA more (see Table 8.5). Finally at 100V, fluctuation around the 1 A are clearly noticeable in the data. Observe that across the on-state, the mismatch on reaching the ideal current value is present, yet it still retains a straight line behavior through the offset and the R_{DSon} measurement is executed.

8.3.3 Power Dissipation

Tables 8.7 , 8.8 and 8.9 show the power dissipation at the minimum R_{DSon} value. Under all conditions of the testing the power dissipation across device is below 1 Watt. DUT 1 exhibited the lowest power dissipation of all the devices. Regarding

Table 8.5 : MAX Current of DUT 2(Amps)

	DUT #2		
TEST NUMBER	50V	75V	100V
1	4.494E-01	8.701E-01	1.03E+00
1	4.554E-01	8.637E-01	1.06E+00
3	4.634E-01	8.219E-01	9.740E-01
4	4.537E-01	8.281E-01	1.164E+00
5	4.568E-01	7.862E-01	9.531E-01
6	4.646E-01	7.579E-01	1.016E+00
7	4.585E-01	7.818E-01	1.092E+00
8	4.566E-01	7.699E-01	1.002E+00
9	4.573E-01	7.874E-01	9.939E-01
10	4.619E-01	8.041E-01	-
AVG	4.578E-01	8.071E-01	9.301E-01

Table 8.6 : MAX Current of DUT 3(Amps)

	DUT #2		
TEST NUMBER	50V	75V	100V
1	4.513E-01	8.314E-01	9.763E-01
1	4.536E-01	8.081E-01	1.080E+00
3	4.617E-01	7.689E-01	9.710E-01
4	4.528E-01	7.947E-01	1.157E+00
5	4.612E-01	7.871E-01	9.548E-01
6	4.637E-01	8.293E-01	1.059E+00
7	4.528E-01	7.751E-01	1.079E+00
8	4.562E-01	7.486E-01	-
9	4.548E-01	7.977E-01	-
10	4.600E-01	7.874E-01	-
AVG	4.568E-01	7.928E-01	7.278E-01

the behavior on increasing load voltages the dissipation increased as the load voltage increased, this was an expected behavior from the equation in Ch.2.

Table 8.7 : Power Dissipation of DUT 1(Watts)

	DUT #1		
TEST NUMBER	50V	75V	100V
1	6.287E-02	9.650E-02	1.851E-01
1	4.628E-02	9.209E-02	1.660E-01
3	4.349E-02	8.824E-02	1.157E-01
4	4.073E-02	8.488E-02	1.470E-01
5	4.050E-02	8.192E-02	1.586E-01
6	3.994E-02	7.932E-02	1.308E-01
7	3.823E-02	7.703E-02	1.707E-01
8	3.781E-02	7.500E-02	1.354E-01
9	3.661E-02	7.319E-02	1.476E-01
10	3.686E-02	7.159E-02	2.118E-01
AVG	4.233E-02	8.198E-02	1.569E-01

Table 8.8 : Power Disspation of DUT 2(Watts)

	DUT #2		
TEST NUMBER	50V	75V	100V
1	3.900E-02	1.257E-01	1.979E-01
1	4.114E-02	1.202E-01	9.009E-02
3	4.084E-02	1.091E-01	9.967E-02
4	3.928E-02	1.038E-01	4.643E-02
5	3.819E-02	9.481E-02	9.895E-02
6	6.854E-02	8.391E-02	3.069E-02
7	5.008E-02	9.131E-02	9.534E-02
8	4.583E-02	9.322E-02	1.288E-01
9	4.272E-02	9.431E-02	1.105E-01
10	4.274E-02	1.003E-01	-
AVG	4.484E-02	1.017E-01	8.983E-02

Table 8.9 : Power Dissipation of DUT 3(Watts)

	DUT #3		
TEST NUMBER	50V	75V	100V
1	1.054E-01	1.323E-01	2.237E-01
1	8.898E-02	1.166E-01	2.300E-01
3	6.141E-02	1.285E-01	1.767E-01
4	5.270E-02	1.106E-01	2.276E-01
5	8.309E-02	9.960E-02	2.155E-01
6	7.952E-02	1.412E-01	1.787E-01
7	7.292E-02	1.277E-01	1.883E-01
8	5.126E-02	1.045E-01	-
9	7.533E-02	1.332E-01	-
10	5.881E-02	1.208E-01	-
AVG	7.294E-02	1.215E-01	1.440E-01

8.3.4 R_{DSon} Measurement

Table 8.10 shows the average behavior across the DUT's and load voltages. Here an interesting trend can be observed. The average indicates that as the load voltage increased, the R_{DSon} decreased. Overall, across the different load voltages and devices, even if there were some shifts regarding the expected current levels, these did not deter the execution of an R_{DSon} measurement.

Fig. 8.11 shows the general trend and distribution of R_{DSon} for single pulse measurement. We can observe that the general trend on the R_{DSon} is to fall below the 200 mohm range. From the DUT datasheet, the static value of the R_{DSon} is 190 mohms. The majority of data value falls in the vicinity of that value.

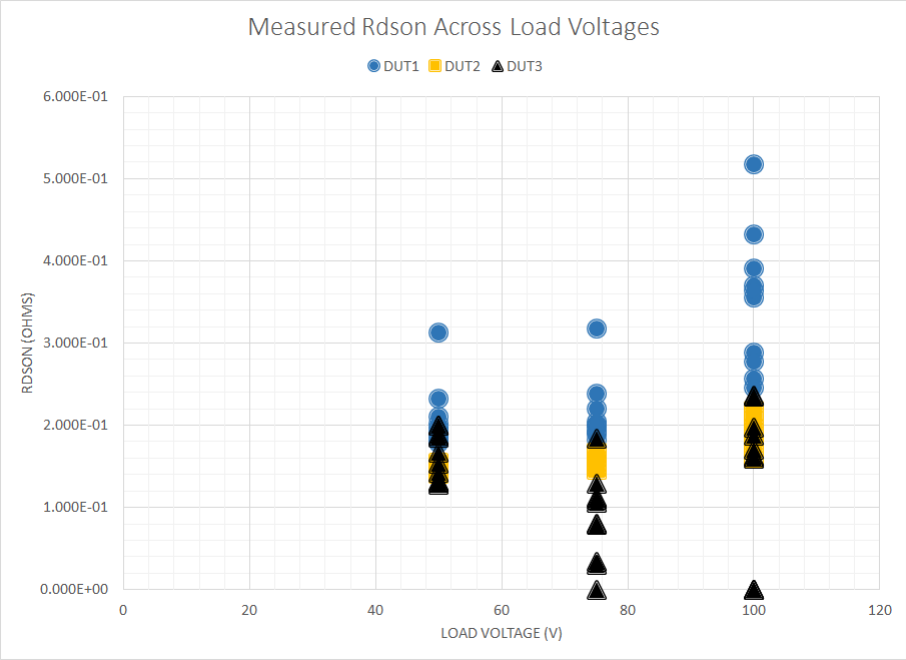


Figure 8.11 : R_{DSon} Measurement Distribution by DUT and Load Voltage

Table 8.10 : R_{DSon} Across Load Voltages and DUT's(Ohms)

	DUT #1, #2, #3		
TEST NUMBER	50V	75V	100V
1	3.124E-01	1.543E-01	1.998E-01
2	2.321E-01	1.523E-01	1.660E-01
3	2.109E-01	1.505E-01	1.316E-01
4	2.025E-01	1.488E-01	1.297E-01
5	1.970E-01	1.473E-01	1.871E-01
6	1.925E-01	1.459E-01	1.279E-01
7	1.885E-01	1.446E-01	1.531E-01
8	1.849E-01	1.434E-01	1.421E-01
9	1.817E-01	1.422E-01	1.844E-01
10	1.787E-01	1.412E-01	1.998E-01
11	1.931E-01	1.661E-01	1.840E-01
12	1.983E-01	1.612E-01	7.874E-02
13	1.902E-01	1.615E-01	1.051E-01
14	1.908E-01	1.513E-01	3.430E-02
15	1.830E-01	1.534E-01	1.089E-01
16	3.175E-01	1.461E-01	2.971E-02
17	2.383E-01	1.494E-01	7.995E-02
18	2.198E-01	1.573E-01	1.283E-01
19	2.043E-01	1.521E-01	1.119E-01
20	2.003E-01	1.551E-01	-
21	5.174E-01	1.914E-01	2.347E-01
22	4.325E-01	1.785E-01	1.971E-01
23	2.880E-01	2.173E-01	1.874E-01
24	2.570E-01	1.751E-01	1.699E-01
25	3.907E-01	1.608E-01	2.364E-01
26	3.697E-01	2.053E-01	1.594E-01
27	3.557E-01	2.125E-01	1.616E-01
28	2.464E-01	1.864E-01	-
29	3.641E-01	2.094E-01	-
30	2.780E-01	1.949E-01	-
AVG	2.572E-01	1.652E-01	1.276E-01
STD	8.776E-01	2.320E-01	7.133E-01
SE	1.602E-01	.4235E-01	1.302E-01
RSE	6.230E-02	2.564E-02	1.021E-01

8.4 R_{DSon}: Stress Test Measurements

The remaining figures and tables expose the results of the stress test execution. Recall that the stress test conditions are 10 minutes, 1 measurement per minute at the load voltage of 50 volts. The biasing condition of the test circuit remains the same. During the stress test, two main trends occur: the increase in R_{DSon} as the test progresses, and that the device after each test did not increase the R_{DSon} value.

Figure 8.12 gives a more visual description of the R_{DSon} stress test execution. Observe how across the test execution a linear behavior but at some instances of execution some values off set such as in the fourth measurement in the second and third stress test.

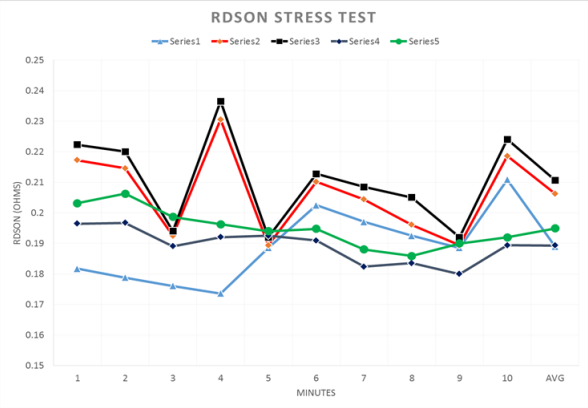


Figure 8.12 : R_{DSon} Stress Test Measurement

Tables 8.12 and 8.13 are the current across the device and power dissipation during the repetitions of the stress test. During the repetitions of the stress test, the current remained stable with no major fluctuation observed. The power dissipation remain in the subwatt range across the stress test execution.

Table 8.11 : R_{DSon} Stress Test Measurements (Ohms)

Minutes	Test 1	Test 2	Test 3	Test 4	Test 5
1	1.817E-01	1.909E-01	1.947E-01	1.964E-01	2.031E-01
2	1.787E-01	1.823E-01	1.880E-01	1.967E-01	2.062E-01
3	1.760E-01	1.835E-01	1.859E-01	1.890E-01	1.987E-01
4	1.736E-01	1.799E-01	1.899E-01	1.920E-01	1.962E-01
5	2.109E-01	2.186E-01	2.240E-01	2.306E-01	2.365E-01
6	2.025E-01	2.101E-01	2.127E-01	2.160E-01	2.257E-01
7	1.970E-01	2.043E-01	2.085E-01	2.172E-01	2.223E-01
8	1.925E-01	1.960E-01	2.050E-01	2.145E-01	2.200E-01
9	1.885E-01	1.894E-01	1.919E-01	1.925E-01	1.940E-01
10	1.849E-01	1.944E-01	2.035E-01	2.117E-01	2.186E-01
AVG	1.886E-01	1.950E-01	2.004E-01	2.057E-01	2.121E-01
STDEV	1.210E-02	1.266E-02	1.240E-02	1.406E-02	1.439E-02

Table 8.12 : Current Across Stress Test(Amps)

Minutes	Test 1	Test 2	Test 3	Test 4	Test 5
1	5.264E-01	5.356E-01	5.383E-01	5.447E-01	5.472E-01
2	5.176E-01	5.228E-01	5.285E-01	5.355E-01	5.416E-01
3	5.098E-01	5.160E-01	5.185E-01	5.241E-01	5.329E-01
4	5.028E-01	5.082E-01	5.083E-01	5.106E-01	5.122E-01
5	4.966E-01	4.984E-01	5.068E-01	5.084E-01	5.126E-01
6	4.910E-01	4.993E-01	5.018E-01	5.062E-01	5.145E-01
7	4.861E-01	4.936E-01	5.026E-01	5.046E-01	5.080E-01
8	4.817E-01	4.909E-01	4.977E-01	5.030E-01	5.119E-01
9	4.778E-01	4.861E-01	4.870E-01	4.888E-01	4.896E-01
10	4.743E-01	4.754E-01	4.844E-01	4.872E-01	4.943E-01
AVG	4.964E-01	5.026E-01	5.074E-01	5.113E-01	5.165E-01
STDEV	1.748E-02	1.814E-02	1.707E-02	1.854E-02	1.883E-02

Table 8.13 : Power Disspation in Stress Test(Watts)

Minutes	Test 1	Test 2	Test 3	Test 4	Test 5
1	5.034E-02	5.291E-02	5.594E-02	5.736E-02	5.939E-02
2	4.788E-02	5.184E-02	5.629E-02	5.839E-02	6.087E-02
3	4.574E-02	4.824E-02	5.048E-02	5.297E-02	5.615E-02
4	4.387E-02	4.586E-02	4.850E-02	4.982E-02	5.266E-02
5	5.199E-02	5.225E-02	5.655E-02	5.947E-02	6.023E-02
6	4.882E-02	5.182E-02	5.364E-02	5.675E-02	6.012E-02
7	4.655E-02	4.982E-02	5.225E-02	5.566E-02	5.801E-02
8	4.466E-02	4.630E-02	4.849E-02	5.083E-02	5.199E-02
9	4.303E-02	4.492E-02	4.633E-02	4.944E-02	5.099E-02
10	4.161E-02	4.325E-02	4.625E-02	4.843E-02	5.028E-02
AVG	4.645E-02	4.872E-02	5.147E-02	5.391E-02	5.607E-02
STDEV	3.317E-03	3.483E-03	4.038E-03	4.097E-03	4.206E-03

Chapter 9
Conclusion and Future Work

9.1 Conclusion

This work presented the design and implementation of an automated extraction process for dynamic on-resistance of a power MOSFET using low cost equipment. To achieve these objectives, a systematic procedure to extract the dynamic on resistance was established. The automation process to perform measurements in packaged devices was designed and implemented in LabVIEW.

The automation process designed and developed in LabVIEW allows for extracting R_{DSon} packaged devices without human intervention after specifying the parameters and biasing conditions for the test. This software was designed with a linear architecture that provides a scalable code for future updates and reviews.

The implementation of the test was done using low cost commercially available equipment. This allows for ease of implementation and replication or modification of the setup. From a cost perspective, the instrumentation setup was calculated at near $40,000$ dollars.

9.2 Contributions

The contributions of this work include:

- Accurate dynamic R_{DSon} value of a power MOSFET can be obtained through an automated setup using low cost equipment.

- A replicable and systematic procedure to obtain the dynamic on-resistance of a power MOSFET.

- An automation procedure to extract dynamic on-resistance with minimal human intervention.

- A procedure that implements a stress test functionality

- Knowledge about considerations to be taken when performing automated characterization tests for power MOSFETS.

- Knowledge of the R_{DSon} behavior over time that can be used for modeling or prognotics purposes.

9.3 Future Work

This work can be expanded in several scenarios. From a hardware perspective, efforts can be made towards the circuit for higher current or higher voltage conditions. From a software perspective, breaking the linear structure into a modular one is advantageous. Furthermore, improvement in the stress test capture can be performed by implementing a producer/consumer structure, that would allow for even more rapid capture of the data. Also, having instrumentation that can test a variety of devices from different materials is yet another step in the extension of this work. Finally, further work enhancing the use of R_{DSon} as a prognostic agent by expanding the capability of the test suite to observe and decide based on R_{DSon} captured data is another possible expansion of this work.

Appendices

Appendix A
LabVIEW Code Specifics

LabVIEW CODE:Block Diagrams

A.1 User Info

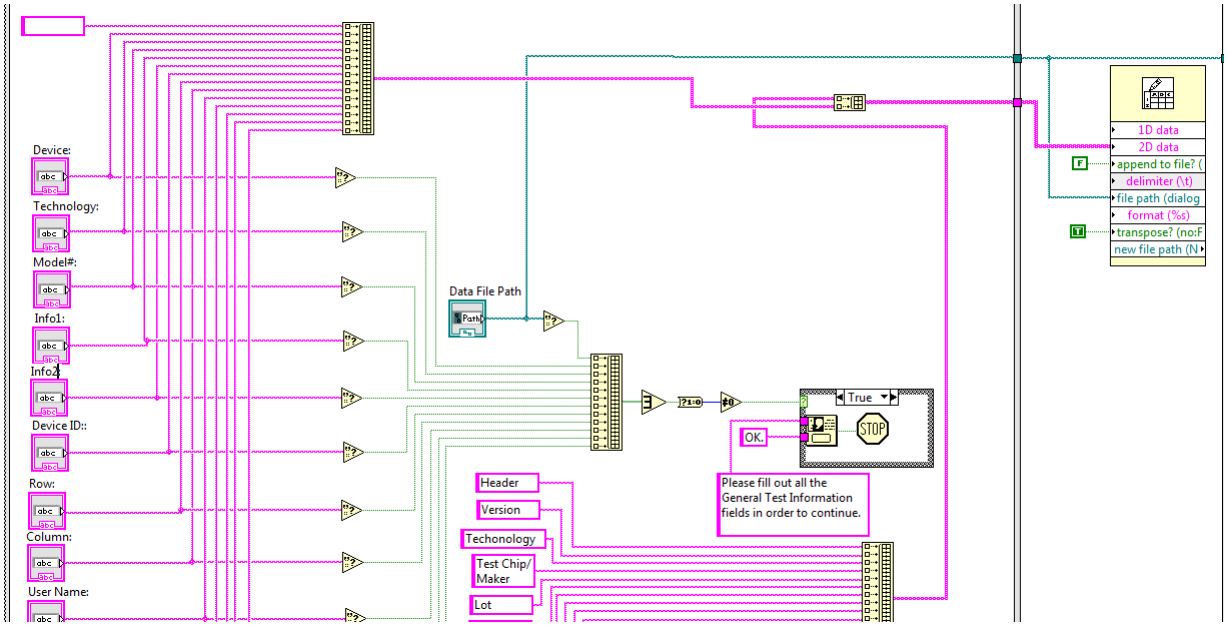


Figure A.1 : User Test Information

This part of automation sequence the allows the user to place information about the test into the excel file that is generated via the test execution.

A.2 Instrument Configuration

This section shows the LabVIEW Code dedicated to setting up the instruments used in the test.

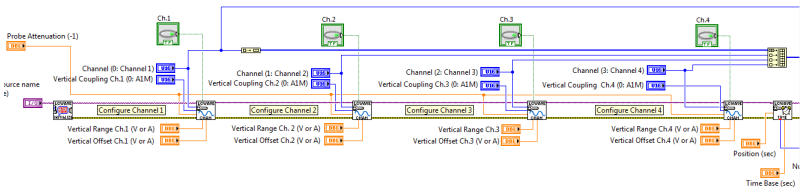


Figure A.2 : LeCroy DSO Setup.

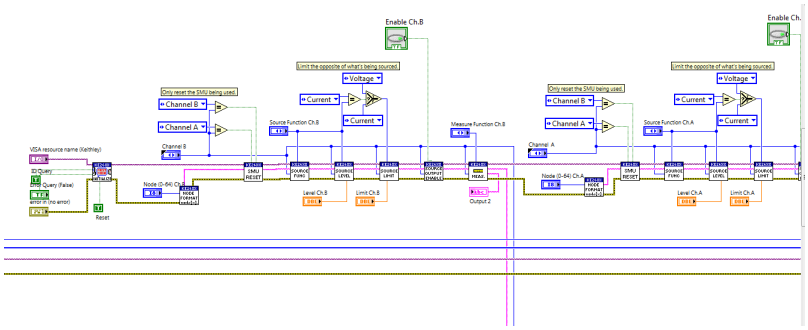


Figure A.3 : K2612 SMU Setup.

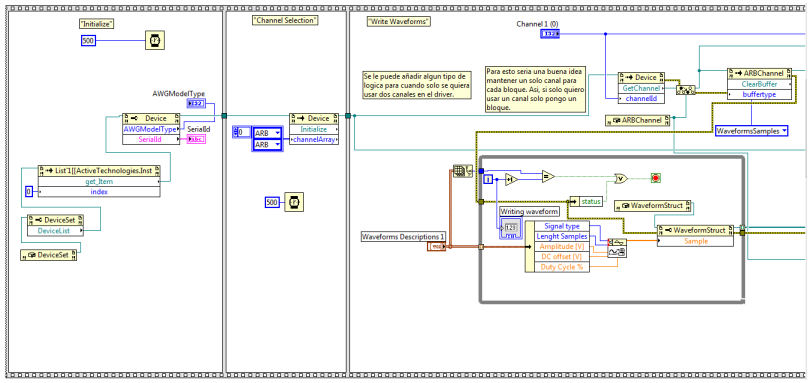


Figure A.4 : ArbStudio Waveform Generator Setup.

A.3 Data Capture

This section shows the LabVIEW Code dedicated to the actual data capture and storage of information.

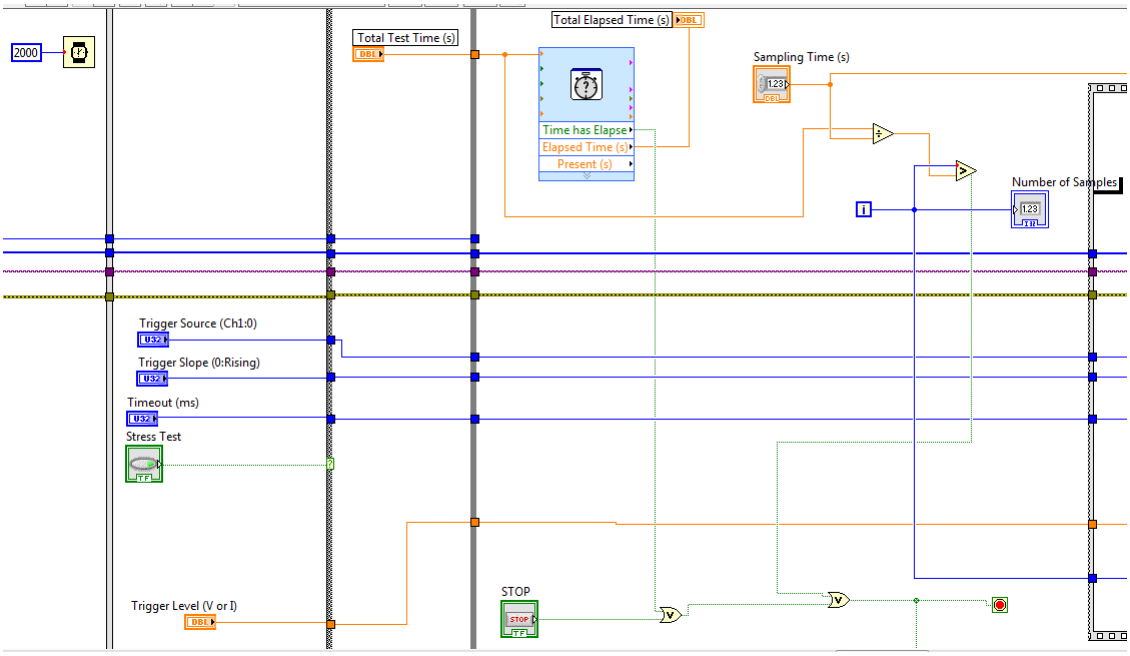


Figure A.5 : Selection and Implementation of Single or Stress Test Measurement

A.4 Closure

This section shows the LabVIEW code dedicated to terminate the test and the communication with devices. The figure at hand shows the termination of the waveform generator and the K2612 SMU.

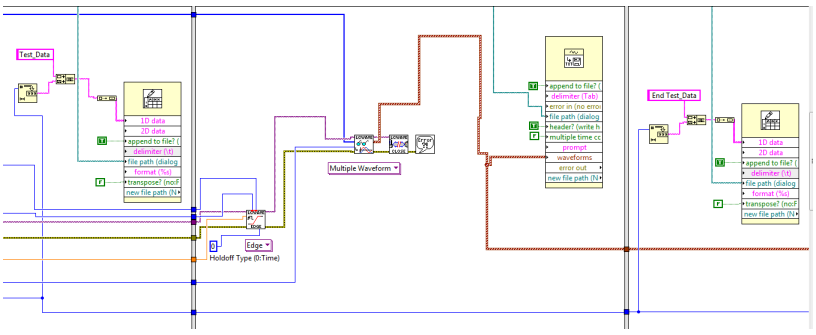


Figure A.6 : Capture and Storage of Data

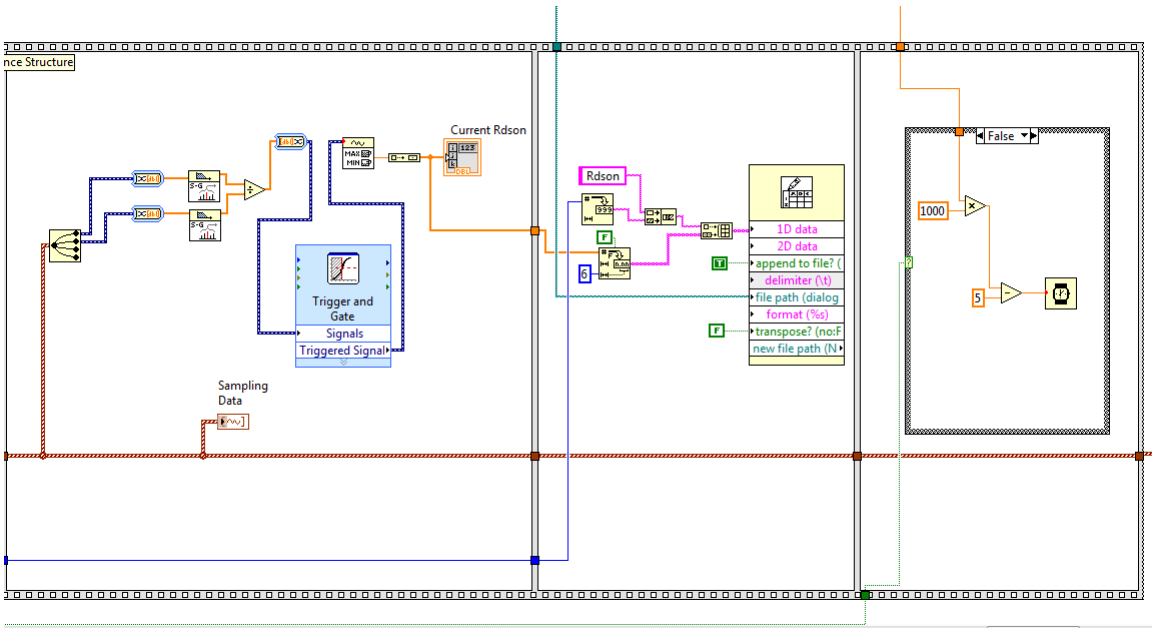


Figure A.7 : Processing and Storage of Data

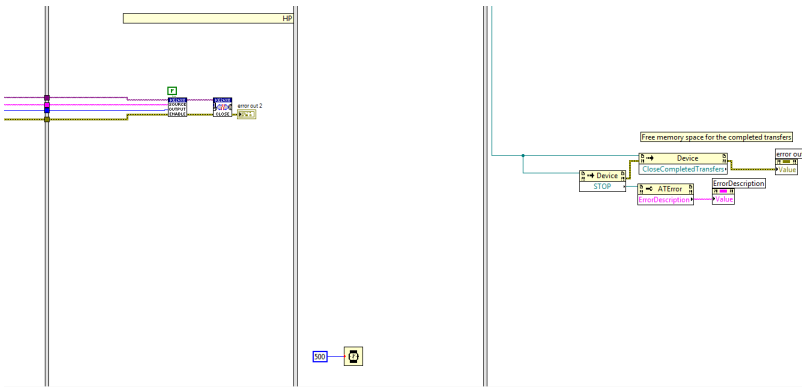


Figure A.8 : End Test and Terminate Communications with Instruments

Appendix B
Data Storage Sample

B.1 Sample Excel DataSheet from Rdson Test

Fig. B.1 shows the resulting spreadsheet after it has been processed through the R_{DSon} vi. There are two main sections:

- Header Section
- Data Section

Header Section The header section allows the user to set known test and device information so it can be stored with the data coming from the test.

Data Section The data section is where the data collected from the LeCroy DSO is stored in the spreadsheet. It has beginning and end markers. The "X" present after the verbal indicator is for the Stress Test. The X is a variable that stores the loop index value as the stress test is being executed. The "END" indicates the last data set capture and the closure of the spreadsheet after test execution.

	Name Box	B	C	D	E
1	Header				
2	Device	1			
3	Techonology	MOSFET			
4	Model #	x1234			
5	Structure	3			
6	Additional Info	Y			
7	Additional Info	Z			
8	Row	5			
9	Column	6			
10	User Name	Tester			
11	Temperature	25			
12	Date Time:	mm/dd/yyyy			
13	End Header				
14	Detail				
15	Test DATA X				
16	TIME	CH1 DATA	CH2 DATA	CH3 DATA	CH4 DATA
17					
18					
19					
20					
21					
22		DATA GOES HERE			
23					
24					
25					
26					
27					
28	End Test DATA X				
29	END				

Figure B.1 : Sample Spreadsheet

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