SPICE MODEL IMPROVEMENT FOR ANNULAR MOSFET SIMULATION USING AUTOMATED PARAMETER EXTRACTION

By

Boris Miguel Contreras Ospino

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Approved by:

Gladys Ducoudray, Ph.D. Chair, Graduate Committee	Date
Rogelio Palomera, Ph.D. Member, Graduate Committee	Date
Guillermo Serrano, Ph.D. Member, Graduate Committee	Date
Mauricio Cabrera, Ph.D. Graduate Studies Representative	Date
José Colom, Ph.D. Department Chairperson	Date

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December 2016

Chair: Dr. Gladys Ducoudray
Department: Electrical and Computer Engineering Department

In industry, the creation of an accurate standard MOSFET model in a new technology may take several months. After the model is developed, it can be use to predict the behavior of devices created under the same process, allowing the simulation of a circuit while the final device or prototype is being fabricated. For annular MOSFETs, standard transistor models fail to predict and simulate its electrical behavior, due to its asymmetrical geometry.

A validated experimental solution to extract parameters such as MOS technology aspect ratio, can be used for long periods of time. For this reason gaps between old and new solutions for experimental extractions can be found, including used methods and equipments.

This thesis presents the design of low-cost hardware and software automated solution to improve a SPICE model for annular/gate enclosed MOSFETs simulation. The automated solution involves the experimental aspect ratio (W/L) extraction of annular MOSFETs, along with DC level 1 parameter calculations. This works also presents a mathematical alternative to calculate the annular transistors aspect ratio through conformal mapping.

The accuracy of each extracted parameter and annular MOSFETs W/L were verified by comparing with foundry provided values and other previously validated methods respectively. The results show that the automated implementation for DC level 1 parameter and annular MOSFETs W/L extraction can be use to minimize the user intervention and time for the tests execution.

Resumen de tesis presentado a la Escuela Graduada
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MEJORAS AL MODELO DE SPICE PARA SIMULACIÓN DE MOSFET ANULARES UTILIZANDO UNA EXTRACCIÓN DE PARAMETROS AUTOMATIZADA

Por

Boris Miguel Contreras Ospino

Diciembre 2016

Consejero: Dr. Gladys Ducoudray
Departamento: Ingeniería Eléctrica y Computadoras

En la industria, la creación de un modelo preciso de MOSFET estándar en una nueva technología puede tomar varios meses. Después de que el modelo es creado, este puede ser usado para predecir el comportamiento de dispositivos creados bajo el mismo proceso, permitiendo la simulación de un circuito mientras el dispositivo o prototipo final está siendo fabricado. Los modelos de transistores estándares fallan en predecir y simular el comportamiento eléctrico de MOSFETs anulares debido a su geometría asimétrica.

Una solución experimental validada para extraer parametros como la relacion de tamaño en tecnología MOS, puede ser usada por largos periodos de tiempo. Por esta razon se pueden encontrar brechas entre soluciones previas y nuevas para extracciones experimentales, esto incluye equipos como metodos usados.

Esta tesis presenta el diseño de una solución de hardware y software de bajo costo para mejorar un modelo de SPICE para la simulación de MOSFETs anulares/compuerta encerrada. La solucion automatizada incluye la extracción experimental de relación de tamaño (W/L) de MOSFETs anulares, junto con el cálculo de parámetros DC de nivel 1. Este trabajo también presenta una alternativa matemática para calcular la relación de tamaño de transistores anulares mediante mapeo conforme.

La precisión de cada parámetro extraído y el tamaño W/L de MOSFETs anulares fue verificada comparando con valores provistos por el fabricante para los parámetros y otros métodos previamente validados para la determinación del tamaño W/L respectivamente. Los resultados muestran que la implementación automatizada para la extracción de parámetros DC de nivel 1 y W/L de MOSFETs anulares puede ser usada para minimizar la intervención del usuario y tiempo para ejecutar las pruebas.

This work is dedicated to family and friends who were always there supporting me until the end of this journey.

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List of Abbreviations

MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
DC	Direct Current.
VI	Virtual Instrument
DUT	Device Under Test
PCB	Printed Circuit Board
ANOVA	Analysis of Variance

List of Symbols

I_D	Drain Current.
I_{DS}	Drain to Source Current
V_D	Drain Voltage.
V_G	Gate Voltage.
V_{GS}	Gate to Source Voltage
V_S	Source Voltage.
V_B	Body Voltage.
V_P	Pinch-off Voltage.
V_{TH}	Threshold Voltage
W/L	Aspect Ratio (Effective Channel Width/Length)

Chapter 1
INTRODUCTION

Rectangular MOSFETs (metal–oxide–semiconductor field-effect transistors) are known to be radiation sensitive due its layout design. Radiation introduces trapped charges in the Si/SiO_2 interface and gate oxide SiO_2 which affect the performance of MOS transistors by reducing threshold voltage [1]. A proposed solution for this problem was to scale down the oxide thickness, in result the amount of charge trapped would be smaller [2]. The scale down solution has an issue known as "bird's beak", this reduces the effective channel width and causes an increment in radiation sensitivity to the oxide of MOS devices. By the end of 1990, a new approach called shallow trench isolation was introduced, obtaining satisfactory results with the "bird's beak" and channel width. In [3] some cases of failure for shallow trench isolation were pointed out. The geometry used was still radiation sensitive because there are some regions in rectangular MOSFETs where the leakage crosses over the field of isolation which causes a threshold voltage shift, making the device susceptible to failure.

Using radiation hardened by design (RHBD) technique, the mentioned problem can be solved. Annular or enclosed layout MOSFET, is a RHBD approach where the drain/source is surrounded by the gate and source/drain outside. This prevents the generation of oxide isolation that could invert and causes diffusion (drain-source) leakage [4]. Using this type of layout has proven its effectiveness at higher radiation doses against the traditional rectangular transistor layout [5]. For this design, there are some limitations in terms of size because the area used is increased in order to accomplish the annular geometry. Having a larger area increases the gate

capacitance, the W/L ratio cannot be smaller than 2.26 [6] due to its asymmetric geometry. Also, modeling the electrical response is more difficult compared to a symmetric rectangular (regular) transistor. In industry, the creation of an accurate regular MOSFET model in a new technology, may take several months. For annular transistors, designers usually simulate each transistor as two large parallel transistors in order to increase the accuracy in simulation. The issue for this solution is that, due to the non-conventional geometry conventional rectangular transistor equations do not represent accurately MOSFET behavior. Width over length ratio is an important parameter for any transistor modeling and simulation, thus the importance of its extraction.

The objective of this research is to develop a fast low-cost automated DC level 1 parameter extractor and aspect ratio (W/L) calculation using LabVIEW^{TM} with available test equipment. This allows the test to need minimal supervision. A MATLAB® script with the Schwarz-Christoffel transformation is used, such that, an accurate approximation of a gate enclosed transistor aspect ratio (Width over Length) can be obtained.

This document is organized as follows: Chapters 2 and 3 show the theoretical background and previous work related to annular MOSFETs, conformal mapping and parameter extraction. Chapters 4 and 5 present the Problem Statement and Objectives of this proposal respectively. Chapter 6 shows the Methodology used to obtain the proposed objectives. In order to design a proper test board, Chapter 7 shows the procedure to extract the aspect ratio for annular transistor along with other DC level 1 parameters. Chapter 8 shows the automation procedure along with the used equipments. Finally, chapters 9 and 10 shows the obtained results, discussion and conclusion of this thesis.

Chapter 2
BACKGROUND

2.1 Radiation Harsh Environment

Radiation environments are characterized by their spectrum of particles and energy distribution. The produced radiation can come from natural (Space, Terrestrial) environments or man-made (Nuclear power, Atmospheric weapons testing, Medical diagnostics, Airline travel) ones [7].

Space is a radiation harsh environment where semiconductor devices and materials have their main application in space missions. In this harsh environment radiation can come from:

- Trapped protons and electrons
- Galactic Cosmic Ray Ions
- Solar Flare Protons
- Solar Flare Heavy Ions

The sources of radiation levels in space depend on the sun activity [8]. These sources of radiation emit a low dose rate (10^{-4} to 10^{-2} rad/s), but since a space mission usually take years. The amount of radiation (total ionizing dose - TID) accumulates to the order of 10^5 rad this cause different effects on semiconductors (MOSFETs) [9].

1. Ionization - Causes trapped oxide charges leading to threshold voltage shift.
2. Sigle-Event Effects - can be destructive or nondestructive

- Latch-up (Destructive).
- Burnout (Destructive).
- Gate Rupture (Destructive).
- Upset[1] (Nondestructive).
- Transients (Nondestructive).
- Functional Interrupt (Nondestructive).
- Stuck Bits (Nondestructive).

2.2 Radiation hardened by design

Radiation Hardened by Design (RHBD) are techniques to enhance CMOS integrated circuits tolerance to ionizing radiation environments such as nuclear power industries and outer space. The RHBD techniques can be applied at different levels [10].

- Layout level
- Transistor level
- Gate level
- Register transfer level
- Software level

2.3 Annular MOSFETs

Annular MOSFETs also known as Enclosed Layout Transistors (ELT). This technique for RHBD at layout level, is used to increase immunity to Single-Event Upsets with bigger capacitance in the sensitive nodes. Another important use of Annular

[1] Toogles

MOSFETs is elimination of the leakage path radiation-induced between drain and source [10]. Annular transistors can be found in different geometries:

- square
- circular
- square edgeless
- octagonal

2.4 The Schwarz–Christoffel Formula

The Riemann Mapping Theorem implies that any simply connected domain with the exception of the entire complex plane, can be conformally mapped into the unit disk preserving signed angles satisfying the Laplace equation. The Schwarz–Christoffel Formula it's based on The Riemann Mapping Theorem and is used to compute conformal maps of the unit disk onto a general polygon, in this way an abnormal geometry can be mapped onto a regular one as shown in Figure 2.1 [11].

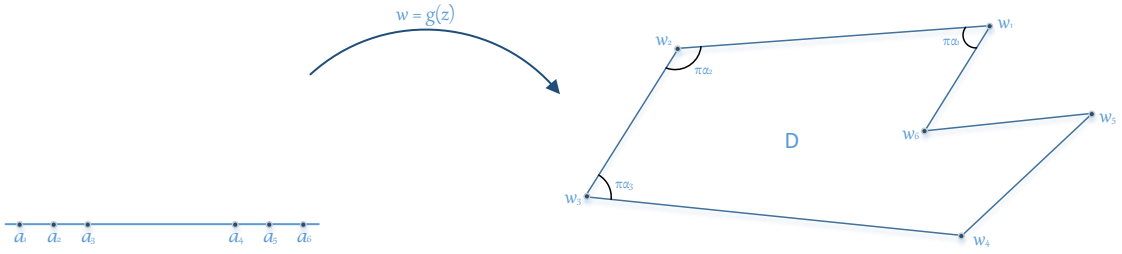


Figure 2.1 : Conformal Mapping [11].

The Schwarz–Christoffel Formula:

$$g(z) = A \int_{z_0}^{z} (t - a_1)^{\alpha_1 - 1} \cdots (t - a_m)^{\alpha_m - 1} dt + B \tag{2.1}$$

This formula is used to perform the transformation from one geometry to another. Where A and B are complex constants, a_m are the prevertices, w_m are the vertices and α_m are the interior angles of the mapped polygon D, as shown in Figure 2.1 .

2.5 MOSFET Parameter Extraction

MOSFET models are used to describe its electrical behavior, used to simulate and test MOS circuits functionality before sending a final design to fabricate. These models are the link between designers and foundries, therefore the accuracy of fundamental parameter extraction is an important for device model development or even correction [12].

There are different models that have their equations and functions based on:

- Threshold-voltage-based models (BSIM3 and BSIM4)
- Surface-potential-based models (HiSIM, MM11, and PSP)
- Charge-based models (EKV, ACM, and BSIM5)

As mention in [13] there are two reasons for model parameter extraction to be difficult, the use of approximations to derive de device model and the dependency of some parameters to other whose accurate value is not known. It also mentions that a commonly used solution is to choose dominants parameters in an operating region to null the effects of the unknown parameters.

Chapter 3
PREVIOUS WORK

Throughout this chapter, a brief summary of relevant publications found in aspect ratio calculation for annular transistors and parameter extraction automation for MOSFETs is presented. The main focus of the mentioned approaches will be in the different techniques used to calculate the aspect ratio of an annular transistor, the efforts committed to develop an automated parameter extractor. The next section introduces the theoretical aspect of the radiation effects in MOS technology.

3.1 Radiation effect in MOS technology

The effect caused by radiation in MOS transistors is known as radiation-induced trap charge, which builds up in the gate oxide and Si/SiO_2 interface, this causes a shift in the threshold voltage. When the shift is large (negative for NMOS), the device cannot be turned off even at zero volts applied at the gate [2].

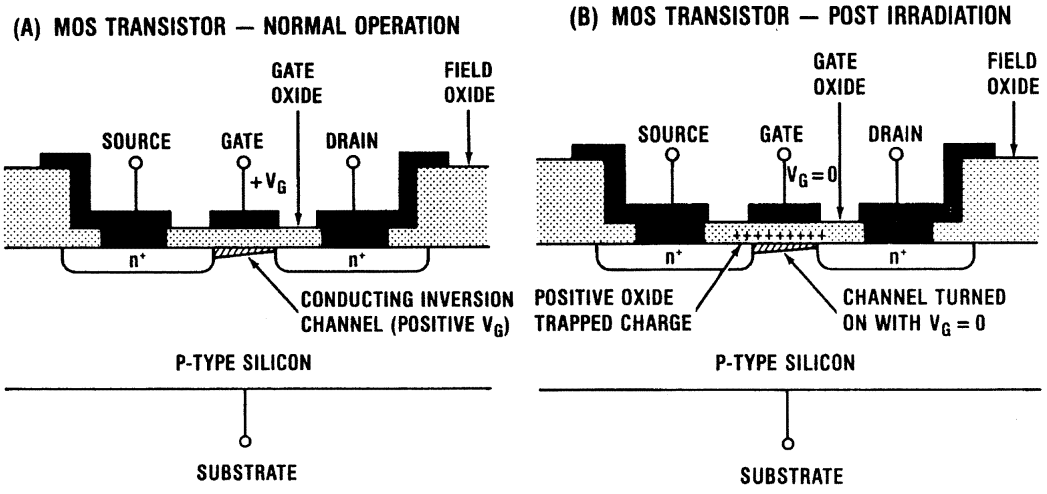


Figure 3.1 : Radiation Effects in MOSFETs [2].

For PMOS transistors, this effect causes fewer problems because holes are less mobile and the charge accumulated in the oxide will push the n-substrate or n-well into accumulation without danger of inversion layer formation [14]; but a threshold voltage shift has to be taken into account for very narrow PMOS devices [15]. The technique used to improve NMOS Transistors tolerance to radiation is the Gate Enclosed Layout also known as annular or edgeless transistors. Where the drain/source is surrounded by the gate, and the gate by source/drain. This geometry has proved to reduce current leakage between drain and source due to charge accumulation [6]. Transistor geometry aspect ratio, width over length (W/L), is an important factor for MOS technology to develop a new model. Many electrical equations for MOSFETs are W/L depended. For annular or enclosed layout transistors it is not possible to use regular (rectangular) MOSFETs equations to develop a model due its abnormal geometry. Fan Xue et al. demonstrated that the information provided by foundry needed an adaptation, because the extraction tool used works only for two-edged MOSFETs due to the asymmetric geometry of annular transistors [16]. The presented approach to calculate the W/L ratio is a direct method where the annular transistor (Square geometry) is divided into 4 equal sized rectangular transistors. The corners are estimated using a constant variable (C_{ab}). As shown in equation 3.1.

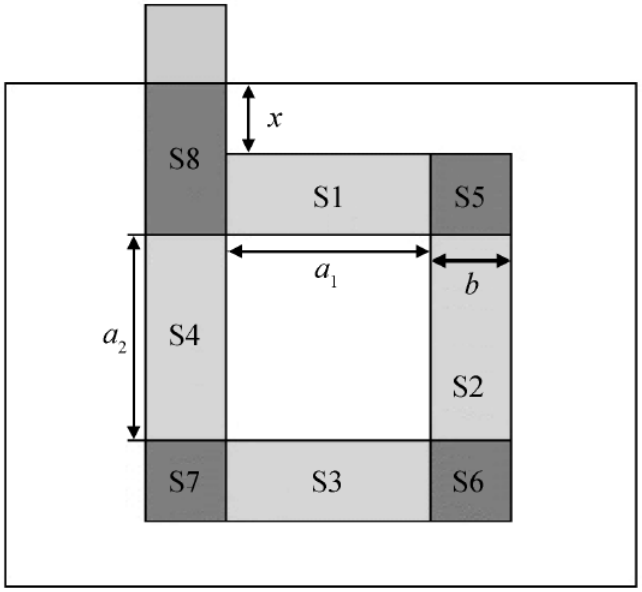


Figure 3.2 : Schematic layout of an annular transistor [16].

C_{ab} is an empirical constant value between 1 and 2.

$$\left(\frac{W}{L}\right)_{eff} = \sum \left(\frac{W}{L}\right)_{RR} + C_{ab} \tag{3.1}$$

$$\left(\frac{W}{L}\right)_{eff} = \frac{2a_1 + 2a_2}{b} + C_{ab} \tag{3.2}$$

They stated that if C_{ab} is larger than 2 the contribution of the four corner devices would be overestimated. Alan Hastings presents another approach to calculate the Width and Length of annular MOS devices (square and circular) [17]. W and L of square annular transistors are approximated using equation 3.3.

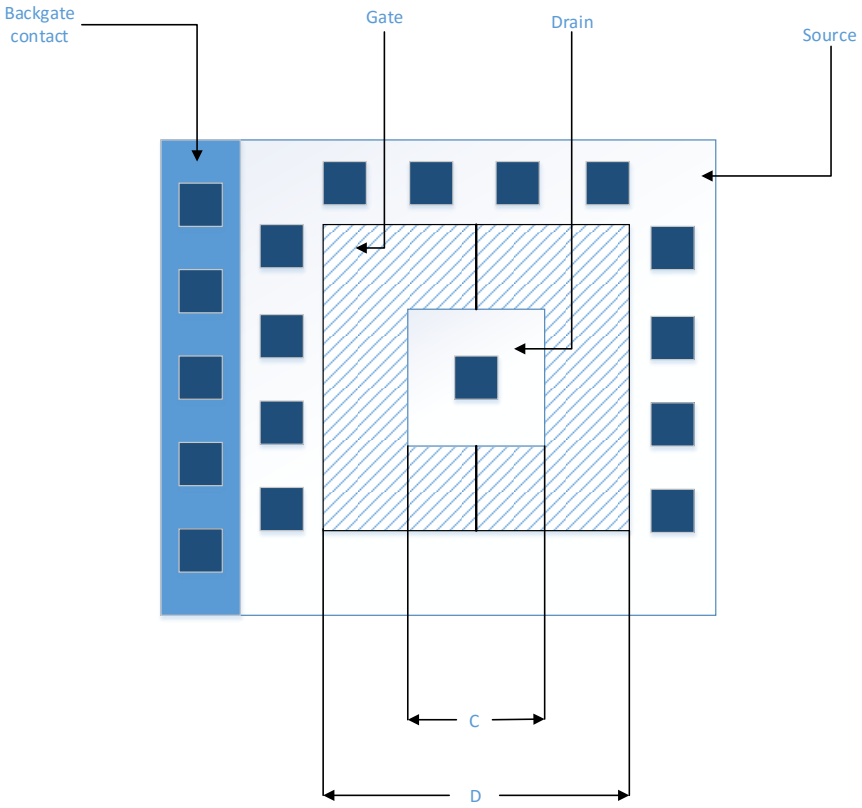


Figure 3.3 : Square Annular Transistor. Where C is the inner gate side length, and D the outer gate side length [17].

$$W = 2(C + D)$$
$$L = (D - C)/2 \tag{3.3}$$

The corner contribution is not included in this approximation. Another common technique used is the elongation of annular transistors this way the corner effects are smaller and it is modeled as two parallel rectangular MOSFETs giving a higher accuracy compared to the not elongated annular MOSFET but the area is greatly increased, resulting in higher costs.

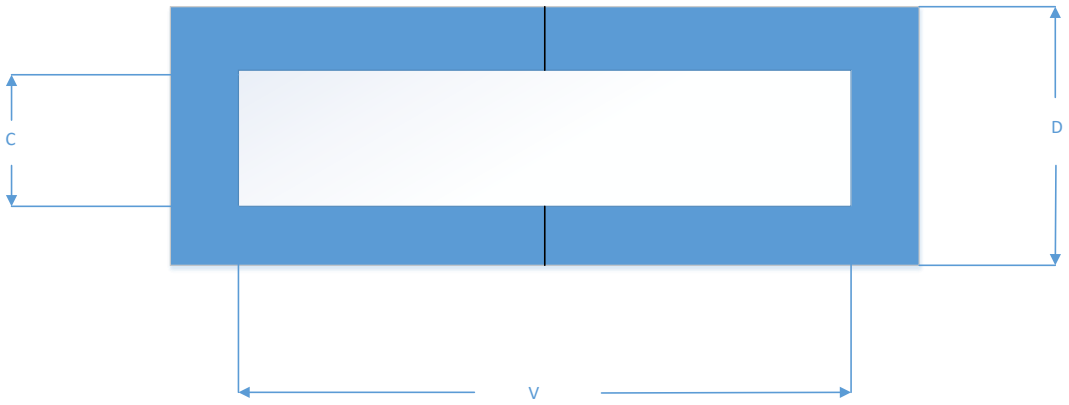


Figure 3.4 : Elongated Square Annular Transistor. Where C is the inner gate height, D the outer gate height and V is the inner gate length [17].

$$W = 2V + C + D$$
$$L = (D - C)/2 \tag{3.4}$$

The gate enclosed layout MOSFETs has a non-symmetrical geometry, using circular, square, broken square and rectangular MOSFETs. Giraldo et al. developed different analytical models for selected gate enclosed shapes mentioned above to evaluate the current expression at a low drain bias [18]. Giraldo's layout presented a broken square edge gate, because circular or 90° gate corners were not possible according to design rules. A contribution due to the corner transistor was added, this was solved using conformal mapping.

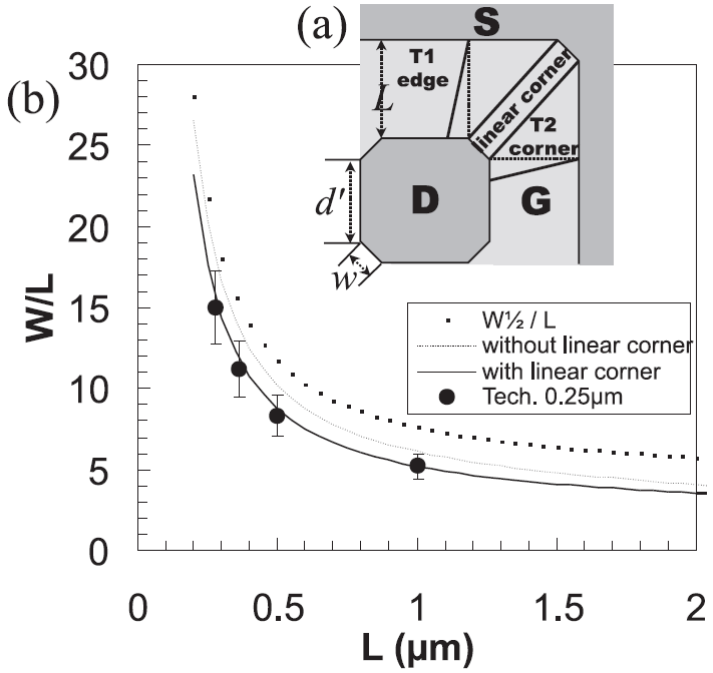


Figure 3.5 : (a) Decomposition of the broken corner square MOSFET into edge (T1), corner (T2), and linear corner, (b) extracted W/L for square MOSFETs in T0.25-μm from our model with $\alpha = 0.05$, our model without considering the linear corner contribution, mid-channel approximation and experimental data for which the dispersion is also shown (1 - σ value) [18].

$$\left(\frac{W}{L}\right)_{eff}^{broken} = 4 \cdot 2\left(\frac{\alpha}{\ln\left(\frac{d}{(d-2\alpha L)}\right)} + \frac{1}{\Delta(\alpha)}\frac{(1-\alpha)}{-\ln(\alpha)} + \frac{1}{2}\frac{w}{L\sqrt{2}}\right) \tag{3.5}$$

$\alpha = 0.05$ is used as a fitting value and $\Delta(\alpha) = \frac{1}{2}\sqrt{\alpha^2 + 2\alpha + 5}$.

An experimental aspect ratio extraction comparing $I_D - V_{GS}$ characteristics is also presented in [18]. It compares a standard MOSFET and gate-enclosed (GE) transistor using the same gate length, and assuming μC_{ox} to be equal for both devices. Standard and GE transistors transconductances are calculated from drain current in triode region. Then, by multiplying the transconductances (g_m) ratio by the standard transistor W/L as shown in equation (3.6), GE W/L is extracted.

$$\left(\frac{W}{L}\right)_{eff}^{enc} = \left(\frac{W}{L}\right)_{eff}^{std} \frac{g_m^{enc}}{g_m^{std}} \tag{3.6}$$

Another experimental W/L extraction was presented in [6]. It uses a comparison between standard and GE MOSFETs drain current at same gate-to-source voltage minus threshold voltage ($V_{GS} - V_{TH}$). Both experimental W/L extraction methods need standard devices with same drawn gate length (L).

Champion and La Rue, used the Schwartz-Christoffel transformation toolkit from MATLAB with a modification to automate the aspect ratio extraction for annular MOSFETs [19].

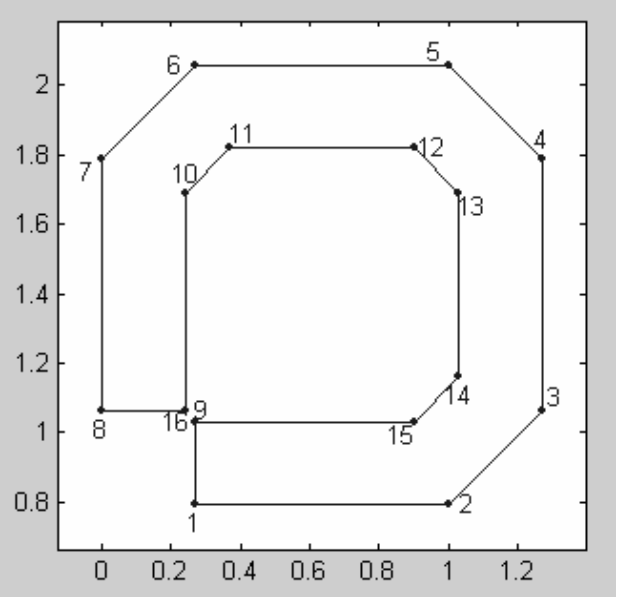


Figure 3.6 : Annular FET Entered into Code [23].

This solution is compared with simulated measurements, this can lead to greater error when compared with experimental data. For alternative aspect ratio calculation the chosen technique is the Champion and La Rue method since it uses the Schwartz-Christoffel transformation.

3.2 MOSFET Parameter Extraction

A common procedure to extract MOSFET parameters is to use a semiconductor parametric test system [20] or parameter analyzer, controlled by a PC using a software (LabVIEW^{TM}) [6] or just using a parameter analyzer with automated routines to control the measurement data [21]. Another way to do a MOSFET parameter extraction is by running algorithms on previous measured information from voltage and current transistors curves [22]. These works have in common the use of equations to extract parameters in a sequential manner.

Table 3.1 : Gate Enclosed MOSFETs previous works summary

Author	Automated Test	LabVIEW^{TM}	MATLAB®	SPICE Model Modification	Experimental Extraction (W/L)
Anelli [6]	Yes	Yes	No	No	Yes
Xue [16]	No	No	No	No	No
Hasting [17]	No	No	No	No	No
Giraldo [18]	No	No	No	No	Yes
Champion [19]	Yes	No	Yes	Yes [23]	No

Width over Length aspect ratio calculation was a common output for the summarized works mentioned above.

Chapter 4
PROBLEM STATEMENT AND HYPOTHESIS

4.1 Problem Statement

The problem addressed is how to improve an existing SPICE model for Annular/Gate Enclosed MOSFET technology simulation. An automated parameter extraction using experimental data through a low cost equipment. A PC algorithm that allows the calculation of aspect ratio for Annular/Gate Enclosed MOSFET, which is a important factor for transistors.

4.2 Hypothesis

This work is presented under the hypothesis that aspect ratio calculation and automated parameter extraction for annular MOSFET using experimental data, can potentially improve an existing SPICE model to accurately simulate its electrical behavior.

Chapter 5
OBJECTIVES

5.1 General Objective

The main objective of this work is to develop an automated parameter extractor for MOS technology using experimental data. A PC algorithm to calculate the aspect ratio of Annular MOSFET to improve an existing SPICE model to accurately simulate Gate Enclosed electrical behavior. To accomplish this objective specific tasks must be completed.

5.2 Specific Objectives

1. Development of a virtual instrumentation environment to measure current and voltage (I-V) from NMOS transistor.
2. Development of an automated DC level 1 parameter extractor for Annular NMOS Transistor.
3. Development of a program to determine the aspect ratio (W/L) of an Annular MOSFET.
4. Comparison with other W/L calculation techniques.
5. Modify an existing SPICE model to accurately simulate Gate Enclosed electrical behavior
6. Compare simulated SPICE model with experimental measured I-V characteristics.

Chapter 6
METHODOLOGY

With the main and specific objectives set, a methodology is needed to accomplish the proposed objectives. Figure 6.1 shows a flowchart for the methodology.

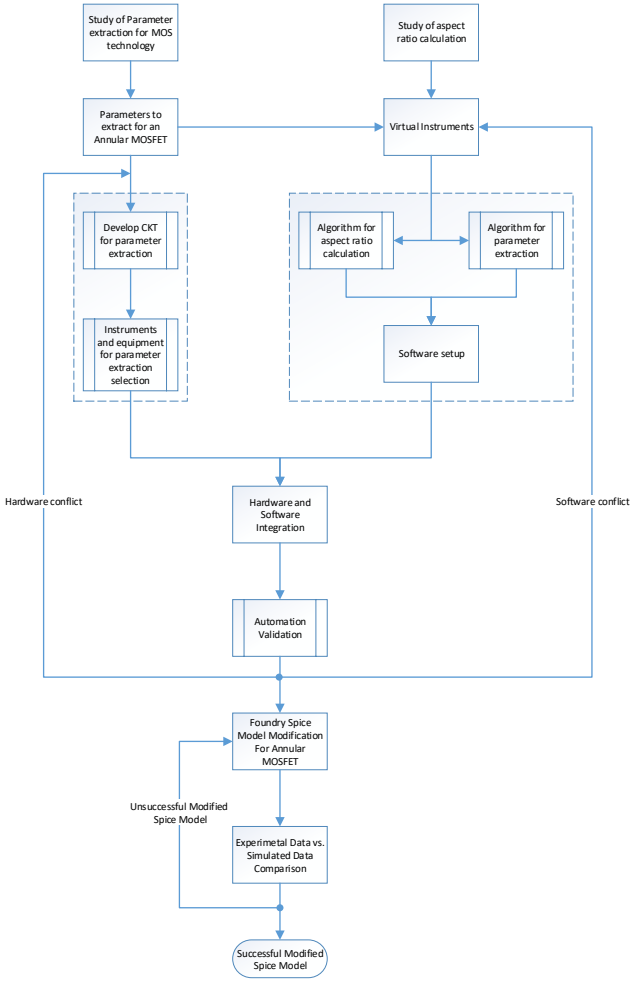


Figure 6.1 : Methodology Flowchart

The methodology for this work consists in a Foundry SPICE model modification for Annular MOSFET in order to improve simulated data compared to experimental data. For this, the implementation of previous work on aspect ratio calculation for abnormal geometries, extraction of MOSFET parameters and software automation to control the equipment is used to execute each needed test. Based on the literature revision a test board with a design to allow multiple connections is selected for parameter extraction. Also, software automation and algorithms are used to calculate Annular Transistor aspect ratio, and the test experimental setup to execute a parameter extraction is also presented.

6.1 MOSFET Parameter Extraction Test Board

After reviewing different parameter extraction methods for MOSFETs, a test board circuit topology was developed. It provides inputs/outputs for each MOSFET terminal (Gate, Drain, Source and Bulk). Important measures were taken in the board design for its interface with the DUT and the instrumentation for each test. Having all the terminals on the test board helps to perform different tests that sense current and voltage curves, from which DC level 1 MOSFET parameters are extracted. Therefore a good interface between DUT and equipment aids on the parameter extraction procedure.

6.2 MOSFET Parameter Extraction Automation

For a successful test automation there are 2 steps to take into account:

1. *MOSFET DC level 1 Parameter Extraction Background*

   Understanding the use of different MOSFET equations and regions of operation to perform DC level 1 Parameter Extraction is addressed in this stage.

2. *Hardware Understanding*

   A review of all the equipments to be use before starting an automation is

an essential task. This way, eliminates possible errors in measurement or performance.

Automated test designs can take a considerable amount of time due to specifications and number of equipments to control. A manual test on the other hand is only time efficient when is executed a few times. After a test is automated can be considerable faster than a manual test. Also, the minimal human intervention helps to minimize the possible errors.

6.3 Hardware and Software Integration

For the integration LabVIEW^{TM} (Laboratory Virtual Instrumentation Engineering Workbench) is selected as a link between equations to calculate parameters and hardware used to obtain the experimental data from each current and voltages curves. LabVIEW^{TM} offer a wide range of drivers to control many devices such as source-meters. These drivers can be modified to execute DC tests on the DUT where source-meters are used to source current/voltage and measure voltage/current, while saving the experimental data for further analysis and also use the equations to extract the parameters. LabVIEW^{TM} offers different ways to execute a program, sequential, in a loop (For - While). The execution can be also by the combination of sequential and loops [24], which is used to optimize a program while it does every programmed task.

The communication with LabVIEW^{TM} can be through different protocols (Ethernet, Serial, GPIB and USB), these protocols refers to the speed at which the data can be acquired. GPIB communication can be accessed with a physical board installed on a PC or using an adapter this allows to control via software several devices using a laptop making it more portable when it comes to using different equipments.

6.4 Validation

For the DC level 1 extracted parameters a comparison with the foundry was made to validate each developed test. Experimental aspect ratio calculation was compared with a validated solution. The modified SPICE model and alternative aspect ratio calculation are validated trough root mean square error relative to the experimental measurements. Also, a graphical comparison was used for simulated and experimental curves.

$$rms = \frac{100}{N}\sqrt{\sum_{i=1}^{N}\left(\frac{exp_i - sim_i}{exp_i}\right)^2} \tag{6.1}$$

Chapter 7
PARAMETER EXTRACTION TEST

In this chapter presents the hardware used for Annular/Gate Enclosed MOSFET parameter extraction from current and voltage measurements. Three main components for this are: circuit board which acts as an interface with the DUT and electronic equipment, this being the second component and lastly the software that controls the equipments and is used for parameters calculations from the measured data. To develop the circuit test board a review on how each chosen parameter is calculated from the measured data is explained next.

7.1 Used Methods for DC Level 1 Parameters calculation

7.1.1 Threshold Voltage (V_{TH})

For threshold voltage (V_{TH}) extraction the Transconductance Change (TC) method was used [25], which states as follows: the inversion charge increases almost exponentially with band-bending. Below threshold, the band-bending tends to be linear with gate-to-source voltage (V_{GS}). Therefore, the change in inversion charge with respect to V_{GS} is almost exponential below threshold. This change in inversion charge is proportional to the transconductance. However, at and beyond threshold, the band-bending begins to stay fairly constant (varies logarithmically).This approximation uses the second derivative of the drain-to-source current (I_{DS}) with respect to the V_{GS} with a fixed low drain-to-source voltage (V_{DS}). The change of I_{DS} to a variation on the gate-to-source voltage is defined as transconductance ($\delta I_{DS}/\delta V_{GS}$) and the change of transconductance is defined as ($\delta g_m/\delta V_{GS} = \delta^2 I_{DS}/\delta V_{GS}^2$). With

this approximation the gate enclosed transistor's V_{TH} is obtained. This is defined as the V_{GS} where the change on transconductance is maximum.

Transconductance to current ratio method (g_m/I_D) as described in [12] is used to determine a set of first order DC Parameters for MOS Transistors, V_{TH} and the specific current (I_{Spec}) are calculated. The voltage where g_m/I_D is approximately 50% of its maximum value is the equilibrium V_{TH} or V_{T0}, this is for $V_{DS} \cong$13mV, congruent to half thermal voltage ($V_t \approx$ 26mV). Both methods use the circuit shown in Figure 7.2 .

Challenges in both methods are:

- Noise in the second derivative used in the TC method. This method is appealing only when the transistor size is considerably larger than minimum size.
- For g_m/I_D method, an approximately 50% of g_m/I_D maximum value is not easy to obtain because the used data comes from discrete experimental measurements.

To overcome each of the mentioned limitations a combination of TC and g_m/I_D is used. The TC method is used on a large and wide transistor to reduce the signal to noise ratio limitation. The V_{TH} is extracted and compared with the applied V_{GS} to obtain the corresponding percentage. This is used as a reference point for the g_m/I_D method. Then the same percentage is applied to subsequent transistors to be measured. Figure 7.1 shows an example of how the percentage is obtained for the g_m/I_D using the TC method.

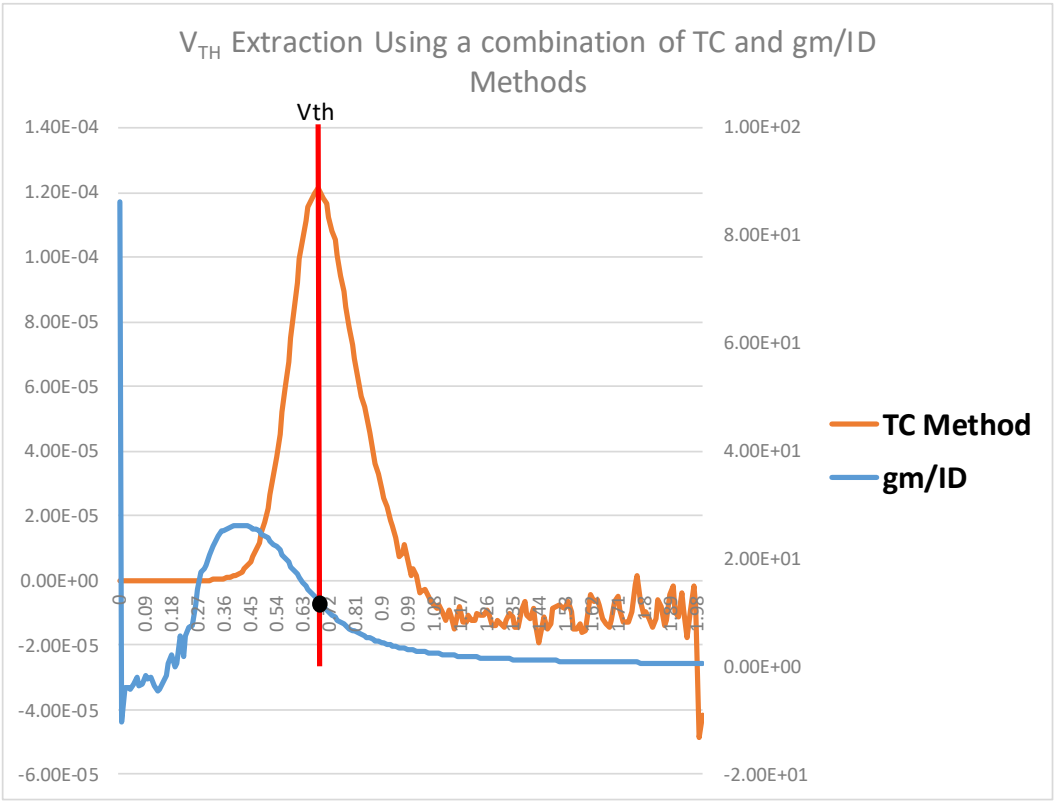


Figure 7.1 : Example of V_{TH} extraction using the combination of the TC and g_m/I_D methods

7.1.2 μ_0 Extraction

After successfully extracting V_{TH}, Low Field Mobility (μ_0) is calculated from a standard rectangular transistor with known W/L, using the transconductance in triode region and derived equations from [26].

$$\mu_0 = \frac{g_m[1 + \theta(V_{GS} - V_{TH})^2]L}{WC_{ox}V_{DS}} \tag{7.1}$$

The mobility reduction factor θ was calculated as follows

$$\theta = \frac{[\frac{I_D}{g_m(V_GS - V_{TH})} - 1]}{(V_{GS} - V_{TH})} \tag{7.2}$$

7.1.3 Width over Length Calculation

With V_{TH} and μ_0 extraction methods defined, the aspect ratio (W/L) of an annular MOSFET is obtained using current equation for triode region. W/L experimental extraction gives an accurate approximation considering that it comes from $I_D - V_{GS}$ device characteristics.

$$I_D \approx \frac{W}{L}\mu_{eff}C_{ox} \cdot (V_{GS} - V_{TH})V_{DS} \tag{7.3}$$

Where

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \tag{7.4}$$

Equation 7.3 is an approximation valid for $V_{DS} \ll 2(V_{GS} - V_{TH})$ [27].

Solving 7.3 for W/L gives

$$\frac{W}{L} = \frac{I_D}{\mu_{eff}C_{ox} \cdot (V_{GS} - V_{TH})V_{DS}} \tag{7.5}$$

Using the same gate length is a disadvantage if we don't have a standard MOSFET

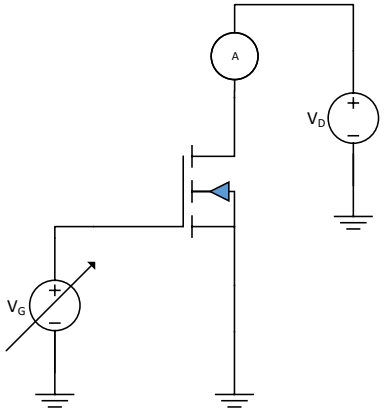


Figure 7.2 : V_{TH}, μ_0 and W/L extraction DUT setup

with this specification to compare with. The proposed solution assumes μ_0 equal for annular and standard transistors. Therefore, GE transistor W/L experimental

extraction is independent of the standard MOSFET gate length. The measurements for V_{TH}, μ_0 and W/L are made with the transistors operating in the triode region.

7.1.3.1 Schwarz-Christoffel Conformal Mapping Transformation

Using the Schwarz-Christoffel conformal mapping transformation a numerical W/L calculation can be obtained where the electrical properties are preserved. Figure 7.3 shows an example of this transformation.

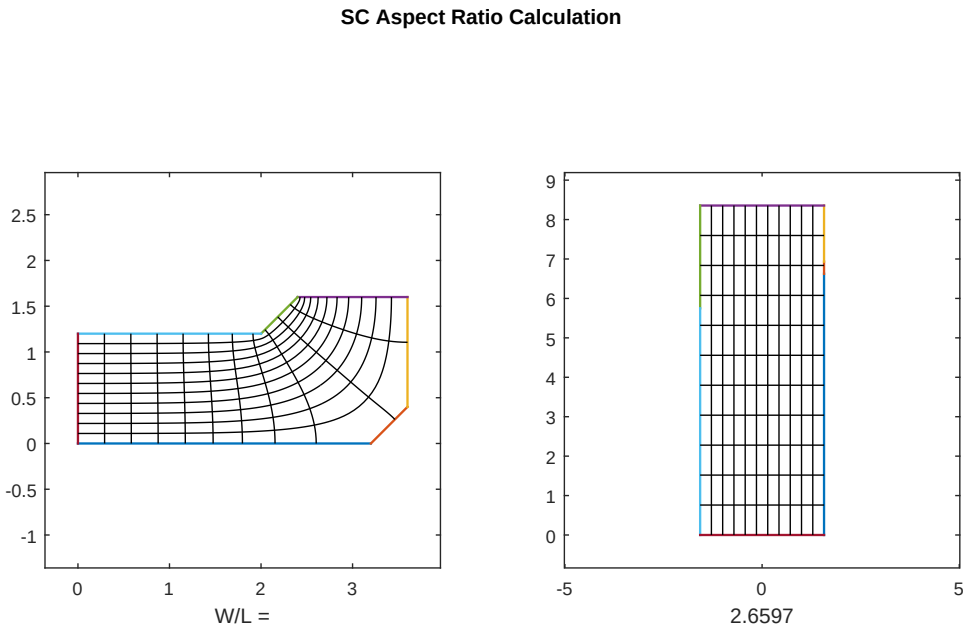


Figure 7.3 : Schwarz-Christoffel Conformal Mapping Transformation

7.1.4 The Body Effect Factor(Gamma-γ)

After successfully obtaining the threshold voltage at equilibrium V_{T0} and specific current (I_{Spec}), a parameter call Slope Factor n (from EKV model) can be used to determine body effect factor (γ) and bulk Fermi potential (ϕ_F) (calculation of n is shown in [28]). The calculation of n needs a pinch-off voltage (V_P) which is equal to

source voltage (V_S) when the normalized forward current $i_f = 3$ in equation 7.6 [12]. $i_f = \frac{I_D}{I_{SPEC}}$, also since i_f is greater than one this guarantee the MOSFET to operate in suturation region, therefore the slope factor will be greater than 1, as showed in equation 7.8.

$$\frac{V_P - V_S}{\phi_t} = \sqrt{1 + i_f} - 2 + ln(\sqrt{1 + i_f} - 1) \tag{7.6}$$

Since $i_f = I_D/I_{Spec}$, then I_D needs to be three times I_{Spec} to meet the requirements for $V_P = V_S$. The circuit in Figure 7.4

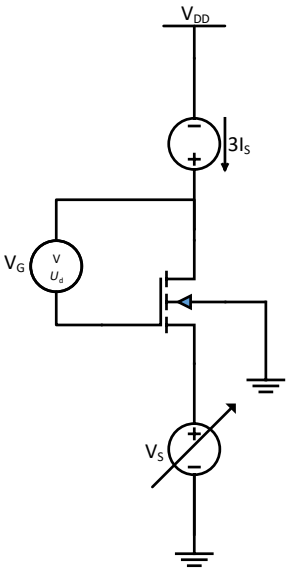


Figure 7.4 : Slope Factor n, Body Effect Factor (γ) and Bulk Fermi Potential (ϕ_F) extraction DUT setup

Equation 7.7 is used to calculate slope factor n from experimental measurements of V_P and V_G.

$$n = \frac{1}{(\frac{dV_P}{dV_G})}. \tag{7.7}$$

The slope factor n can also be expressed as:

$$n = 1 + \frac{\gamma}{(2\sqrt{2\phi_F + V_P})}. \tag{7.8}$$

Solving equation 7.8 for γ and ϕ_F gives

$$\frac{1}{(n-1)^2} = \frac{4V_P}{\gamma^2} + \frac{8\phi_F}{\gamma^2}. \tag{7.9}$$

From 7.9 and using a linear regression between $\frac{1}{(n-1)^2}$ and V_P, γ and $2\phi_F$ can be calculated.

7.2 Circuit Test Board

For test circuits 7.2 and 7.4 the MOSFET (DUT) terminals (Gate, Drain, Source and Bulk) connections need to be independent one from the other, this way sourcing and measuring current or voltage can be made for each terminal. Breadboards and alligator clips are a high noise source, with a Printed Circuit Board (PCB) the signal to noise ratio is reduced due to the internal connections designed in the board layout. This helps the signal by reducing interference from external noises. For PCB trace width calculation equation 7.10 was used.

$$TW = \frac{\left[\frac{I}{(k1 * \Delta T^{k2})}\right]^{\frac{1}{k3}}}{(t * 1.378[mil/oz])} \tag{7.10}$$

Where

- TW = Trace width (mil)
- I = Current (Amps)
- k1 = 0.048, k2 = 0.44 and k3 = 0.725 are constants resulting from curve fitting to the IPC-2221 curves for external layers
- ΔT = Maximum temperature rise (°C)
- t = Conductor thickens (oz)

The current chosen was 1 Amps, being this higher than the normal drain current for a traditional NMOS transistor (not POWER), conductor thickens 1oz and maximum temperature rise of 10°C. Equation 7.10 gives a TW = 11.8 mil. For this PCB TW

= 24 mil was used to reduce the trace impedance. A ground large enough to avoid noise problems was implemented too. Figure 7.5 shows the designed PCB without the components.

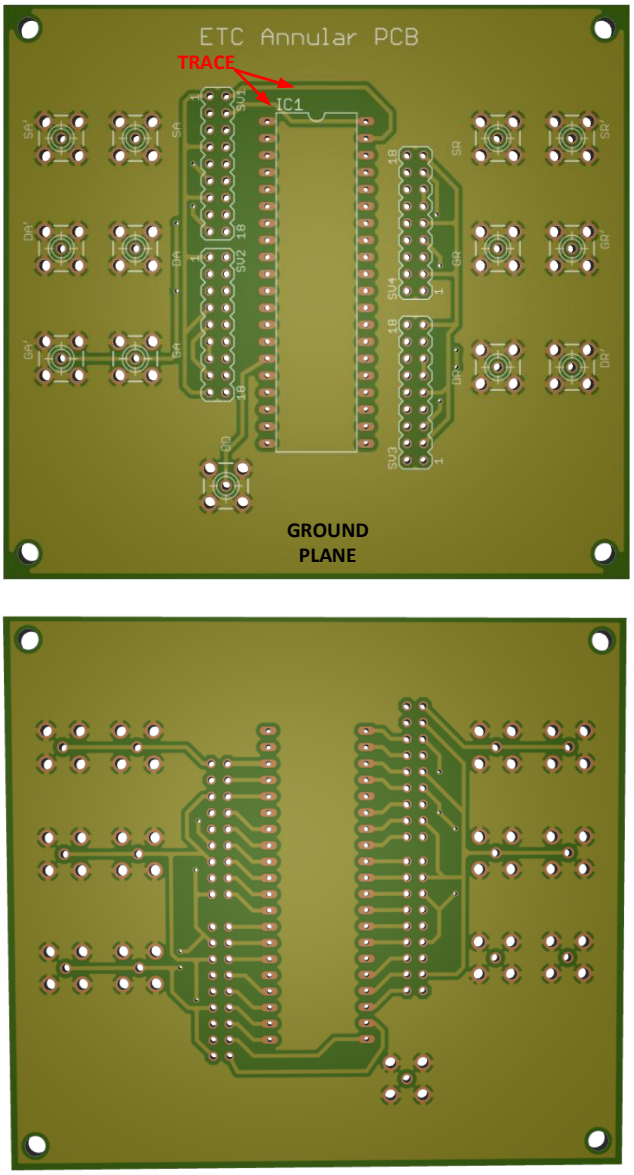


Figure 7.5 : Test Board For DC Parameter Extraction (Top and bottom view)

Figure 7.6 shows the boards with all the electronic materials installed. SMA connectors allow each terminal to interface with a dedicated source-meter channel using SMA to BNC cables, because the provided equipment output/input use a BNC

connection. The pin headers and jumpers are used to test one transistor at the time and a 40 pins socket was soldered to prevent IC chips be exposed to heat.

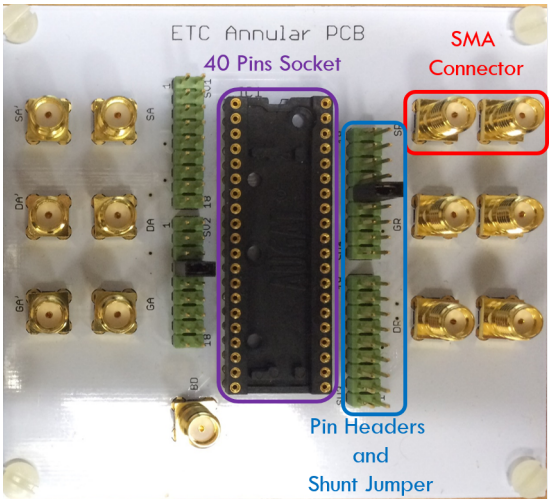


Figure 7.6 : Test Board

Chapter 8
AUTOMATION AND EXPERIMENTAL SETUP

To minimize human interaction the DC parameters extraction and experimental aspect ratio calculation were implemented using LabVIEW^{TM} software. The modification of Schwarz-Christoffel MATLAB® toolbox was used for aspect ratio numerical calculation . Hardware setup and software programs are presented in this chapter.

8.1 Hardware Setup

Figure 8.1 shows the hardware setup with all the used equipments and their connections.

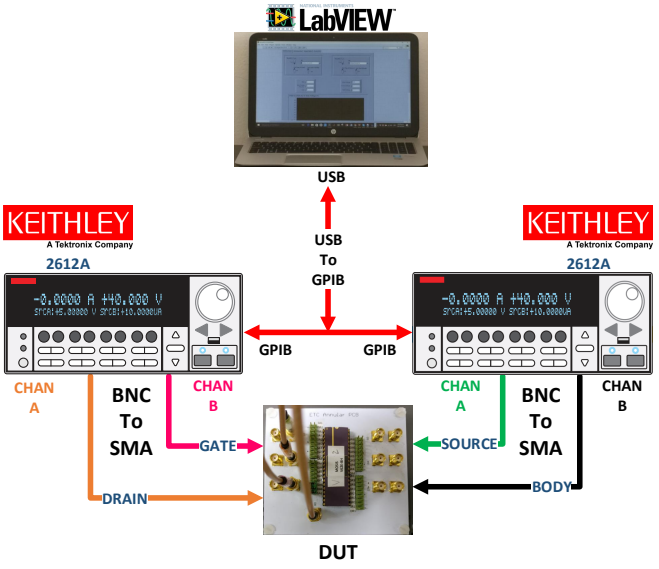


Figure 8.1 : Equipment Setup

8.1.1 Keithley 2612A System SourceMeter®

A Keithley 2612A has two channels (A and B) that can source current (I) or voltage (V). While the Keithley is sourcing a signal, it can be set to measure current and voltage through the same channel. For this work, two Keithleys were needed to bias each DUT terminal, four channels in total. The communication was made using a USB to GPIB adapter with LabVIEW^{TM} to control both Keithleys. Following bias conditions were set as needed:

- Keithley 1, Channel A: Drain current or voltage sourcing, while measuring one or both (I-V).
- Keithley 1, Channel B: Gate current or voltage sourcing, while measuring one or both (I-V).
- Keithley 2, Channel A: Source current or voltage sourcing, while measuring one or both (I-V).
- Keithley 2, Channel B: Body current or voltage sourcing, while measuring one or both (I-V).

The typical error obtained when programming the Keithleys for voltage sourcing was $108\mu V$, which is lower than the resolution specified by the manual guide ($500\mu V$ for a range of 20V).

8.1.2 Portable Personal Computer (Laptop)

Software programs were developed in laptop. LabVIEW^{TM} Virtual Instruments (VI) were designed to automate the experimental DC parameter extraction and calculate DUT's W/L. Measured data from SourceMeters were collected using USB to GPIB adapter. The MATLAB® solution presented in [23], appendix A, was modified to obtain a numerically aspect ratio calculation.

8.1.3 DUT

A chip with annular edgeless and traditional rectangular transistors were designed in AMI $0.6\mu m$ process fabricated by MOSIS. DIP 40 package was provided by the foundry, where 12 transistors were placed. Figure 8.2 shows the pin-out diagram for the chip, with 6 annular (A_x) and 6 rectangular (R_x) MOSFETs. In table 8.1 a description of each transistor is presented.

Table 8.1 : Transistors Sizes and Terminals Positions

ID	W	L	S	D	G	B
A_1	1.8*	1.2	39	40	1	15
A_2	2.4*	1.2	2	3	4	15
A_3	3*	1.2	6	7	8	15
A_4	3.6*	1.2	9	10	11	15
A_5	4.2*	1.2	12	13	14	15
A_6	8.4*	1.2	18	17	16	15
R_1	50	50	20	19	21	15
R_2	50	50	23	22	24	15
R_3	20	0.6	28	27	26	15
R_4	20	0.6	30	29	31	15
R_5	3	0.6	33	32	34	15
R_6	3	0.6	38	37	36	15

* Refers to the drawn inner width. To clarify this Figure 8.3 shows an example of a annular edgeless transistor layout.

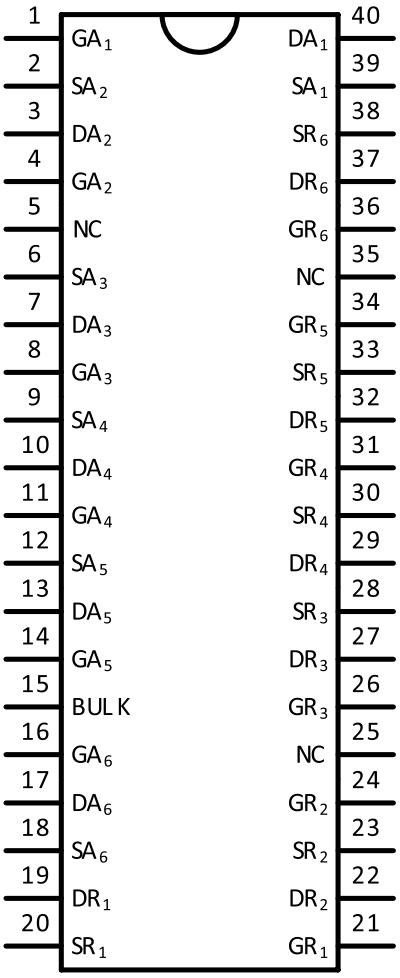
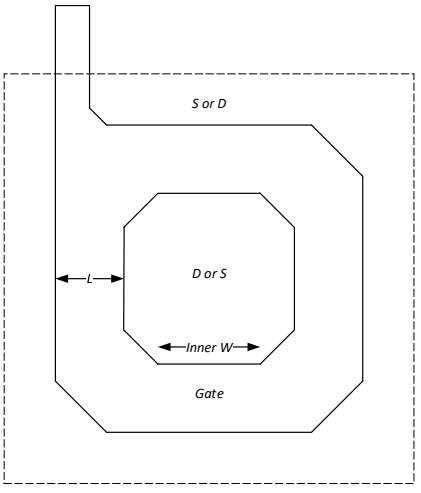


Figure 8.2 : Pin-out Diagram of Designed CHIP



8.2 Test Automation

The DC parameter extraction and W/L experimental calculation were made directly in LabVIEW using MathScripts. After measuring I-V responses, the information was processed with different mathematical blocks. This was to make the data manipulation easier. For a numerically aspect ratio calculation, MATLAB SC toolbox was used. The software solutions are explained next.

8.2.1 LabVIEW Automation

LabVIEW main function is used to link the equipment with the DUT to extract DC level 1 parameters and annular MOSFET's W/L. To achieve this there are four (4) modules in each VI developed:

1. Initialization and configuration
2. I-V measurements
3. Closure
4. Data processing

A general test sequence is presented in Figure 8.5 . The following figures show a example for each module.

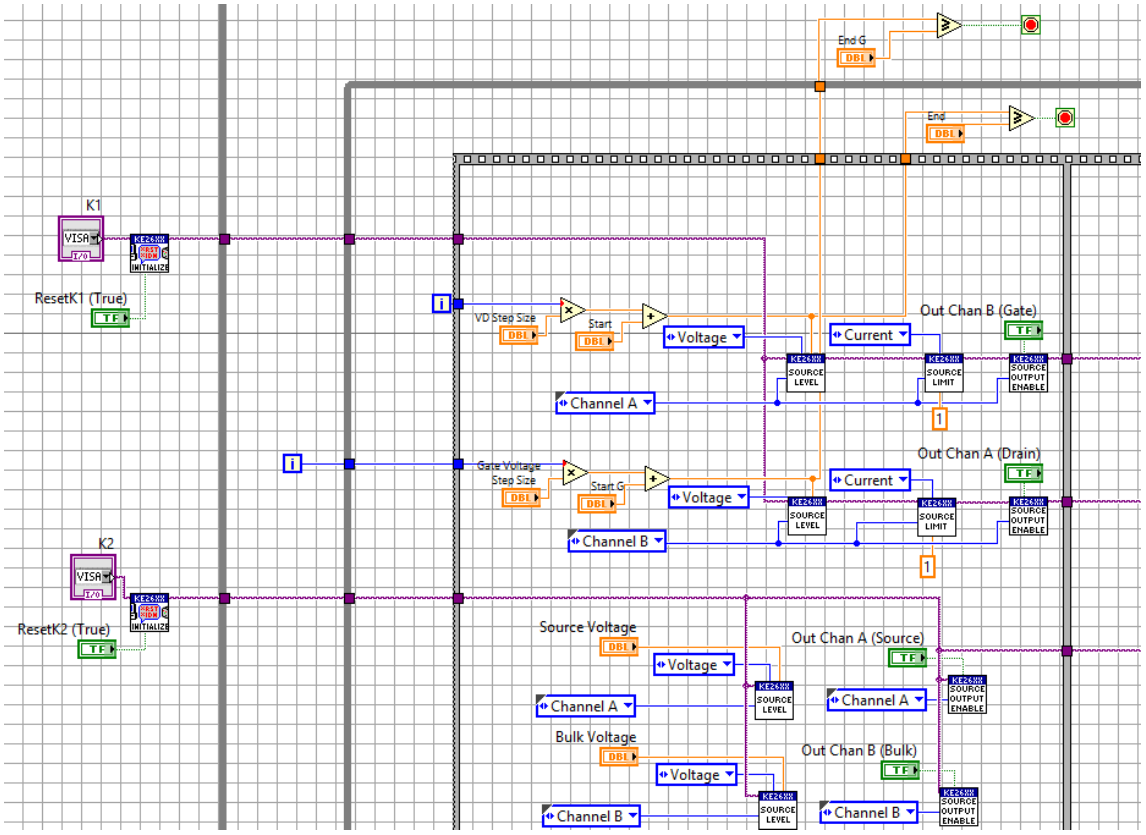


Figure 8.4 : Initialization and Configuration

Figure 8.4 shows the use of LabVIEW drivers provided by the equipment company for the first module. As mention before, each Keithley has two SourceMeter channels, for the test four sourcemeter channels are needed. Therefore, two Keithleys have to be initialized and all the channels need to be configured.

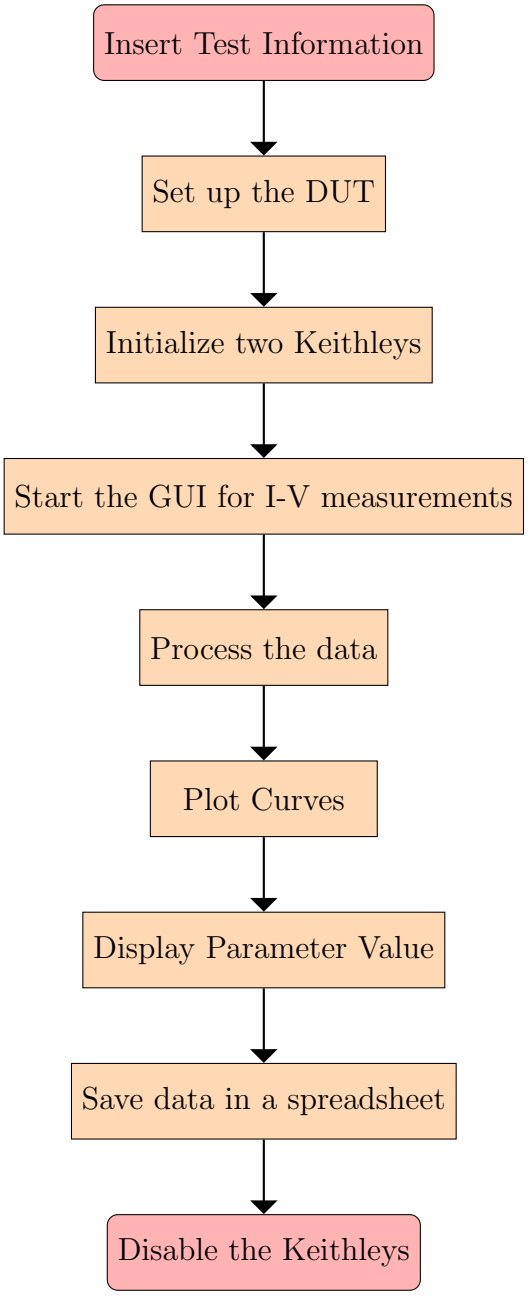


Figure 8.5 : Sequence for LabVIEW test Automation

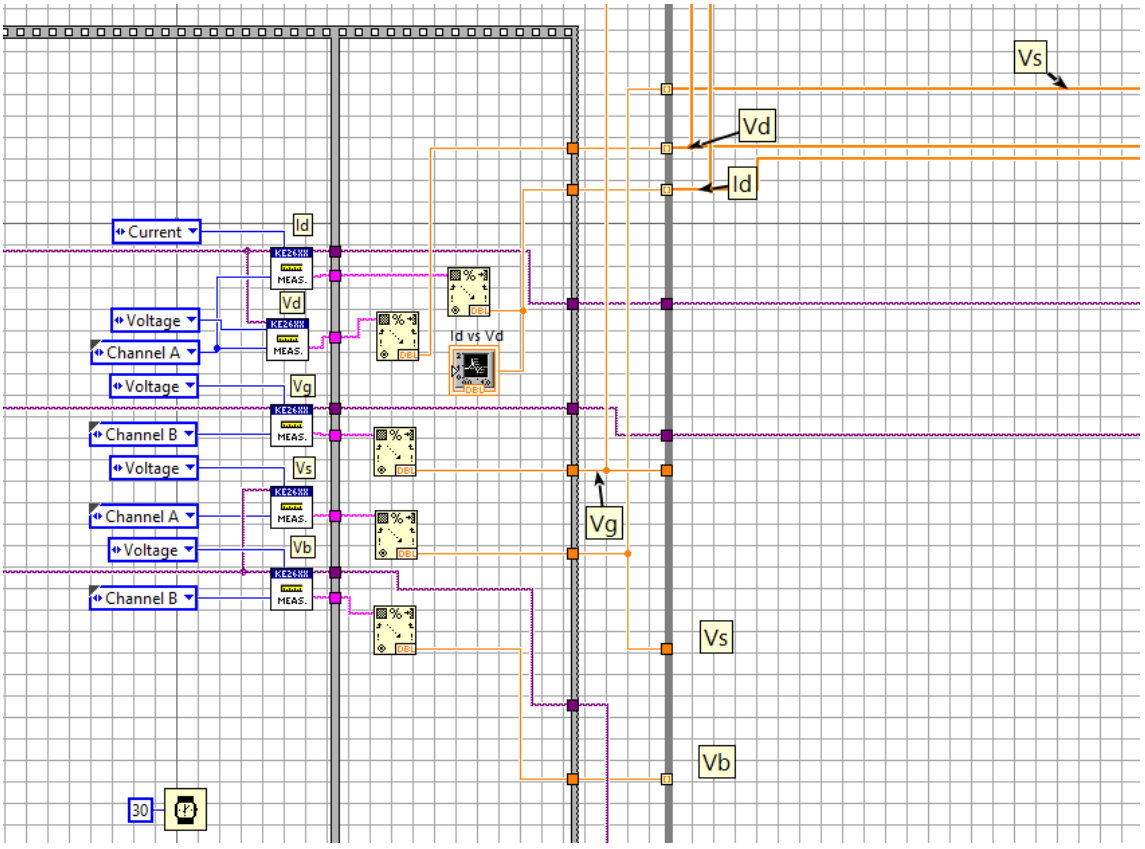


Figure 8.6 : I-V Measurements

Second module has three parts shown in figure 8.6 :

- The measurements are acquired by a measure block.
- Data is converted from string to double-precision, floating-point number.
- Data is stored in LabVIEW by using the indexing tunnel model option. This works in WHILE and FOR loops generating an array of data points.

After collecting all the needed information from each Keithley, the closure part is made by disabling each channel. The module shown in Figure 8.7 ends the communication between LabVIEW and the Keithleys.

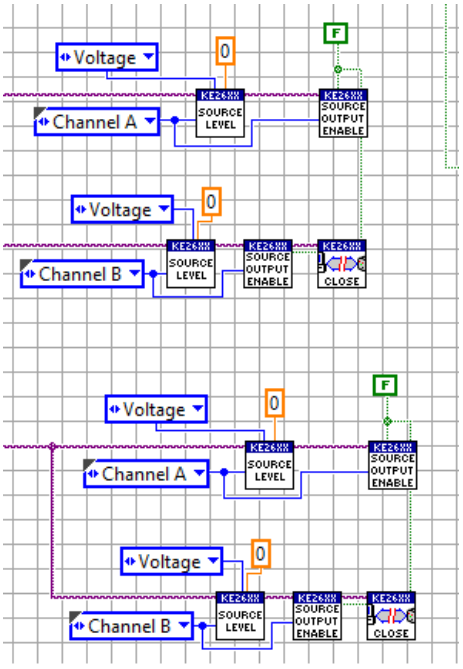


Figure 8.7 : Closure

The closure doesn't mean that the data is lost. By having a flat sequence the VI only stops when the data is processed. Figure 8.8 shows the last module, where the value is calculated and then stored in a spreadsheet.

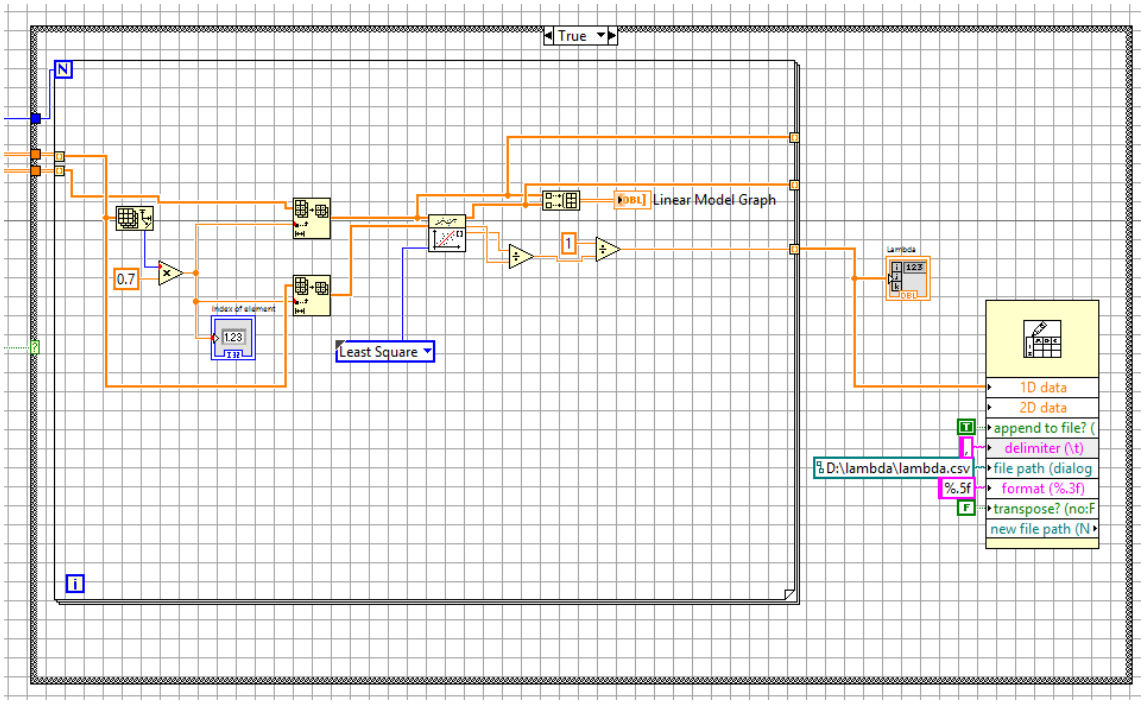


Figure 8.8 : Data Processing and Spreadsheet Generation

8.2.2 Modified Schwarz-Christoffel (SC) MATLAB Toolbox

The conformal mapping, specifically the Schwarz-Christoffel transformation, is used to obtain an accurate approximation of a gate enclosed transistor. Fig 8.9 shows the mapping of an annular edgeless layout to a rectangular one. As shown, real and imaginary parts of the mapping satisfy Laplace's equation, so the equipotential and field lines are preserved [29]. This is performed by the modified MATLAB toolbox. An annular edgeless transistor is created by defining all the complex points for the geometry with polygon function.

p=polygon([0 3.3 4.35+1.05i 4.35+4.95i 3.3+6i -0.6+6i -1.65+4.95i -1.65+1.65i -0.45+1.65i -0.45+4.35i 4.8i 2.7+4.8i 3.15+4.35i 3.15+1.65i 2.7+1.2i 1.2i]);

The function rectmap(P, CORNER) constructs a Schwarz-Christoffel rectangle map object for the polygon P. CORNER is a four-vector containing the indices of the vertices that are the images of the rectangle's corners. These indices should be

specified in counterclockwise order, and the first two should be the endpoints of a long side of the rectangle. An example of this function is presented next:

f=rectmap(p,[1 4 5 7]); p is the polygon and [numbers] are the four selected corners to do the transformation.

Then by using a specifically designed plot function the polygon and mapped rectangle are presented, see Figure 8.9 . The plot function calls an rplot function which is used to calculate the W/L using the Schwarz-Christoffel transformation [23].

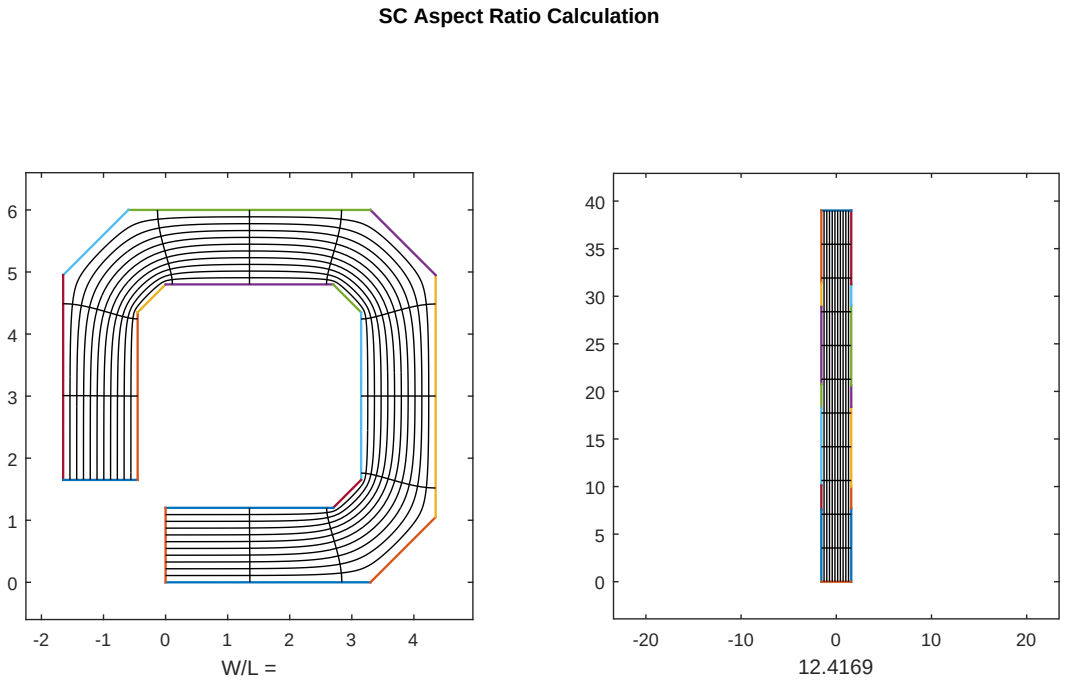


Figure 8.9 : Aspect Ratio Calculation Example Using the Modified SC MATLAB Toolbox

Chapter 9
RESULTS

This chapter discusses the procedure for automated experimental aspect ratio extraction, DC level 1 parameter calculation and simulation of modified SPICE model for annular MOSFETs. Also, the validations for mentioned procedures along with the alternative aspect ratio calculation are presented. A view of the developed layout and a example of an annular MOSFET is shown in Figure 9.1

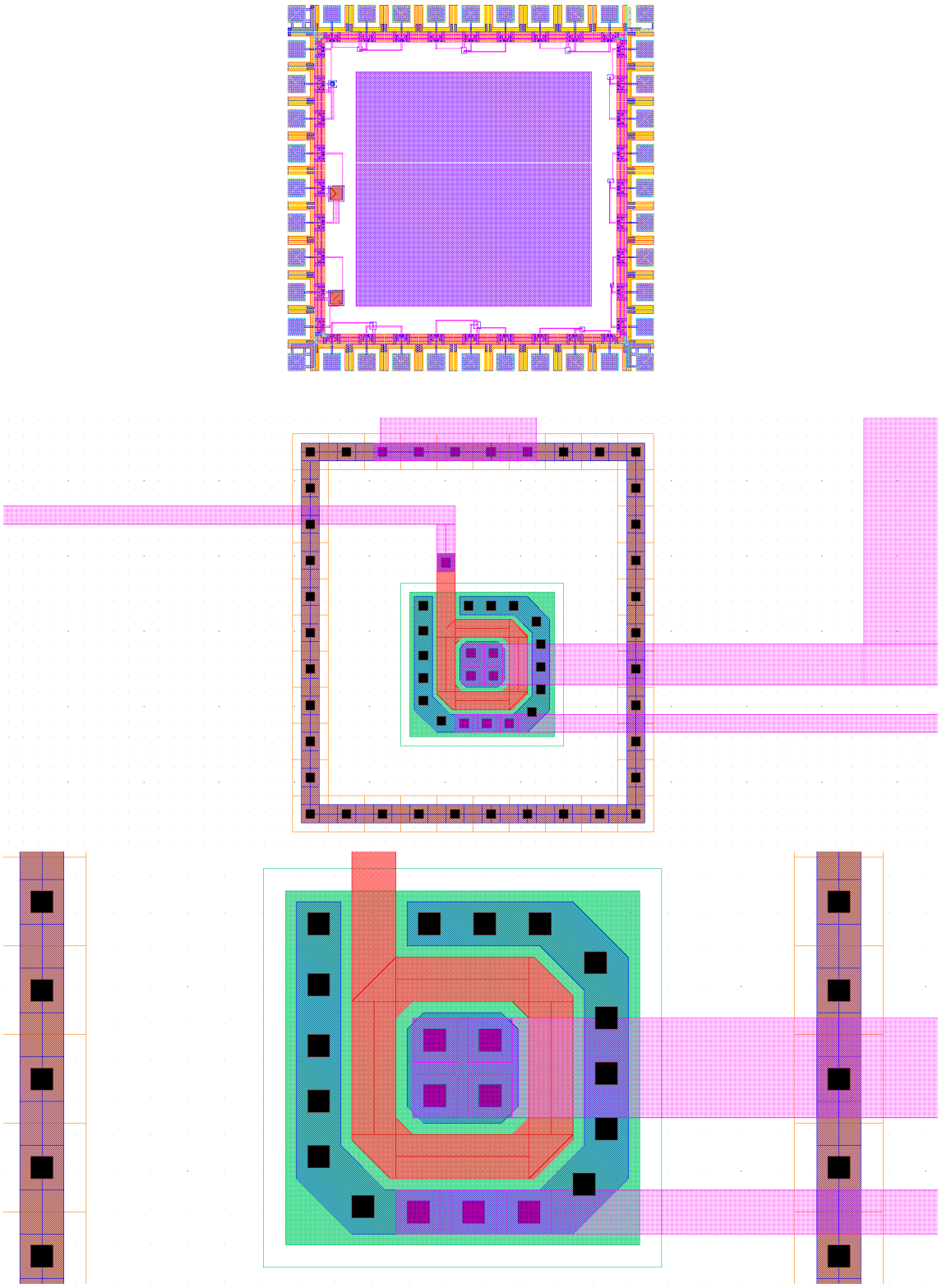


Figure 9.1 : Parameter Extraction Setup

9.1 DC level 1 Parameters and Aspect ratio (W/L) Extraction

The first parameter that has to be calculated for any of the extraction is the threshold voltage, considering that this parameter is essential to obtain the specific current (used to calculate the body factor effect), low field mobility and aspect ratio.

9.1.1 Threshold Voltage V_{TH}

Figure 9.2 shows the graphical user interface (GUI) setup developed for parameter extraction in triode operation region and the measured drain current curve. The Keithley SourceMeters® are initialized and configured. The test information is inserted as follows:

- Drain voltage of 50mV to guarantee triode region operation.
- Gate voltage sweep from 0 to 1.5 Volts (V) with steps of 0.01V.
- Number of times the test is going to be performed.

In Figure 9.3 an example of extracted V_{TH} of a standard MOSFET (W/L = $50\mu m/50\mu m$) is shown. This was made with the $\delta g_m/\mathrm{I}_D$ method, where the V_{TH} value is denoted by the white dot, which is the voltage where $\delta g_m/\mathrm{I}_D$ is approximately 50% of its maximum value. This extraction was also used to obtain the V_{T0} presented in Figure 9.4 by setting the drain voltage at 13mV [12].

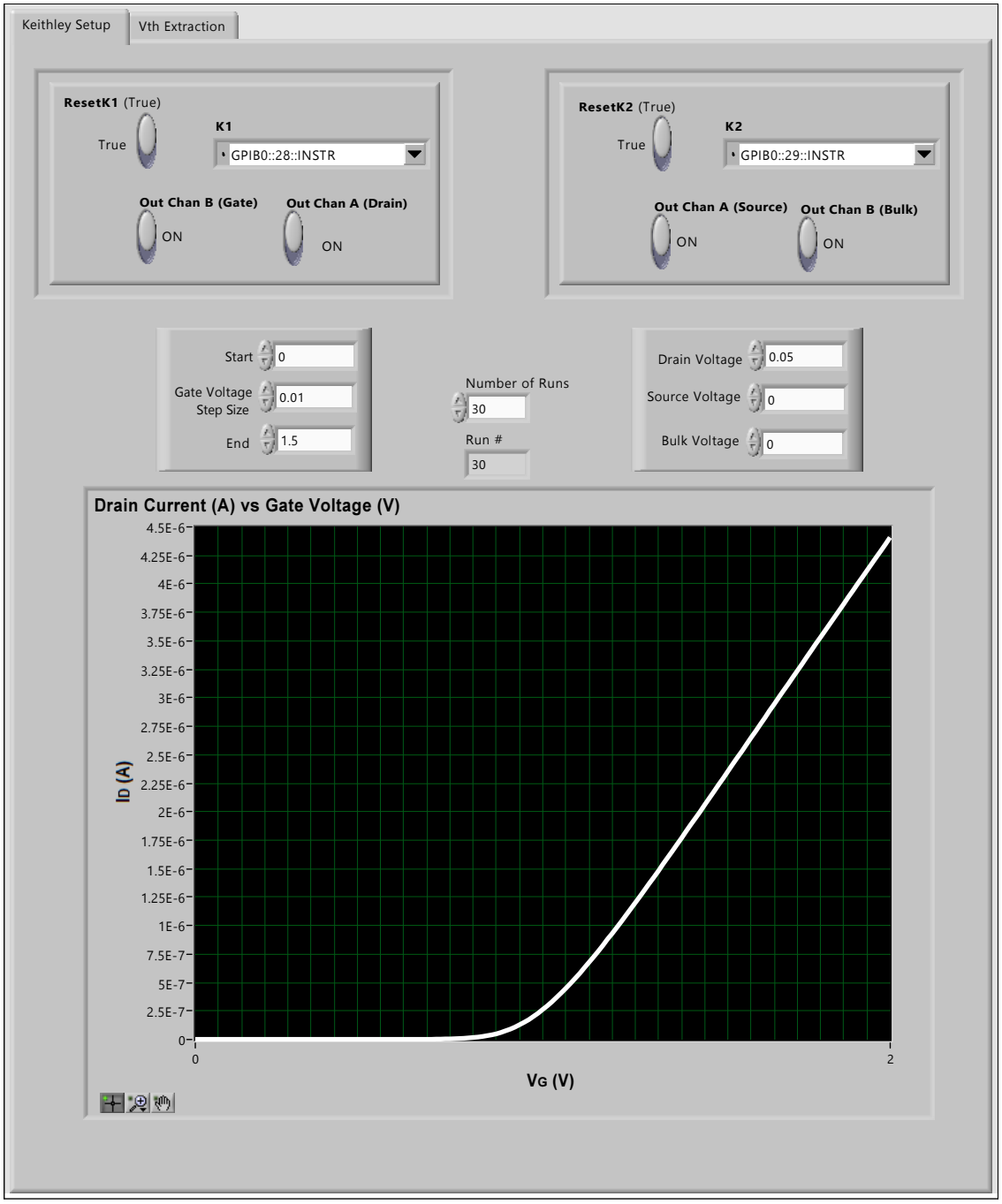


Figure 9.2 : Parameter Extraction Setup

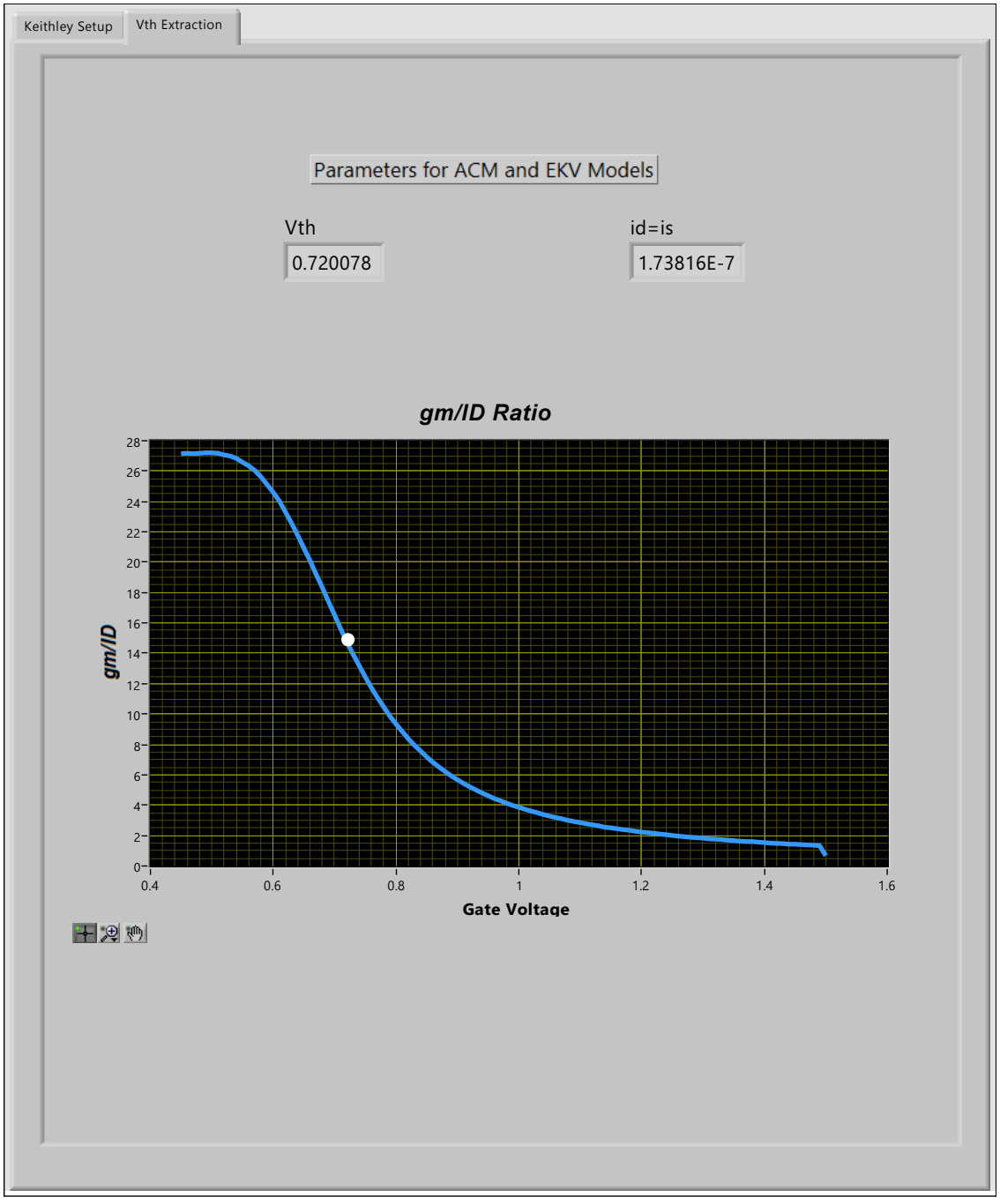


Figure 9.3 : Extracted V_{TH} for a standard MOSFET (W/L = $50\mu m/50\mu m$)

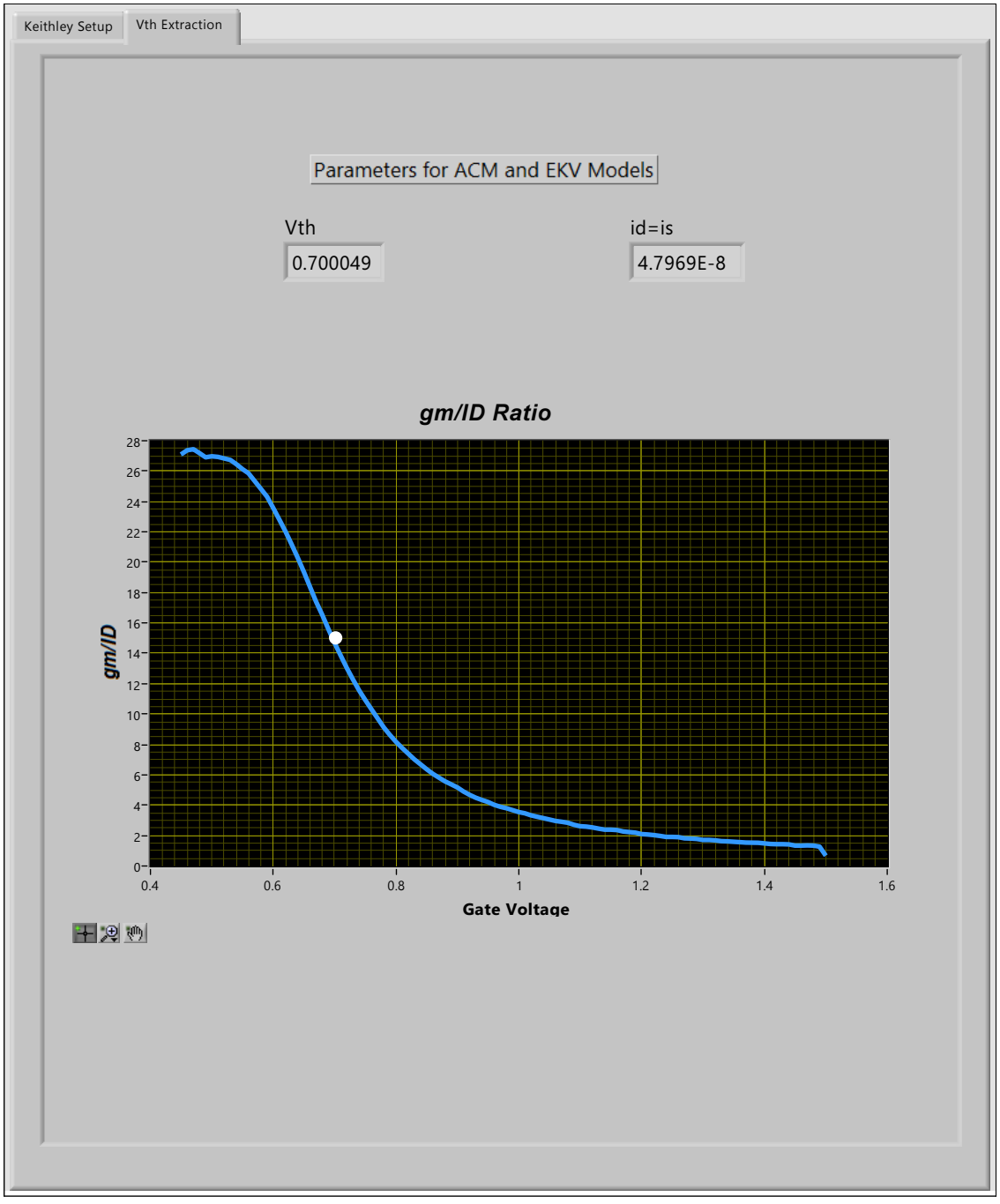


Figure 9.4 : Extracted V_{T0} for a standard MOSFET (W/L = $50\mu m/50\mu m$)

9.1.2 Low Field Mobility μ_0

The test setup in 9.2 is used with a change in VG sweep (0-3 V) with the same step size for μ_0 calculation. Figure 9.5 shows three curves.

1. Theta (effective mobility reduction factor).
2. Low field mobility.
3. MOSFET effective mobility.

As is shown in Equations 7.1, 7.2 and 7.4, V_{TH} is an important parameter for their calculations. By knowing V_{TH} value the equations are evaluated at a V_{GS} greater than the threshold voltage. This is to avoid having a θ parameter too big due to a $V_{GS} - V_{TH}$ value. The μ_0 was later validated by comparing it with the one provided by the foundry.

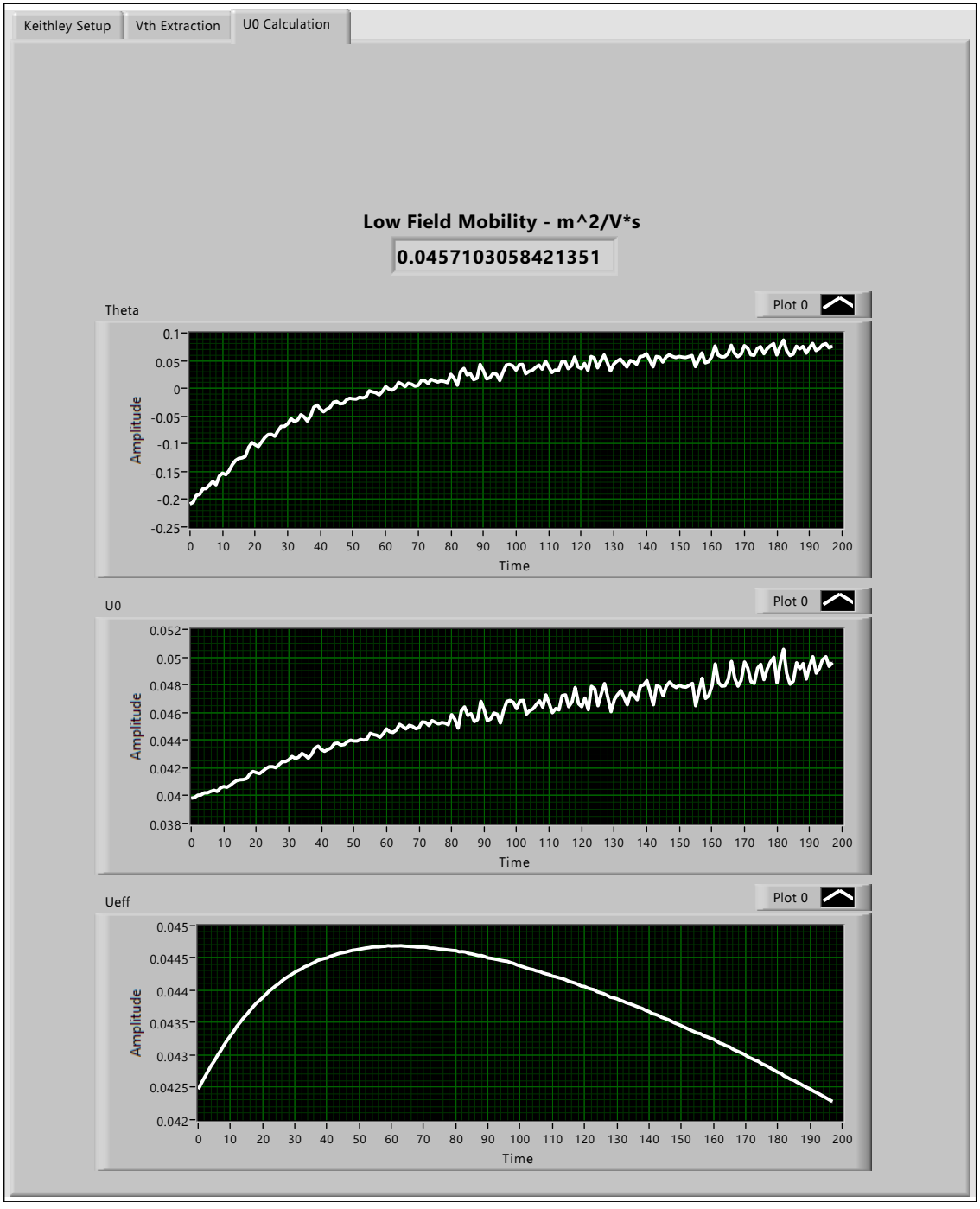


Figure 9.5 : Extracted μ_0 for a standard MOSFET (W/L = $50\mu m/50\mu m$)

9.1.3 Width over Length Calculation

As mentioned in 7.1.3 the W/L extraction is performed in triode region. Figure 9.6 shows the extracted value for a standard MOSFET as a proof of concept. The curve shape is due to the values of $V_{GS} - V_{TH}$ and I_D in equation 7.5.

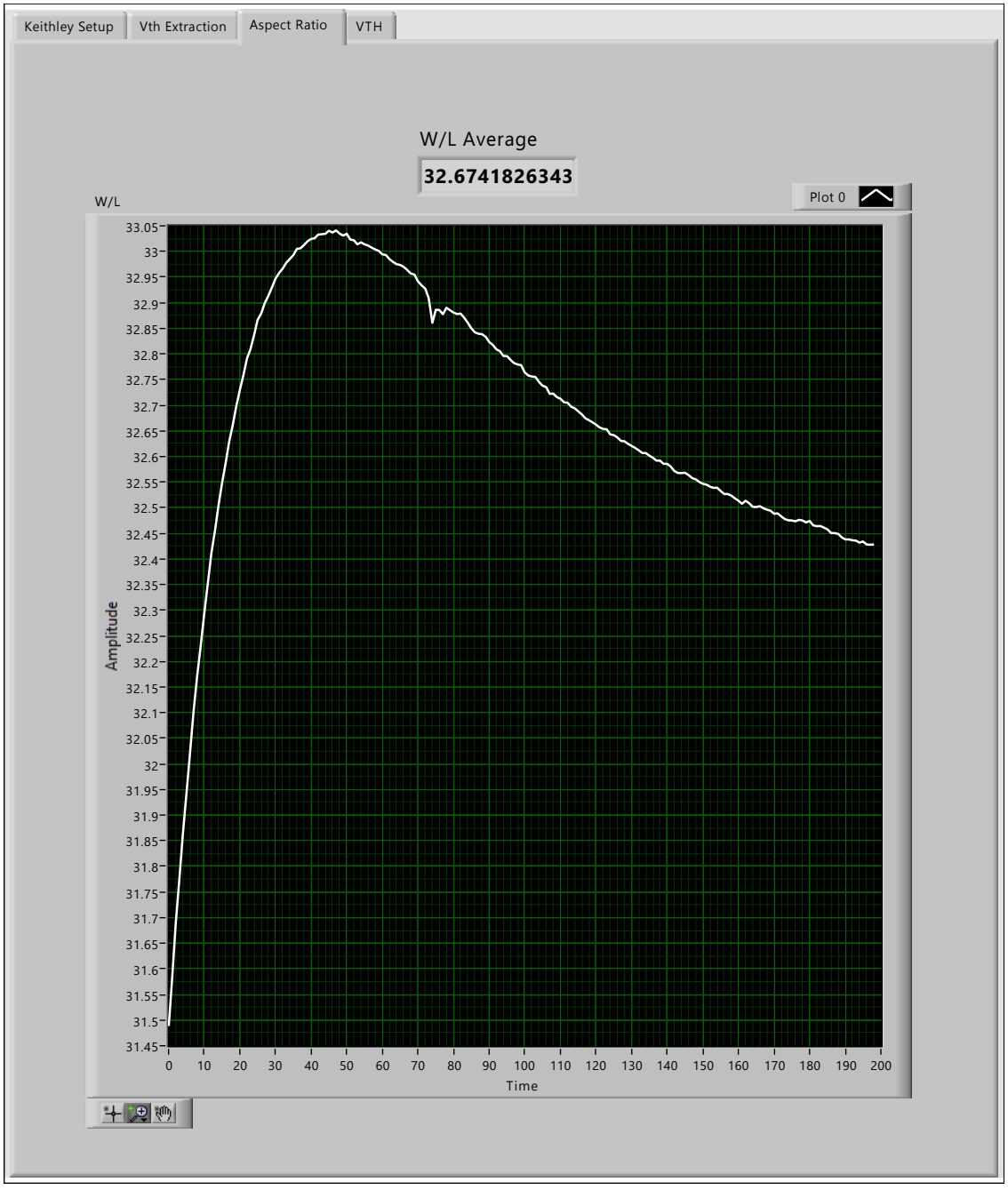


Figure 9.6 : Extracted W/L for a standard MOSFET (W/L = $20\mu m/0.6\mu m$)

9.1.4 The Body Effect Factor γ

In 7.1.4 the used circuit setup shows a source voltage (V_S) sweep with a constant drain current (I_D) while the gate voltage is being measured. Figure 9.7 this setup is shown with the V_G plot.

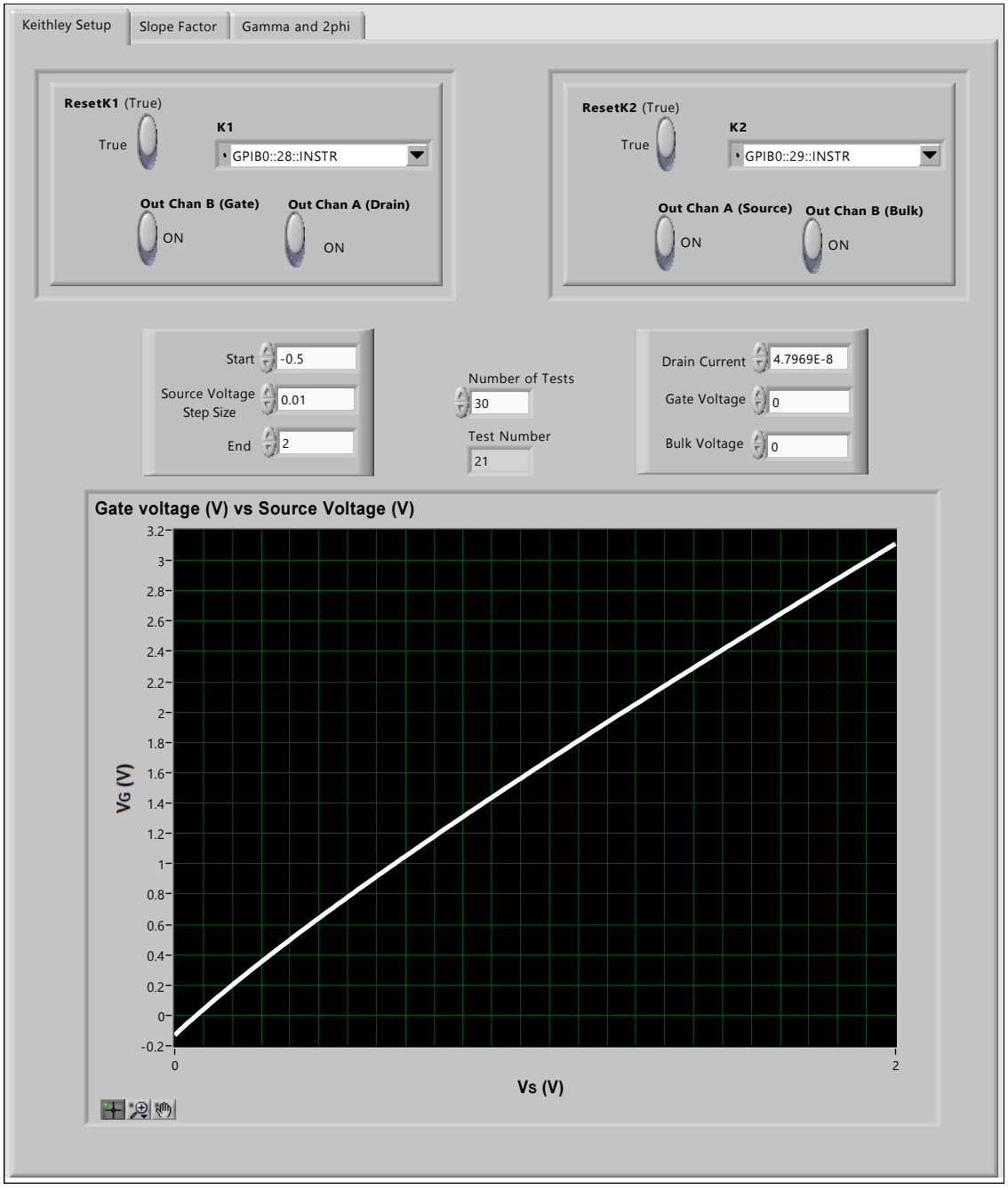


Figure 9.7 : γ Extraction Setup

In Figures 9.8 and 9.9 the Slope Factor n and γ are presented. The n value is the average of calculated points in the curve.

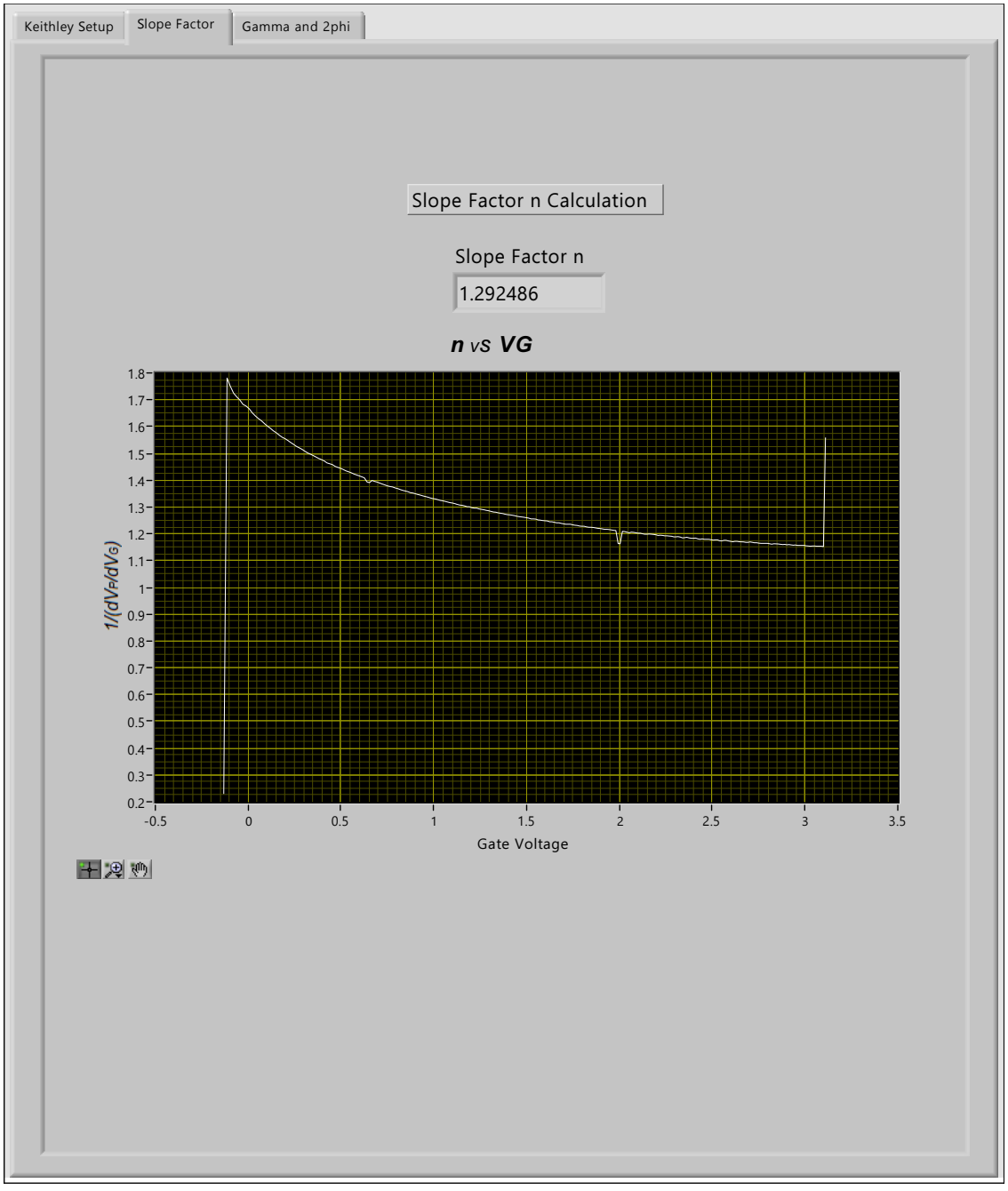


Figure 9.8 : Extracted Slope Factor n for a standard MOSFET (W/L = $50\mu m/50\mu m$)

For γ, white plot shows the calculated values from the experimental measurements and red plot shows the fitted values using a linear regression [12].

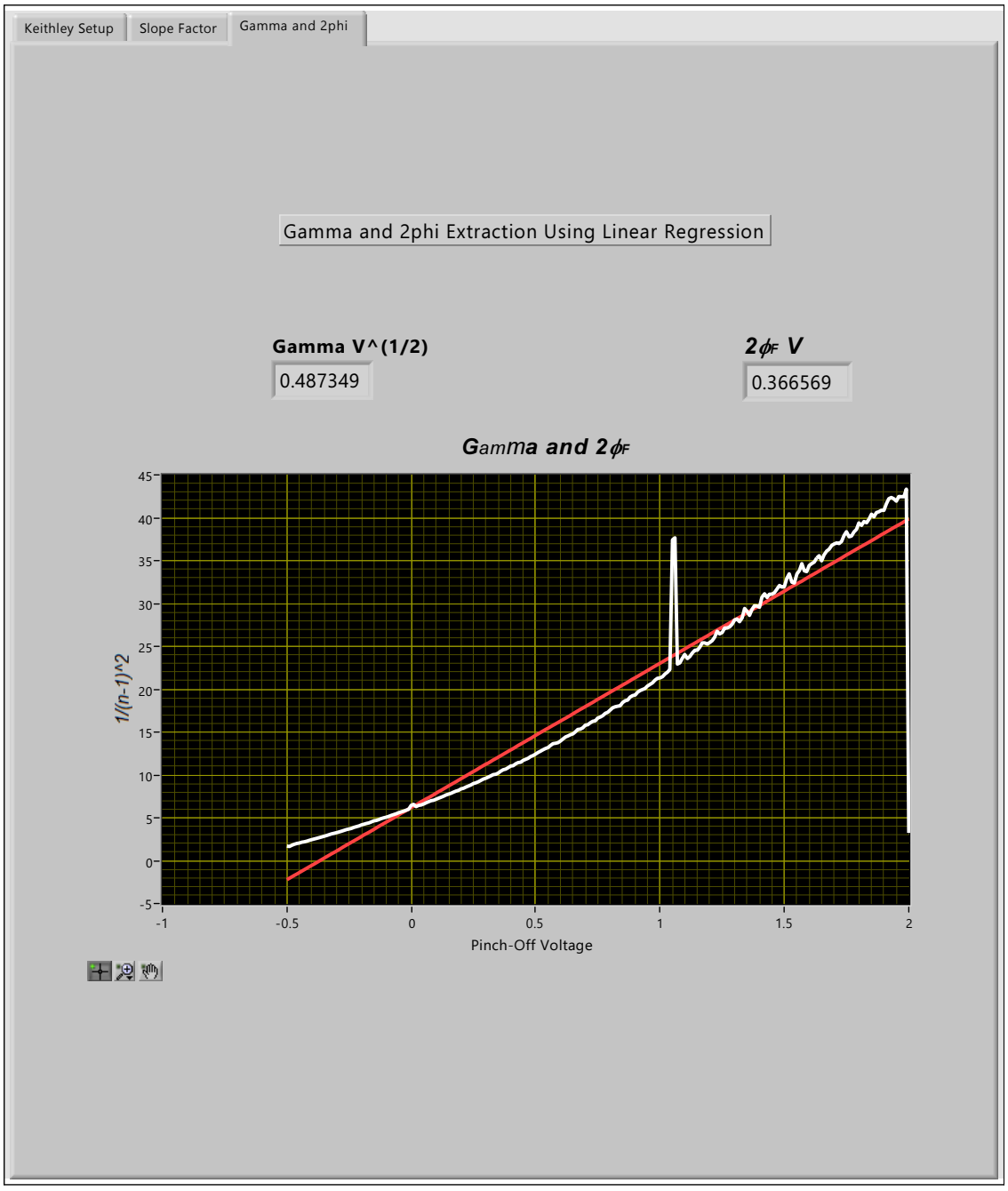


Figure 9.9 : Extracted γ for a standard MOSFET (W/L = $50\mu m/50\mu m$)

9.1.5 I_D vs V_D at Different V_G Curve Extraction

The setup for I_D vs V_D at different V_G curve extraction is shown in Figure 9.10 . The test information for this curve extraction is:

- Drain voltage sweep 0 to 3 Volts with 0.01 steps
- Gate voltage sweep 1 to 3 Volts With 0.2 steps

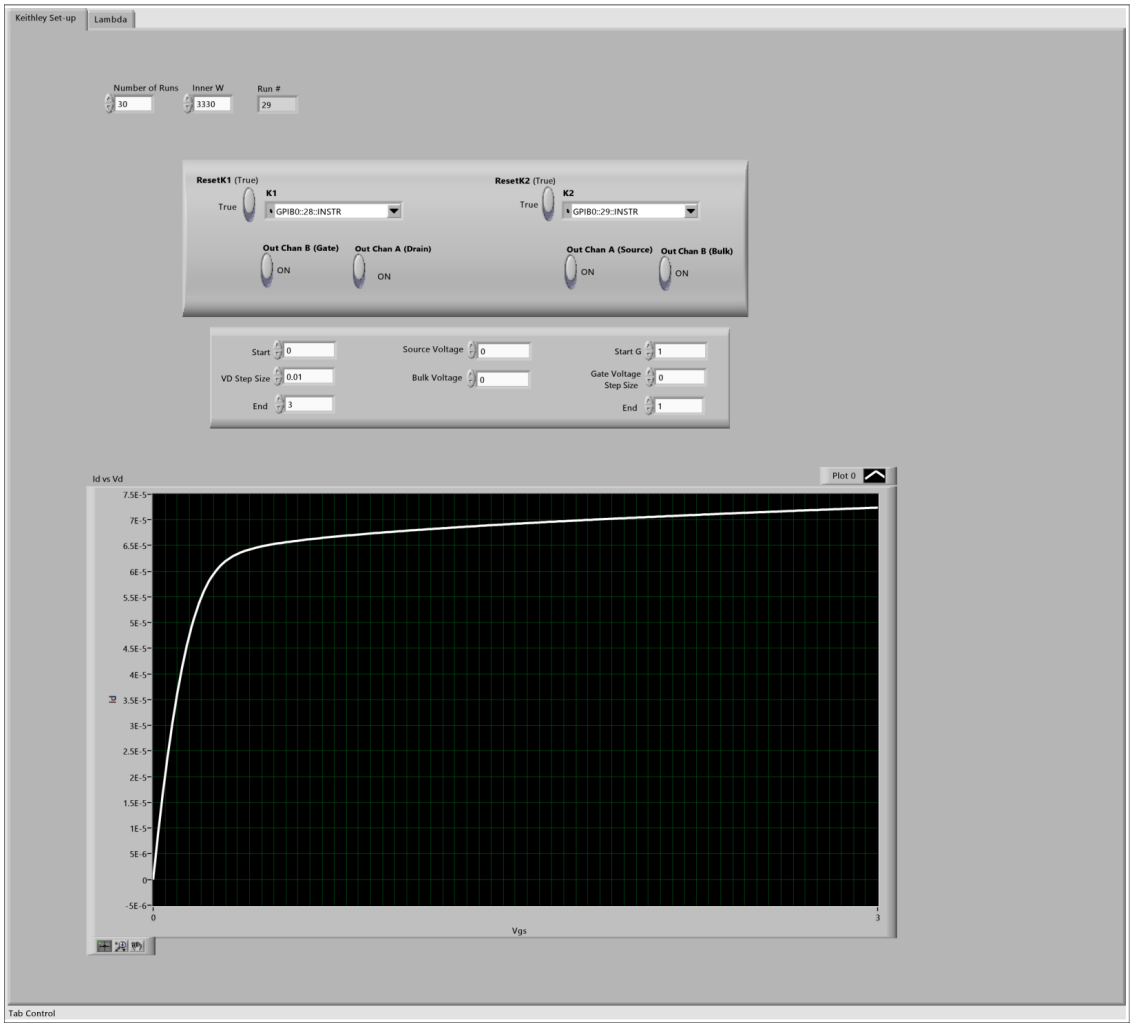


Figure 9.10 : I_D vs V_D at Different V_G Curve Extraction Setup

For repeatability test the gate voltage was set at 1 Volt and the test was run 30 times for the same device as shown in Figure 9.11 . This test was also used for the modified SPICE model validation.

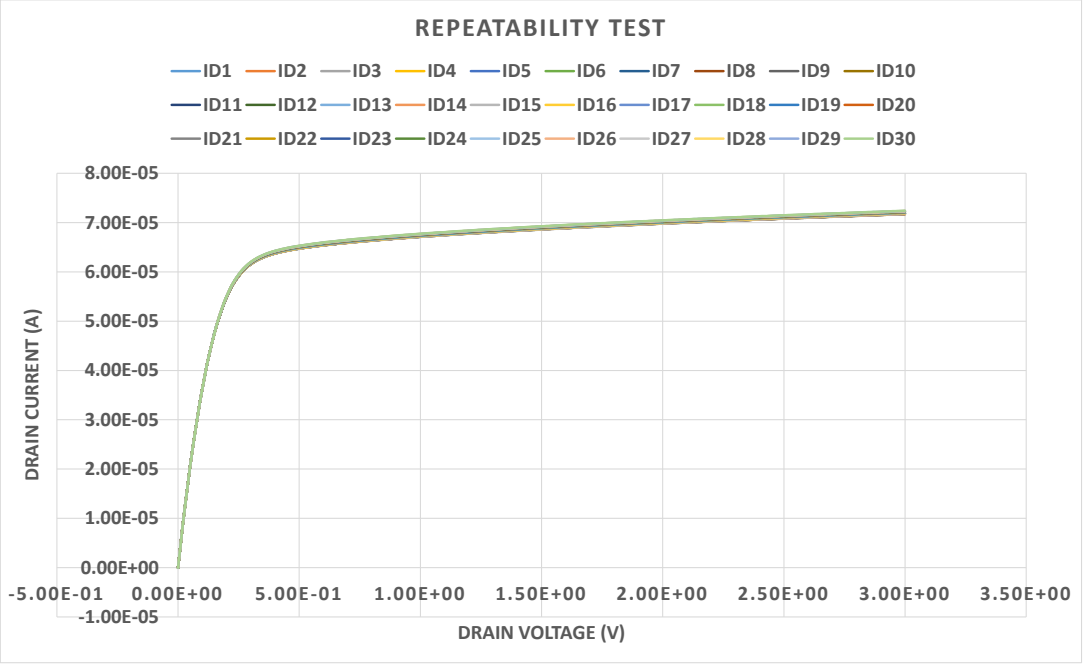


Figure 9.11 : Repeatability Test

As it can be seen, the 30 tests results were almost identical.

9.2 Validation

The validations for DC parameters, proposed W/L experimental extraction, Modified SPICE model for gate enclosed MOSFET simulation and the alternative W/L calculation are presented in next subsections. The acceptable error used to validate percentage errors and differences comparisons was 10%.

9.2.1 DC level 1 Parameters

Threshold voltage (V_{TH}), low field mobility (μ_0), body effect Factor(Gamma-γ), where validated by comparing them with those provided by the foundry (MOSIS) with the requested data for run v62e, see appendix A.

In Table 7.2 a maximum error of 0.010% for V_{TH} and 0.535% for γ is presented, these small differences are used as a validation, considering an error bellow 1%. For

μ_0 where the maximum error was 5.039% as shown in Table 9.2 , which is also an acceptable error (below 10%).

Table 9.1 : Threshold Voltage V_{TH} and Gamma-$\gamma(V^{0.5})$

V_{TH}			
W/L	MOSIS	Automated Extraction (Average of 30 Samples)	Error
$50\mu m/50\mu m$	0.72	0.720072	0.010%
$20\mu m/0.6\mu m$	0.7	0.700054	0.008%
γ			
$50\mu m/50\mu m$	0.47	0.467484333	0.535%

Table 9.2 : Low Field Mobility $\mu_0(\frac{m^2}{V \cdot s})$

MOSIS	W/L	Automated Extraction (Average of 30 Samples)	Error
0.045116292	$50\mu m/50\mu m$	0.042999745	4.691%
	$20\mu m/0.6\mu m$	0.042843005	5.039%

9.2.2 Aspect Ratio (W/L) Extraction

9.2.2.1 Standard MOSFET

Using a set of standard MOSFETs the proposed W/L experimental extraction was tested as a proof of concept. This also helps to validate the μ_0, θ and μ_{eff} calculations. A maximum error 9.819% is obtained with the smaller transistor, because Length and Width variations are more noticeable when scaling down MOSFET size. This is shown in Table 9.3

Table 9.3 : Standard MOSFETs

Drawn W/L	Ideal Aspect Ratio	Experimental Calculation	Percentage Error
$50\mu m/50\mu m$	1	1.029464743	2.946%
$20\mu m/0.6\mu m$	33.3	34.42445082	3.377%
$7.8\mu m/1.2\mu m$	6.5	6.456807864	0.664%
$6.6\mu m/1.2\mu m$	5.5	5.629206547	2.349%
$5.4\mu m/1.2\mu m$	4.5	4.424032103	1.688%
$4.2\mu m/1.2\mu m$	3.5	3.156328468	9.819%

9.2.2.2 Annular MOSFET

The proposed W/L experimental extraction was validated with [18] and [6] methods, by a similar approach of using I_D response for standard and gate enclosed (GE) transistors. The proposed W/L extraction also has the assumption of same μ_0 for standard and gate enclosed MOSFET. Even though the proposed solution has a starting point similar to the previous mentioned methods, there are some differences:

- The Aspect ratio calculation is not made by comparing standard and GE MOSFETs.
- A gate length independent standard transistor is used to extract the low field mobility value.

The second difference can be seen as a advantage by not having to include a standard MOSFET with same length as the GE to calculate the W/L.

Table 9.4 : Annular MOSFET Aspect Ratio Extraction. g_m Ratio [18] and Proposed Automated Extraction

Drawn Inner W and L	g_m Ratio (Average of 30 Samples)	Automated Extraction (Average of 30 Samples)	Percentage Difference
$1.2\mu m$ and $1.2\mu m$	7.897002219	8.422757654	6.443%
$2.7\mu m$ and $1.2\mu m$	14.48994568	14.91082142	2.863%
$7.5\mu m$ and $1.2\mu m$	31.83949757	30.8897649	3.028%

Table 9.4 shows the percentage difference of experimental extracted W/L for three annular MOSFETs, using the proposed method and [18]. An percentage difference bellow 10% can be consider acceptable.

9.2.3 Modified SPICE Model

The simulations for the modified SPICE model was made using the industry standard software Cadence® Virtuoso® for Analog Design Environment (EDA). Three annular devices were simulated and their responses were compared to the experimental extracted curves using the rms error as a quality index.

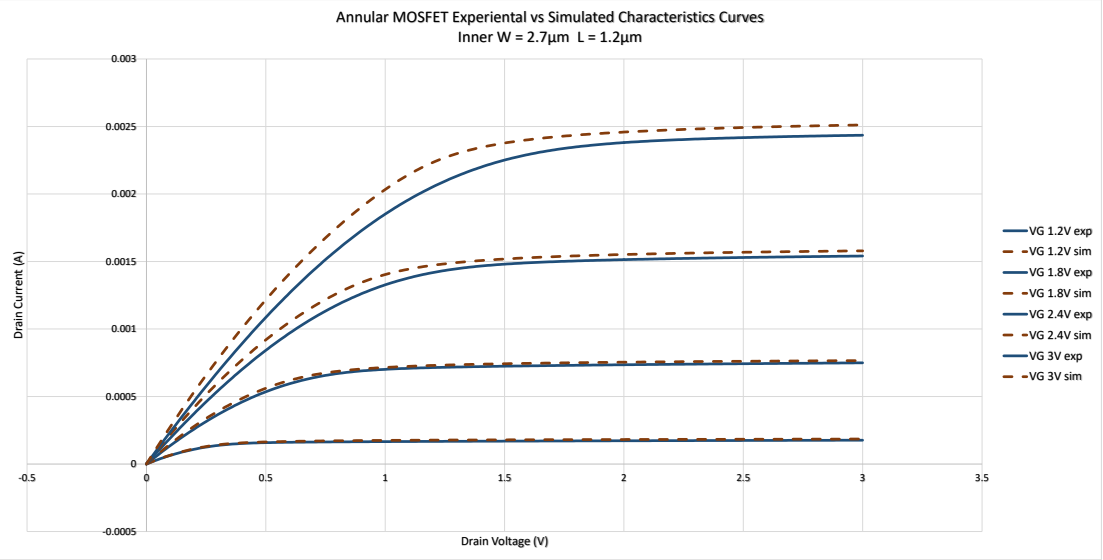


Figure 9.12 : Experimental and Simulated $I_D vs V_D$ at Different V_G Curves - 301 measured values (Inner W $2.7\mu m$ L $1.2\mu m$)

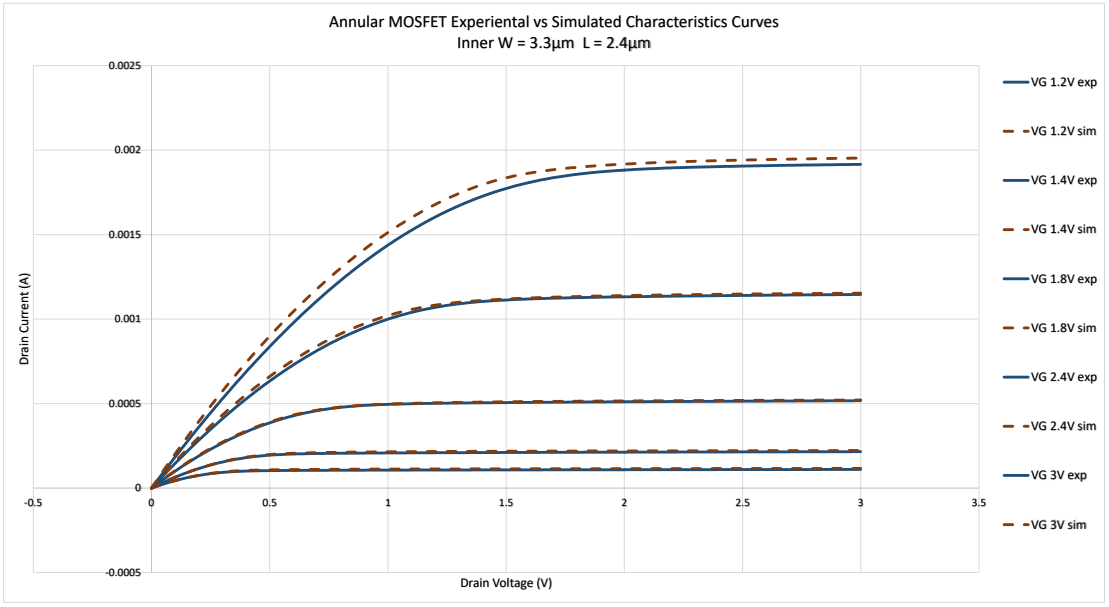


Figure 9.13 : Experimental and Simulated $I_D vs V_D$ at Different V_G Curves - 301 measured values (Inner W 3.3μm L 2.4μm)

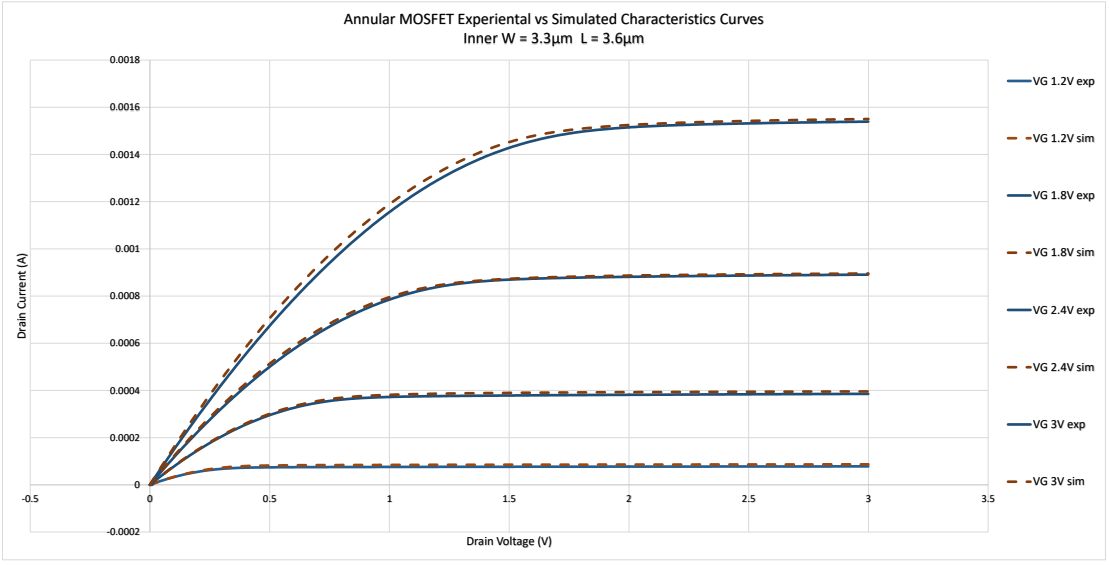


Figure 9.14 : Experimental and Simulated $I_D vs V_D$ at Different V_G Curves - 301 measured values (Inner W 3.3μm L 3.6μm)

Figures 9.12 , 9.13 and 9.12 show the graphical comparison between experimental and simulated measurements. The extracted W/L for each compared device is shown in Table 9.5 .

Table 9.5 : Automated Experimental Extracted W/L

Inner W = 2.7μm L = 1.2μm	Inner W = 3.3μm L = 2.4μm	Inner W = 3.3μm L = 3.6μm
14.615502	9.8859543	7.5831493
14.673916	9.9089977	7.5835258
14.681387	9.9529699	7.5836537
14.835249	9.9540587	7.583793
14.839858	9.9659597	7.5839381
14.84152	9.9682769	7.5844686
14.843517	9.9685361	7.5852824
14.843779	9.9719675	7.5859934
14.844094	9.9749697	7.5901225
14.845221	9.9758568	7.5913774
14.847307	9.9766701	7.5917445
14.851084	9.9769026	7.5933976
14.851205	9.9803584	7.5999483
14.878139	9.9822157	7.601777
14.946958	9.9842987	7.6041492
14.95177	9.9863569	7.6044929
14.959003	9.9902977	7.6058598
14.959072	10.070324	7.6069038
14.964197	10.07753	7.6087012
14.965293	10.081802	7.6095587
14.96793	10.085327	7.6095631
14.969726	10.096682	7.6097782
14.974647	10.098683	7.6114957
14.976956	10.107578	7.6141526
15.155516	10.18227	7.6148504
15.242626	10.186219	7.6149632
15.266709	10.186258	7.6159554
Average		
14.910821	10.021382	7.598985

V_{T0} was set by averaging 90 extracted values 30 for each annular MOSFET, see Table 9.6 . After extracting and comparing the DC level 1 parameters with the provided SPICE model, V_{T0} was the only parameter that could be changed. W/L values were inserted in Cadence® Virtuoso® for each simulation.

Table 9.6 : Extracted V_{T0}

Inner W and L		
2.7μm and 1.2μm	3.3μm and /2.4μm	3.3μm and /3.6μm
0.690025	0.720012	0.710008
0.690024	0.72001	0.670038
0.700011	0.720016	0.690034
0.679994	0.720013	0.710018
0.690027	0.700007	0.710014
0.700007	0.720012	0.710007
0.700008	0.720004	0.710015
0.700011	0.709988	0.710013
0.700009	0.720008	0.710013
0.700016	0.719996	0.710006
0.720022	0.680003	0.720029
0.730002	0.690018	0.720035
0.710003	0.679999	0.700024
0.730011	0.70002	0.72003
0.710008	0.690023	0.72003
0.700014	0.700009	0.720033
0.720023	0.700013	0.700022
0.720017	0.700018	0.720031
0.720009	0.700015	0.71001
0.720014	0.700022	0.720022
0.709996	0.670028	0.720026
0.729996	0.710008	0.720026
0.730005	0.720021	0.720037
0.730011	0.71	0.720033
0.730007	0.700011	0.720019
0.730004	0.720016	0.720026
0.71	0.710005	0.720028
0.730002	0.720024	0.720035
0.730007	0.700026	0.720028
0.73001	0.70001	0.72004
Average		
	0.7105709	

Table 9.7 shows the quality index rmse for drain current (I_D). It suggests that the modified SPICE model simulation is close to the experimental measurements thus validating the changes. Graphically some simulated curves in Figure 9.12 show a

small differences when compared to the experimental ones due to the lack of higher level parameters for short channel effects. Even with those small differences the modified SPICE model can be used to simulate any of the three annular MOSFETs. Each curve has 301 samples (experimental and simulation).

Table 9.7 : RMSE Between Experimental and Simulated Measurements for Drain Current (I_D)

	Inner W and L		
Gate Voltage (V)	2.7μm and 1.2μm	3.3μm and 2.4μm	3.3μm and 3.6μm
1	0.375405011%	0.35621146%	0.446794%
1.2	0.440125178%	0.448025162%	0.695981%
1.4	0.400810888%	0.374734959%	0.517496%
1.6	0.389963583%	0.344548117%	0.411608%
1.8	0.401882936%	0.339626672%	0.364448%
2	0.425722684%	0.34454785%	0.347907%
2.2	0.456430218%	0.355351186%	0.344945%
2.4	0.488853975%	0.370556973%	0.35778%
2.6	0.522400703%	0.389979713%	0.354291%
2.8	0.556496825%	0.414630466%	0.364371%
3	0.588914375%	0.44235565%	0.377385%
	RMSE		

Table 9.7 shows the rms error for triode and saturation combined. In Tables 9.8 , 9.9 and 9.10 are shown each region (triode and saturation) rms error for each transistor I_D (simulation vs experimental).

Table 9.8 : Inner W = 2.7μm L = 1.2μm

Gate Voltage	Triode	Saturation
1	3.671381%	0.17184%
1.2	2.135641%	0.33168%
1.4	1.547124%	0.25344%
1.6	1.245167%	0.19759%
1.8	1.074587%	0.17678%
2	0.971744%	0.17810%
2.2	0.906266%	0.19439%
2.4	0.858650%	0.21826%
2.6	0.822597%	0.25173%
2.8	0.794049%	0.30022%
3	0.768740%	0.36288%

Table 9.9 : Inner W = 3.3μm L = 2.4μm

Gate Voltage	Triode	Saturation
1	3.69162%	0.10436%
1.2	2.11226%	0.35145%
1.4	1.48008%	0.21856%
1.6	1.14282%	0.11892%
1.8	0.93970%	0.06360%
2	0.80840%	0.04024%
2.2	0.72118%	0.04537%
2.4	0.66230%	0.05843%
2.6	0.62192%	0.09221%
2.8	0.59641%	0.14687%
3	0.57965%	0.22191%

Table 9.10 : Inner W = 3.3μm L = 3.6μm

Gate Voltage	Triode	Saturation
1	3.610254%	0.324907%
1.2	2.280394%	0.706006%
1.4	1.561105%	0.489237%
1.6	1.176006%	0.319796%
1.8	0.947208%	0.205226%
2	0.799222%	0.129370%
2.2	0.696630%	0.080180%
2.4	0.621181%	0.050027%
2.6	0.566744%	0.039549%
2.8	0.526738%	0.053742%
3	0.497544%	0.080683%

9.2.4 Schwarz-Christoffel Conformal Mapping Transformation

The modified MATLAB SC toolbox [23] with an adjustment on the used polygon, was presented as an alternative aspect ratio calculation method. For this, one section of the drawn gate enclosed transistor is transformed into its rectangular equivalent, then it is multiplied by 4. By doing this, the gate handle part is not included when the transformation is made. Figure 9.15 shows one section of an annular MOSFET mapped into a rectangular shape.

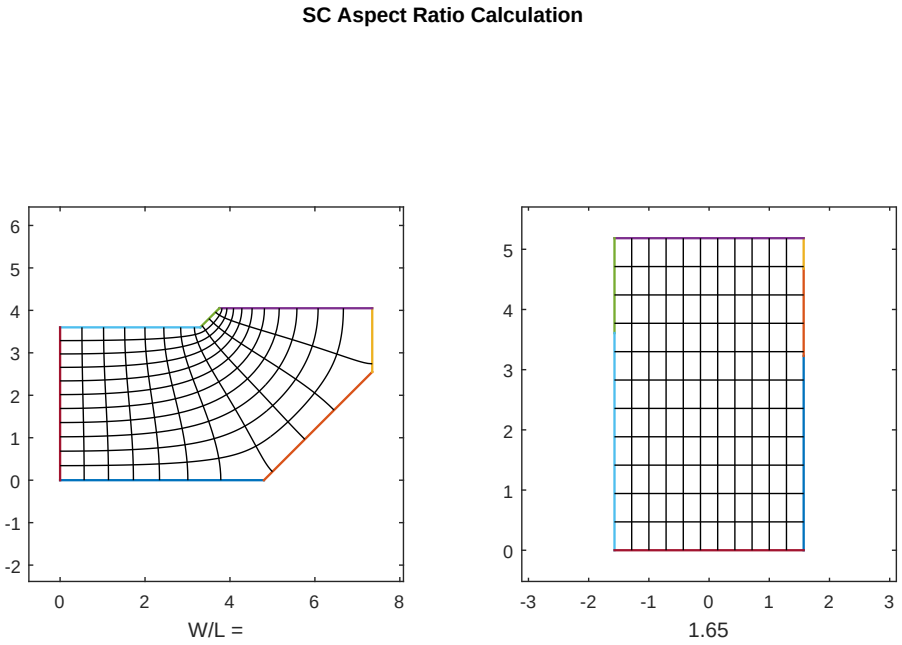


Figure 9.15 : Aspect Ratio Calculation of one Section of an Annular MOSFET (Drawn Inner W = 3.3μm, L = 3.6μm)

Table 9.11 : Alternative W/L Calculation Validation

		W/L Extraction Method			
Inner W	L	Experimental	Alternative	Giraldo [18]	Champion [23]
2.7μm	1.2μm	14.91082142	13.4039517	12.1053482	12.41689138
3.3μm	2.4μm	10.0213822	8.88690494	8.07401679	8.071707121
3.3μm	3.6μm	7.598985028	6.600145	6.06257389	6.037514898
rms errors			6.69210948%	11.2566261%	10.95691962%

A comparison between the proposed alternative W/L calculation and two other methods is presented in Table 9.11 . For this the experimental extracted W/L is used as reference. The rms errors shows that the proposed alternative W/L calculation can be used for numerical simulation, when is not possible to perform the experimental W/L extraction.

Chapter 10
CONCLUSION AND FUTURE WORK

10.1 Conclusion

This work presented the design and implementation of different DC level 1 parameters and annular MOSFET aspect ratio experimental extraction. A modified SPICE model to improve annular MOSFETs simulation was achieved by establishing a procedure for DC level 1 parameters and annular MOSFET aspect ratio experimental extraction. The automation to perform all the need test was made using LabVIEW.

The experimental W/L extraction was made using a standard transistor to obtain the low field mobility value in case the foundry does not provide it. For this, the standard transistor can have any gate length size. The available equipment was automated using LabVIEW to perform the measurements without human intervention after setting the conditions for each test.

An alternative annular transistor aspect ratio calculation using MATLAB was also presented in this thesis, and compared with other validated models. This numerical calculation can be used to obtain the W/L for gate enclosed MOSFETs.

10.2 Contributions

The main contribution of this work was the development of an automated experimental W/L extraction for annular MOSFETs. Using a standard MOSFET (independent of its gate length), to obtain the needed parameters for the W/L calculation. Other contributions of this work include:

1. An accurate annular/gate enclosed transistor DC level 1 parameter and aspect ratio (W/L) extraction using an automated setup with low cost equipment.
2. A procedure that incorporates different techniques for gate enclosed MOSFET DC level 1 parameter calculation.
3. A repeatable procedure for gate enclosed MOSFET DC level 1 parameter calculation and W/L extraction.
4. A procedure to extract gate enclosed MOSFET W/L and DC level 1 parameters with minimal human intervention.
5. Knowledge of annular MOSFET I-V behavior that can be used for modeling.

10.3 Future Work

This work can be expanded in several scenarios. From a hardware perspective, by designing a PCB layout that reduces the board parasitics capacitances and proper equipment for capacitance measurements in the order of femto farads (fF). A more complete level 1 MOSFET model which includes capacitance parameters can be developed. Further work on annular/gate enclosed MOSFETs parameter extraction can be used for a compact model generation this can be used to simulate a circuit design and predict its behavior. The implementation of a procedure to obtain an annular MOSFET equivalent from a designed rectangular aspect ratio for a specific current. Finally, efforts to automate all experimental test is a possible expansion of this work.

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Appendices

Appendix A
SPICE MODEL PROVIDED BY MOSIS

MOSIS WAFER ELECTRICAL TESTS

RUN: V62E VENDOR: ON-SEMI
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SHR

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot.

COMMENTS: SMSCN3ME06_ON-SEMI

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.82	-0.92	volts
SHORT	20.0/0.6			
Idss		459	-248	uA/um
Vth		0.70	-0.90	volts
Vpt		12.5	-12.4	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.72	-0.95	volts
Vjbkd		10.6	-11.7	volts
Ijlk		169.5	<50.0	pA
Gamma		0.47	0.57	V^0.5
K' (Uo*Cox/2)		58.7	-19.0	uA/V^2

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

COMMENTS:

PROCESS PARAMETERS	N+	P+	N_W	_U	POLY	PLY2_HR	POLY2	M1	UNITS
Sheet Resistance	83.2	108.9	794.7	24.1	1075		41.0	0.09	ohms/sq
Contact Resistance	60.5	151.1		16.2			24.9		ohms
Gate Oxide Thickness	139								angstrom

PROCESS PARAMETERS	M2	M3	N_W	UNITS
Sheet Resistance	0.09	0.05	789	ohms/sq
Contact Resistance	0.83	0.77		ohms

COMMENTS:

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	408	715	88		29	12	8	87	aF/um^2
Area (N+active)			2480		38	17	12		aF/um^2
Area (P+active)			2399						aF/um^2
Area (poly)				885	70	16	9		aF/um^2
Area (poly2)					57				aF/um^2
Area (metal1)						32	13		aF/um^2
Area (metal2)							33		aF/um^2
Fringe (substrate)	338	214			50	34	25		aF/um
Fringe (poly)					60	39	28		aF/um
Fringe (metal1)						48	33		aF/um
Fringe (metal2)							45		aF/um
Overlap (N+active)			185						aF/um
Overlap (P+active)			226						aF/um

COMMENTS:

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.04	volts
Vinv	1.5	2.31	volts
Vol (100 uA)	2.0	0.50	volts
Voh (100 uA)	2.0	4.46	volts
Vinv	2.0	2.49	volts
Gain	2.0	-19.28	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		92.89	MHz
D256_WIDE (31-stg,5.0V)		152.27	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.46	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		0.97	uW/MHz/gate

COMMENTS: SUBMICRON

V33R SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Jul 17/13
* LOT: v33r                  WAF: 2105
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 1.4E-8
+XJ      = 1.5E-7        NCH     = 1.7E17          VTH0    = 0.6320109
+K1      = 0.9145878     K2      = -0.1090989      K3      = 22.6724565
+K3B     = -9.8238627    W0      = 2.654411E-8     NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0               DVT2W   = 0
+DVT0    = 0.8185996     DVT1    = 0.3395204       DVT2    = -0.5
+U0      = 451.1629214   UA      = 3.677855E-13    UB      = 1.226024E-18
+UC      = 1.655554E-12  VSAT    = 1.861999E5      A0      = 0.5403581
+AGS     = 0.0899246     B0      = 2.05136E-6      B1      = 5E-6
+KETA    = -5.208211E-4  A1      = 3.32698E-5      A2      = 0.312812
+RDSW    = 944.9075273   PRWG    = 0.1457938       PRWB    = 0.0174966
+WR      = 1             WINT    = 2.131408E-7     LINT    = 8.519713E-8
+XL      = 1E-7          XW      = 0               DWG     = -4.431704E-9
+DWB     = 3.88832E-8    VOFF    = 0               NFACTOR = 0.4855649
+CIT     = 0             CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0             ETA0    = 1.864194E-3     ETAB    = -2.372887E-4
+DSUB    = 0.0939504     PCLM    = 2.4308835       PDIBLC1 = 7.735498E-5
+PDIBLC2 = 2.040149E-3   PDIBLCB = 0.0549985       DROUT   = 9.945166E-4
+PSCBE1  = 4.019179E8    PSCBE2  = 4.868242E-6     PVAG    = 4.143291E-4
+DELTA   = 0.01          RSH     = 81.7            MOBMOD  = 1
+PRT     = 0             UTE     = -1.5            KT1     = -0.11
```

```
+KT1L     = 0              KT2      = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18      UC1      = -5.6E-11       AT       = 3.3E4
+WL       = 0              WLN      = 1              WW       = 0
+WWN      = 1              WWL      = 0              LL       = 0
+LLN      = 1              LW       = 0              LWN      = 1
+LWL      = 0              CAPMOD   = 2              XPART    = 0.5
+CGDO     = 3.12E-10       CGSO     = 3.12E-10       CGBO     = 1E-9
+CJ       = 4.264707E-4    PB       = 0.879971       MJ       = 0.4289757
+CJSW     = 3.109887E-10   PBSW     = 0.8            MJSW     = 0.1988328
+CJSWG    = 1.64E-10       PBSWG    = 0.8            MJSWG    = 0.2019414
+CF       = 0              PVTH0    = 0.0237077      PRDSW    = 170.7916215
+PK2      = -0.0864032     WKETA    = -0.0113383     LKETA    = 2.770737E-3     )
*
.MODEL CMOSP PMOS (                                  LEVEL    = 49
+VERSION = 3.1             TNOM     = 27             TOX      = 1.4E-8
+XJ       = 1.5E-7         NCH      = 1.7E17         VTH0     = -0.9152268
+K1       = 0.553472       K2       = 7.871921E-3    K3       = 20.3090487
+K3B      = -0.9336872     W0       = 6.080092E-7    NLX      = 1.223804E-9
+DVT0W    = 0              DVT1W    = 0              DVT2W    = 0
+DVT0     = 0.5290776      DVT1     = 0.3624489      DVT2     = -0.3
+U0       = 201.3603195    UA       = 2.48572E-9     UB       = 1.005454E-21
+UC       = -1E-10         VSAT     = 1.803251E5     A0       = 1.0265509
+AGS      = 0.1161837      B0       = 2.587614E-7    B1       = 0
+KETA     = -4.865785E-3   A1       = 2.988942E-4    A2       = 0.3299163
+RDSW     = 3E3            PRWG     = -0.0219769     PRWB     = -0.0911451
+WR       = 1.01           WINT     = 2.35933E-7     LINT     = 9.97637E-8
+XL       = 1E-7           XW       = 0              DWG      = -1.866812E-9
+DWB      = -1.956278E-8   VOFF     = -0.0475195     NFACTOR  = 0.5569109
+CIT      = 0              CDSC     = 2.4E-4         CDSCD    = 0
+CDSCB    = 0              ETA0     = 9.402686E-3    ETAB     = -0.2
+DSUB     = 1              PCLM     = 2.2792229      PDIBLC1  = 0.0770242
+PDIBLC2  = 4.198712E-3    PDIBLCB  = -0.0365814     DROUT    = 0.2771064
+PSCBE1   = 6.7472E10      PSCBE2   = 7.562499E-8    PVAG     = 0.0121581
+DELTA    = 0.01           RSH      = 105.1          MOBMOD   = 1
+PRT      = 0              UTE      = -1.5           KT1      = -0.11
+KT1L     = 0              KT2      = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18      UC1      = -5.6E-11       AT       = 3.3E4
+WL       = 0              WLN      = 1              WW       = 0
+WWN      = 1              WWL      = 0              LL       = 0
+LLN      = 1              LW       = 0              LWN      = 1
+LWL      = 0              CAPMOD   = 2              XPART    = 0.5
+CGDO     = 4.52E-10       CGSO     = 4.52E-10       CGBO     = 1E-9
+CJ       = 7.288496E-4    PB       = 0.9485685      MJ       = 0.4937868
+CJSW     = 2.609534E-10   PBSW     = 0.8            MJSW     = 0.3535404
+CJSWG    = 6.4E-11        PBSWG    = 0.8            MJSWG    = 0.2261452
+CF       = 0              PVTH0    = 5.98016E-3     PRDSW    = 14.8598424
+PK2      = 3.73981E-3     WKETA    = -7.708624E-4   LKETA    = -0.0123442      )
*
```

Appendix B
LabVIEW^{TM} Code: Block Diagrams

B.1 Instruments Initialization and Configuration

This code section shows the LabVIEW sequence for initializing and configuring the Keithley 2612A System SourceMeters®.

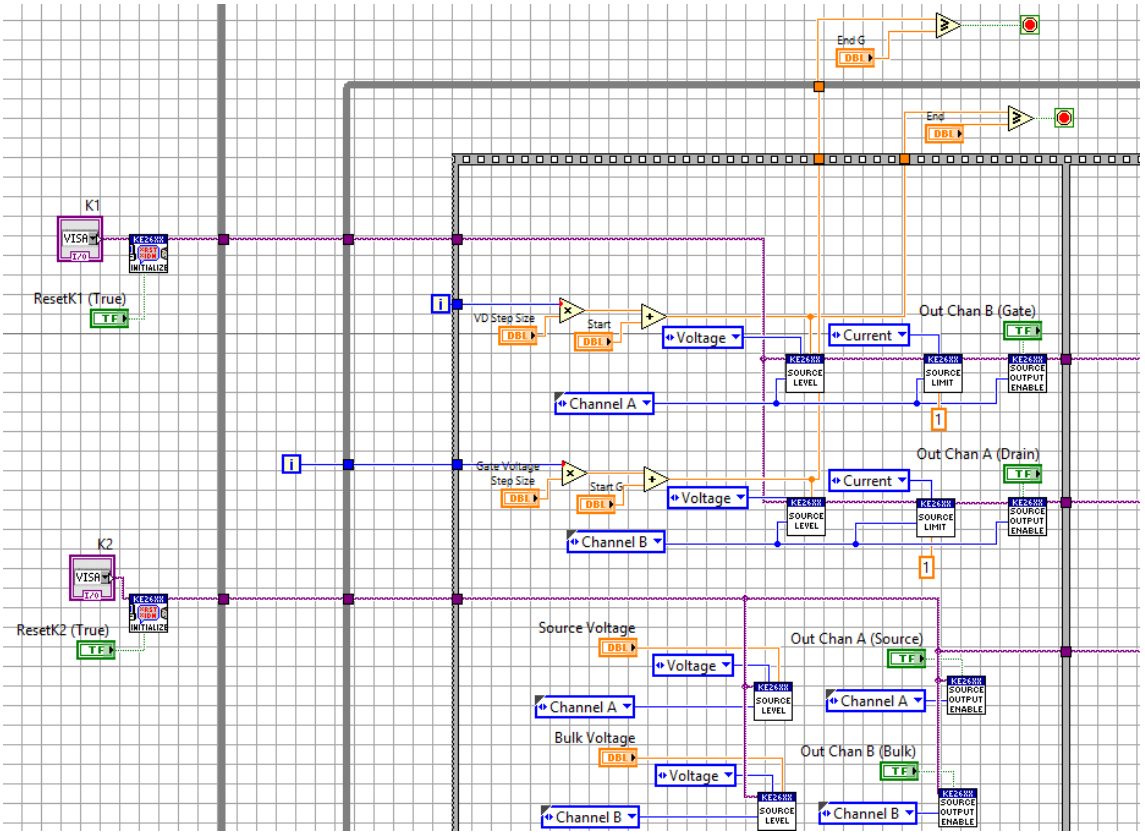

Figure B.1 : Initialization and Configuration

B.2 Closure

This section ends the communication via software with the Keithley 2612A System SourceMeters®

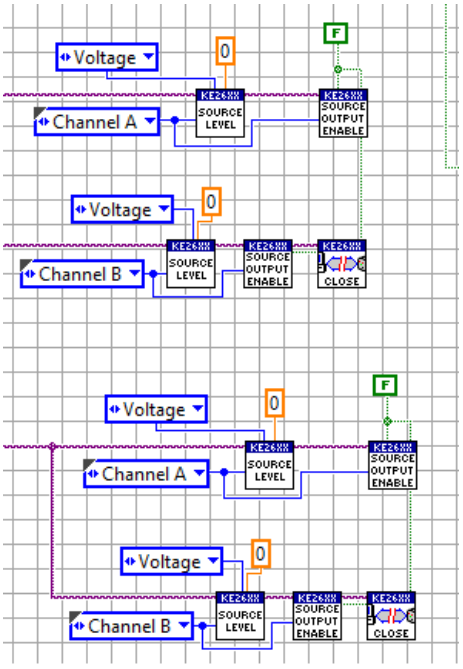

Figure B.2 : Instruments Communication Closure

B.3 Data processing

This part shows the LabVIEW code for data manipulation.

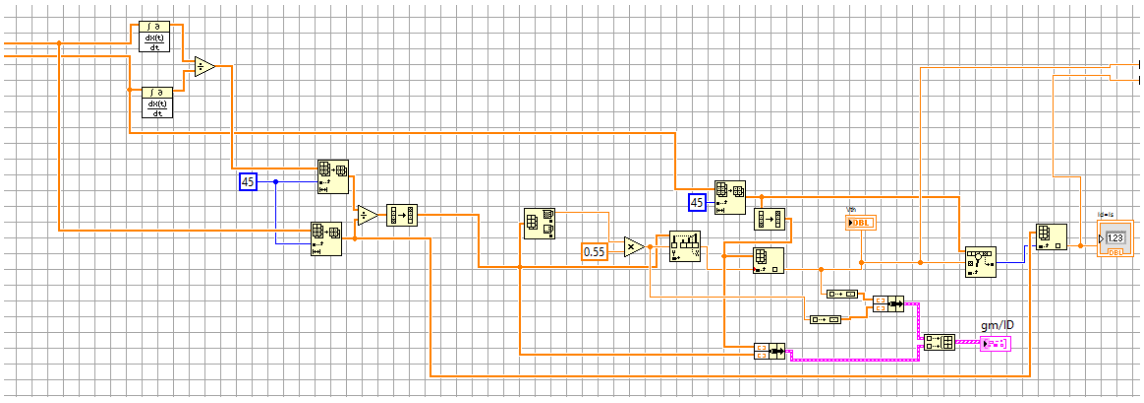

Figure B.3 : Threshold Voltage and Specific Current Extraction

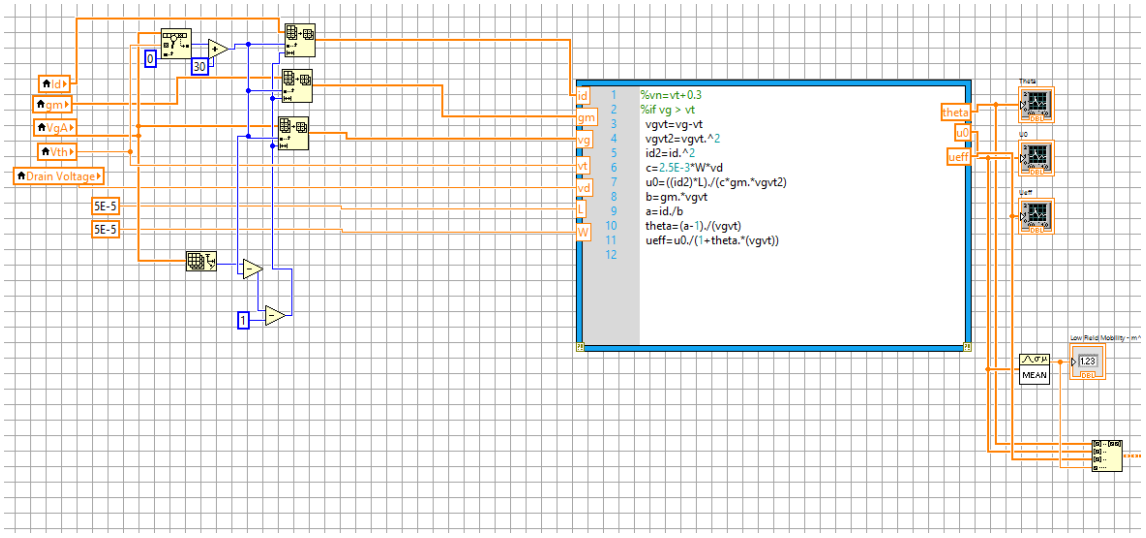

Figure B.4 : Low Field Mobility Calculation

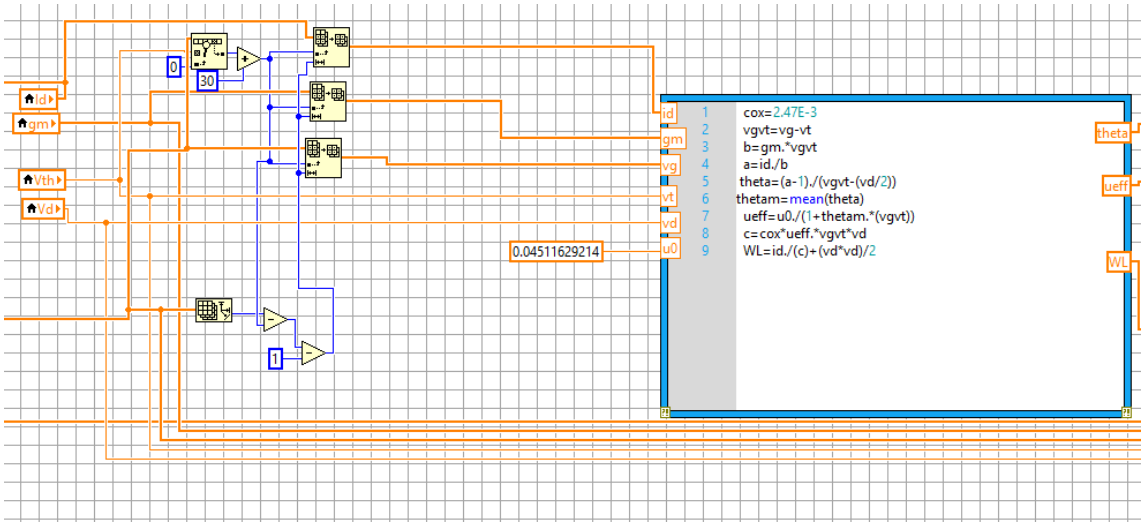

Figure B.5 : Aspect Ration Extraction

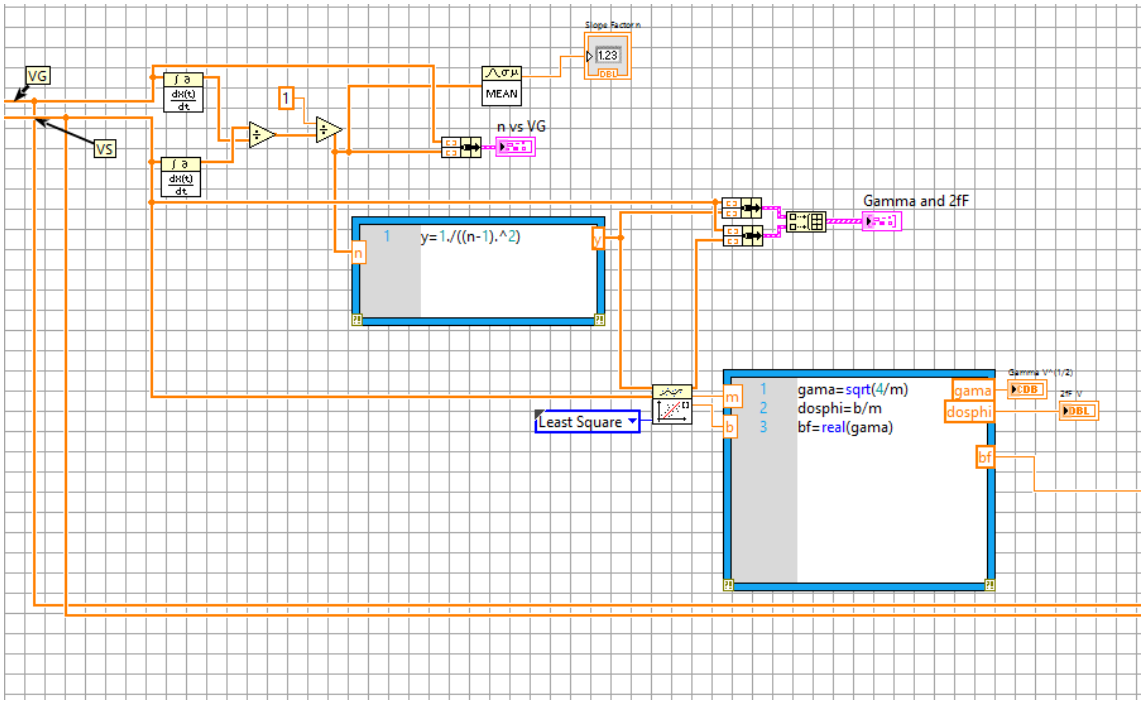

Figure B.6 : Body Effect Factor (Gamma) Extraction

B.4 Data Storage

In this section the information obtained from each test is generate a spreadsheet and saves it in the PC.

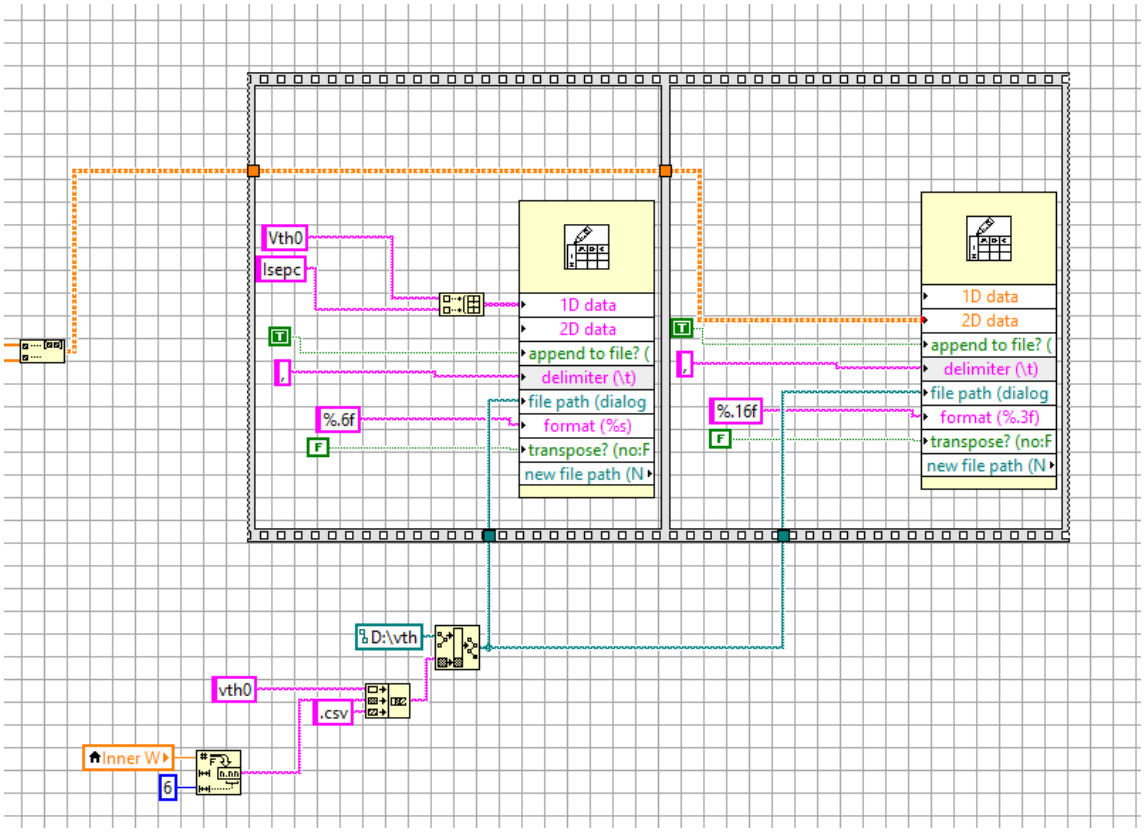

Figure B.7 : Threshold Voltage and Specific Current Spreadsheet Generation

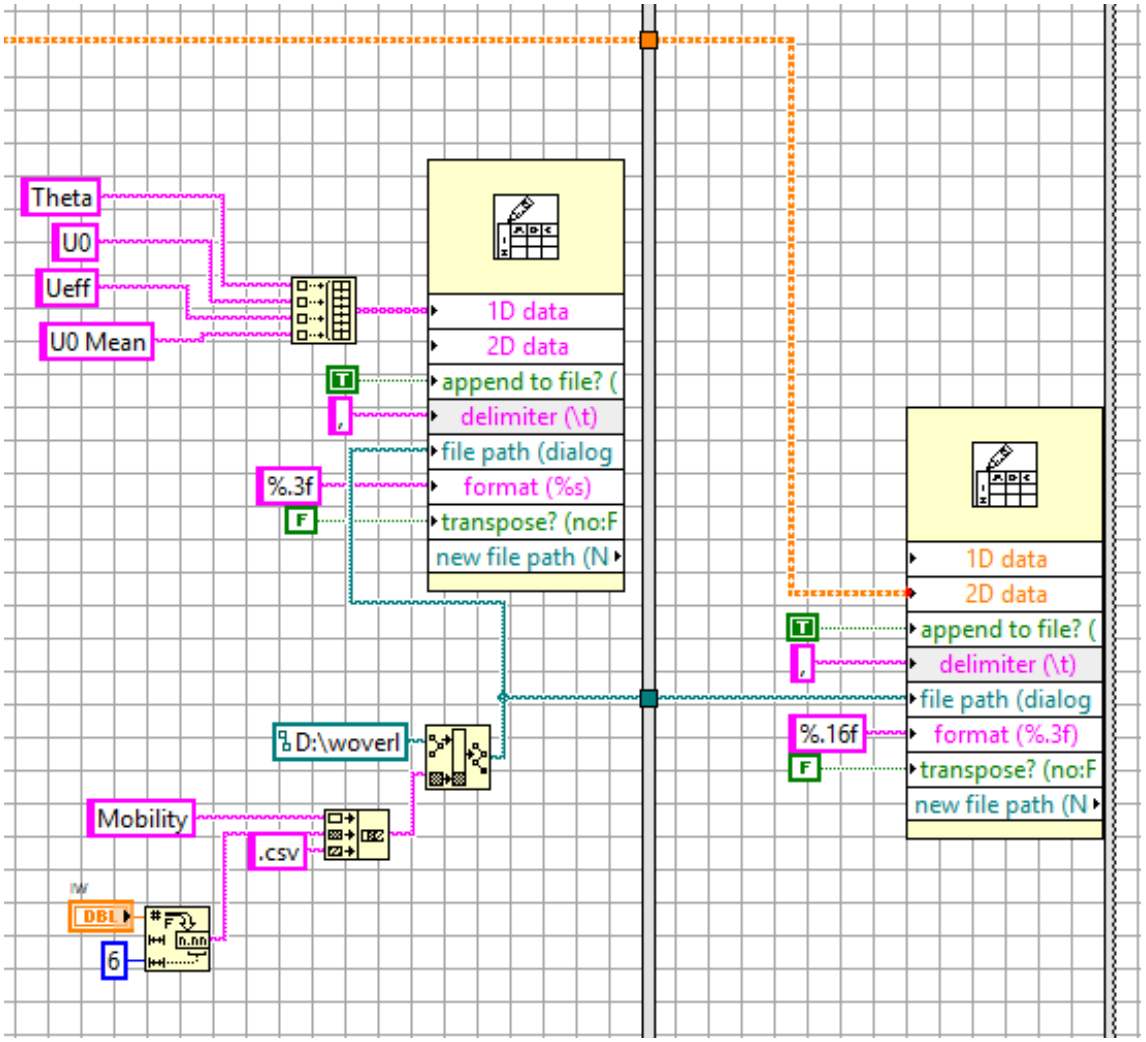

Figure B.8 : Low Field Mobility Spreadsheet Generation

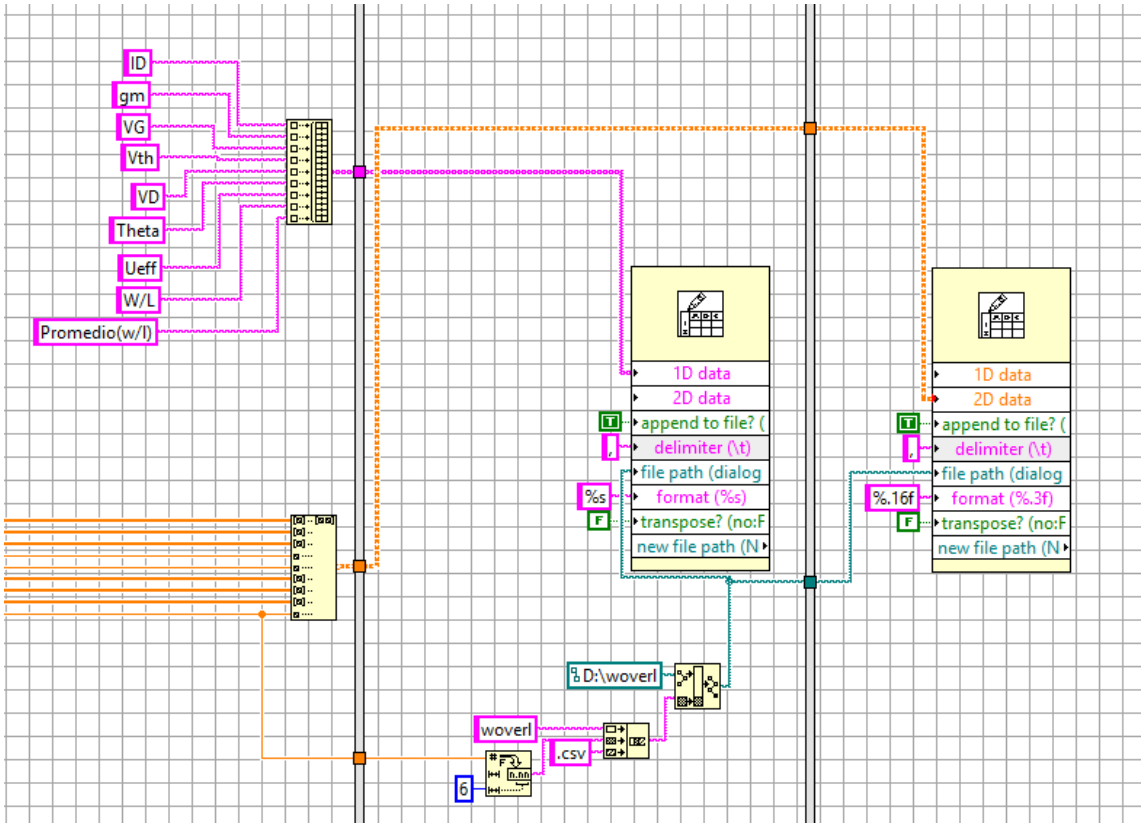

Figure B.9 : Aspect Ration Spreadsheet Generation

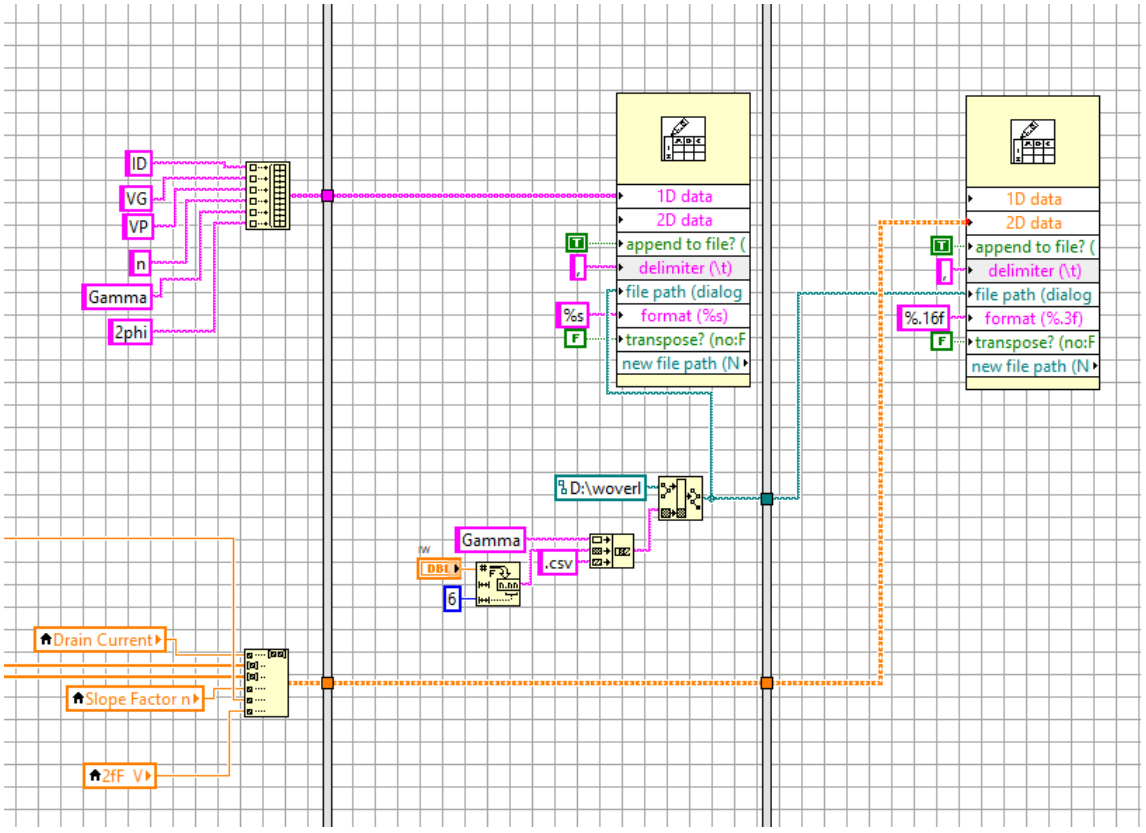

Figure B.10 : Body Effect Factor (Gamma) Spreadsheet Generation

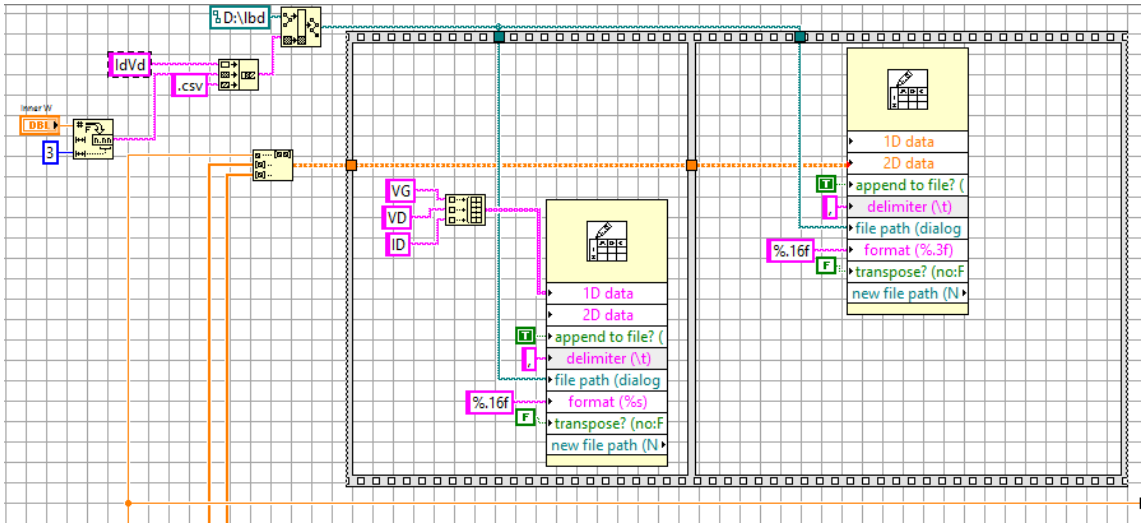

Figure B.11 : ID vs VD Curve Data Storage

Appendix C
Information Storage Example

C.1 Spreadsheet Sample for W/L Extraction

In Figure C.1 a sample for the aspect ratio calculation of an standard MOSFET (W/L = $20\mu m/0.6\mu m$) is shown. The header part shows the name for each column

- ID - Measured Drain Current
- gm - MOSFET Transconductance
- VG - Sourced Gate Voltage
- Vth - Extracted Threshold Voltage
- VD - Fixed Drain Voltage
- Theta - Effective Mobility Reduction Factor
- Ueff - Effective Mobility
- W/L - Extracted MOSFET Aspect Ratio
- Average (W/L) - Average of the Extracted W/L

	A	B	C	D	E	F	G	H	I
1	ID	gm	VG	Vth	VD	Theta	Ueff	W/L	Average(W/L)
2	8.9407E-12	8.7732E-10	4.375E-05	0.709995	0.0499515	0.01291062	0.0407061	31.4881325	32.67418263
3	8.8096E-12	-4.173E-12	0.0100415	0	0	0.00872358	0.04057416	31.5835519	0
4	8.8572E-12	1.8483E-11	0.0200412	0	0	0.02427686	0.04044308	31.6875669	0
5	9.1791E-12	1.3114E-11	0.0300354	0	0	0.05371538	0.04031219	31.7751862	0
6	9.1195E-12	8.9392E-12	0.0400396	0	0	0.06462381	0.04018279	31.8616727	0
7	9.3579E-12	2.1462E-11	0.0500384	0	0	0.08075455	0.04005371	31.9428891	0
8	9.5487E-12	3.3985E-11	0.0600353	0	0	0.07478753	0.03992583	32.0199715	0
9	1.0037E-11	5.6035E-11	0.0700318	0	0	0.09378413	0.0397989	32.1036481	0
10	1.0669E-11	7.1514E-11	0.0800324	0	0	0.13420847	0.03967227	32.1705226	0
11	1.1468E-11	8.5832E-11	0.090035	0	0	0.1430646	0.03954694	32.2310777	0
12	1.2386E-11	1.1028E-10	0.100032	0	0	0.14237522	0.0394219	32.2925237	0
13	1.3673E-11	1.4182E-10	0.110033	0	0	0.14832528	0.03929815	32.3530277	0
14	1.5223E-11	1.8119E-10	0.120037	0	0	0.17682606	0.03917504	32.4106747	0
15	1.7297E-11	2.3018E-10	0.130034	0	0	0.19319811	0.03905234	32.4558287	0
16	1.9825E-11	2.8744E-10	0.140028	0	0	0.19246269	0.03893077	32.5039936	0
17	2.3043E-11	3.8443E-10	0.150024	0	0	0.20806222	0.03880959	32.54922	0
18	2.7514E-11	4.857E-10	0.160029	0	0	0.21480746	0.03868953	32.5888136	0
19	3.2759E-11	6.2343E-10	0.170027	0	0	0.23096314	0.03856985	32.6299834	0
20	3.9983E-11	8.2119E-10	0.18003	0	0	0.23552953	0.03845138	32.6610335	0
21	4.9186E-11	1.0423E-09	0.190031	0	0	0.2359952	0.03833351	32.6990641	0
22	6.0833E-11	1.3435E-09	0.200033	0	0	0.25151227	0.03821614	32.7298322	0
23	7.6008E-11	1.7361E-09	0.209996	0	0	0.24874463	0.03809971	32.75958	0

woverl32.674183

Figure C.1 : W/L stored data Example (Excel)