AN ANALYSIS OF CAPACITANCE MULTIPLIERS BASED ON GENERAL IMPEDANCE CONVERTERS

By

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December 2009

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An analysis at system level applying two port and three terminal network theory is used to establish limitations of frequency and parasitic effects for IC capacitance multipliers. From this analysis, a new model for a floating simulated capacitance based on positive impedance converter was derived. An example of a new electronically tunable implementation based on OTAs and CCCII and focused on low frequency operation has been realized. The circuit was developed with PNP and NPN transistors, whose parameters corresponds to the PRN200P and NR200N of the ALA400 transistor array from AT&T. Pspice simulations show that the circuit can work for ± 2.5 V voltage supplies with a grounded 20 pF capacitor. The equivalent simulated capacitances are in the range of 1 nF to 18 nF. Therefore, a tunable gain factor of 50 to 300 times the capacitance load is achieved in afrequency range of 160 Hz up to 30 kHz.

Resumen de Disertación Presentado a Escuela Graduada
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UN ANALISIS DE MULTIPLICADORES DE CAPACITANCIAS BASADO EN CONVERTIDORES DE IMPEDANCIA GENERALES

Por

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December 2009

Consejero: Rogelio Palomera-García
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Un análisis de multiplicadores de capacitancia a nivel de sistemas utilizando teoría de redes de dos puertos y tres terminales permite establecer limitaciones de frecuencia y las debidas a efectos parasíticos. Se presenta un nuevo modelo basado en convertidores positivos de impedancia para simular capacitancias flotantes, y se implementó usando OTAs y CCCII. El circuito fue desarrollado con transistores BJT, modelos PRN200P y NR200N del arreglo de transistores de ALA400 de AT&T. Los resultados obtenidos mediante el software de Cadence Pspice muestran que el circuito opera a un voltaje de $\pm$ 2.5 V con una capacitancia de carga de 20 pF. Más aun, las capacitancias equivalentes obtenidas están en un rango de 1 nF hasta 18 nF. Por lo tanto, se logró un factor de ganancia ajustable entre 50 a 300 veces la capacitancia de carga, en un rango de frecuencia que va desde 160 Hz hasta 30 kHz.

I would like to dedicate this work to my role models in life, Dr. Ramón Vásquez and Engineer José M. Chamoun (†).

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LIST OF ABBREVIATIONS

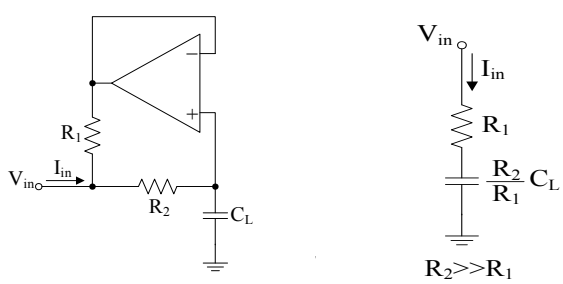
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
PIC	Positive Impedance Converter
GIC	Generalized Impedance Converter
OA	Operational Amplifier
OTA	Operational Transconductance Amplifier
CCCII	Current Controlled Current Conveyor
VCVS	Voltage Controlled Voltage Source
CCCS	Current Controlled Current Source
FCM	Floating Capacitance Multiplier
SOC	System On a Chip
PCB	Printed Circuit Board

LIST OF SYMBOLS

α	The VCVS multiplier factor
β	The CCCS multiplier factor
V_T	The thermal voltage

CHAPTER 1
INTRODUCTION

For a long time, the concept of capacitance multiplication has been used to mimic "high" capacitance values in different applications. Frequency multipliers [1] (1962), amplifiers [2] (1969) and power supplies [3] are early examples where this technique was necessary. The advent and popularization of IC operational amplifiers gave rise to more capacitance multiplier realizations. One example is the circuit of Figure 1–1a developed by Signetics Company [4] which was included in the popular series of books edited by Rudolf F. Graf in the eighties, the Encyclopedia of Electronic Circuits [5]. The multiplication effect by R_1/R_2, is seen in the equivalent impedance shown in Figure 1–1b. It is assumed that $R_1 >> R_2$, very often by a factor of 100 or more. Although conceptually simple, the large ratio required for resistors is one of the reasons why this circuit is inappropriate for integration.



(a) (b)

Figure 1–1: Capacitance multiplier using an IC Operational Amplifier [4]

The progress of integrated circuit technology has allowed an exponential growth of the number of applications where the complete system is integrated on a chip,

SOC. On the other hand, applications like integrated lock-in amplifiers, linear regulators, capacitive sensor interfaces, pacemakers, sampled data systems, and phase locked loops require large capacitance values. However, the issues of the area required for passive elements remain as important challenges in IC technology, as well as, the associated power consumption. In particular, large values of elements like capacitors are not feasible. Integration of values above 100 pF are impractical since its implementation on a standard CMOS polysilicon layer would cover the silicon area of thousands of transistors [6].

The requirement of large capacitance values in SOC applications has increased research on the field of capacitance multipliers. In fact, a cost analysis is introduced in the following section to explain the importance of capacitance multipliers when it is required to minimize area consumption. The analysis is focused on bipolar technology since the developed tunable floating capacitance multiplier discussed in chapter 4 and 5 consists of bipolar transistors and a 20 pF grounded capacitor.

Most designs are focused on grounded capacitance multipliers and medium to high frequency applications. The relatively few designs focused on floating capacitance emulation also apply to the same frequency ranges. Both grounded and floating cases have encountered important problems among which we find the need of large load capacitances and therefore large area requirements. Serious difficulties when attempting to go to low and very low frequency ranges are common too. Others encounter large capacitance deviations, high power dissipation, and lack of tunability.

Low frequency applications in low voltage circuits have become more and more important because of the increased research in medical and biological applications. Other areas for low frequency applications are in Geology, Marine Science, Botany, and so on. Hence, the solution of these problems has become important. This thesis is a contribution in this direction.

1.1 IC cost considerations of multipliers vs capacitors

Tables 1–1, 1–2, and 1–3 are used to compare area consumption between an integrated capacitor and the proposed capacitance multiplier circuit discussed in chapter 4 and 5. The first table shows the equivalent area consumption for the integration of different types of IC capacitors. The second estimates the amount of area occupied by bipolar transistors when different technologies are taken into consideration. Although, a 5 and 10 μm technologies are obsolete they are shown to put in perspective the relevance of area consumption. For the proposed tunable floating capacitance multiplier developed with bipolar technology a total area estimation for the different technologies is given in Table 1–3.

Table 1–1: IC Capacitors [7]

Capacitor type	Capacitance per unit area (pF/mm^2)	Breakdown voltage (V)	Size of 1 nF (mm^2)	Size of 16 nF (mm^2)	Size of 20 pF (mm^2)
Collector-base junction C_{CB}	125	50	8	128	.16
Emitter-base junction C_{EB}	1000	7	1	16	.02
Collector-substrate C_{CS}:					
With N+ burried layer	90	50	11	178	.22
No N+ burried layer	60	50	17	267	.33

Table 1–2: IC Bipolar transistors

Technology (μm)	BJT area (mm^2)	BJT/mm^2
10	.017	61
5	.004	242
1	.00017	6061
.8	.00012	9470

Table 1–3: The estimated total area cover by the proposed FCM (116 BJTs)

Technology (μm)	Size of 20 pF (mm^2)	BJT area (mm^2)	Total FCM area (mm^2)
10	.16	1.9	2.1
5	.02	.5	.5
1	.22	.02	.24
.8	.33	.01	.34

In Table 1–1 an emitter-based junction capacitor of 1 nF occupies an area of 1 mm^2, meaning that the integration of 16 nF requires 16 mm^2. Notice that the proposed floating capacitance multiplier circuit is tunable and the amount of area is independent of the size of the equivalent tunable capacitances which goes from 1 nF up to 16 nF. For a .8 μm technology, Table 1–3 gives an estimated area consumption of .34 mm^2. Therefore, for a 16 nF the proposed multiplier is 47 times smaller than the emitter-based junction capacitor. Even if a 1 nF emitter-based junction capacitor is compared with the multiplier, still in the .8 μ technology the multiplier saves 3 times the area of the IC capacitor. However, the breakdown voltage value is one of the reason why this type of capacitors is usually avoided. It is worth remarking that the amount of area covered by the multiplier is essentially that of the 20 pF grounded capacitor.

1.2 Thesis objectives

The initial proposal for this research was to find alternative circuit configurations to deal with the main problems stated above. In particular, to find a new configuration with improved performance in the low frequency region, with tunable gain and low power requirements. Some theoretical derivations were expected in the process that would allow to solve some of the general limitations for this type of circuits.

However, as the research advanced, the problems seemed to be without solution or else the trade offs very stringent. Thus, if power and voltage supply values are not of concern, getting high multiplication factors with relatively low valued load capacitance can be achieved for medium to high frequency ranges. Trying to apply similar techniques for low frequency applications found other problems. Similarly, reducing power consumption brought up new problems, including serious deviations with respect to the realization goal.

These drawbacks forced us to take another look at the initial problem and shift the emphasis of this investigation. The thesis objectives became then the following:

- To make an analysis of capacitance multipliers from a systems point of view which should allow to
  1. derive a set of general limitations for these circuits;
  2. derive guidelines for the design of these circuits when low frequency and low power/voltage objectives come into play
- To propose a circuit realization with tunable multiplication factor following the guidelines derived from the general analysis.

1.3 Thesis contribution

The main contribution of this research are the results in Chapter 3, where the study of capacitance multipliers from an abstract circuit theoretical point of view has allowed us to derive important characteristics for the elements which set limitations on the achievable goals, and/or point to the trade offs that should be encountered in the process.

One or more of the limitations derived in Chapter 3, were mentioned as probable reasons for the poor performance of their designs when tested in the low frequency range. Yet, they were mentioned either as a conjecture or apparently with knowledge

but no formal proof. For these cases, the formal proofs provided in this thesis may also be considered as a contribution.

The floating capacitance multiplier with tunable gain offered in Chapter 4 is also a contribution of this thesis. Besides tunability, it is offered as a proof of concept of how the guidelines derived in Chapter 3 can be used to design the circuit with reasonable and achievable goals, and how to work with trade offs. Unfortunately, within the time frame for this research, this circuit was not optimized.

1.4 Thesis Overview

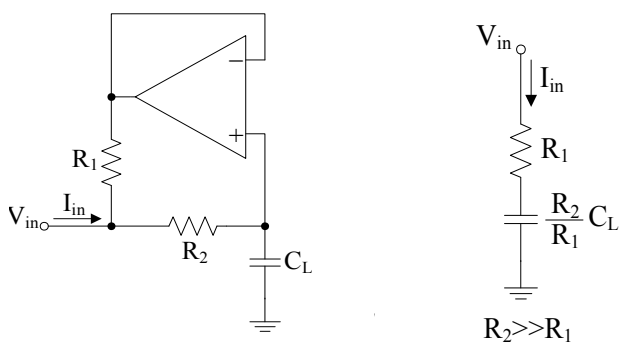
- **Chapter 2:** makes a literature review of capacitance multiplier realizations, it points out the limitations that have been consistently encountered regarding frequency and size. Corrections to previous publications are also offered.
- **Chapter 3:** offers a theoretical analysis on the topology of multipliers as terminated two-ports or three-terminals configurations, which embraces the general case under which all previous works have been realized. This approach has allowed us to understand the theoretical background that explains the limitations and restrictions encountered by previous authors.
- **Chapters 4 and 5:** are devoted to the realization and simulation of a new multiplier based on OTA's. The design uses guidelines derived from the work presented in Chapter 3. The simulations include applications to verify its performance. The new multiplier has not been optimized to any particular goal, but has been used to validate the analysis presented in chapter 3.

CHAPTER 2
ANTECENDENTS OF CAPACITANCE MULTIPLIERS

This chapter reviews some previous works on capacitance multipliers, highlighting the main problems that the most recent proposals have encountered when integrated circuit realizations are considered.

2.1 Initial considerations

As mentioned in Chapter 1, capacitance multipliers have been in use for several decades. Figure 1–1, repeated for convenience in Figure 2–1, is a multiplier published by Signetics Corporation [4] which is still popular mainly among hobbyists and to solve many problems. This, like many other early designs, included the equivalent series resistance (ESR) as part of the process. An analysis of the circuit is presented next to illustrate both the multiplication and the design method.



(a) (b)

Figure 2–1: Capacitance multiplier using an IC Operational Amplifier [4]

For the OA circuit, the equivalent input impedance is described as follows. Taking nodal equations at the input node and at the capacitance C_L node (V_2), yields

$$\left(\frac{1}{R_1}+\frac{1}{R_2}\right)V_{in}-\left(\frac{1}{R_1}+\frac{1}{R_2}\right)V_2=I_{in} \tag{2.1a}$$

$$-\frac{1}{R_2}V_{in}+\left(sC_L+\frac{1}{R_2}\right)V_2=0 \tag{2.1b}$$

The OA output potential equal to V_2 was already taken into consideration. From these equations we can then deduce the input impedance is then described as

$$Z_{in}=\frac{V_{in}}{I_{in}}=sC_L\left(1+\frac{R_2}{R_1}\right)+\frac{R_1\,R_2}{R_1+R_2}\approx sC_L\left(\frac{R_2}{R_1}\right)+R_1 \tag{2.2}$$

where $R_2 >> R_1$ allows simplification.

This example, as well as many other capacitance multipliers, uses discrete and IC components. This offers many advantages in the choice of elements; however,there is a price in the PCB real state layout and in additional parasitics related to this technique.

Recently, however, there is the tendency toward SOC (Systems on a Chip) realizations, imposing the limitations that IC technology has. One very important limitation, albeit not the only one of IC technology, is the size of practical capacitors. With a density of 1 fF/μm^2 for sub-micron CMOS, for example, one 100 pF capacitor occupies an area equivalent to thousands of transistors or hundreds of operational amplifiers [8]. Hence, even for equivalent capacitance realizations in the nano and micro range there may arise serious problems in real state. Other issues concerning this problem are considered later.

2.2 Related works using current and voltage mode techniques

This section covers some representative IC realizations highlighting the limitations that have been encountered. Basic realizations are the current and the voltage mode ones shown in Figure 2–2. The latter is based on Miller effect.

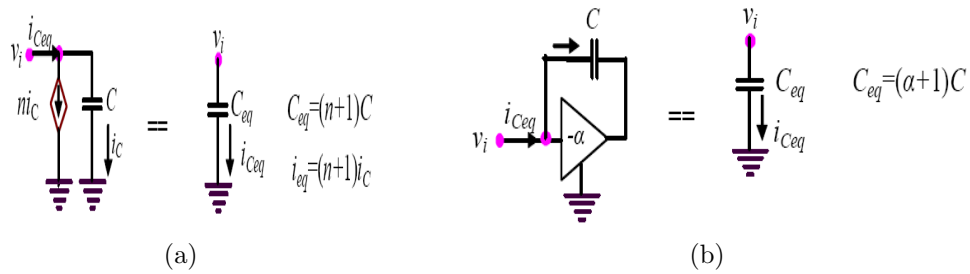


Figure 2–2: Basic capacitance multiplier models: (a) current mode, (b) voltage mode [9]

The main advantages of the current mode version (Figure 2–2a) are its high swing and high frequency performance. Its main disadvantages are low multiplication factor, poor tunability, low input resistance and DC leakage current. On the other hand, voltage mode (Figure 2–2b) multipliers have a higher multiplication factor but several practical problems. They have stability problems when the floating capacitor load is too small, thereby requiring from the beginning large capacitor values. They also have a low input swing value and require additional DC bias [9].

Based on current techniques the floating capacitance multiplier model in Figure 2–3 was implemented by M. Siripruchyanan and W. Jaikla [6].

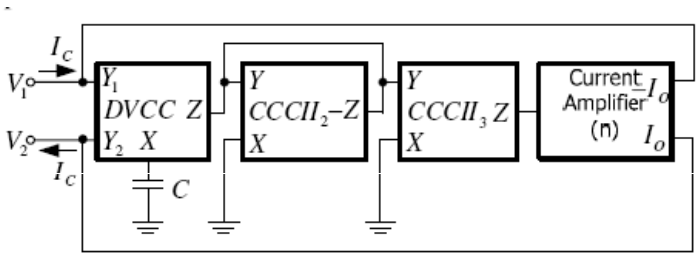


Figure 2–3: Floating Capacitance Multiplier Model [6]

This circuit consists of three main blocks: the DVCC, the CCCIIs and the current amplifier (CA). The input impedance is given by equation (2.3).

$$Z_{in} = \frac{V_1 - V_2}{I_c} = \frac{R_{x3}}{nsCR_{x2}} \tag{2.3}$$

Here, C is the grounded capacitor, whose value is fixed to 50 pF; n is a fixed gain factor given by a current amplifier, R_{x2} and R_{x3} are the intrinsic input resistances of the $CCCII_2$ and $CCCII_3$, determined as, $R_x = V_T/2I_B$, where V_T is the thermal voltage (typically 26 mV at room temperature) and I_B is the bias current.

The equivalent capacitance C_{eq}, is given then by equation (2.4). Different multiplication values may be obtained varying either R_{x2} or the ratio R_{x2}/R_{x3}, these values are tuned by the bias currents.

$$C_{eq} = n\frac{R_{x2}}{R_{x3}}C \tag{2.4}$$

Simulation results using the transistor level realizations given in the reference article have shown that below 3 MHz the circuit is temperature insensitive, has higher frequency limitations due to parasitic elements and a power dissipation of 7.3 mW at ±2.5 V supply voltages.

On the downside, the design is not suitable for low frequency applications. Moreover, the circuit cannot sense lower values of capacitance C, so the performance requires a large value for the grounded load capacitor. The authors indicate that their attempts to lower this value degraded performance.

Another model that exploits current mode techniques through OTAs is in Figure 2–4 [10].

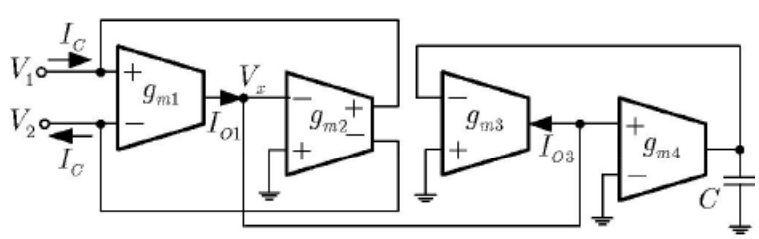


Figure 2–4: Floating Capacitance Multiplier with OTAs [10]

For this circuit, the input impedance Z_{in} is given by equation (2.5),

$$Z_{in} = \frac{V_1 - V_2}{I_c} = \frac{g_{m3}g_{m4}}{sCg_{m1}g_{m2}} \tag{2.5}$$

and the equivalent capacitance in equation (2.7) is dependent on the ratio of transconductance gains given in a general expression as,

$$g_m = \frac{I_B}{2V_T} \tag{2.6}$$

Therefore, its value is controlled by the OTA bias current I_B when the thermal voltage V_T is constant.

$$C_{eq} = \frac{g_{m1}g_{m2}}{g_{m3}g_{m4}}C \tag{2.7}$$

This paper deserves a special comment. The authors report in Figure 6 (Figure 2–5) of their paper that the circuit works for a frequency bandwidth between 1 Hz to 3 MHz for a multiplication factor of 1000 and a 10 pF load capacitor.

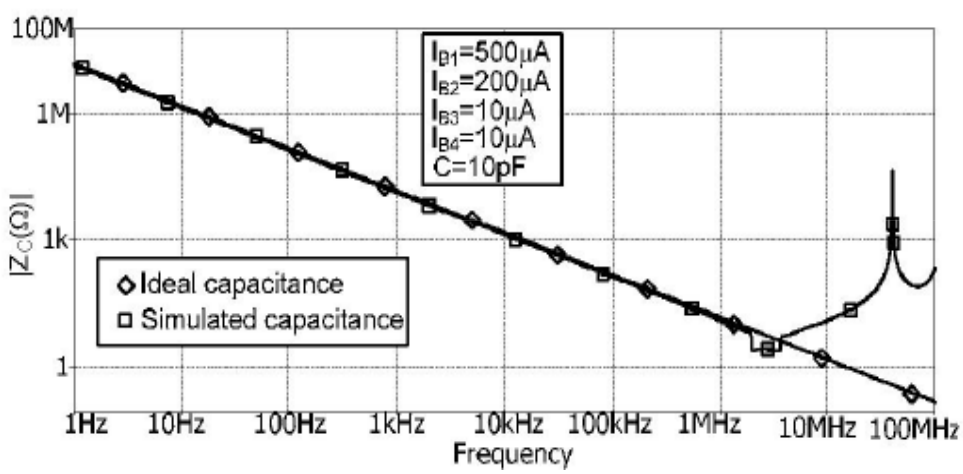


Figure 2–5: Figure 6 in Jaikla's work [10]

Since these results are in contradiction with the analysis realized in this thesis and presented in Chapter 3, the simulation was repeated here. The result of this simulation, using the same parameters presented by the authors, is shown in Figure 2–6. Here, we see that the multiplier works between 10 kHz up to 3 MHz with an offset between the ideal and the simulated capacitance. These results are in agreement

with the predictions made in Chapter 3 of this thesis, contradicting the authors' claims. These findings were reported to the authors, who reviewed their work and acknowledged the error [1]

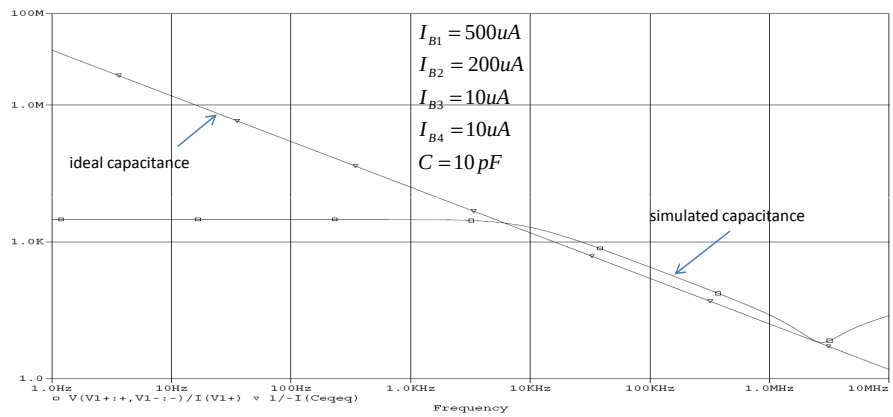


Figure 2–6: The repeated simulation

The model shown in Figure 2–7 combines current and voltage mode techniques to develop a grounded capacitance multiplier [9], offering a variation for the Miller effect.

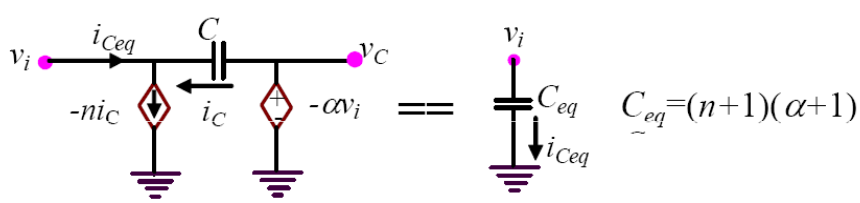


Figure 2–7: Grounded Capacitance Multiplier [9]

Here, M = (n+1)(α+1) is the multiplication factor. The current source connected between input and ground introduces a high resistance to avoid leakage current. Unfortunately, stability problems arise from the small floating capacitor connected between input and output.

[1] private communication from Prof.Jaikla

Further problems are found when looking into the transistor realization. Figure 2–8 shows a simplified schematic of the multiplier and Figure 2–9 its final implementation.

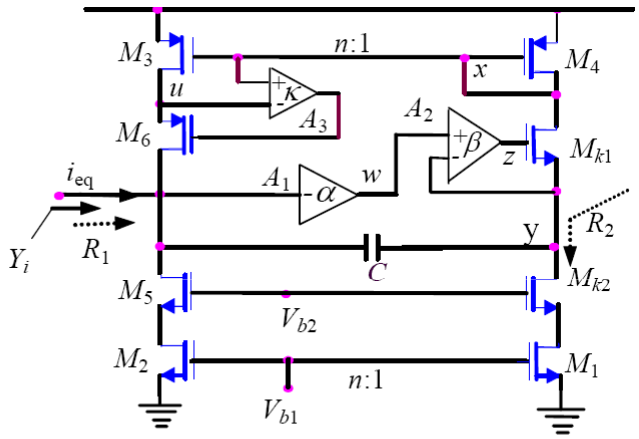


Figure 2–8: Capacitance Multiplier in [9]

To obtain practical values of equivalent capacitance a large gain for A_1 is required, resulting in an increase of the M factor with more power dissipation as a consequence. Also, the value of C has to be increased to keep stability of the circuit, resulting in a large area occupation.

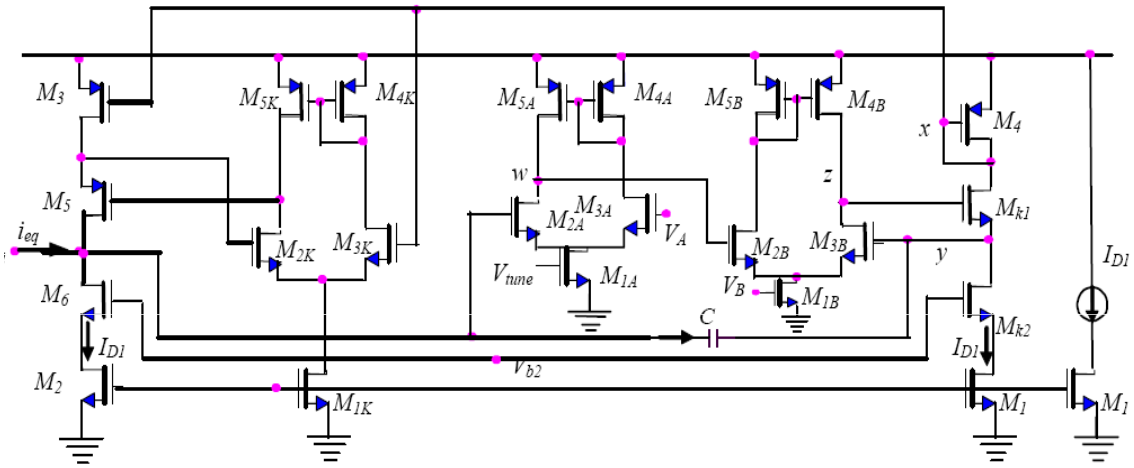


Figure 2–9: Final realization of the modified Miller topology [9]

In the complete schematic, the voltage V_{tune} is used for adjusting A_1, providing a range of equivalent capacitances that goes from 1.22 nF to 5.5 nF. A main drawback here is a large leakage current, in the order of 1 μA to 3 μA. Moreover, linear behavior

has a strong dependence on high voltage swing limiting the dynamic rage in V_{tune} from 1.3 V to 2.3 V.

The grounded capacitance multiplier based on impedance scaler in Figure 2–10 was proposed [11]. The circuit works as follows: transistor $M1$ senses the current flowing from the capacitor C and mirrors it through transistor $M5$ with a gain of $1 : M$ ($M = 25$ in the Figure). By applying a small voltage variation in node A there will be a current variation M times larger than the one provided by C. This returns in a smaller impedance seen from node A.

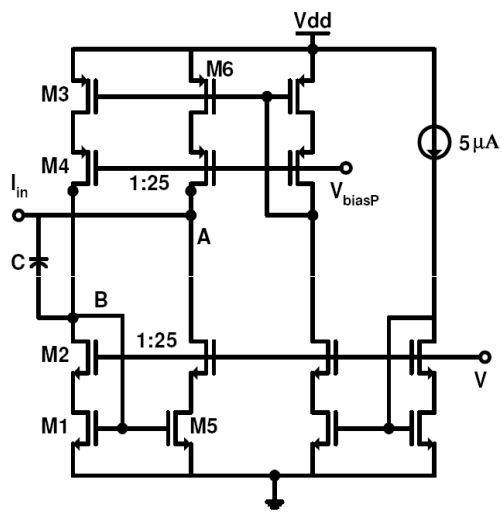


Figure 2–10: GCM using Scaler concept [11]

The equivalent capacitance described in equation (2.8) has resulted from the multiplication factor $(M + 1)$ and the grounded capacitor.

$$\frac{1}{sC_{eq}} = \frac{1}{s(M+1)C} \tag{2.8}$$

Some of the problems for this circuit arise from the fact that the finite output impedance at low frequency draws more leakage current and therefore increases the power dissipation. At higher frequencies the output impedance introduces a nonlinear factor. In summary, this grounded capacitance multiplier will work from 100 Hz up to 1 MHz.

Petchakit et al. [12] proposed the two floating capacitance multipliers in Figure 2–12 based on the model in Figure 2–11.

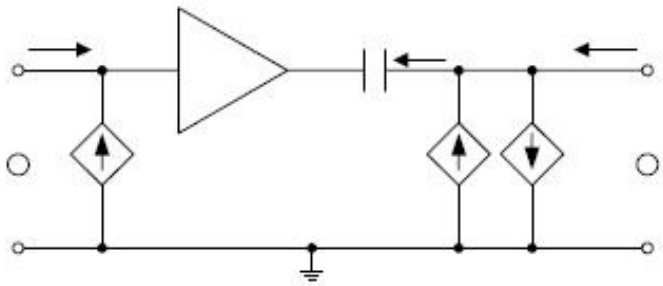
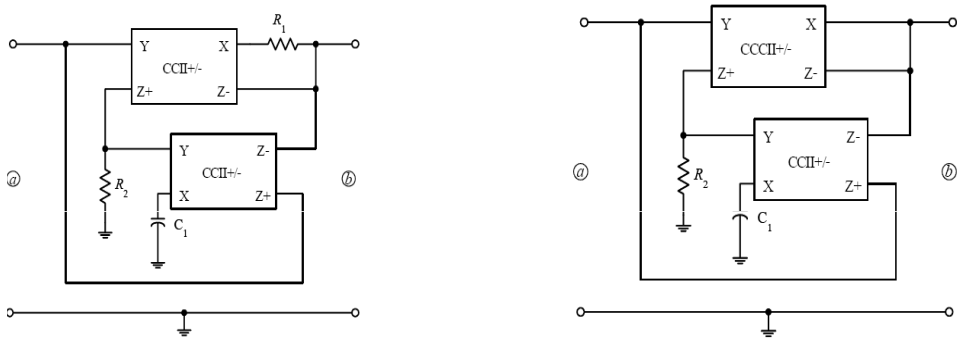


Figure 2–11: Capacitance Multiplier model in [12]



(a) (b)

Figure 2–12: (a)CCII±s based a floating capacitance multiplier,(b)The electronically tunable floating capacitance multiplier [12]

The first multiplier shown in Figure 2–12a consists of two CCIIs± (each one implemented by the circuit in Figure 2–13), two external resistances R_1 and R_2, and a grounded capacitor. The equivalent capacitance, given by equation (2.9), can be tuned by either R_2 or the ratio R_2/R_1, but does not allow electronic tunability.

$$C_{eq} = \frac{R_2}{R_1}C \tag{2.9}$$

In a second implementation, Figure 2–12b, one CCII± has been substituted by a CCCII± [12] to allow the passive resistance R_1 to be replaced by the CCCII

intrinsic resistance R_x, which can be tuned by the CCCII bias current I_0.

$$R_x = \frac{V_T}{2I_0}C \tag{2.10}$$

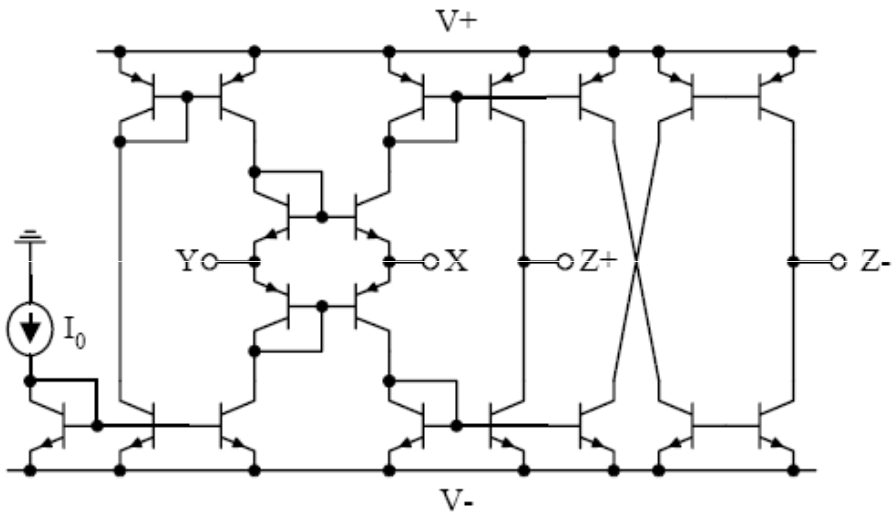


Figure 2–13: Second Generation of Current Conveyor (CCII±)

However, passive elements were not eliminated at all and for high multiplication factors it may become impractical for integration.

H.Y. Darweesh et.al. proposed designs for grounded and floating capacitance multipliers based on current multiplier cells (CMC) [13],[14]. The CMC cell consists of cascaded CMOS inverters and an operational amplifier as shown in Figure 2–14.

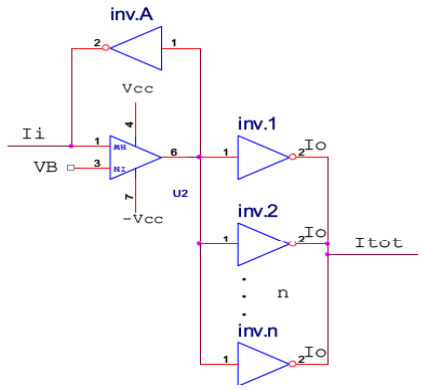


Figure 2–14: Proposed CMC cell [13]

The CMC cell in Figure 2–15 is defined by equations given in matrix form by (2.11). The I_Z (or I_{tot}) current has resulted from the multiplication of I_X (or I_i) by the number of output loaded inverters n.

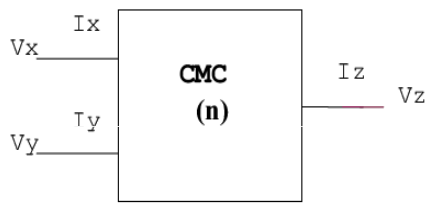


Figure 2–15: Block diagram of CMC [13]

$$\begin{pmatrix} V_x \\ I_z \\ I_y \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & n & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix} \tag{2.11}$$

For the grounded multiplier in Figure 2–16 [13], applications are constrained to low voltage and low power applications (LVLP). Yet, the circuit does not offer tunability since its equivalent capacitance is subject to the number of inverters (in this design there were 10 inverters in each CMC cell) which has incremented by using two CMC stages. Therefore, with a grounded capacitor of 1 pF the circuit can only yield an equivalent capacitance of 100 pF, which is still very low.

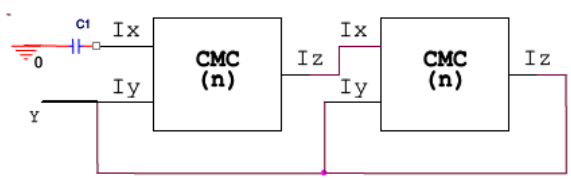
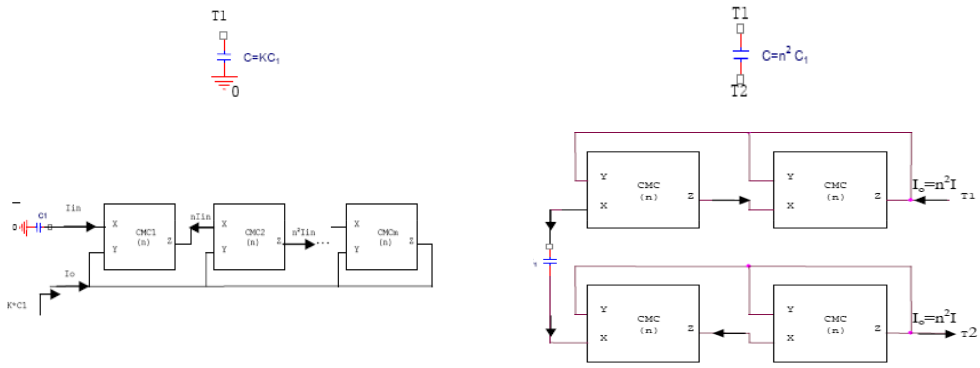


Figure 2–16: Active capacitance multiplier structure [13]

The CMC cells are also used to develop two additional capacitance multipliers [14]. The grounded and floating capacitance multipliers are shown in Figures 2–17a and 2–17b on the next page. Both configurations offer poor control of the multiplication factor and thus are not appropriate for many applications which may require

a wide range of capacitance values of capacitance. The small floating capacitor in the second configuration adds additional parasitic elements.



(a) (b)

Figure 2–17: Realizations for: (a) Grounded capacitance, (b) Floating capacitance [14]

Negative impedance converter (NICs) were also employed for the multipliers in Figures 2–18 and 2–19 [15].

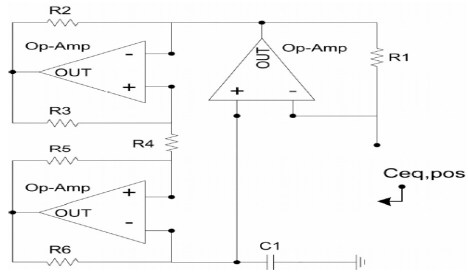


Figure 2–18: Grounded positive capacitance multiplier [15]

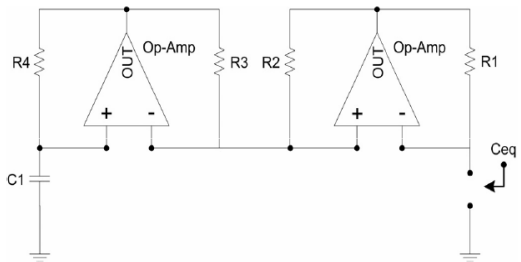


Figure 2–19: Positive grounded capacitance multiplier in double bridge configuration [15]

The circuits are able to operate at very low frequencies, between 159 Hz down to 400 mHz. Unfortunately, electronic tunability is not accomplished. The equivalent

capacitance in equation (2.12) is dependent on resistor values which is undesirable due to the fact that passive elements occupy more area and also introduce significant source of errors.

$$C_{eq} = C_1 \frac{R_4 R_2}{R_3 R_1} \tag{2.12}$$

In Figure 2–21, the CMOS capacitance multiplier [16] works as follows: Transistor $M1$ is a voltage follower. The current through capacitance C is sensed by transistor $M2$. Thus $M4$ will reply the current seen by $M2$ sending it to the current mirror $M5 - M7$. The gate in transistors $M1$ and $M3$ are connected together to the input in order to keep same electrical conditions. In this way, the current sensed from C will be more accurate.

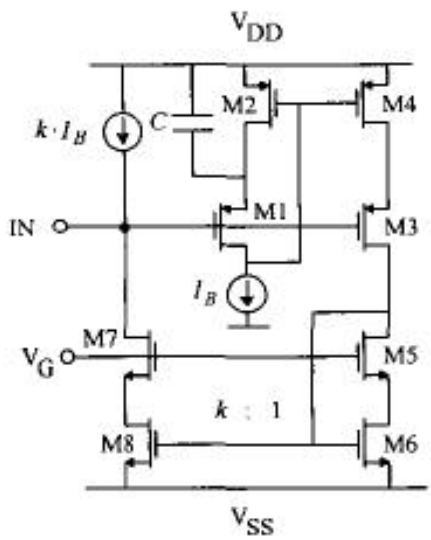


Figure 2–20: Basic idea of the proposed capacitance multiplier [16]

Unfortunately, power dissipation and quiescent current are proportional to the multiplication factor. To overcome this problem a new scheme was introduced in Figure 2–21. Now, the multiplication factor k is the product of three current gains: k_1, k_2, k_3, but the quiescent current is kept constant, equal to I_B.

$$k = k_1 k_2 k_3$$

The total output current satisfies,

$$I_{Qtot} = (4 + k_1 + k_2 + k_3)I_B$$

instead of that obtained by the circuit in Figure 2–21,

$$I_{Qtot} = (2 + k_1k_2k_3)I_B$$

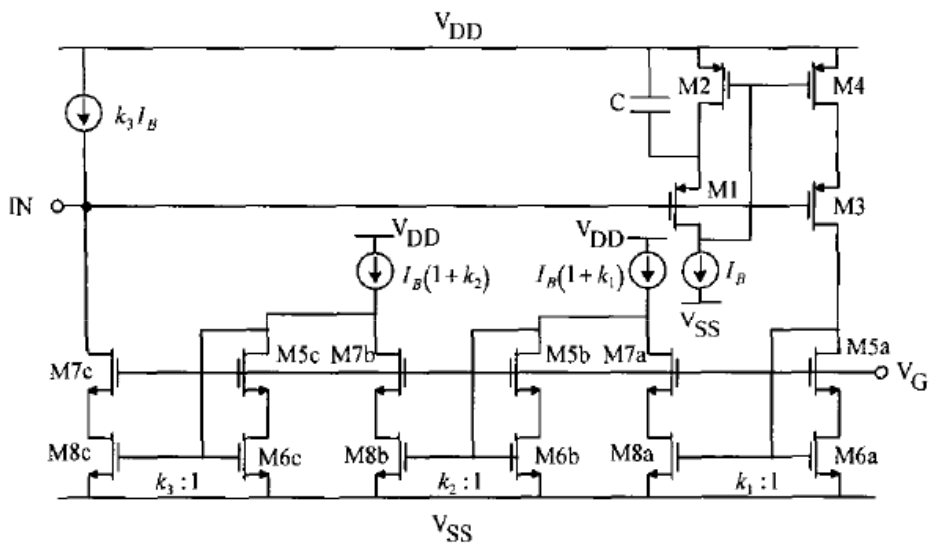


Figure 2–21: Improved capacitance multiplier [16]

For the last current mirror, the tuning circuit in Figure 2–22 is used. Here, when V_{tune} is negative (positive), then I_{out} will be lower (greater than I_{in}). The latter is due to the effect on the transconductance at $M8$ which becomes lower (greater) than that of $M7$. If V_{tune} is zero, balance condition occurs.

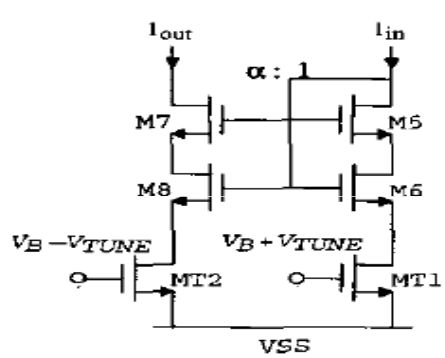


Figure 2–22: Tuning technique using triode biased transistor [16]

Some problems that are still present in the improved multiplier are offset and gain errors. The first is due to the fact that the circuit is working at high frequencies, where the input parasitic capacitance effect is not negligible. The gain error is introduced by the transfer gain of the current mirror (see Table 1 in [16]). Moreover, a main drawback is that realization of larger equivalent capacitances increases power dissipation.

Other solutions [17] based on current gain capabilities of the CCIIs are in Figures 2–23 and 2–24. The first topology is not realizable when larger values of capacitance are required, since its power dissipation is proportional to the multiplication.

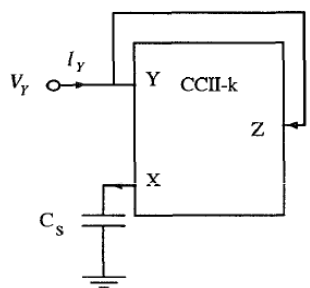


Figure 2–23: Single-CCII based capacitance multiplier [17]

A second solution in Figure 2–24 consists of two CCIIs with two resistors for tuning the multiplication factor.

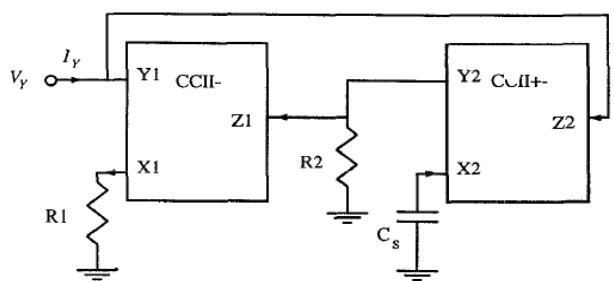


Figure 2–24: Second solution employing two CCIIs [17]

The circuit provides a maximum gain factor of up to 10^5 obtained from a maximum resistance ratio of up to 10^3 and the fixed gain at the CCIIs of 10. Although both circuits offer good accuracy with a 1 pF grounded capacitor, power dissipation is still one of the main drawbacks. Moreover, the circuits do not have electronic tunability.

Another design [18] has included COAs (Current Operational Amplifier) and CCIIs for implementing a low supply voltage capacitance multiplier.

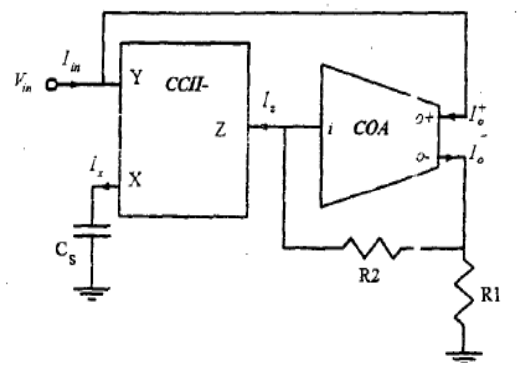


Figure 2–25: Capacitance Multiplier based on COA and CCII [18]

The COA offers a very low gain not allowing the circuit to obtain large equivalent capacitances. Also, due to voltage and current transfer inaccuracy of the conveyor, the equivalent capacitance deviates from the expected value. Moreover, the multiplication factor is severely limited by the finite resistance at the input terminal x, the bandwidth limitation of the COA and the finite output resistance. Lastly, the multiplication factor is tuned using two resistors which, as mentioned before, results in an increased power dissipation.

In [19], the current conveyor in Figure 2–26 is used as a voltage amplifier. Due to the floating capacitor, a stability problem arises that will also limit the bandwidth. The circuit has reported equivalent capacitances for high frequency in the range of 10 pF up to 4 nF when a floating capacitor of 8 pF is used. As before, tuning is realized by passive resistors.

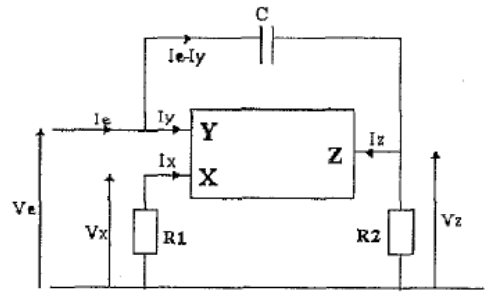


Figure 2–26: Capacitive multiplier implementation [19]

2.3 Summary

The work discussed above shows when current mode techniques are used to obtain high gain factors, there is a correlation between the equivalent capacitance values and power dissipation.

Other works have used floating capacitors which introduced unstable behavior. Offset errors between the equivalent capacitances and the theoretical expected arise from the equivalent input resistance that is in parallel with the equivalent capacitive impedance. Since the resistance is not high enough, it can not be discarded.

Most works in the literature have shown an excessive use of passive/active elements for tuning the multiplication factor, yielding a high power dissipation which make these designs impractical for integration.

There are several works that use current mode techniques and are designed for the high frequency range. The main drawback of these current mode blocks is that they do not offer larger gain factors, thus the current at the capacitor to be increased by multiplying is more dependent on the frequency range than on the multiplication factor. This latter is not desirable, since most applications of capacitance multipliers are in low frequency.

CHAPTER 3
FLOATING CAPACITANCE MULTIPLIER MODEL

This chapter introduces a system view for capacitance multipliers, thereby providing an overview on limitations and possibilities. Most results and conclusions in this chapter are a contribution of this research. Some results may be inferred from isolated works in literature, but they have not been explicitly stated and were presented under a different context. In this sense, even for those results, the organized mathematical derivation presented here may be considered a contribution.

3.1 Capacitance and Capacitors

A brief review on capacitance and capacitors is given to put the objectives of simulation in perspective.

3.1.1 Ideal capacitance

The linear capacitance whose symbol is shown in Figure 3–1 is an ideal circuit model defined by

$$i = C\frac{dv}{dt} \tag{3.1}$$

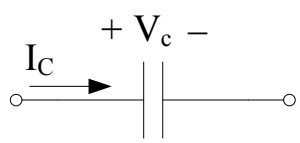


Figure 3–1: Ideal Capacitance Model

The capacitance is measured in Farads (F). In voltage terms, for any t_0 and $\Delta t \geq 0$,

$$v(t_0 + \Delta t) = \frac{1}{C} \int_{t_0}^{t_0+\Delta t} i(t)dt \; + v(t_0) \tag{3.2}$$

From equation (3.2), it is found [20] that if the current is bounded then the voltage is a continuous function of time, because $v(t_0 + \Delta t) \rightarrow v(t_0)$ when $\Delta t \rightarrow 0$. Also, if $i = 0$ A, then $v(t_0 + \Delta t) = v(t_0)$, which means that an ideal capacitance maintains the charge forever when disconnected. Similarly, the capacitance supports rapid changes of current.

When a charged capacitor is connected to a resistance R in parallel (Figure 3–2), the capacitance is discharged according to

$$v(t) = V_0 e^{-t/RC}, \quad t > 0 \tag{3.3}$$

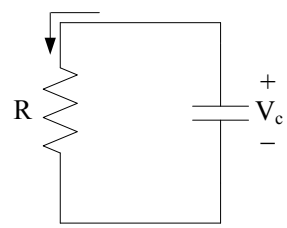


Figure 3–2: Discharging Capacitance

Here, V_0 is the capacitance voltage at $t = 0$ s, when the capacitor is connected to the resistance, and $\tau = RC$ is called time constant. For all practical purposes, the capacitance is discharged in four to five time constants.

In the frequency domain, the impedance Z is the ratio of the voltage V to the current I. It is expressed as

$$Z = \frac{V}{I} \tag{3.4}$$

For a capacitor the impedance Z_C has only a reactance component X_C.

$$Z_C = \frac{1}{sC} \quad X_C = -\frac{1}{2\pi f C} \tag{3.5}$$

The frequency response of the impedance for an ideal capacitance is therefore a straight line with a slope of -20 dB/dec.

For an ac voltage of amplitude $|V|$ and frequency f Hz, the current amplitude $|I|$ is given by

$$|I| = 2\pi f C|V| \tag{3.6}$$

3.1.2 Real capacitors

Real capacitors have characteristics determined by the dielectric properties, the assembly structure, frequency of operation, etc. Losses due to leakage currents when a capacitor is used on DC prevent indefinite storage capacity. The time constants of discharge may go from several days, as in the case of discrete Polystyrene capacitors [21] to nanoseconds in integrated circuit capacitors. Moreover, at very low and very high frequencies, there is an increase of loss which sets a limit to the practical use of a capacitor.

Figure 3–3: Low Frequency simple models for Capacitors : (a) Single resistance; (b) Shunt and series resistance

Practical capacitors may be modeled in different ways. Two simple models are given in Figure 3–3. The resistances in these models are actually frequency dependent, but for the purpose of this discussion they may be considered constants. The resistance in series with the capacitance is called Equivalent Series Resistance (ESR). For Figure 3–3a, the impedance is given as

$$Z_1 = \frac{R_p}{sCR_p + 1} \tag{3.7}$$

The frequency response is shown in Figure 3–4. Notice that as $R_p \to \infty$, the subcircuit behaves as a pure capacitance. The same is true for frequencies above the pole $1/R_pC$, where the resistance value is much greater than the reactance. However, from the Figure we see that the pure capacitance behavior at higher frequencies does not correspond to the pure capacitance case; there is a small difference.

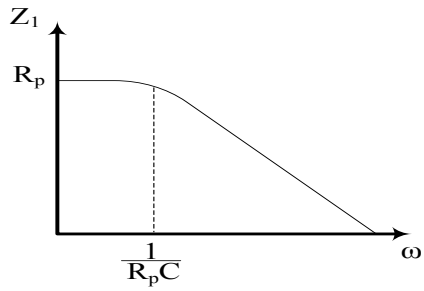


Figure 3–4: Frequency Response for Z_1

For the model of Figure 3–3b, the impedance is given by equation (3.8) with the frequency response shown in Figure 3–5, with a frequency region where the circuit can be approximated by a pure capacitance behavior. Notice the presence of the zero which occurs at high frequencies.

$$Z_2 = \frac{R_p\left(R_sCs+1\right)}{\left(R_s+R_p\right)Cs+1} \tag{3.8}$$

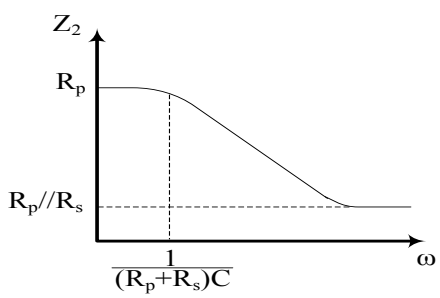


Figure 3–5: Frequency Response for Z_2

3.1.3 IC Capacitors

Integrated circuit capacitors are limited to relatively low values. With a density of 1 fF/μm^2 for sub-micron CMOS, for example, capacitors of 20 pF or 100 pF occupy an area equivalent to thousands of transistors or hundreds of operational

amplifiers [8]. In addition, they introduce parasitic capacitances of significant value between the terminals and ground. A good model for IC capacitors is shown in Figure 3–6 [22].

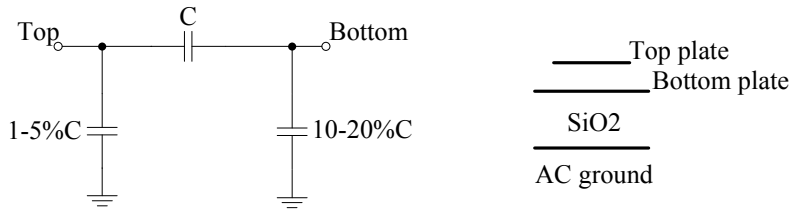


Figure 3–6: Equivalent circuit for an IC capacitor [22].

The IC capacitor model shows one of the main problems with floating capacitors as found in several realizations, namely, the presence of additional parasitic capacitances. For an ideal model this is actually not a problem. Unfortunately, parasitics play a very important role in setting limitations for low frequency applications too, as we will see later.

3.2 Considerations on simulated capacitors

Equivalent impedances comply with the mathematical restrictions put on the equations that relate voltages and currents in the simulated element. However, it is an error to assume that the physical properties are also preserved. For example, it is impossible to create an electromagnet with a simulated inductance. This should be taken into consideration when talking of a multiplied capacitance. In particular, we have the following considerations to look after [8].

a) Energy storage cannot be improved, and

b) Current cannot be supplied instantaneously.

In other words, although the capabilities of the on-chip capacitor are enhanced through the use of transistors, there is required greater time response for sudden current changes. This is different to real capacitors which support better such changes.

3.3 Capacitance Multiplier: two port description

After reviewing the necessary equations for two-ports, the concept of a multiplier as a terminated two-port is reviewed from the ideal point of view. This type of realization is convenient for grounded simulations.

3.3.1 Two-port equations

We start by considering a multiplier as a terminated two-port network, like the one in Figure 3–7. The two-port can be described with the chain parameters by equations (3.9a) and (3.9b) or in matrix notation as (3.10).

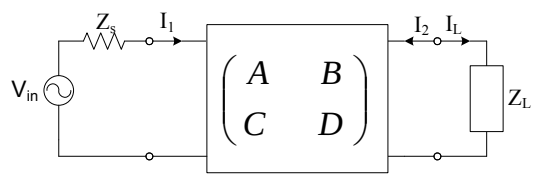


Figure 3–7: General form of terminated two-port Network

$$V_1 = AV_2 - BI_2 \tag{3.9a}$$

$$I_1 = CV_2 - DI_2 \tag{3.9b}$$

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{3.10}$$

Here, the A,B,C, and D parameters, also named chain parameters, are defined by equations (3.11a) to (3.11d).

$$\frac{1}{A} = \left.\frac{V_2}{V_1}\right|_{I_2=0} \tag{3.11a}$$

$$\frac{1}{B} = \left.\frac{-I_2}{V_1}\right|_{V_2=0} \tag{3.11c}$$

$$\frac{1}{C} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \tag{3.11b}$$

$$\frac{1}{D} = \left.\frac{-I_2}{I_1}\right|_{V_2=0} \tag{3.11d}$$

Focusing on the input impedance seen at the terminals of the two-port, which can be expressed as

$$Z_{in} = \frac{AZ_L + B}{CZ_L + D} \tag{3.12}$$

impedance multiplication requires B = C = 0, getting

$$Z_{in} = \frac{A}{D} Z_L \tag{3.13}$$

The two-port with this characteristics, is called Positive Generalized Impedance Converter(GIC) [23] or scalors [24].

3.3.2 Realization of the Positive Impedance Converters

For different conditions for the chain parameters, different situations may be considered for realizing a GIC.

1. General Case: Using

$$A = \frac{1}{\alpha} \text{ and } D = \beta \tag{3.14}$$

the general case shown in Figure 3–8a can be realized. Figure 3–8b shows the terminated case, where $-I_2$ is already changed into I_L.

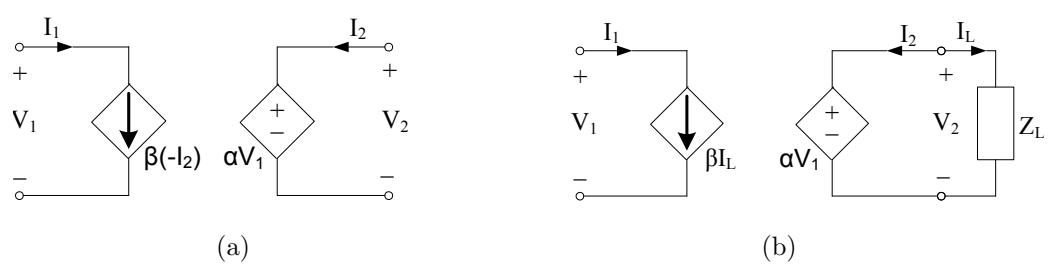


Figure 3–8: (a)General GIC Implementation; (b) terminated GIC

For this case the input impedance (3.13) can be rewritten in the form (3.15).

$$Z_{in} = \frac{Z_L}{\alpha\beta} \tag{3.15}$$

The current and voltage modes arise as particular cases of the general impedance converter.

2. Current mode case: Using

$$A = 1 \text{ and } D = 1 + \beta \tag{3.16}$$

the realization shown in Figure 3–9a is obtained. Figure 3–9b shows the terminated case, where the current mode topology for multipliers is recognized.

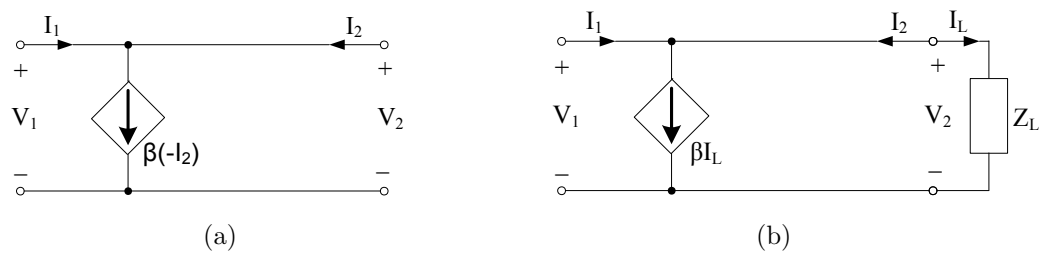


Figure 3–9: (a) Current mode two-port; (b) terminated GIC

For this case the input impedance (3.13) can be rewritten in the form (3.17).

$$Z_{in} = \frac{Z_L}{1+\beta} \tag{3.17}$$

3. Voltage mode case: Using

$$A = \frac{1}{1+\alpha} \text{ and } D = 1 \tag{3.18}$$

the realization shown in Figure 3–10a is obtained. Figure 3–10b shows the terminated case,

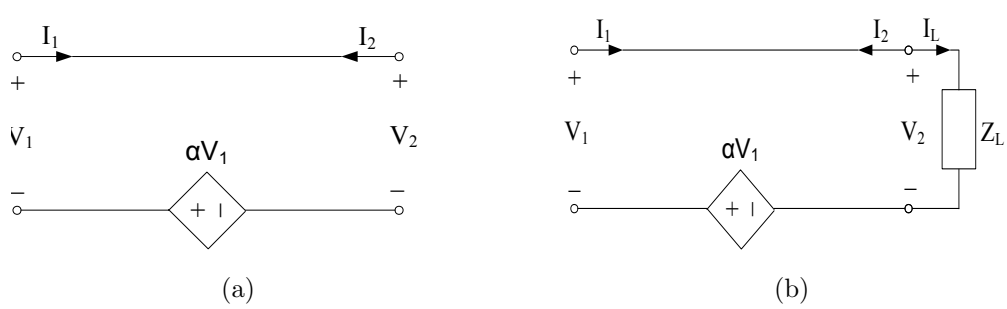


Figure 3–10: (a) Voltage mode two-port; (b) terminated GIC

where the voltage mode topology for multipliers will be recognized after redrawing the circuit as it is done in the next section.

For this case the input impedance (3.13) can be rewritten in the form (3.19).

$$Z_{in} = \frac{Z_L}{1+\alpha} \tag{3.19}$$

3.4 Capacitance multipliers models from GIC converters

When the load is a capacitor C_L, the previous input impedance equations yield the expression by which the capacitance is multiplied when $Z_L = 1/sC_L$ is introduced. On the other hand, the multiplier itself may be grounded or floating. By grounded multiplier it is meant that the equivalent capacitance seen from port 1 has one terminal connected to ground; the other port may or may not be grounded. A floating multiplier mimics a floating equivalent capacitance from port 1, with no terminal connected to ground. Both cases are treated separately next.

3.4.1 Grounded Capacitance Multiplier Model

The grounded multiplier versions are presented in Figure 3–11. These are obtained by substituting the load Z_L by a capacitance C_L in the respective cases. The voltage mode case has been redrawn in the more familiar form of Miller configuration.

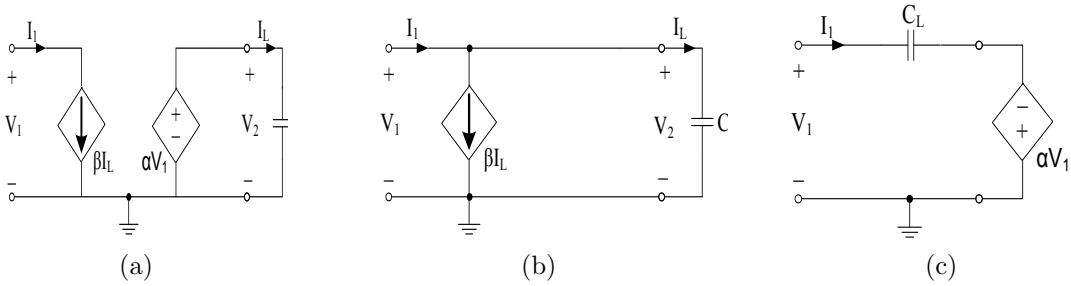


Figure 3–11: Grounded Capacitance Multipliers: (a) General case; (b) current mode; (c) voltage mode

Each realization yields an equivalent capacitance given as follows:

For the general case:

$$C_{eq} = \alpha\,\beta\,C_L \tag{3.20a}$$

For the current mode case:

$$C_{eq} = (1+\beta)\,C_L \tag{3.20b}$$

And for the voltage mode case:

$$C_{eq} = (1+\alpha)\,C_L \tag{3.20c}$$

3.4.2 A Floating Capacitance Multiplier Model based on GIC Converter

The objective now is to obtain a floating capacitance multiplier, that is, to emulate a floating capacitance. The current mode and voltage mode positive converters do not allow a direct realization unless floating dependent sources and capacitances are used, a fact highly undesirable. To reduce parasitic effects, the goal should be such that sources and load capacitances are grounded whenever possible. This constraint also restricts the two port GIC to be used directly as it was the case for grounded realization; since a floating source is required.

To better attack the problem, this may be restated turning the attention toward the use of three terminal networks. In particular for this thesis, the interest is in terminating one of the three terminals with a grounded capacitor only, so the current at this terminal becomes the capacitance current, and the potential at the terminal is the same as the one for the capacitance. The other two terminals are then used to simulate the impedance of interest, in which case the current entering to one of the terminals must leave the other. With this in mind, it is expected that a configuration like the one shown in Figure 3–12a can be used to emulate the two-port (or three

terminal) shown in Figure 3–12b for a floating capacitance, defined by

$$I_1 = -I_2 \text{ and } V_1 - V_2 = (1/sC_{eq})I_1 \tag{3.21}$$

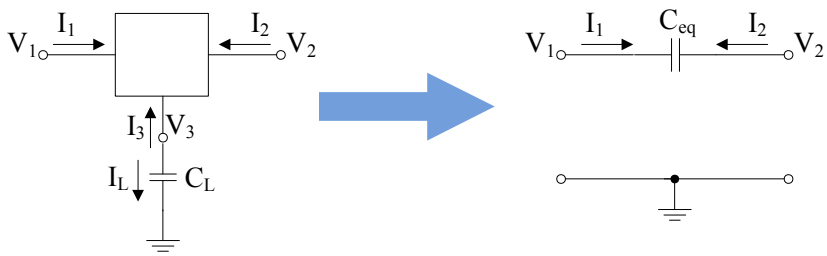


Figure 3–12: Scheme for the floating capacitance realization

One way to achieve this goal is as follows:

Step 1: Start with the general GIC two port realization of Figure 3–11a, grounding the output port, that is, and make it a three terminal subnetwork terminated at terminal 3 with C_L. The terminals of the current source become terminals 1 and 2 of the subnetwork, so the input voltage now is given by $V_{in} = V_1 - V_2$. Mathematically, this is the only change that occurs with respect to Figure 3–8b. Since ground does not affect mathematical results of this type, the equivalent capacitance seen between terminals 1 and 2 is still given by (3.20a).

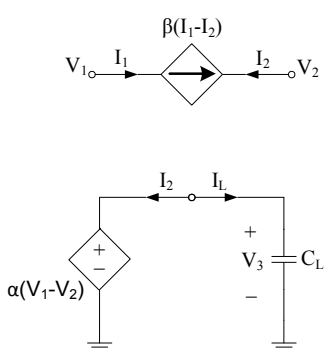


Figure 3–13: First step to convert toward floating multiplier

Step 2: Apply the current source shifting theorem [20] illustrated in Figure 3–14 to the dependent current source of Figure 3–13. The result is shown in Figure 3–15.

Figure 3–14: Current source shifting theorem [20].

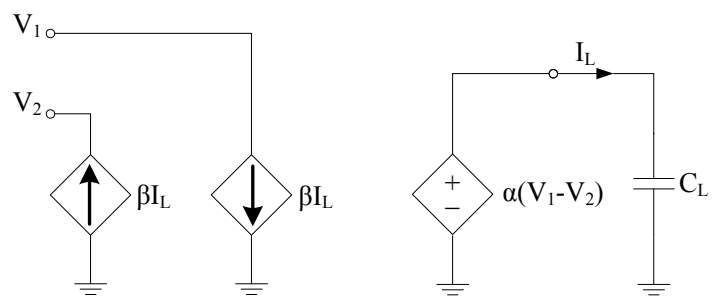


Figure 3–15: Ideal Floating Capacitance Multiplier Model

Since none of the circuit transformations presented changes the mathematics involved, the final result behaves like a capacitance between terminals 1 and 2, characterized by,

$$I_1 = -I_2 = s\beta\alpha C_L(V_1 - V_2) \tag{3.22}$$

yielding an equivalent floating capacitance

$$C_{eq} = kC_L \quad k = \alpha\beta \tag{3.23}$$

This is the same expression as the one obtained for the grounded case in (3.20a), to be expected considering the way in which the configuration was derived.

3.5 Analysis on constraints

The models derived in the previous sections are ideal ones realizing a perfect multiplier. We now look into the practical issues. First, a look into the frequency constraints for realization and then into the parasitic effects. For the latter objective, we concentrate on the general systems view using macromodels.

3.5.1 Frequency constraints

When realizing dependent sources by means of amplifiers or any other method, the parasitic capacitances present in transistors will certainly limit the operation at higher frequencies. Now, in the very low frequency range, which has appeared to be of great importance as a goal, capacitance multipliers methods have consistently failed as it was pointed out in the literature review. Moreover, on-chip load capacitances have also been too "large", in the several tens to hundred picofarads range. These obstacles are not accidental and have an explanation as seen next.

The current amplifiers used in the general GIC configurations, both grounded and floating realizations, have as input the current in the load capacitor. This current is given as

$$I_L = s\, C_L\, V_L$$

where s is the complex frequency and the capacitor voltage V_L is obtained from the output of a voltage amplifier, that is, a voltage dependent source. Now, for one frequency f, $s = j\,2\pi f$, the magnitude of this current becomes

$$|I_L| = 2\pi f C_L\, |V_L|\,. \tag{3.24}$$

The voltage applied to C_L is the output of a voltage amplifier and thus it cannot exceed the rail to rail value. Being conservative, for "low voltage" circuits, this sets an upper limit of, say, 2 V. On the other hand, the capacitance value corresponds

to a physical on–chip capacitor, so it cannot exceed several tens of pico farads. Let us take as an example 50 pF. For these "large values" we have

$$I_L \leq (0.62 \times 10^{-9})f$$

We see therefore that reducing the frequency takes the current to be amplified down to noise levels, making the results far from reliable or valid. In other words,

as the load capacitance and rail to rail voltage decrease, the applicable minimum frequency of operation has to be increased so as to bring the current amplifier input to acceptable values above noise level.

This result explains the difficulties that previous authors have encountered trying to go into the low frequency range, on the one side, or using low values of load capacitance. Remark again that the upper bound used to illustrate this result has been set with relatively high values of voltage and capacitance. Further restrictions come from other parasitics.

3.5.2 Floating Capacitance Multiplier Analysis Including Parasitic Effects

The realizations for grounded and floating multipliers have assumed ideal dependent sources. However, realistic sources have input and output resistances and capacitances which should be considered. One way to deal with these parasitics is to represent the three terminal subnetwork by its admittance representation. Yet, it is of particular interest to this research to associate the parasitics directly with the realizations of the dependent sources, or amplifiers. The voltage source VCVS can be considered with one input impedance, although a more complex but not necessarily more complete result can be obtained if it is decomposed in the common mode and differential mode input resistances. On the other hand, the two current sources, being complementary, can be considered to come from one "three port" element,

with one input and two outputs. Having said that, Table 3–1 gives the notation for the different parasitics used in the more accurate model of Figure 3–16.

Table 3–1: Parasitics Elements

VCVS	
Input Resistance	R_{12}
Input Capacitance	C_{12}
Output Resistance	r_x
CCCS	
Input Resistance	R_2
Output Resistances	R_{01} and R_{02}
Output Capacitances	C_{01} and C_{02}
At the load	
Output capacitance	C_0

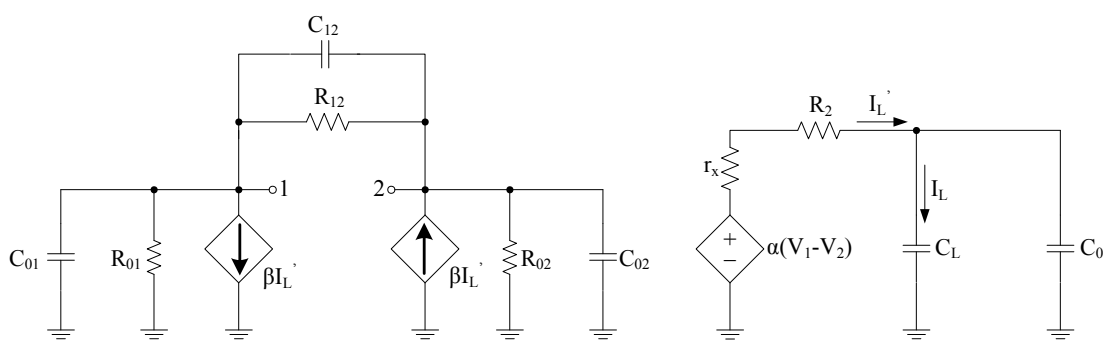


Figure 3–16: Non-Linear Floating Capacitance Multiplier Model

Assuming $C_{0x} = C_{01} = C_{02}$ and $R_{0x} = R_{01} = R_{02}$, the equivalent input impedance Z_{in} becomes

$$Z_{in} = \frac{1}{\frac{1}{2(R_{0x}||\frac{1}{sC_{ox}}}) + \frac{1}{R_{12}||\frac{1}{sC_{12}}} + \frac{s\alpha\beta(C_L+C_0)}{(r_x+R_2)s(C_L+C_0)+1}} \tag{3.25}$$

Analysis for the high and low frequency region are dealt with separately to illustrate the limitations on the circuit.

High Frequency Region

In the high frequency operation the capacitances become dominant and the following approximations are valid:

$$2(R_{0x}||\frac{1}{sC_{ox}}) \approx \frac{2}{sC_{ox}}$$

$$\frac{1}{R_{12}}||\frac{1}{sC_{12}} \approx \frac{1}{sC_{12}}$$

Using these results, (3.25) becomes

$$Z_{in_H} = \frac{s(C_L + C_0)(r_x + R_2) + 1}{(\frac{sC_{ox}}{2} + sC_{12})[s(C_L + C_0)(r_x + R_2) + 1] + 2s\alpha\beta(C_L + C_0)} \tag{3.26}$$

The numerator in Z_{in_H}: $s(C + C_0)(r_x + R_2) + 1$ introduces a zero z_1 expressed as

$$z_1 = \frac{1}{(C_L + C_0)(r_x + R_2)} \tag{3.27}$$

This zero z_1 not only limits the high frequency operations, but also causes a mismatching between V_{C_L} and the voltage amplifier's output, bringing down the magnitude of the current I_L and thereby affecting the achievable equivalent capacitance C_{eq}. I_L is now expressed as

$$I_L = I_C = \frac{\alpha(V_1 - V_2)(s(C_L + C_0))}{(r_x + R_2)s(C_L + C_0) + 1} \tag{3.28}$$

Low Frequency Region

For low frequency operation, parasitic capacitances, C_{12}, C_{0x} and C_0 can be neglected. This is done because typical values for these elements are in the order of

5 to 10 fempto farads and technically their impedance are ∞. This approximation yields the model in Figure 3–17.

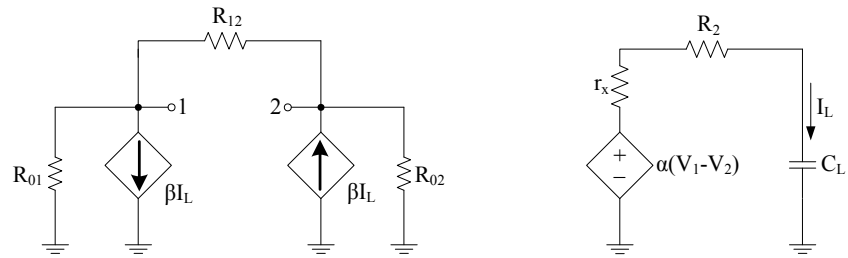


Figure 3–17: Low Frequency Floating Capacitance Multiplier

The equivalent input impedance Z_{in_L} now becomes

$$Z_{in_L} = \frac{1}{\frac{1}{2R_{0x}} + \frac{1}{R_{12}} + s\alpha\beta C} = R_{12}||2R_{0x}||\frac{1}{sC_{eq}} \tag{3.29}$$

Figure 3–18 shows the equivalent circuit representation for this impedance, which it is seen to be of the same form as in Figure 3–3a.

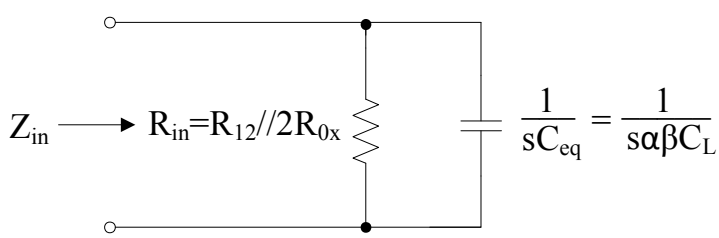


Figure 3–18: FCM Z_{in} for Low Frequency

The most important limitation to consider here is the input pole p_1 shown in 3–19, where

$$p_1 = \frac{1}{R_{in}C_{eq}} = \frac{1}{R_{in}kC_L}$$

Proper operation of a "pure" multiplied capacitance occurs only above p_1. Less than a decade a 3 dB difference may serve as a tolerance limit. The pole can be moved to a very low frequency only if a very large input resistance R_{in} exists, such that,

$$Z_{in_L} = R_{in}||\frac{1}{sC_{eq}} \approx \frac{1}{sC_{eq}}$$

This is not easy to accomplish in a low voltage design without affecting the equivalent capacitance; the same occurs with an increment in the equivalent capacitances. Therefore, there is a trade off between low frequency operation and equivalent capacitance values that may be considered. Notice that this is not a fixed pole, but depends on the multiplication k factor.

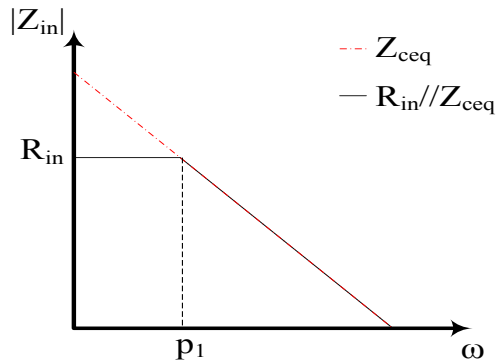


Figure 3–19: Bode Plot for Z_{in}

3.6 A Macromodel simulation for the Floating Capacitance Multiplier in Low Frecuency region

To verify the previous analysis and better understand the low frequency restrictions on multiplier performance, a low frequency macromodel (Figure 3–20) for a floating capacitance multiplier based on Figure 3–17 was developed for simulation with Cadence Pspice.

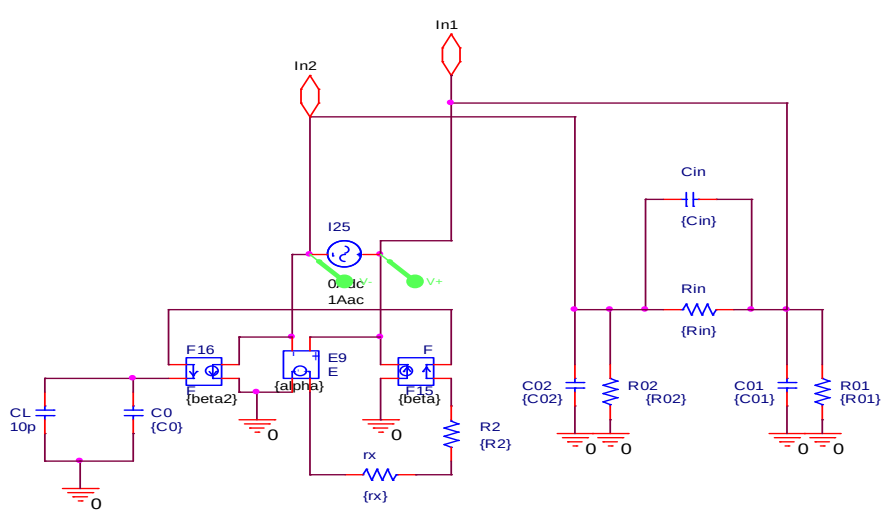


Figure 3–20: Floating Capacitance Multiplier Macromodel

3.6.1 Results of simulation

The simulation results in Figure 3–21 correspond to a k factor of 100 with a load capacitor $C_L = 10pF$. An ideal 1 nF capacitance (in dashed) is used for comparison. It is seen they are similar for frequencies above approximately 300 Hz. The input pole p_1 is limiting low frequency operation creating a cutoff frequency f_L calculated as,

$$f_L = \frac{p_1}{2\pi} = \frac{1}{2\pi R_{in} C_{eq}} = \frac{1}{2\pi(R_{12}||2R_{0x})(kC_L)} = \frac{1}{2\pi(1M\Omega)(100)(10pF)} = 239Hz$$

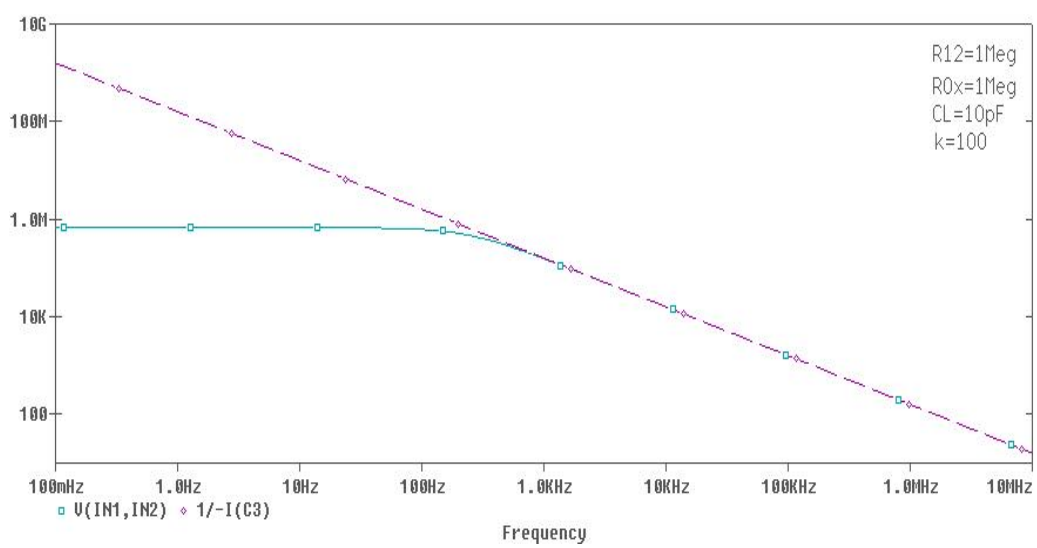


Figure 3–21: Simulation results for a 239 Hz pole

If the input resistance R_{in} is increased, such that,

$$R_{in}||Z_{C_{eq}} \rightarrow Z_{C_{eq}}$$

the floating capacitance multiplier will be able to work at frequencies below 100 Hz. For example, when R_{in} is 10 times larger than the previous value, the low

frequency operation will be 10 times lower. According to it, the circuit is working at frequencies above 24 Hz as shown in Figure 3–22.

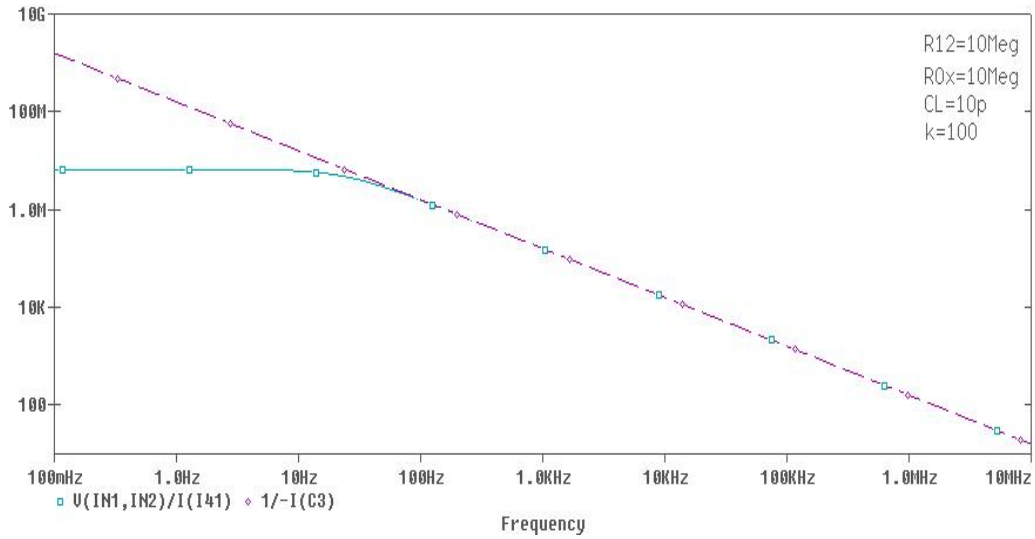


Figure 3–22: Simulation results for a 24 Hz pole

The tunable multiplier factor k also affects the input pole p_1. The lower cutoff frequency decreases when larger k values are used, moving the pole p_1 to the left. This effect is appreciated in Figure 3–23.

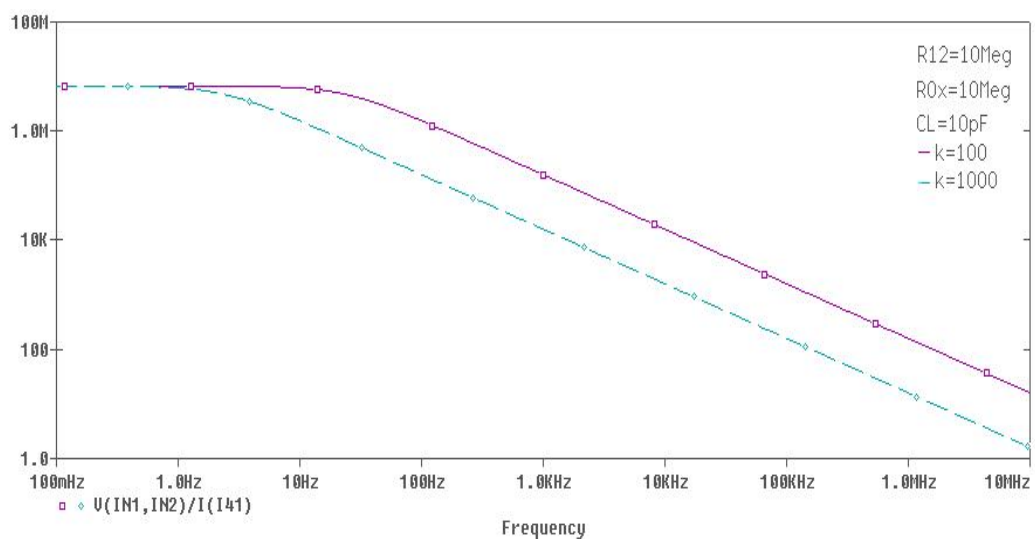


Figure 3–23: Simulation results for different k values

The violet (solid) line is under the same conditions as the blue (solid) line in the previous Figure, such that an equivalent capacitance C_{eq} of a 1 nF value is seen at frequencies above 239 Hz. For the blue line, the k factor is ten times larger, yielding

a 10 nF equivalent capacitance C_{eq} able to work at a frequency of 24 Hz, which is ten times lower than the previous simulation.

High Frequency performance in low frequency low voltage designs

The resistances r_x and R_2 determining the zero z_1 for high frequency response in (3.27) are an output resistance of a voltage amplifier and the input resistance of a current amplifier. They are ideally zero and by hypothesis should be low. However, these resistances are proportional to factors of the form $1/I$ or else V_T/I. In the application intended for IC multipliers working in low frequency, low voltage or low voltage arenas, the current I is in the nano to few micro ampere range. Thus, values of these resistances in the mega ohm range are often encountered.

Figure 3–24 shows the simulation looking at the high frequency effect introduced by the zero z_1. The circuit has a 10 pF load capacitor and $R_2 = r_x = 10M\Omega$. It is seen that for a low frequency application the zero at 1 kHz is indeed of high value, but it is really necessary to increase the load capacitance very much or decrease the resistances, meaning increasing power and voltage supplies values.

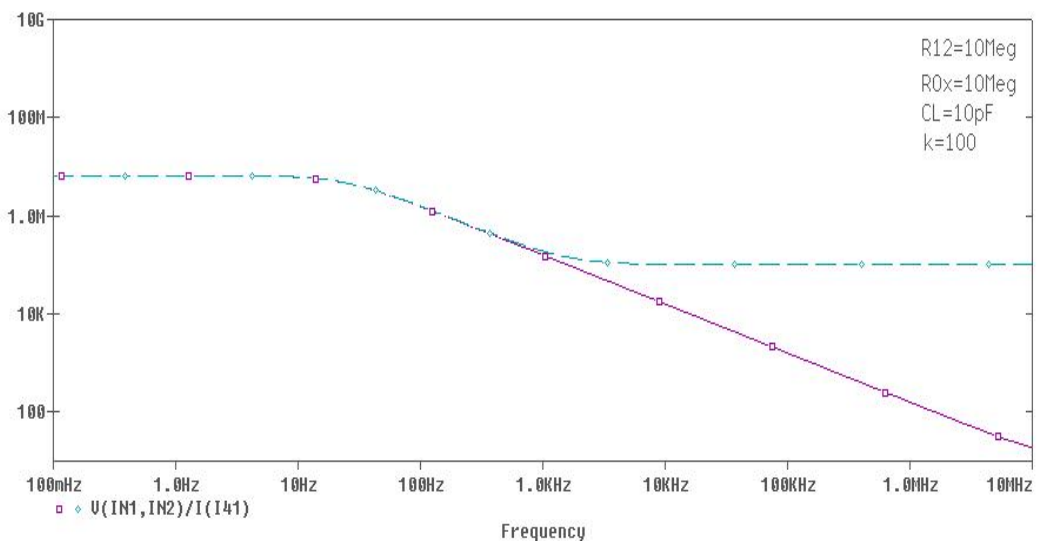


Figure 3–24: Simulation results for high frequency analysis

3.7 A modified three terminal impedance converter

The three terminal realization of Figure 3–15, although theoretically correct, has two serious problems that show up when a direct implementation of the sources is realized in a low frequency design. Namely, the realization will look like the one in Figure 3–25, where the input to the current source is floating and both the input resistance of the current source and the output resistance of the voltage source are in series with the capacitance C_L, limiting the bandwidth of the multiplier, as seen in the previous section. If the current source goes to ground, then the capacitance is floating, which does not solve completely the problem.

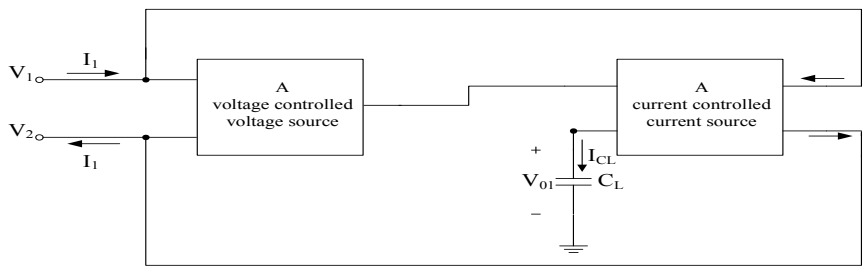


Figure 3–25: A direct realization of Figure 3–15

A possible solution to this problem is shown in Figure 3–26 where a three terminal nullor is introduced. The nullor, which is practically approximated with another realization, isolates the capacitor and the voltage amplifier output. Moreover, it overcomes the additional problems that would arise with a floating input current amplifier.

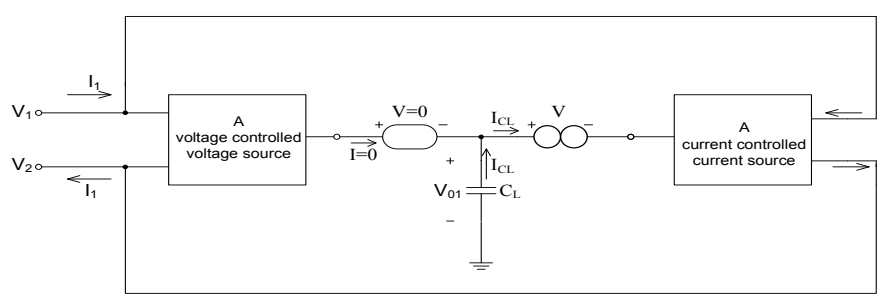


Figure 3–26: A direct realization of Figure 3–15

When the nullor is substituted by, for example a current conveyor, the resistance seen by the capacitance C_L is of a lower value and will push the high frequency limit

to higher bounds. This will become clear with the practical realization in the next chapter.

3.8 Chapter summary

A consideration of capacitance multipliers as two ports or three terminals led the research to show that practically the positive impedance converter is the subnetwork that achieves the goal. It has been known for a long time that this subnetwork can be used for that purpose, but an analysis of the situation has led to the conclusion that in the terminated two port or three terminal topology, it is practically the only option.

An analysis of the system showed the limitations in frequency and parasitic effects. In particular, the realization in the very low frequency presents serious obstacles like the need of high on chip capacitances, large amplifications and rail to rail values, etc. High frequency design is in this respect easier to accomplish. This is perhaps a good reason why almost all works in literature avoid low frequency applications with this technique.

CHAPTER 4
FLOATING CAPACTICANCE MULTIPLIER IMPLEMENTATION

This chapter offers the design of a new circuit realization in which the results of the analysis done in Chapter 3 are used. The design itself has not been thoroughly optimized; it is offered mainly as a proof of concept for the theoretical results when used as a guide for working toward the low frequency range.

4.1 Block diagram and initial constraints

The circuit was designed following the block diagram of Figure 4–1. This diagram follows the guidelines from Section 3.4.2 for the ideal construction, as depicted in Figure 3–15.

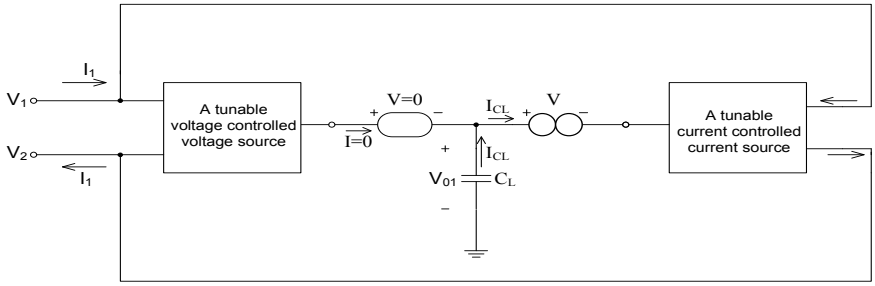


Figure 4–1: Floating Capacitance Multiplier Block Diagram

The voltage controlled source is represented now by the block on the left; the block on the right takes care of the current sources. The nullor, which is practically approximated with a current conveyor block, is introduced for two reasons. One, it isolates the capacitor and the voltage amplifier output. Second, it overcomes the additional problems that would arise with a floating input current amplifier. The

tunable blocks, the OTA's, allow a control of the multiplication factor k within certain limits. For linearity convenience, the OTA's are to be realized with bipolar transistors.

Since one objection to previous multipliers is the use of large load capacitances, the proposed circuit uses a C_L of a 20 pF. Although still large, reducing this value will place severe limitations in the lower limit of our frequency range. Let us now see how this choice affects initial considerations in the selection of other parameters.

Equation (3.24) will help in stating our lower bound of the frequency limits. The magnitude at the output of the voltage amplifier will vary depending on the signal. The current $|I_L| = 2\pi C_L\, f |V_{C_L}|$ should have a safe magnitude in the worst case. Assuming a worst case of 20 nA,

$$f|V_{01}| = \frac{20\text{nA}}{2\,\pi\,(20\text{pF})} = 159.15\text{V}\cdot\text{Hz}$$

From here, there must be a trade off between low frequency bound and power supplies. Assuming ± 2.5 V power supplies, a minimum output for the voltage amplifier could be thought around 1 V, setting lower bound of frequency around 160 Hz. If the design is set at this value, then a higher magnitude of voltage will bring the current to a higher value, on the safe side. A lower bound for the frequency requires either larger power supplies or higher C_L.

Dynamic ranges of the amplifiers also set limits to the achievable equivalent capacitances. Since the multiplying factor is the product of the voltage and current amplifier gains, $k = \alpha\beta$, increasing the dynamic range for the input of the voltage amplifier reduces this factor k. Again, a trade off comes into play. Playing on the dynamic range side, the equivalent capacitance will be set within the 1 nF to 16 nF range, meaning 50 to 300 times C_L.

Considerations on power constraints led to setting reasonable upper limits. To keep power within acceptable limits, the currents used for tuning cannot be "high",

given the rail to rail voltage of 5 V. This will set the output resistance of the voltage amplifier and the input resistance of the current amplifier in the several hundreds kΩ to several MΩ range. The upper frequency limit could low in this case, as discussed and illustrated in §3.6.1, although the introduction of the CCCII improves the bandwidth. For the purposes of our design, an upper bound is needed. To play safe, given the low frequency objectives of the design, let us set 1 kHz as the upper bound. The realization will set the actual limit.

Note that, starting with one limitation, namely the C_L value, the discussion from Chapter 3 has led us to establish acceptable design parameters for the multiplier. Some constraints, like the lower frequency bound, which is one of the important factors to consider in low frequency applications, have been established without any considerations with respect to the actual circuit realization. The consideration of other points makes use of the model that is obtained when non ideal macromodels for the amplifiers are introduced into the ideal circuit design constraints.

4.2 General Description for the Multiplier

The voltage and current amplifier circuits are implemented with operational transconductance amplifiers (OTAs). For the nullor element, a CCCII is used. This is illustrated in Figure 4–2. The first two OTAs (OTA1 and OTA2) are used for the VCVS realization, while OTA3 and OTA4 are for the CCCS.

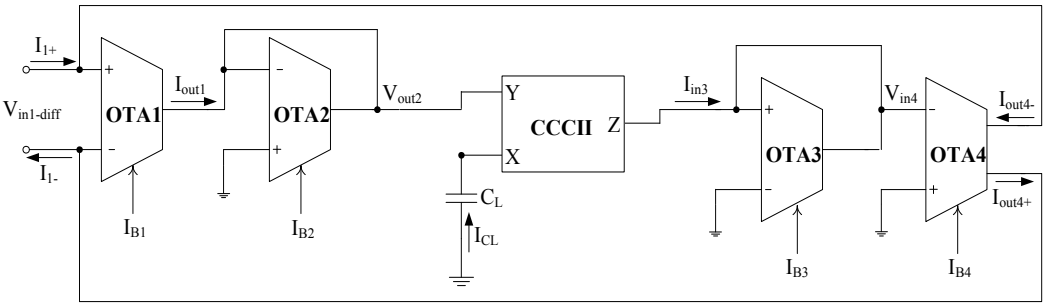


Figure 4–2: The Floating Capacitance Multiplier

At the current conveyor CCCII, the grounded capacitor is connected to the X terminal, the VCVS output voltage to the Y terminal and terminal Z goes to the current amplifier input. Recall that the terminal relations for the CCCII are given by

$$V_Y = V_X \tag{4.1a}$$

$$I_Y = 0 \tag{4.1b}$$

$$I_Z = I_X \tag{4.1c}$$

Similarly, the current leaving the single ended OTA output is given by (4.2), while the transconductance g_m for bipolar OTA's depends on the bias current I_B as in equation (4.3). This last, is the relation that allows tunability through the bias current for the OTA's gain and, as a consequence, for our circuit.

$$I_o = g_m V_{in} \tag{4.2}$$

$$g_m = I_B/2V_T \tag{4.3}$$

The proposed configuration works as follows: the input differential voltage $V_{in1-diff}$ is multiplied by the transconductance g_{m1}, yielding in an output current I_{out1} for OTA1 given by

$$I_{out1} = g_{m1} V_{in1-diff} \tag{4.4}$$

OTA2 is being used as a current to voltage converter with a variable resistance $R_{OTA2} = 1/g_{m2}$, that depends on the biasing I_{B2} value. This produced the voltage V_{out2} established in equation (4.5), which is the input to terminal Y of the current conveyor.

$$V_{out2} = \frac{I_{out1}}{g_{m2}} = I_{out1} R_{OTA2} \tag{4.5}$$

Because of the CCCII voltage property (4.1a), this input voltage to the Y terminal is reflected into the X terminal to which C_L is connected, producing

$$V_{C_L} = V_{o2} = \frac{g_{m1}}{g_{m2}}(V_{in1-diff}) = \alpha(V_{in1-diff}) \tag{4.6}$$

The VCVS tunable gain factor is defined by

$$\alpha = \frac{g_{m1}}{g_{m2}} = \frac{I_{B1}}{I_{B2}} \tag{4.7}$$

By the current relations for the X and Z terminals (4.1c), the current I_{C_L} is replied into the CCCS input terminal of the OTA3, which is also connected as a current to voltage converter. Therefore,

$$I_{in3} = I_{C_L} = sC_L V_{C_L} \tag{4.8}$$

and

$$V_{out3} = V_{in4} = \frac{I_{in3}}{g_{m3}} = I_{in3} R_{OTA-3} \tag{4.9}$$

Since $I_{out4\pm} = \pm g_{m4} V_{in4}$, using equation (4.9) in this relation yields (4.10):

$$I_{out4\pm} = \pm \frac{g_{m4}}{g_{m3}} I_{in3} = \pm \beta I_{in3} \tag{4.10}$$

where, the CCCS tunable gain factor is defined by

$$\beta = \frac{g_{m4}}{g_{m3}} = \frac{I_{B4}/2}{I_{B3}} \tag{4.11}$$

Due to the electronic feedback this output current $I_{out4\pm}$ is also equivalent to that in the VCVS input terminals $I_{1\pm}$.

Finally, the equivalent input impedance equation is determined by equation (4.12), where k is the $\alpha\beta$ multiplication factor given by (4.13).

$$Z_{in_{eq}} = \frac{V_{in1-diff}}{I_1} = \frac{1}{skC_L} \tag{4.12}$$

$$k = \frac{g_{m_1} g_{m_4}}{g_{m_2} g_{m_3}} \tag{4.13}$$

4.3 Block realizations

To get into other restrictions for the design, more specific data about the actual realization is needed. Therefore, this section offers the topology and main characteristics relative to the transistor parameters. As mentioned before, the proposed circuit is realized in BJT technology to take advantage of linearity. For the OTA subcircuit, the topology is given by the schematic in Figure 4–3

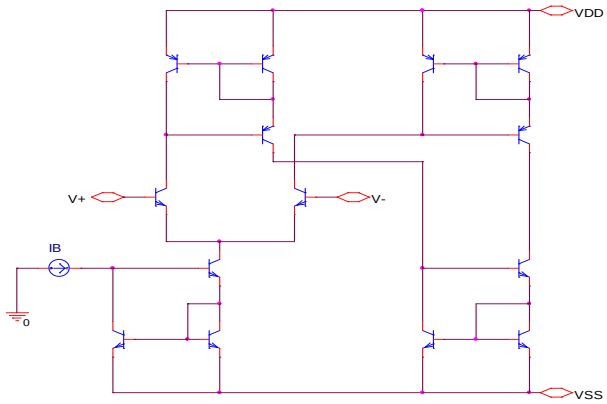


Figure 4–3: BJT version of OTA used in realization [10]

For the current conveyor, the schematic is given in Figure 4–4.

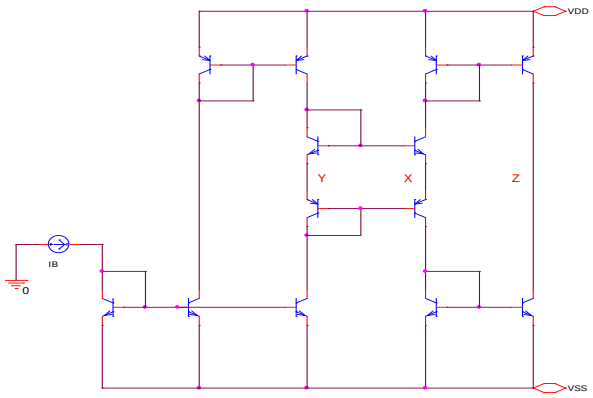


Figure 4–4: BJT version of CCCII used in realization [10]

The transistors are PRN200P and NR200N of the ALA400 transistor array from AT&T. Some of their parameters are used in the following sections: $\beta_n = 137.5$, $\beta_p = 110$, $V_{A_n} = 159.4V$ and $V_{A_p} = 51.8V$.

4.4 Design Considerations For the VCVS

This section discusses some design considerations for the voltage amplifier block formed by OTA's 1 and 2, as shown in Figure 4–5. For a ±2.5 V power supply, let the output voltage swing V_{out2} be limited to a maximum of 2 V in order to avoid amplitude distortion. This can be tuned through I_{B2} for a defined range that is between the following limits, where the lower bound of 1 V was set in §4.1.

$$1V \leq V_{out2} \leq 2V$$

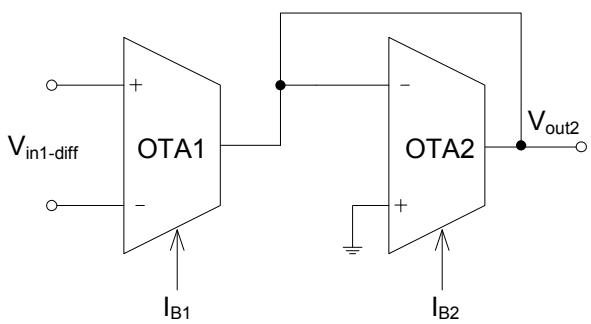


Figure 4–5: VCVS OTA Implementation

Having defined the output voltage range, it is time to look now at the bounds of the current I_{C_L} to double check for viability. Since

$$160Hz \leq f \leq 1kHz$$

the limits for the current become

$$|I_{C_L-min}| = 2\pi f_{min}|V_{out2_{min}}|C_L = 2\pi(160Hz)(1V)(20pF) = 20nA$$

$$|I_{C_L-max}| = 2\pi f_{max}|V_{out2_{max}}|C_L = 2\pi(1kHz)(2V)(20pF) = 251nA$$

Operational transconductance amplifiers have low input dynamic range [26]. Hence, for safety the following limit is set:

$$10\,mV \;\leq V_{in1-diff} \;\leq 20\,mV \tag{4.14}$$

From this, the input/output impedance parameters and the tunable gain factor (α) can be determined.

The VCVS input resistance R_{in_1} is set from the low frequency bound. This is determined in equation (4.15).

$$R_{in_1} = \frac{1}{2\pi f_L C_{eq_{min}}} = \frac{1}{2\pi(160Hz)(1nF)} = 1M\Omega \tag{4.15}$$

Using the known relations for input resistance [27] of BJT OTA's, R_{in_1} is given as

$$R_{in_1} = 2r_\pi = 2\frac{\beta_n}{g_{m1}} = 4\frac{\beta_n V_T}{I_{B1}} \tag{4.16}$$

From (4.16), with the transistor parameters that are being used the bias current I_{B1} for the first OTA is found to be

$$I_{B1} = \frac{4(137.5)(26mV)}{1M\Omega} = 14uA$$

Once set, this bias current is considered fixed because it determines the input resistance of the system and thus the lower frequency bound. Equation (4.17) is used to determine the output resistance for OTA1:

$$R_{out_1} = \frac{\beta_p V_{A_p}}{I_{B1}} \tag{4.17}$$

Substituting values from the transistors parameters,

$$R_{out1} = \frac{110(51.8V)}{14uA} = 407M\Omega$$

At this point, the necessary information to determine I_{B2} is known. Using equation (4.6), after some algebra and substitutions one gets

$$I_{B2_{min}} = \frac{I_{B1_{fixed}} V_{in1-diff_{max}}}{V_{out2_{max}}} = \frac{14uA(20mV)}{2V} = .14uA$$

$$I_{B2_{max}} = \frac{I_{B1_{fixed}} V_{in1-diff_{min}}}{V_{out2_{max}}} = \frac{14uA(10mV)}{2V} = 28uA$$

To avoid loading effects between OTA1 and OTA2, the equivalent resistance realized by the second OTA, R_{OTA-2} should be at least 10 times lower than R_{out1}, that is,

$$R_{OTA-2_{max}} \leq \frac{R_{out1}}{10} = 40.7M\Omega$$

The resistance is maximum when I_{B2} is minimum. Using the previous values yields

$$R_{OTA-2_{max}} = \frac{2V_T}{I_{B2_{min}}} = \frac{2(26mV)}{.14uA} = 371.4k\Omega$$

which effectively satisfies the requirement.

Finally, using these results it is possible to find the bounds for the gain factor for α as calculated below:

$$\alpha_{min} = \frac{g_{m1_{fixed}}}{g_{m2_{max}}} \approx \frac{I_{B1}}{I_{B2_{max}}} = \frac{14uA}{.28uA} = 50$$

$$\alpha_{max} = \frac{g_{m1_{fixed}}}{g_{m2_{min}}} \approx \frac{I_{B1}}{I_{B2_{min}}} = \frac{14uA}{.14uA} = 100$$

That is,

$$50V/V \leq \alpha \leq 100V/V$$

4.5 Design Considerations For a Current Controlled Current Source (CCCS)

This section present some computations for the CCCS operation and design.The input current has previously be determined, since $I_{in3} = I_{C_L}$. Therefore,

$$20nA \leq I_{in3} \leq 251nA$$

At the output terminals, the maximum current $I_{out4\pm}$ is limited by the VCVS input resistance, as established in (4.18).

$$I_{out4\pm_{max}} = \pm\frac{V_{out-max4+} - V_{out-max4-}}{R_{in1}} = \frac{2V - (-2V)}{1M\Omega} = 4uA. \tag{4.18}$$

The current value cannot exceed an amplitude of 4 uA, otherwise the circuit will not behave properly.

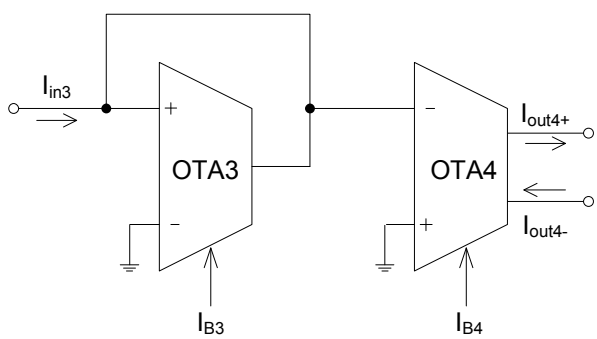


Figure 4–6: CCCS OTA implementation

Another constraint is due to poor linearity in the OTAs. The input voltage range must be kept small, within 20 mV magnitude. This limits the value of R_{OTA3}. From the upper bound of I_{in3} it follows that

$$R_{OTA3} = \frac{V_{in4-max}}{I_{in3-max}} \approx 77\,k\Omega \tag{4.19}$$

This value is then obtained by applying 700 nA bias current to the I_{B3} port:

$$I_{B3} = \frac{2V_T}{R_{OTA3}} = \frac{2(26mV)}{77k\Omega} = 700nA$$

Now, let us analyze the behavior of the OTA4 and the tunable gain factor (β) under the above constraints for the bias I_{B3} and the input I_{in3} currents. Starting with the maximum value for I_{B4}, using equation (4.10) results in

$$I_{B4-max} = \frac{I_{B3} I_{out4-diff_{max}}}{I_{in3-max}} = \frac{700nA(4uA)}{251nA} = 11.16uA$$

This value has to be used in the CCCS expression, from where the maximum β is obtained. Hence,

$$\beta_{max} = \frac{\frac{I_{B4-max}}{2}}{I_{B3-fixed}} = \frac{\frac{11.16uA}{2}}{700nA} = 7.97A/A$$

For the minimum allowable I_{B4} value, the minimum β, that is also related to the minimum equivalent capacitance, is determined as follows:

$$C_{eq_{min}} = \alpha_{min}\beta_{min}C_L = 1nF$$

$$\beta_{min} = \frac{1nF}{50(20pF)} = 1A/A$$

Knowing β_{min}, $I_{B4_{min}}$ is calculated next:

$$\beta_{min} = \frac{\frac{I_{B4-min}}{2}}{I_{B3-fixed}} \rightarrow I_{B4_{min}} = 2\beta_{min} I_{B3-fixed}$$

$$\therefore I_{B4_{min}} = 2(1)(700nA) = 1.4uA$$

Lastly, it is necessary to verify that the CCCS is not affected by loading. This can be ensured if the following inequalities are satisfied:

$$R_{in4-min} \geq 10R_{OTA-3} = 770k\Omega$$

$$R_{out4-diff-min} \geq 10R_{in1} = 10M\Omega$$

Computing the values, one gets

$$R_{in4-min} = 2\frac{2V_T\beta_n}{I_{B4-max}} = \frac{4(137.5)(26mV)}{11.16uA} = 1.28M\Omega$$

$$R_{out4-diff-min} \approx 2\frac{\beta_{p+}V_{A_{p+}}}{I_{B4-max}} = \frac{2(110)(51.8V)}{11.16uA} = 1.02G\Omega$$

which indeed comply with the requirements.

4.6 Summary

The results for the design are summarized in Table 4–1.

Table 4–1: Summary of design parameters

Parameters	Min Value	Max Value
Overall multiplier		
Power Supply	-2.5V	+2.5V
Frequency Range	160Hz	1KHz
Voltage Amplifier		
$V_{in1-diff}$	10mV	20mV
α	50V/V	100V/V
$I_{B1_{fixed}}$	14uA	14uA
I_{B2}	.14uA	14uA
Current Amplifier		
I_{in3}	20 nA	251 nA
β	1 A/A	7.91 A/A
$I_{B3_{fixed}}$	700 nA	700 nA
I_{B4}	1.4 uA	11.16 uA

CHAPTER 5
SIMULATION RESULTS

The simulation results for the multiplier model realization (Figure 5–1) using Candence Pspice software are discussed through this chapter. The circuit has been implemented with PNP and NPN transistors, whose parameters corresponds to the PRN200P and NR200N of the ALA400 transistor array from AT&T respectively.

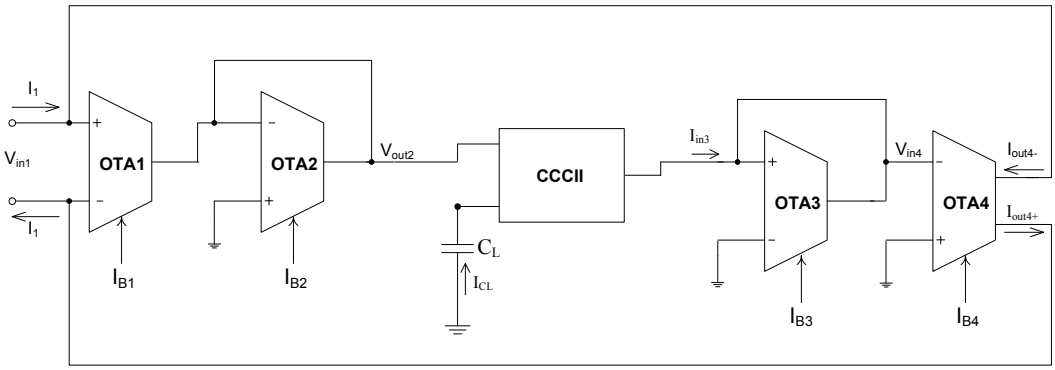


Figure 5–1: The Proposed Multiplier

The Chapter is divided in two main sections:

- The first section includes simulation for the VCVS, CCCII, CCCS and the whole multiplier. The simulations are:
  - the input and output impedance for verifying that the circuit meets requirements to avoid loading effects.
  - the α and β limits corresponding to the VCVS and CCCS tunable gain factors respectively.
- The second section has incorporated the multiplier in a third order high pass filter for a proof of its performance in an application.

5.1 Results for Individual Blocks in the Multiplier

A. *Voltage amplifier*

The schematics of the voltage is shown in Figure 5–2. Figure 5–3 corresponds to its input resistance, showing a 900 kΩ constant resistance over the desired frequency range.

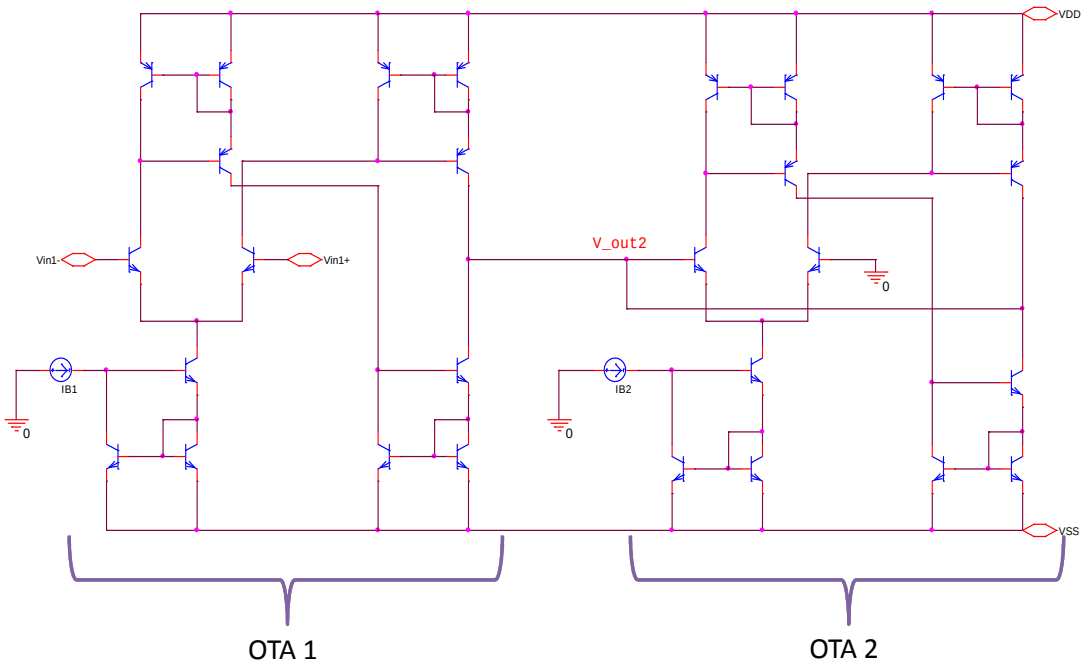


Figure 5–2: The VCVS Schematic

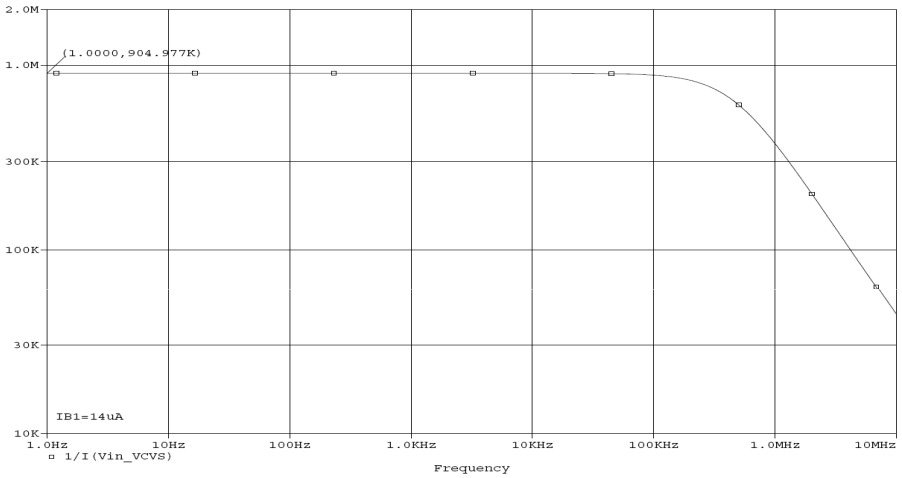


Figure 5–3: Z_{in1} vs. Frequency

The minimum (dashed line) and maximum output resistances are shown in Figure 5–4. These values are closed to the expected ones.

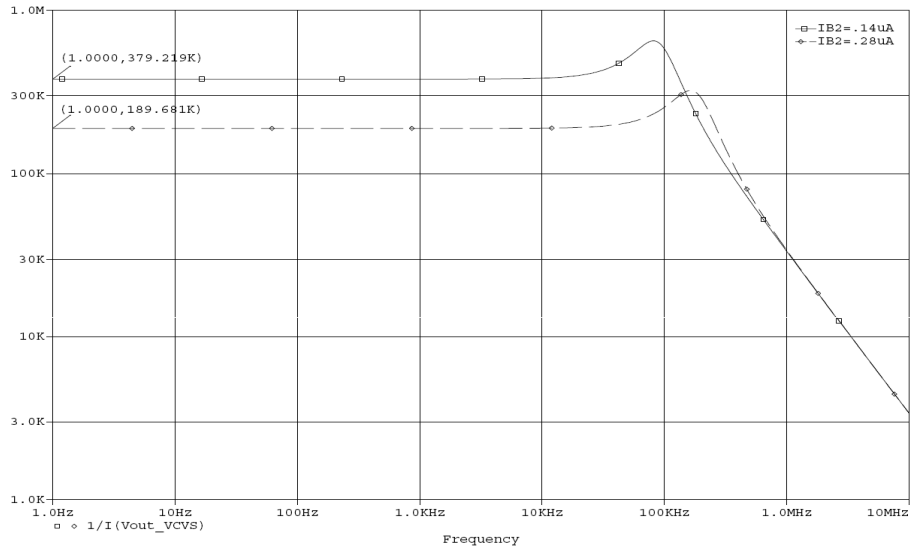


Figure 5–4: Z_{out} vs. Frequency

Figure 5–5 illustrates the minimum and maximum values for α obtained by applying the I_{B2} limits found in Chapter 3 for: $50V/V \leq \alpha_{nom} \leq 100V/V$.

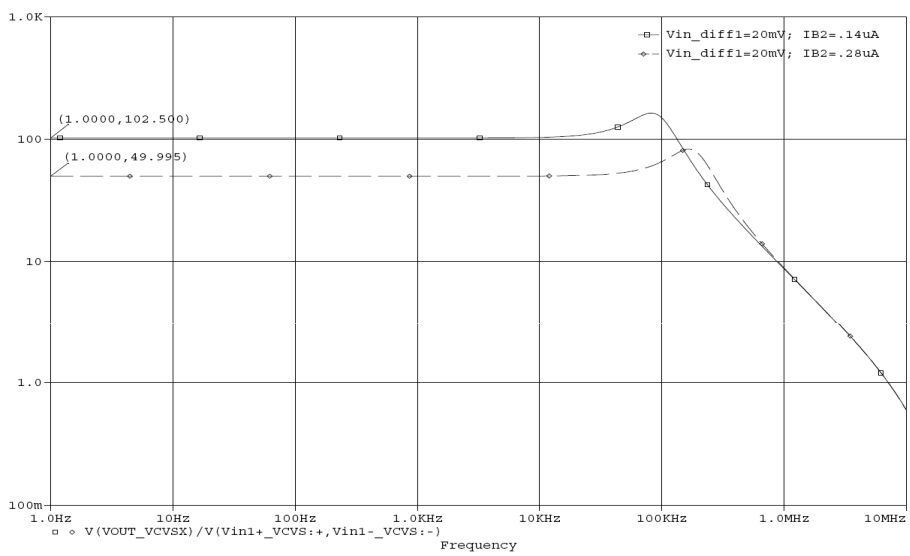


Figure 5–5: VCVS Gain

B. *The CCCII Realization*

The current controlled current conveyor circuit in Figure 5–6 has a fixed bias current I_B of 1 μA. For the conveyor to behave properly, the input resistances at nodes X and Y should be verified. Node Y must have an input resistance which must be high.

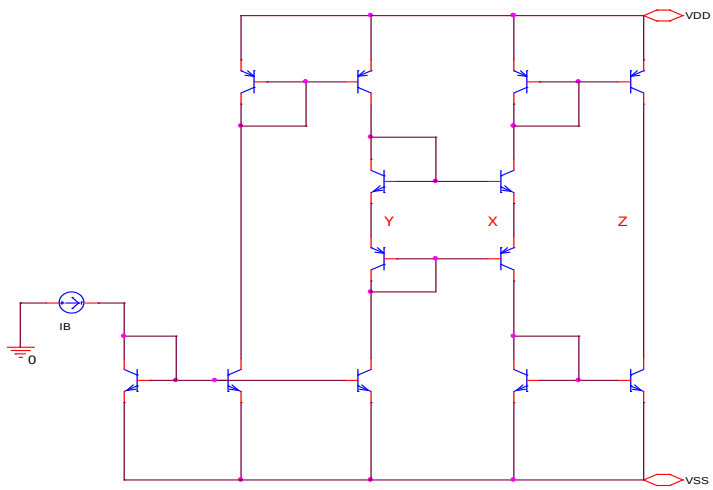


Figure 5–6: The CCCII Schematic

The X-terminal Impedance is shown in Figure 5–7 with a value of 13 kΩ.

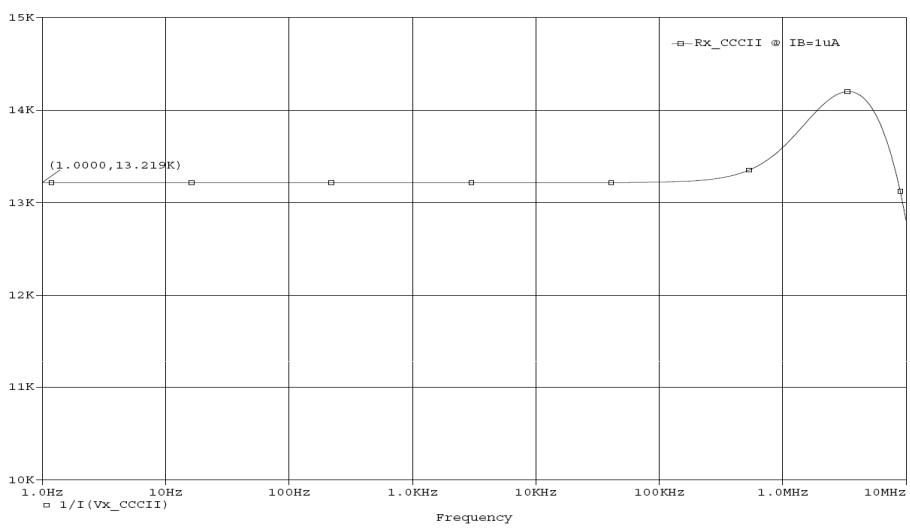


Figure 5–7: CCCII X-terminal Impedance

The Y-terminal Impedance in Figure 5–4, a 1.2 MΩ is seen for R_y. This value is very high compared to the minimum VCVS output resistance, therefore it is ensured no leakage is introduced from the VCVS to the CCCII.

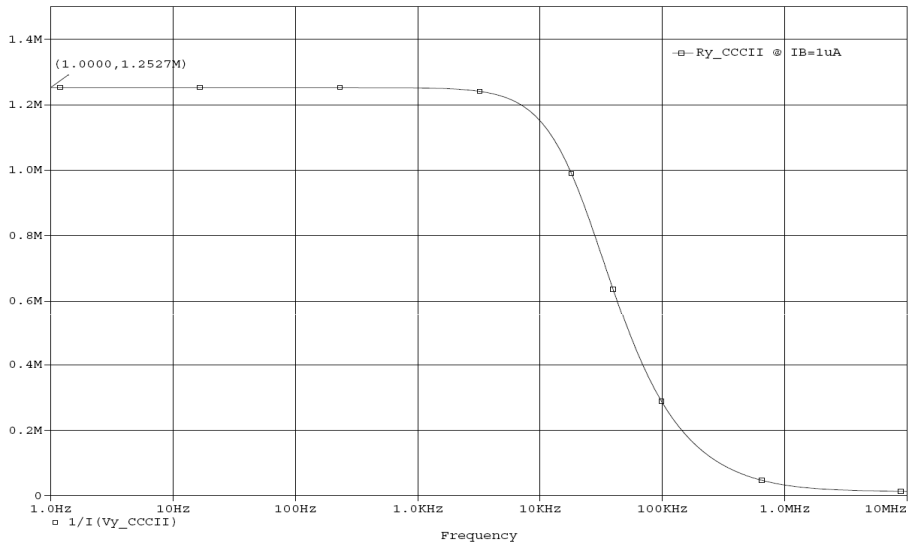


Figure 5–8: CCCII Y-terminal Impedance

The Z-terminal Impedance: The resistance R_Z comes from a single current mirror output. Its value is inversely proportional to the bias current of 1 μA, therefore as shown in Figure 5–13, R_Z is in the order of MΩs.

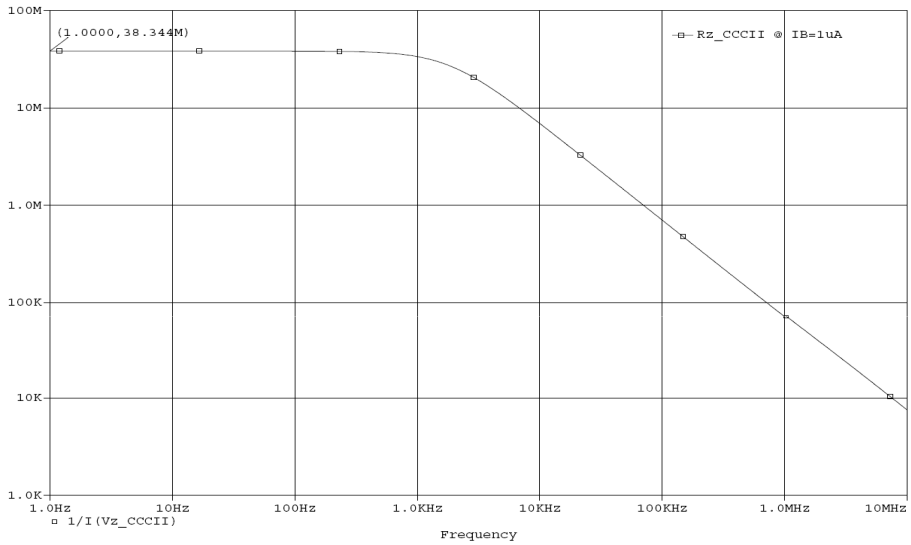


Figure 5–9: CCCII Z-terminal Impedance

To verify the functionality of the current controlled conveyor, according to Figure 5–10 the voltage at terminal Y, which is connected in the multiplier to the voltage amplifier's output, should be compared with the potential X, i. e. , to the capacitor voltage. Similarly, the current in the capacitor should be compared to the current delivered at terminal Z. Figure 5–11, shows the simulations.

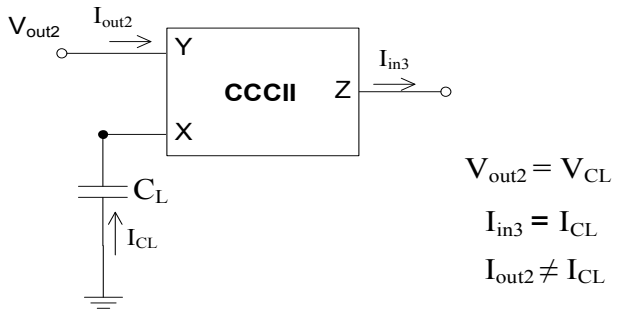


Figure 5–10: CCCII Model

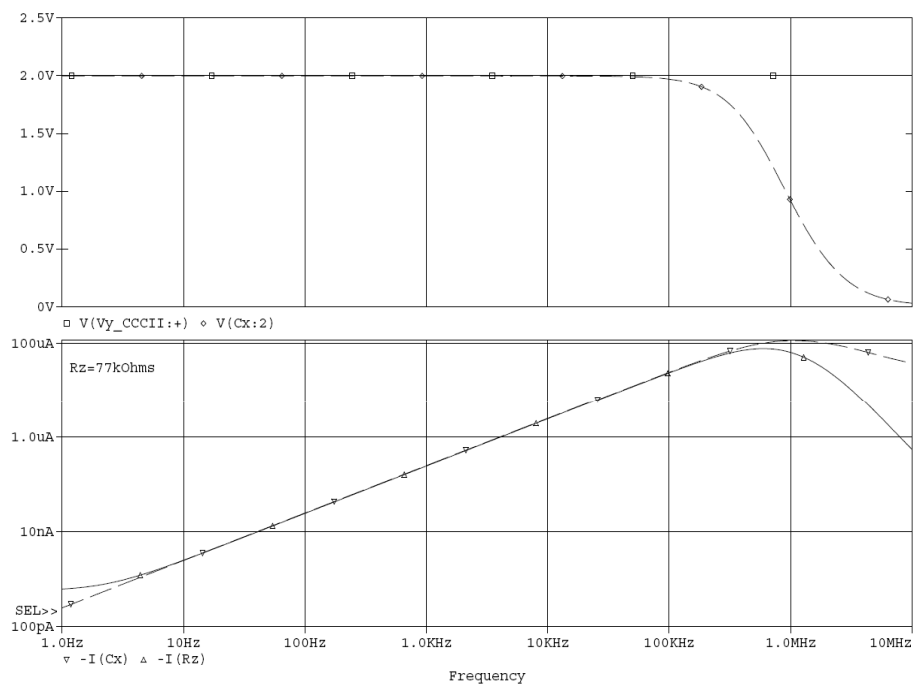


Figure 5–11: CCCII Functionality in the FCM

In Figure 5–11, the top simulation compares voltages at terminals X and Y, showing that V_{out2} and V_{C_L} are similar. In the bottom, the X and Z current properties are accomplished, since $I_Z = I_X$ does not differ from the I_{C_L} current.

C. *The Current source realization*

The schematics of the CCCS is shown in Figure 5–12.

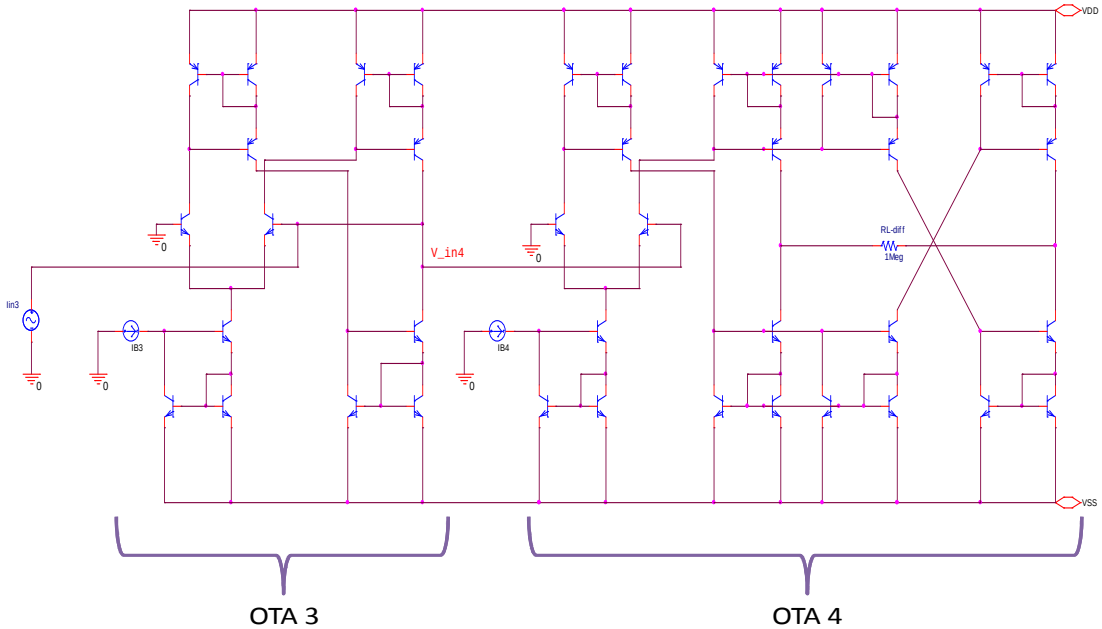


Figure 5–12: Schematic for CCCS

The CCCS input impedance: The simulation given in Figure 5–13 is consistent with the expected theoretical value of 77 kΩ for R_{OTA3} (refer to Chapter 4 for theoretical details). Moreover, under I_{B4} variations the resistance is kept almost constant, which is very important for guaranteeing the full β range.

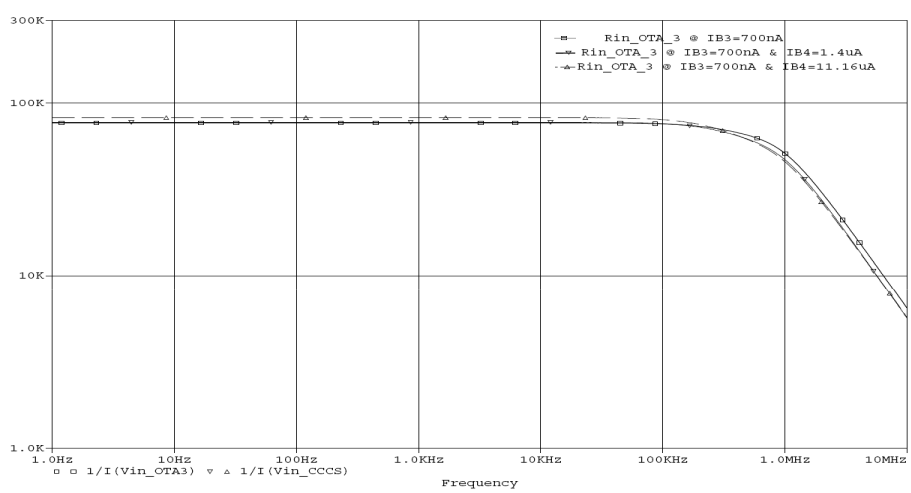


Figure 5–13: CCCS Input Impedance Z_{in3}

The CCCS output impedance was simulated connection at the CCCS output terminals a 1 MΩ load which emulates the VCVS input resistance, to which it will be connected after feedback. The results in Figure 5–14 show the CCCS output resistance is approximately constant over I_{B4} variations, therefore allowing a feedback to VCVS input.

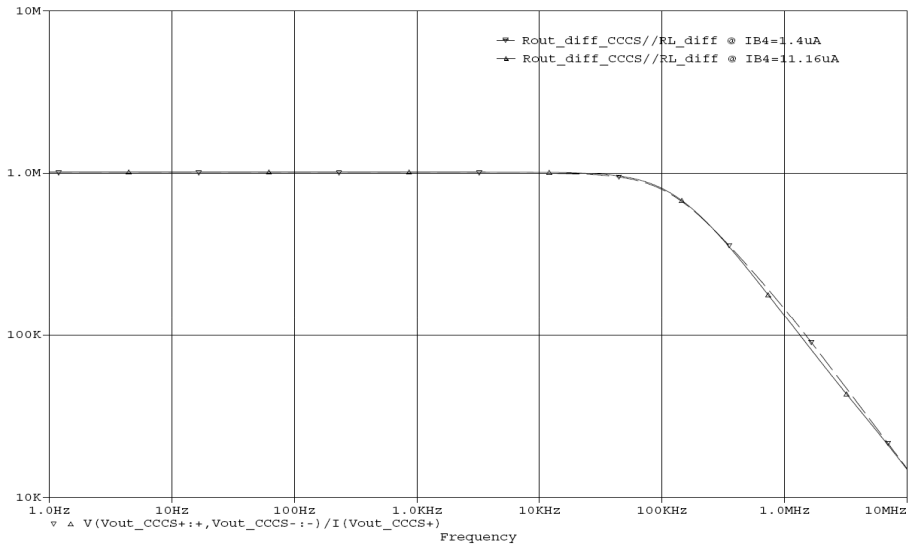


Figure 5–14: CCCS Output Resistance

For the CCCS gain factor, Figure 5–15 shows the minimum (dashed line) and maximum limits for β obtained. This also has confirmed β is proportional to I_{B4}.

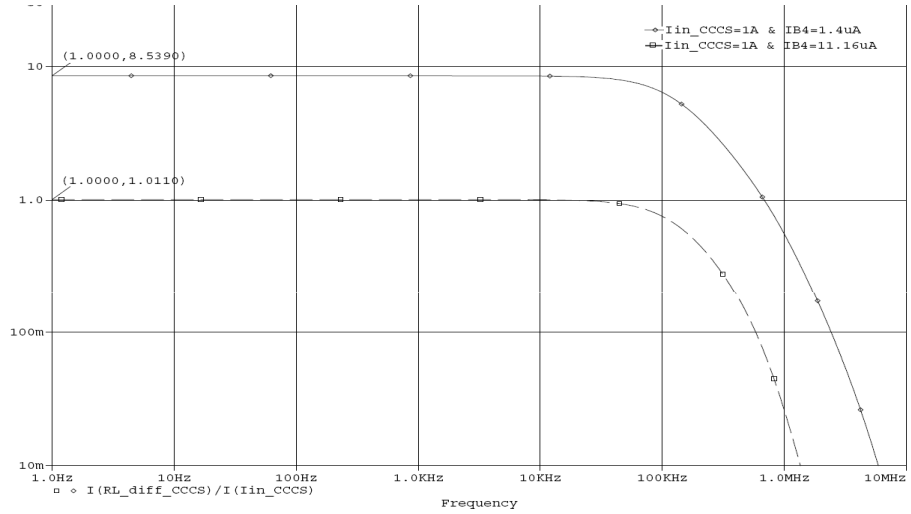


Figure 5–15: CCCS Gain at minimun Iin3

5.2 The Overall Circuit Realization

The schematic of the complete capacitance multiplier is shown in Figure 5–16.

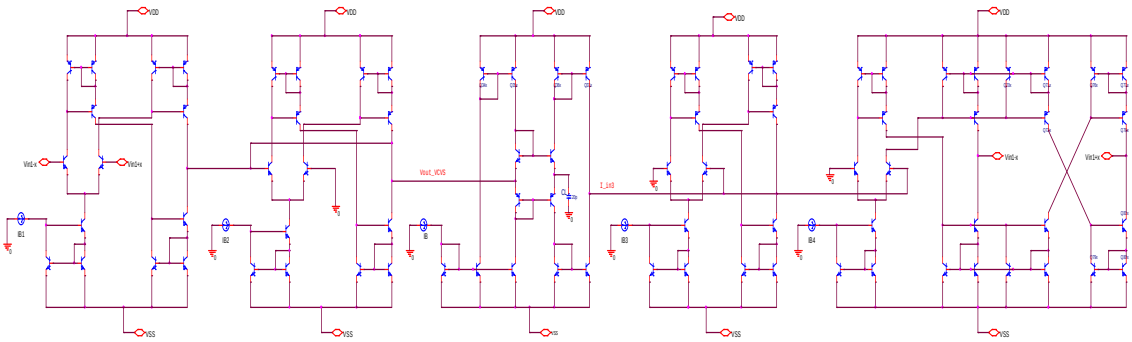
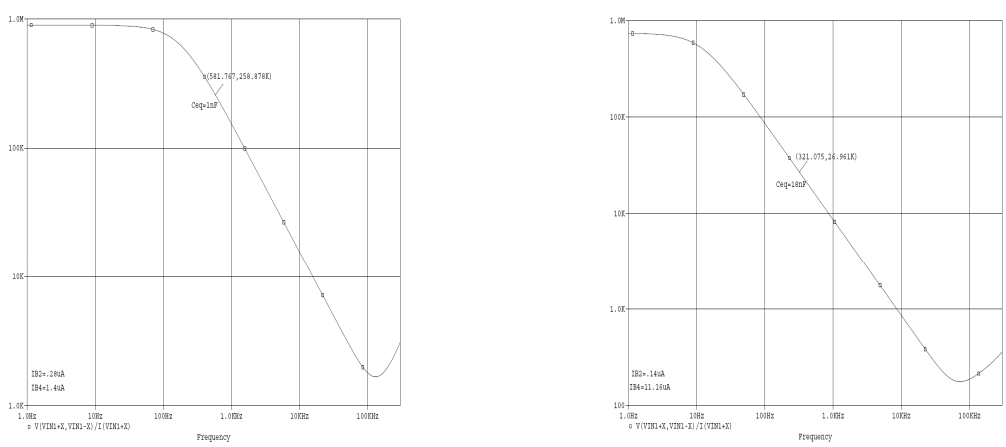


Figure 5–16: FCM Schematic

The achievement of the goal is measured by considering the equivalent input impedance $Z_{in_{eq}}$, which in the frequency of interest must comply with

$$Z_{in_{eq}} \rightarrow \frac{1}{sC_{eq}}$$

In chapter 4, the equivalent capacitance were set to be between 1 nF (k = 50) and 16 nF (k = 800). Looking into Figure 5–17, where the minimum (5–17a) and maximum (5–17b) equivalent capacitances C_{eq} are simulated, it can be inferred that in the desired frequency range, there is a good match between the ideal values and those obtained by the multiplier.



(a) (b)

Figure 5–17: The input impedance Z_{in} for the minimum and maximum k-factors

In Figure 5–18, the equivalent capacitances are simulated in the range of 2 nF up to 18 nF. In the top figure, each descendant steep line represents a different realized capacitance; the corresponding phases are illustrated in the bottom Figure. To obtain different k factors, α was fixed to its maximum (100 V/V), while I_{B4} was tuned in all its range (from 1.4 μA up to 11.16 μA) with a step size of 700 nA. That is,

$$\beta = \frac{\frac{I_{B4}}{2}}{700nA}$$

$$k = \alpha\beta = 100\beta$$

Notice, with an increment in the k-factor (or I_{B4}) the low frequency pole moves from the right to the left, incrementing the equivalent capacitance C_{eq}.

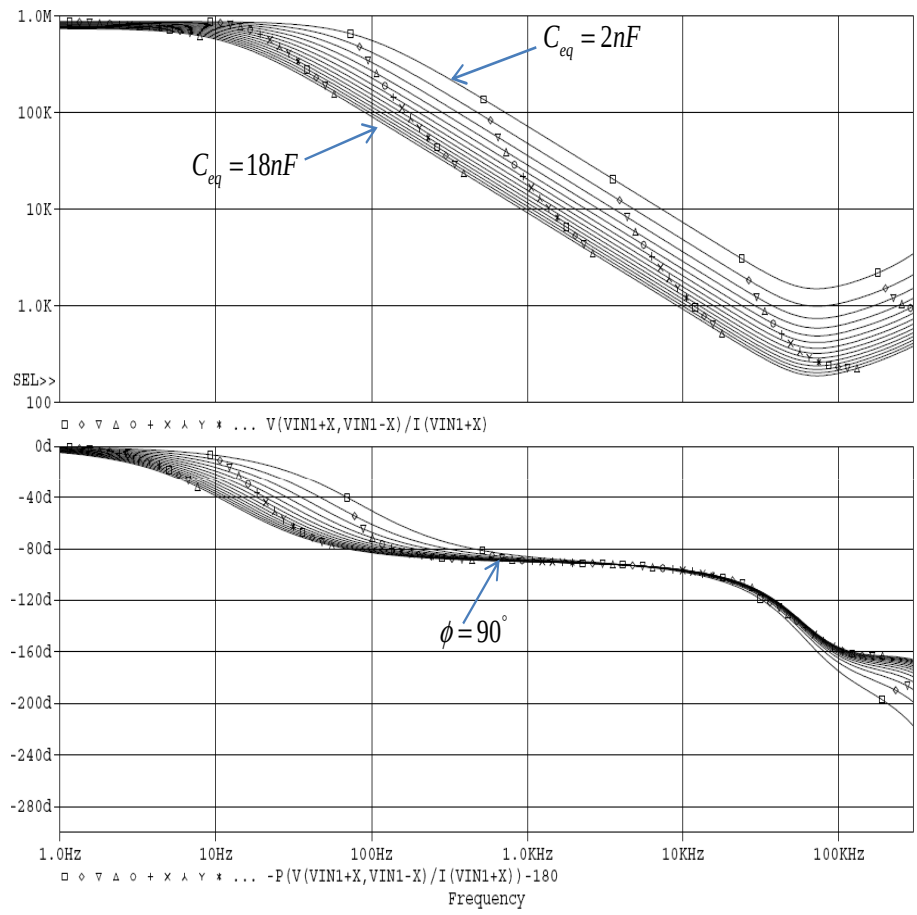


Figure 5–18: (Top) $Z_{in_{eq}}$ and its (Bottom) Phase for different k-factors

5.3 Floating Capacitance Multiplier Application

For the evaluation of the multiplier in an application, a third order high pass filter (HPF) in Figure 5–19 is used. This configuration has a floating capacitor C between terminals 1 and 2, which is the capacitance to be simulated. In the following simulations, an ideal capacitor is compared with that provided by the multiplier.

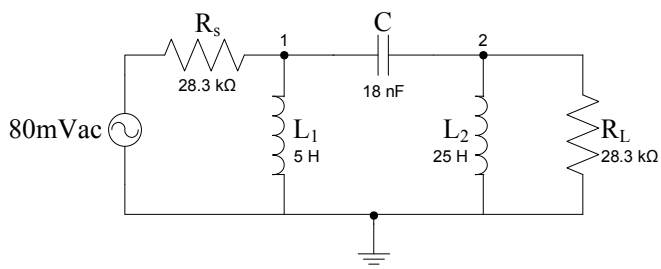


Figure 5–19: High Pass Filter for Multiplier Application

Figure 5–20 shows the simulation for the output response measured at terminal 2 for an ideal (solid line) and a simulated capacitance obtained by the multiplier. After the low cutoff frequency, the dashed line starts to diverge from the solid one. This is a problem that arises from leakage due to the finite equivalent input resistance in the multiplier, which does not has a trivial solution for low voltage design. In this type of application this is, though, a relatively non important problem since it covers the transition bandwidth.

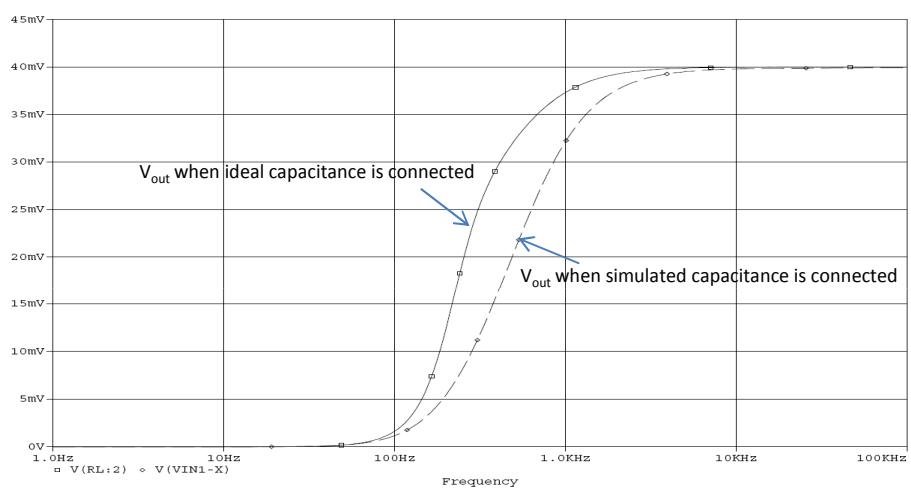


Figure 5–20: The 3rd order High Pass Filter Output Response

In Figure 5–21, the ideal (solid line) and the equivalent capacitance (at the bottom in the Figure) seen at terminals 1 and 2 in the HPF are similar for frequencies above 100 Hz. This is expected due to the allowable frequency range for the multiplier. Although the capacitances don't seem to diverge, their respective voltages and currents do. If the voltages obtained (the top Figure) are compared with Figure 5–20, it can be seen that the difference that arises for the output response is due to the lossless nature in the capacitance voltage.

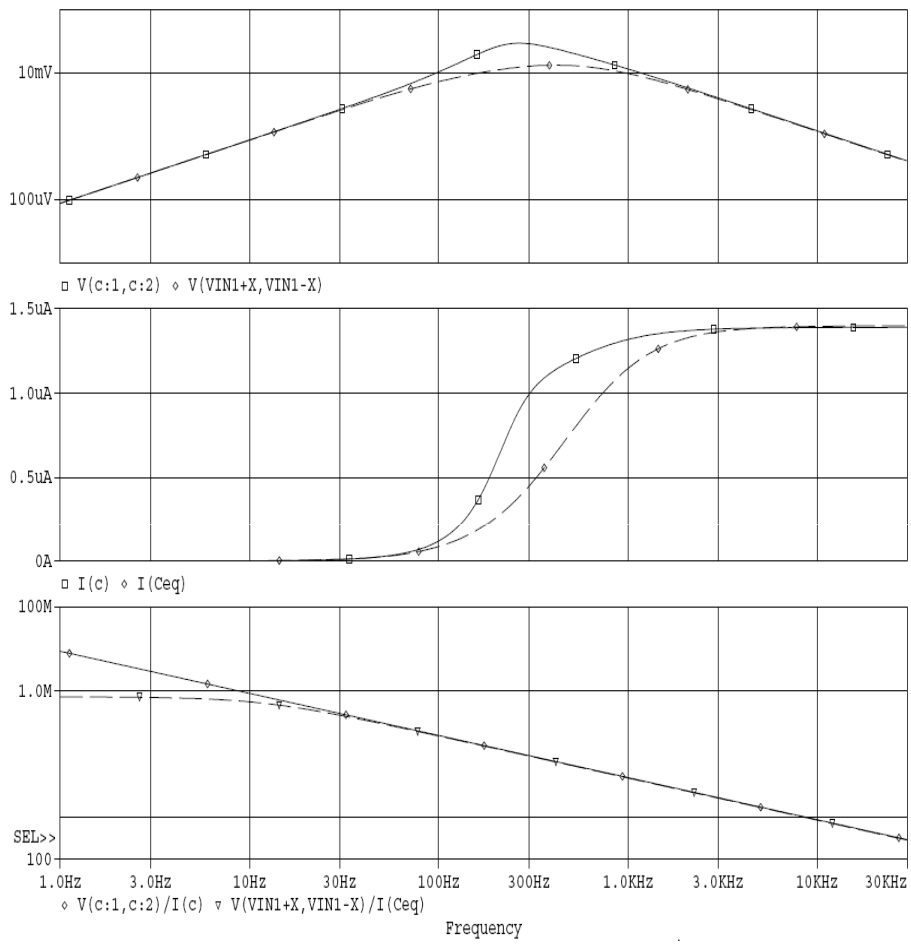


Figure 5–21: The ideal and simulated Capacitance

5.4 Transistors

As mentioned before, the blocks are built with bipolar transistors PRN200P and NR200N of the ALA400 transistor array from AT&T. The Spice parameters for these transistors are as follows:

```
*NR200N-2X NPN TRANSISTOR:
.MODEL NX2 NPN (Rb=262.5 Irb=0 Rbm=12.5 Rc=25 Re=0.5 Bf=137.5
+ Is=242E-18 Eg=1.206 Xti=2 Xtb=1.538 Ikf=13.94E-3 Br=0.7258 Nf=1
+ Vaf=159.4 Ise=72E-16 Ne=1.713 Ikr=4.396E-3 Nr=1.0 Var=10.73 Isc=0 Nc=2
+ Tf=0.43E-9 Tr=0.43E-8 Cje=0.428E-12 Vje=0.5 Mje=0.28 Cjc=1.97E-13
+ Vjc=0.5 Mjc=0.3 Xcjc=0.065 Cjs=1.17E-12 Vjs=0.64 Mjs=0.4 Fc=0.5)

*PR200N-2X PNP TRANSISTOR:
.MODEL PX2 PNP (Rb=163.5 Irb=0 Rbm=12.27 Rc=25 Re=1.5 Bf=110
+ Is=147E-18 Eg=1.206 Xti=1.7 Xtb=1.866 Ikf=4.718E-3 Br=0.04745 Nf=1
+ Vaf=51.8 Ise=50.2E-16 Ne=1.65 Ikr=12.96E-3 Nr=1.0 Var=9.96 Isc=0 Nc=2
+ Tf=0.610E-9 Tr=0.610E-8 Cje=0.36E-12 Vje=0.5 Mje=0.28 Cjc=0.328E-13
+ Vjc=0.8 Mjc=0.4 Xcjc=0.074 Cjs=1.39E-12 Vjs=0.55 Mjs=0.35 Fc=0.5)
```

CHAPTER 6
CONCLUSION AND RECOMMENDATIONS

This work has reported theoretical and practical results for IC capacitance multipliers.

First, a system level analysis was developed based on two-ports and three-terminals network theory. The main results from this analysis are listed below.

- The positive impedance converter (PIC) is practically the only subnetwork that achieves the multiplication goal when properly terminated by a load capacitance C_L.
- Very low and low frequency application encounters serious obstacles such as
  - Need of high valued on chip load capacitance;
  - Large amplifications, if possible rail to rail values
  - A trade off between low voltage supplies and low frequency range
- These obstacles are inherent to the goals associated mainly to the need to avoid noise level signal currents.
- Input resistances of the port and output resistances of current sources are also one of the main limitations for low frequency realizations. Their influence should be considered early in the design level because of the dependence they have on bias conditions

As the applications go toward higher frequency, the constraints relax and allow more freedom.

The system analysis done in chapter 3 served also to explain the limitations that have been reported in the literature to some realizations and which were mainly attributed to a faulty design and not to an obstacle inherent to the pursued goals.

In Chapter 4 a new implementation for a tunable capacitance multiplier is developed following the guidelines proposed in the system analysis of Chapter 3. First the overall limitations are considered, pursuing a relatively low value for C_L and determining a suitable frequency range for that capacitance value. Then, a specific realization at block level on operational transconductance amplifiers (OTA) and current controlled current conveyor (CCCII) is considered. This allows further use of the guidelines derived in the system analysis. The proposed circuit does not include passive elements to avoid extra power dissipation.

The simulations showed the circuit works for voltage supplies of ± 2.5 V with a grounded 20 pF capacitor C_L. Indeed, the results have reported equivalent capacitances in the range of 1 nF up to 18 nF. Therefore, a tunable gain factor of 50 to 300 times C_L is achieved in a frequency range of 160 Hz up to 30 kHz. Unfortunately, within the time frame for this research, this circuit was not optimized, but results for equivalent capacitances and tunable range are better than most of the works presented in the literature.

6.1 Future Work

A good starting point can be to work on optimizing the OTAs and CCCII, either by the topology or by appropriate technology considerations, to enhance the input resistance without a loss of tunable gain. Also, to apply low voltage techniques for power dissipation improvements.

Since one of the limitations arises from generation of noise level signals, working in low noise current and voltage amplifiers could further help in the reduction of the frequency range of applications.

The development in CMOS technology is also encouraged. The nonlinearity of the transconductance and the input capacitance of the MOSFET will bring other challenges that were not included in this work when parasitic capacitance were discarded in low frequency regions.

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