AUTOMATED TEMPERATURE TRIMMING FOR MISMATCH AND PROCESS VARIATIONS IN BANDGAP VOLTAGE REFERENCE

By

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This document shows the work that has been realized to design and simulate an integrated circuit that is capable of correcting mismatch and process variations using an automated temperature trimming circuit. The system will correct Bandgap References to have a temperature coefficient (TC) from 10 to 35 ppm from -40◦ to 100 ºC. To achieve this, the integrated circuit has an on-chip heating element, the output of the Bandgap Reference is tracked at all moments using a slope detector circuit to detect the maximum of the voltage reference. Using the slope detector as feedback, a logic circuit detects the change in sign of the slope. The trimming circuit resolution has been selected to ensure that the BGR will result in a more accurate first order cancellation; resulting in a TC of less than 40 ppm. To validate the circuit Monte Carlo simulation has been used; that will recreate mismatch and process variations to the BGR.

Resumen de Tesis Presentado a Escuela Graduada
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AJUSTE AUTOMATICO EN TEMPERATURA PARA VARIACIONES DE PROCESO Y DISCREPANCIA DE TAMAÑOS EN REFERENCIAS DE VOLTAJE BANDGAP

Por

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Mayo 2018

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Este documento muestra el trabajo que se ha realizado para diseñar y simular un circuito integrado que es capaz de corregir variaciones en proceso y errores de tamaño utilizando un circuito de ajuste de temperatura automático. El sistema corregirá las referencias de Bandgap para tener un coeficiente de temperatura (TC) de 10 a 35 ppm desde -40º hasta 100º C. Para lograr esto, el circuito integrado tiene un elemento de calentamiento en el chip, la salida de la referencia Bandgap se monitorea en todo momento usando un circuito detector de pendiente para detectar el máximo de la referencia de voltaje. Usando el detector de pendiente como retroalimentación, un circuito lógico detecta el cambio en el signo de la pendiente. La resolución del circuito de ajuste se ha seleccionado para garantizar que el BGR dé como resultado una cancelación más precisa de primer orden; dando como resultado una TC de menos de 40 ppm. Para validar el circuito, se ha realizado simulación Monte Carlo; que recreará las discrepancias y las variaciones de proceso en el BGR.

Dedicated to my family, who has always been there and supports me.

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CHAPTER 1
INTRODUCTION

BGRs can be found in most integrated circuits; “A voltage reference is one of the fundamental building blocks used in various devices such as A/D and D/A converters, sensor interfaces, and power management circuits.” [3]. The BGR is an essential block that works as a reference voltage that must have a low TC value across a wide range of temperature [2]. Another quality of the BGR is that it needs to have low power supply sensitivity. The main problem in all BGRs is that after fabrication the circuit will suffer from process and mismatch variations. This will broadly affect the TC of the BGR and other parameters such as offset. This effect is undesired, so there are ways of minimizing these errors. Such are: making a use of advance layout techniques, chopping methods to cancel offsets, post fabrication trimming circuits. Sometimes all three methods must be used to reduce the effect of all errors of post-fabrication.

The work presented in this document is focused on the creation of an automated temperature trimming circuit that does not require any external components to calibrate the BGR. Although previous work had shown that this can be possible [2], [4], [5], [10], previous circuits used too much memory and required ADCs, temperature sensors. Some of them use complex algorithms, which cause high power consumption and will use more area of the die. The presented solution does not require use of external machinery for trimming, ADCs or complex algorithm that use large memory.

CHAPTER 2
PREVIOUS WORK

2.1. Bandgap Voltage References

Different architectures of BGRs had been presented over the years and all are based in the same principle presented in [6], which is the BGR created by Brokaw. A simple way to describe a BGR is how good a voltage proportional to the temperature can cancel a voltage that is complementary to the temperature to obtain a constant voltage over temperature. The CTAT component has a non-lineal behavior, meaning that the BGR will still have some temperature dependence. To cancel this non-linear behavior, many implementations have been developed such as, first order cancellation seen in: [1], [4], [5], [6], and higher order cancellations: [5], [9]. All of them require trimming. In some cases, trimming requires two temperatures as in [7] and [8], meaning that the die requires to be heated to another temperature. This requires uses of external components, such as an air streamer and testing equipment to the pins of the BGR. This additional equipment represents an additional cost in fabrication.

Many implementations use a trimming method called single trim, as in [5], which only requires a measurement at room temperature. This implementation still needs external measurement equipment to complete the trimming process. Implementation [2] has internal compensation and does not require external measuring equipment, it stills requires to be heated to different temperatures, which also consumes more time. The circuit used in [4] offers an implementation that does not requires external measuring or heating. It uses an

on-chip calibration scheme that eliminates process and mismatch variations. It uses the same topology as in [5], which utilizes chopping techniques to eliminate offsets, and has a resistive trimming network, that will change the value of R_T in figure 1. This resistance is seen in figure 2.

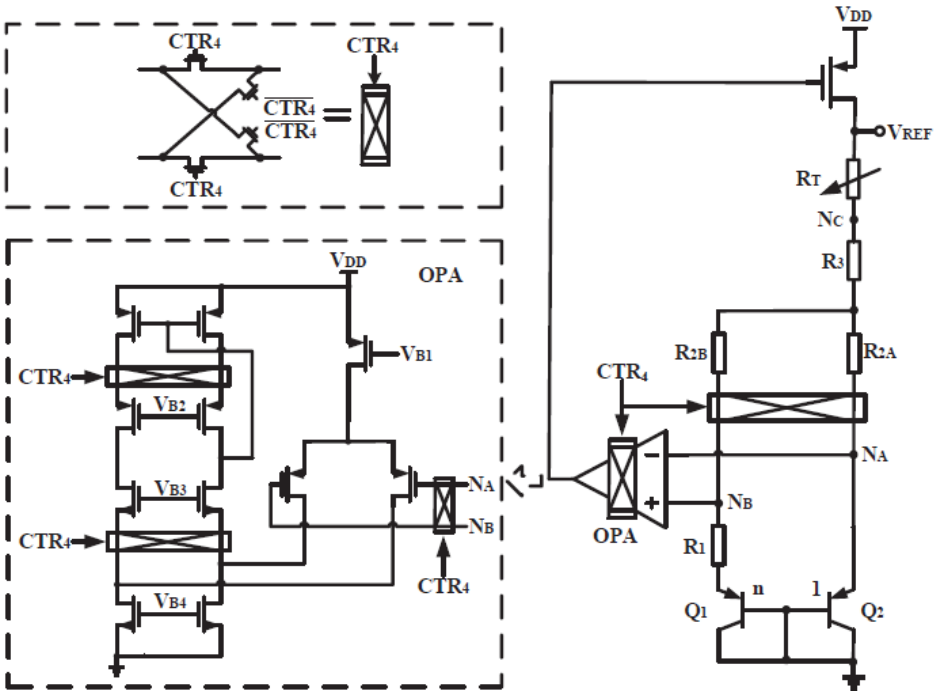

Figure 1. Topology of BGR used in [4] and [5]

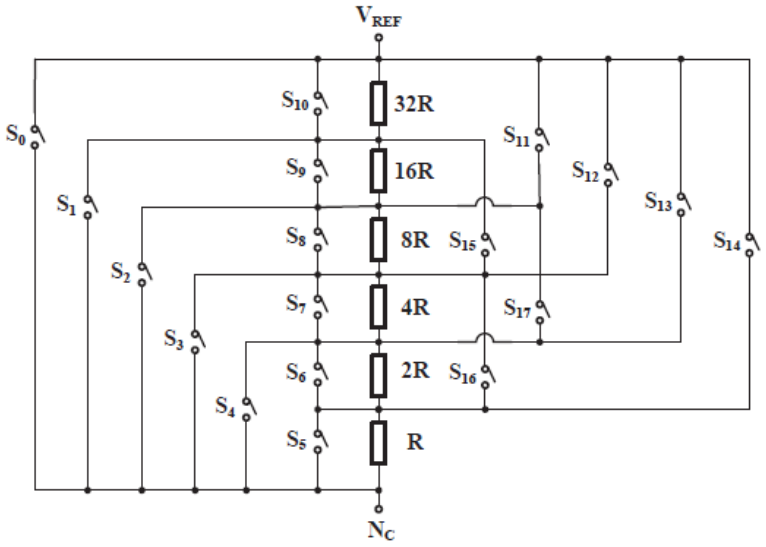

Figure 2. Resistive trimming network use in [4]

The difference between [4] and [5] is that the chopping switches presented in figure 1 are used for chopping in [5] and have a notch filter in the output of the op-amp to reduce the ripple effects of the chopping, this will also add undesired chopping noise. To eliminate the chopping noise and ripple effects, the switches are used to evaluate two states of the BGR, first all switches are in one position to measured voltage V_1, then the switches toggle to another state and a second voltage V_2 is stored. Then, the resistive trimming network changes, repeating this process values until V_1 is greater than V_2. What this accomplishes, is an average of all the mismatch offsets and process variations offsets. The chopping technique does the same and its averaged by a filter, the advantage of this approach is that no ripple and chopping noise is present.

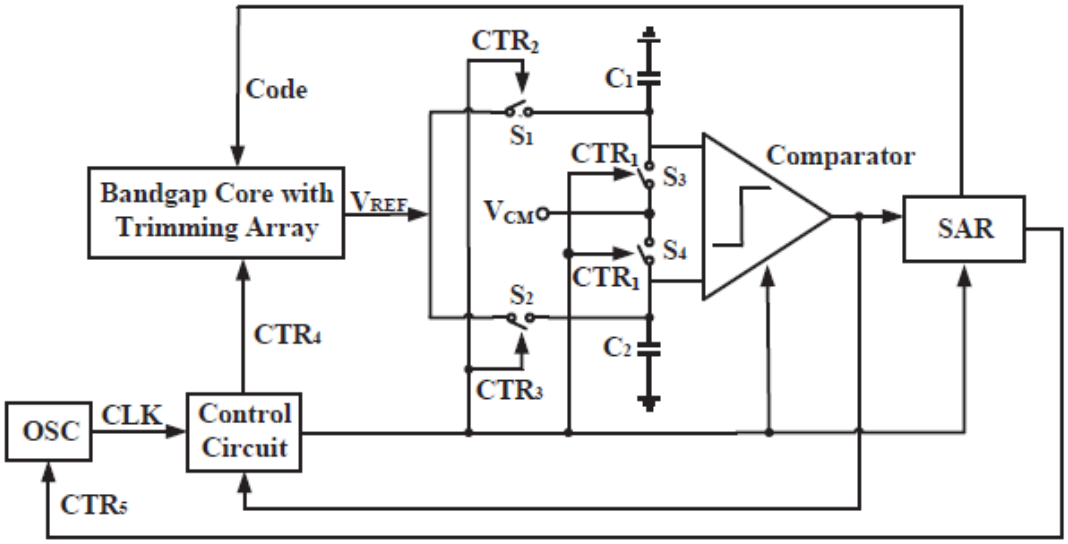

Figure 3. Calibration scheme presented in [4].

This calibration scheme presented in figure 3 still has one drawback, after calibration is done, the offset errors are reduced but the TC gets higher meaning that the curvature compensation has been altered. Since this configuration only uses room temperature, it has no way of monitoring the behavior of the voltage reference over temperature. Solution [2] uses internal compensation across temperature.

In [2] we see a digitally corrected BGR, shown in figure 4 and figure 5 shows the block diagram, that uses a temperature sensor to store the output of the voltage reference for different values. With the stored values it applies Booth's algorithm to calculate the polynomial values. It uses this polynomial function to implement a pulse density modulation (PDM) to a resistor. This resistor network shown in figure 5, will vary accordingly to the PDM. The variation of this resistor will make the reference change accordingly.

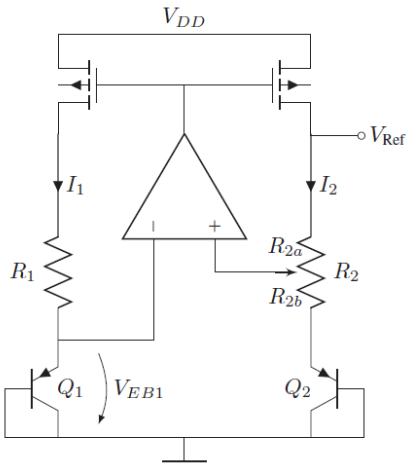

Figure 4. BGR implementation of [2]

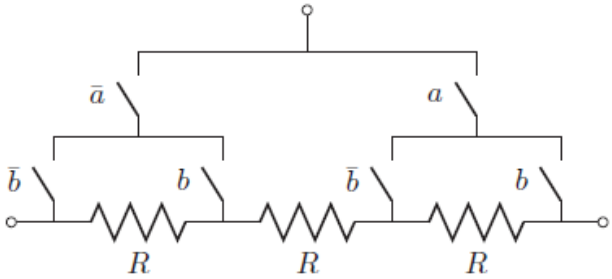

Figure 5. Resistive network used in [2]

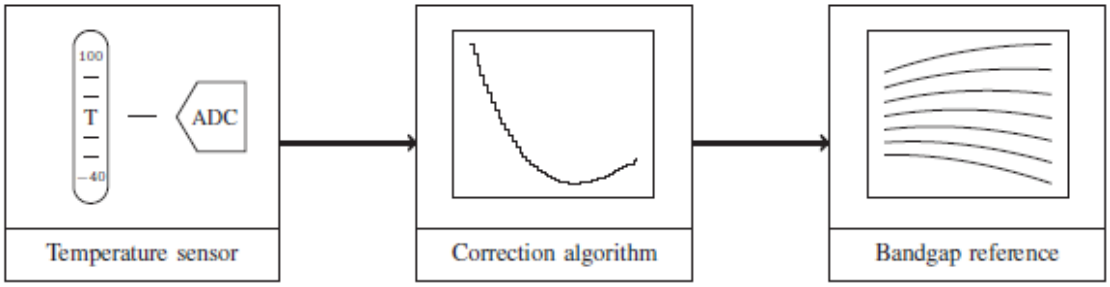

Figure 6. Block Diagram used in [2]

One main disadvantage of this solution is that it requires a lot of circuitry. It uses a complex algorithm to compute the trimming values and it requires a lot of memory for

computation, consuming a large amount of area (0.437 mm^2) in the die. This presents a disadvantage if the BGR is going to be used with other circuits which occupy a larger portion of the die. This implementation also requires external heating.

CHAPTER 3
PROBLEM STATEMENT AND HYPOTHESIS

After fabrication, the design specifications and parameters of the BGR will have shifted from the desired values. This is due to imperfections in the die during the fabrication process. These imperfections are process variations and mismatches that will affect the performance of the BGR. The temperature compensation of the BGR will no longer have a low TC. A simple solution to solve this problem after fabrication is detecting the maximum voltage of the reference, while sweeping the temperature. The maximum of V_{ref} is the point where cancellation should occur, to obtain the optimal cancellation the maximum must occurred at ambient temperature, this will give the lowest TC. Using additional circuitry designed monolithically, it is possible to compensate the BGR. Heating the die internally and trimming V_{ref} accordingly so that the maximum occurs at room temperature. The compensation

3.1. General Objective

Design and simulate an integrated circuit that is capable to correct for the errors in mismatch and process variations such that it gives a lower TC.

3.2. Specific Objectives

1. To design and simulate a bandgap voltage reference, that can have a trimmed TC from 10 to 35 ppm, that before trimming had a worst-case TC of 80 ppm.
2. To design and simulate a slope detection circuit.
3. To design and simulate a heating element circuit.
4. To design and simulate a trimming circuit.
5. To implement and validate an algorithm for the state machine.
6. To design and simulate state machine.
7. To integrate and simulate the complete system.

3.3. Methodology Steps

1. Study of different voltage reference topologies to make selection of one or develop a new architecture.
2. Study of previous work about auto correcting voltage reference, to develop a new method.
3. Study of first order and second order cancellation, to see which method can be implemented.
4. Study of current reference topologies, to see if the auto correcting method can be applied in other types of circuit different than a BGR.

5. Determine and study all the topologies that will be used for the different blocks of the system.
6. Design and simulate the BGR.
7. Design and simulate trimming circuit using the BGR with different errors.
8. Design and simulate a slope detector.
9. Design and simulate a heating circuit.
10. Develop and validate the algorithm for the auto correction of the errors in the BGR.
11. Design and validate the state machine.
12. Integrate all circuits together and make simulation environment to test for different errors in a BGR.

3.4. Methodology Gantt Chart

The time estimated to complete the main tasks of each methodology step are presented in figure 7.

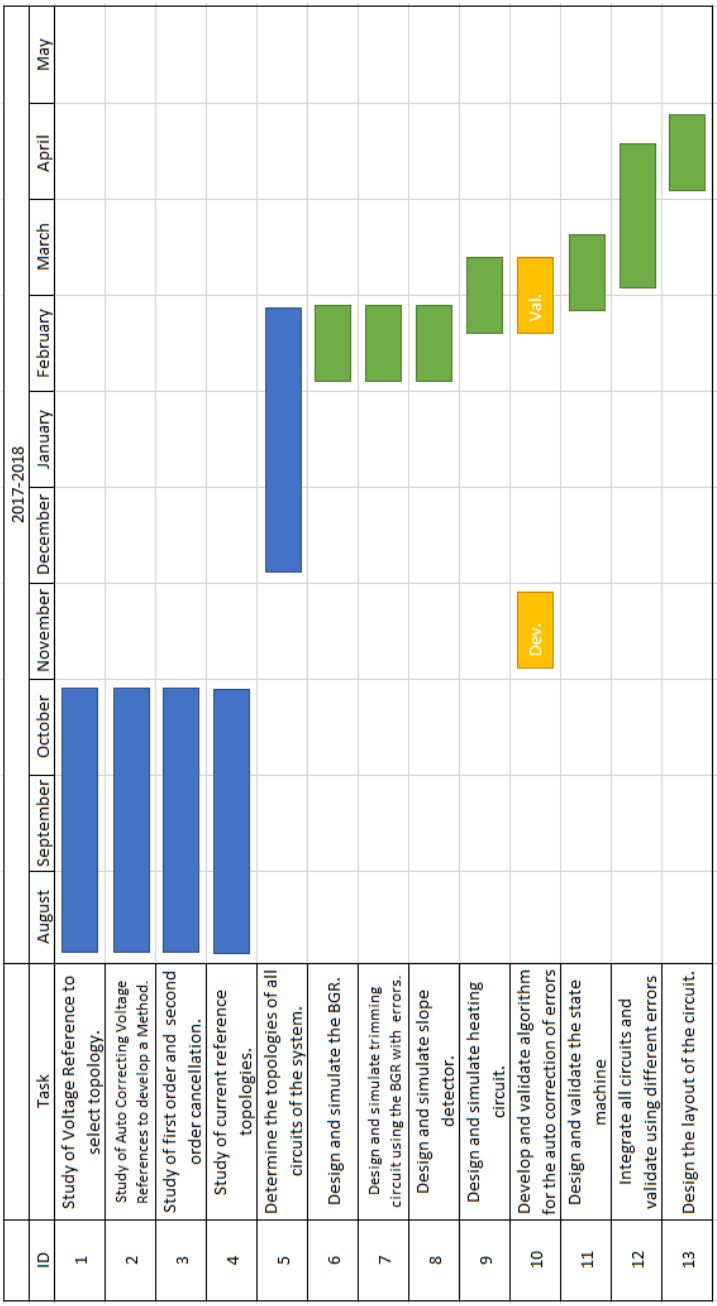

Figure 7. Gantt Chart of Methodology.

CHAPTER 4
THEORETICAL ANALYSIS

4.1. Bandgap Voltage Reference

Bandgap Voltage Reference circuits consist of two principal components, a voltage proportional to the temperature (PTAT) and a voltage complementary to the temperature (CTAT). These two components are designed such that the slope of both components cancel each other so that the voltage does not change with temperature. This is done by multiplying a constant value to the PTAT voltage so that the rate of change with temperature cancels out with the rate of change of the CTAT. To design a PTAT, the voltage difference across two PN junction with different sizes is used. The circuit in figure 8 shows how the voltage across $V_{out} = V_{PTAT}$.

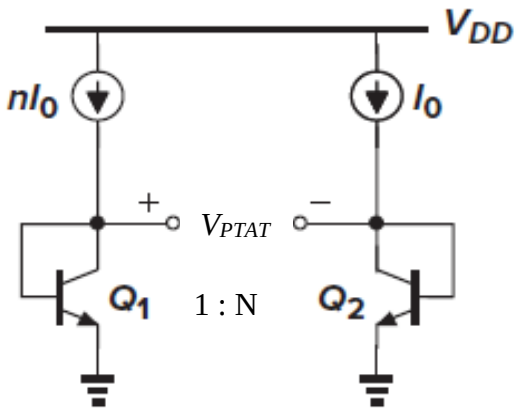

Figure 8. PTAT voltage generation.

$$V_{PTAT} = V_{be2} - V_{be1} = \frac{kT}{q}\ln[N] \quad (1)$$

Where k is the Boltzmann constant, T is the temperature, q is the electron charge, and *N* is the ratio of the transistor sizes (A_2/A_1), where A_n is the area of the transistors. V_{be} is the voltage across a bipolar junction transistor (BJT). To obtain a CTAT voltage; the voltage across a bipolar transistor is used. The voltage across V_{be} behaves like a CTAT. The first problem in designing a voltage reference is finding a voltage that is complementary to the temperature. The V_{be} voltage has a non-linear behavior and is described with this equation:

$$V_{be} = V_{go} - (V_{go} - V_{beo})\frac{T}{T_O} - (n-d)\frac{kT}{q}\ln\left[\frac{T}{T_O}\right] \quad (2)$$

V_{go} is the bandgap voltage of silicon at room temperature, V_{beo} is V_{be} at room temperature. To is the room temperature, *n* is the temperature coefficient of BJTs, and *d* will be 1 if the current of the BJT is PTAT and will be 0 if the current is temperature independent. The equation of a BGR is given by the sum of the PTAT and CTAT voltages.

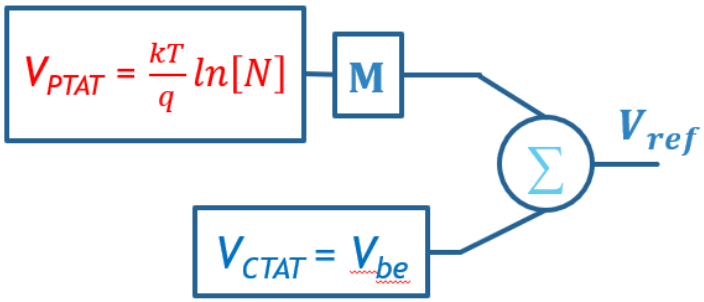

Figure 9. Typical Bandgap Voltage Reference generation.

$$V_{ref} = MV_{PTAT} + V_{CTAT} \quad (3)$$

Substituting (1) and (2) in (3) we get:

$$V_{ref} = M\frac{kT}{q}\ln[N] + V_{go} - (V_{go} - V_{beo})\frac{T}{T_O} - (n-d)\frac{kT}{q}\ln\left[\frac{T}{T_O}\right] \quad (4)$$

To have minimum voltage variation with change in temperature the next condition must be accomplished:

$$\frac{dV_{ref}(T_X)}{dT} = 0 \quad (5)$$

This condition is used to calculate *M* (first order cancellation coefficient). The *M* that satisfies this condition is:

$$M(T_X) = \frac{\left((V_{go} - V_{beo})\frac{1}{T_O} + (n-d)\frac{k}{q}\left(1 + ln\left[\frac{T_X}{T_O}\right]\right)\right)}{\frac{k}{q}\ln[N]} \quad (6)$$

Substituting $M(T_0)$ in (4) gives:

$$V_{ref} = V_{go} + (n-d)\frac{kT}{q}\left(1 - \ln\left[\frac{T}{T_O}\right]\right) \quad (7)$$

Equation 7 shows that V_{ref} will still have some variation with temperature, this variation is in the order of millivolts. The TC, measured in ppm/ºC, for this equation is given by:

$$TC = \frac{1}{V_{ref}(T_o)}\frac{\Delta V_{ref}}{\Delta T}10^6 \quad (8)$$

4.2. Mismatch and Process Variations of BGRs

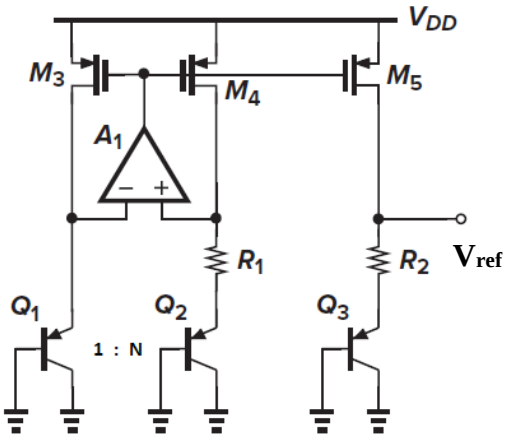

Figure 10. Low Voltage Bandgap Reference

The BGR studied is the low voltage BGR shown in figure 10, which is commonly used. It has components that need to be matched. For example, the *m* that is used to scale the V_{PTAT} is a ratio of two resistances.

$$m = \frac{R_2}{R_1} \quad (9)$$

When these two resistances are fabricated into the die they will have a variation in size that will result in a difference in resistance value. This variation is a mismatch between the two resistors. This will present an error for the V_{PTAT}, another mismatch found here is the *N* which is the ratio size of the two BJT transistors, as the resistances any variation in the sizes will result in a mismatch. Depending on the percentage of mismatch this will result in a V_{PTAT} with a different slope. This will affect the BGR TC.

Process variations will affect the V_{be} used for the V_{CTAT}. These variations occurred to changes during the doping of the semiconductor. The parameters that are affected are: V_{go}, V_{beo}, and *n*. These errors will result for the BGR voltage as an offset and a variation in the TC.

To correct all these errors the auto correction circuit must be capable of adjusting the slope of the PTAT component and scale V_{ref} so that the offset created by process variation in V_{be} can be corrected.

$$V_{ref} = a\left(\frac{R_2}{R_1}V_{PTAT}\right)(1 + Error_{PTAT}) + V_{CTAT}(1 + Error_{CTAT}) \quad (10)$$

$$Error_{PTAT} = \frac{(1+\delta R_2)}{(1+\delta R_1)}\frac{(1+ln[\delta N])}{\ln[N]} + V_{OS} \quad (11)$$

$$Error_{CTAT} = \delta V_{go}\left(1 + \frac{T}{T_O}\right) + \delta V_{beo}\frac{T}{T_O} - \delta n\frac{kT}{q}ln\left[\frac{T}{T_O}\right] \quad (12)$$

$Error_{PTAT}$ is the mismatch and process variation for the PTAT component and $Error_{CTAT}$ is the result of the process variation of the CTAT component; δ to the left of a parameter indicates the error of that certain parameter. The *a* parameter can be used for the correction of the errors in the slope change of the PTAT, where the trimming circuit is implemented. This circuit will correct different types of error. A topology must be selected such that the implementation of equation (10) can be executed.

The cancellation of this errors will occur when:

$$a = \frac{\left(\frac{V_{go}-V_{beo}}{T_O}+(n-d)\frac{kT_O}{q}\right)}{\frac{R_2 k}{R_1 q}ln[N]}\frac{(1+Error_{CTAT})}{(1+Error_{PTAT}-V_{OS})} \quad (13)$$

This will ensure that equation (5) is still valid for the circuit.

Another effect that will affect the BGR performance is the op-amp offset due to transistor size mismatch. This error can be corrected by offset nulling techniques or using chopping. It can also be reduced by carefully designing the layout. In [4] and [5] two different techniques are presented to correct offset.

4.3. Trimming Circuit Resolution

The trimming circuit it used for the fine tuning of the BGR, this will help scale the value of the PTAT component. Different topologies of trimming circuit exist, one of the most popular is to use a resistive trimming network [2], [4], [5]. It consists of transistor that act as switches connected to the resistors; by shorting a resistance or resistances in the network it will make the total resistance value of the network change.

To ensure an accurate trimming resolution the variations of your output must be known. In this case how it detects how the Voltage Reference *Vref* changes with temperature.

$$\frac{dV_{ref}(T)}{dT} = m\frac{dV_{PTAT}}{dT} + \frac{dV_{CTAT}}{dT} \quad (14)$$

To obtain first order cancellation the change of the voltage reference vs temperature must be 0. Making the left side equal to 0 and solving by m gives:

$$m = -\frac{\frac{dV_{CTAT}}{dT}}{\frac{dV_{PTAT}}{dT}} \quad (15)$$

The BGR is affected by different mismatch and process variations. This results in different rates of change of V_{CTAT} and V_{PTAT} with respect to temperature. This gives a range of *m* values, so m_{max} and m_{min} values must be characterize. These values are the maximum and minimum first order cancellation coefficient value (*m*). Recalling equation 9, now the ratio of the resistances R_1 and R_2 needs to vary from m_{max} to m_{min}. R_1 is a fixed value and R_2 is the changing value.

$$m = \frac{R_{2i}+bit*R_{step}}{R_1} \quad (16)$$

$$m_{min} = \frac{R_{2i}}{R_1} \quad (17)$$

$$m_{max} = \frac{R_{2i}+n_{max}R_{step}}{R_1} \quad (18)$$

Equation 16 represents the trimming circuit equation where R_{2i} is the initial value of the minimum resistance required that will result in the minimum first order cancellation coefficient (m_{min}). The variable *bit* is an integer number that is represented by a code and its max value determines the resolution that the circuit has to correct the first order cancellation. R_{step} is the value that represents how much change will result from one code to another. This equation ensures that for a known mismatch and process variations of a

BGR using the topology described in figure 9 will guaranteed that the first order cancellation can be achieved.

4.4. Heating Element

To obtain a change in temperature a heating element inside the chip is required. The heating element uses the Joule Heating law, where current passes through a resistor and produces heat. A change in temperature inside the device can be produced by applying a known current into a resistance for a certain amount of time after having the device by 1º or 2º C below 27º C. The heating element needs to be characterize because the resistance value, current, time and the area of the resistance, will determine how much change in temperature will be produced. This data was characterize using Comsol simulating a resistance that will be used to heat the chip. Appendix A contains the characterized data obtained by the results in Comsol. Since the change in temperature is dependent of time, a counter will be used to verify that it has reached the desired heating temperature. To have a more accurate change in temperature a circuit can be used as temperature monitor, this will ensure that the device is below 27ºC by 1º or 2ºC and can start heating again. To guaranteed that the slope detector can measure the change in the voltage reference the next equation must be stablished.

$$\Delta V_{ref} = Vref(T_o) - Vref(T_1) \quad (19)$$

$$\Delta V_{ref} = \left[m\frac{k}{q}\ln[N] + V_{go} - \left(V_{go} - V_{beo}\right)\frac{1}{T_O}\right]\Delta T - (n-d)\frac{kT_1}{q}\ln\left[\frac{T_1}{T_O}\right] \quad (20)$$

$$\Delta T = T_1 - T_o \quad (21)$$

The ΔT represents the change in temperature where T_1 is the temperature at which the device is heated and T_o is 27º C. This equation is used to determine the sensitivity of the slope detector according to the temperature change applied. The heating element temperature is characterized by this equation.

$$T(t) = T_o + \Delta T\left(1 - e^{-t/\tau}\right) \qquad (22)$$

Where τ represents the constant of time which is dependent of the current, resistance value. If the ambient temperature is at T_o, it will take the same time to reach temperature T_1. The counter circuit will indicate when to measure V_{ref} at T_1 or a circuit can be used to sense the temperature, for simplicity in this work a counter is used.

CHAPTER 5
SYSTEM DESIGN AND COMPONENTS OVERVIEW

This chapter discusses the system architecture from a top-level design and discusses the more important circuits of the design. Figure 11 shows the architecture of the proposed system. The last section of this chapter covers the algorithm of the system described in detail.

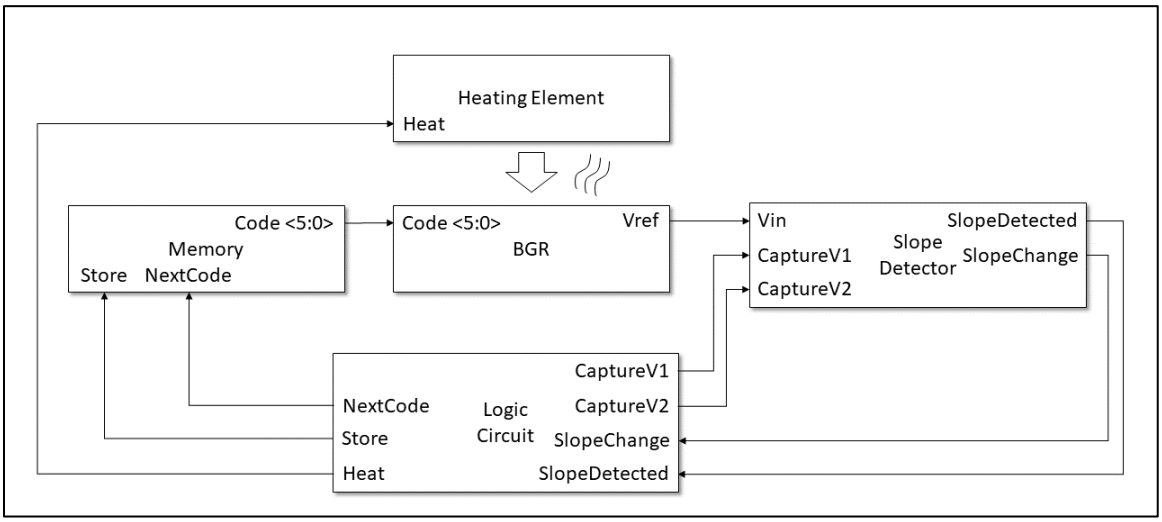

Figure 11. Block Diagram of the Automated Temperature Trimming Circuit

5.1. System Architecture

The proposed architecture of the system is presented in figure 11. It shows all the main blocks that are required to perform a first order automated cancellation on-chip. Starting off with the Bandgap Voltage Reference which is the block that is going to be corrected, the bandgap has a trimming circuit is used to for first order effect cancellation in this case

the trimming circuit consists of a resistor array that is manipulated via switches to change the overall resistance ratio that will make the first order effect cancellation. The slope detector function is simple, it will detect if the slope is positive or negative. It will then feed that information to the main logic circuit that will determine if the optimal code has been found or does it need to check the next code. The heating element function is to produce a change in temperature; then the counter in the logic circuit will determine when to store the first voltage V1 and then the second voltage V2 these two voltages are used by the slope detector to determine the slope sign. When the slope detector has detected a change in the sign of the slope it will create a SlopeChange high output to the main logic circuit storing the trimming code circuit in memory.

The architecture consists of digital blocks and analog blocks. Since the digital blocks are a lot less susceptible to errors of mismatch and process and mismatch, variations they were implemented in VerilogA code blocks. The blocks will have the same behavior of the actual digital circuit. The analog blocks such as the BGR and the slope detector where implemented doing actual transistor level design.

5.2. Bandgap Voltage Reference Architecture

The topology selected is the one presented in figure 12, instead of using conventional current mirrors it uses cascoded current mirror. This will produce a more precise current across variations. The resistance at the output of the BGR is changed with a resistive trimming network. This is used for the calibration of the first order effect cancellation of the BGR circuit.

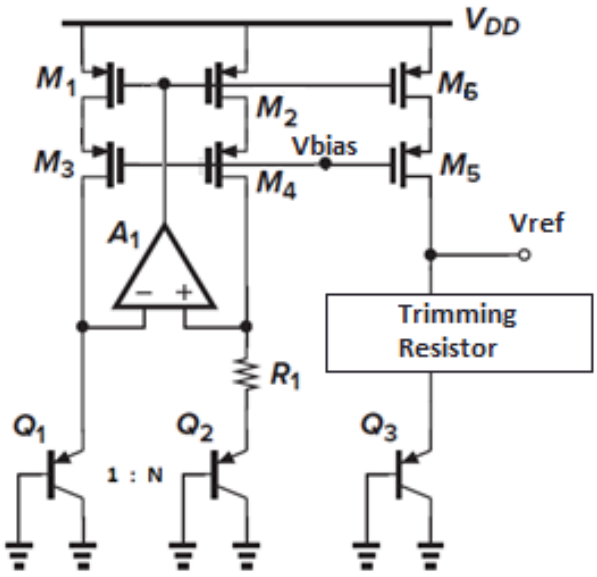

Figure 12. Proposed Bandgap Voltage Reference

The bandgap core shown in figure 12 uses the op-amp A_1. It ensures that the voltages connected to the non-inverting and inverting inputs are the same. This will create current that has a PTAT behavior across resistance R_1. When that current passes through the trimming resistive network it will produce V_{PTAT}. The pn junction of the transistor Q_3 has

V_{CTAT} behavior so the output Vref has a voltage that is the sum of a V_{PTAT} with V_{CTAT}, where the first order cancellation coefficient is controlled by the trimming resistor.

5.3. Trimming Circuit

The trimming circuit selected for the BGR consist of a resistive trimming network with switches in parallel shown in figure 13.

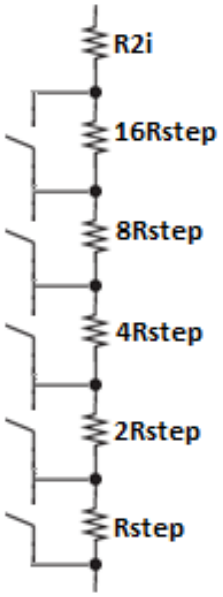

Figure 13. Resistive trimming network used in the BGR circuit.

The values of the resistances where calculated using the equations from 15 to 18 in chapter 2, the maximum bits, and Rstep were chosen based on the mismatch and process values that where characterized using a Monte Carlo simulation with 200 samples.

5.4. Slope Detector

For the slope detector circuit, the topology selected was an op-amp in open loop and one sample and hold circuit were chosen to implement this component (see figure 14).

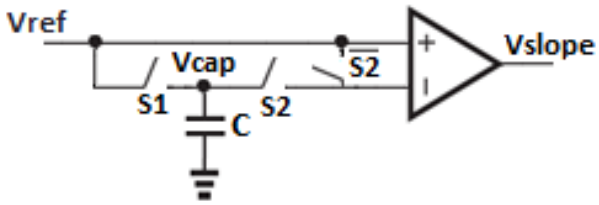

Figure 14. Slope Detector topology.

This circuit samples and holds voltage Vcap at the device temperature and compares with another voltage at the heating temperature. The open loop op-amp will work as a comparator when the S2 signal is high and S1 is open. Vslope will go high if Vref>Vcap or will go to ground if Vref≤Vcap. This circuit is accompanied with digital circuit implemented in VerilogA code that will help detect a change in slope from one trimming code with the previous code. It will simply verify if the previous slope is different from the present one.

The most complex part of this component is designing an op-amp that has low offset. Mismatch and process variations will affect the op-amp input offset, making it difficult to detect small changes of Vref. Across temperature. Equation 19 in chapter 2, show that the values calculated for a change in temperature of 20º C will require an offset of less than 100 µV. So, the op-amp offset must be lower than this.

The amplifier implements the use of auto-zeroing (figure15). A technique where it samples the offset voltage and its store in an auxiliary port via a capacitor to null the offset. Transistor M6 works in the ohmic region, in negative feedback configuration with the inputs shorted and the output of the folded cascode connected V_{AUX}. The voltage at V_{AUX} is proportional to the offset at the input. After the switches are open V_{AUX} will remain storing that voltage and it will compensate for the input offset. While the BGR circuit is being heated, the Op-Amp is detecting its offset. Once its stop heating it will compare Vref with Vcap at the input. Figure 16 shows the timing sequence of the switches.

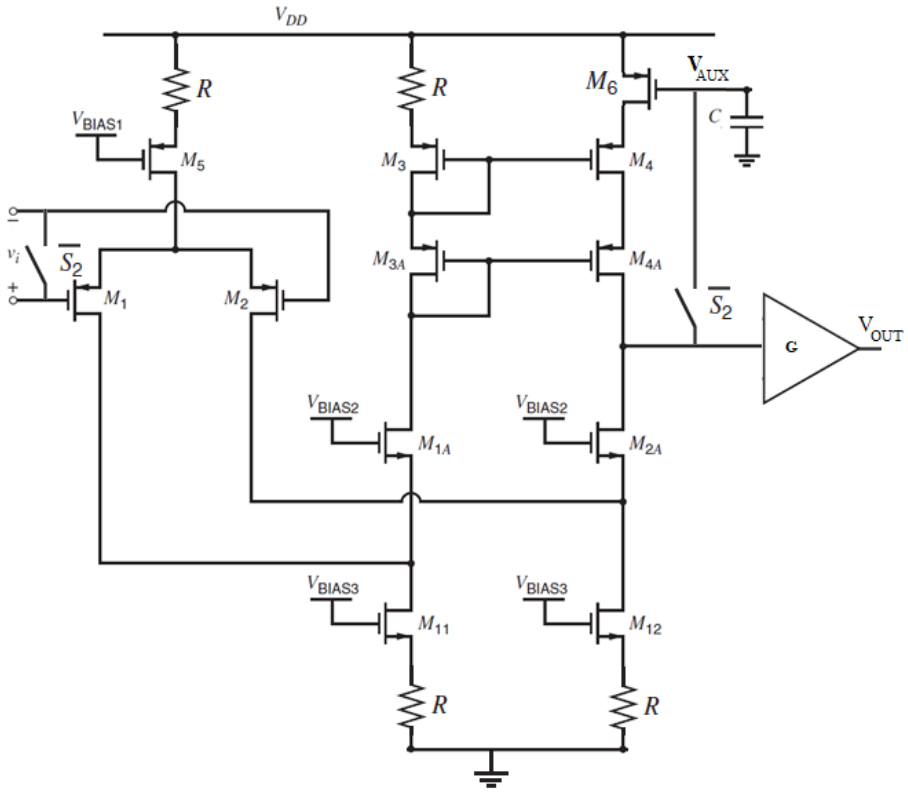

Figure 15. Auto Zero Amplifier Circuit.

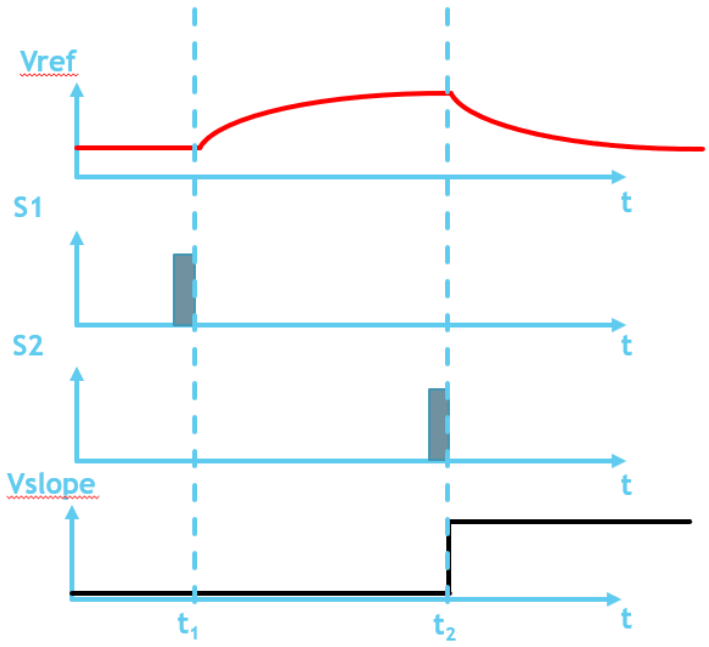

Figure 16. Timing sequence of switches

5.5. Heating Element

For the heating element a simple current mirror (figure 17) of a biasing current with a resistor connected to ground. To turn on and off, a PMOS transistor will pull up or down the gate of the current mirror turning off or on the transistor acting as a current mirror. The size of the resistor and the transistor were chosen according to the amount of current passing through it. The current selected for the circuit was of 20mA.

The layout of the resistor needs to be like a serpentine (figure 18) in top of the BGR core. This way is ensured that the BGR is being heated uniformly. Metal 3 can be used as the heating resistance material in the layout; that way it will be on top of all the circuits inside the chip that need to be heated. The heating element will start heating when the logic

circuit sends an enable signal. It will start heating from the temperature of the device, this temperature will be really close to the ambient temperature outside the device; this is only true if the device doesn't dissipate too much power when operating. To have a low TC from the first order effect cancellation the temperature at which the first point slope is stored must be close to 27º C. Appendix A.2 shows how changing the outside ambient temperature will affect where the maximum occurs. Then when the chip reaches a temperature near within a accuracy of ±3ºC from 47º C the counter in the logic circuit will send a signal to shut down the heating element. It will repeat the process until the system has found the optimal code for the first order cancellation, then it will be off forever. A fuse can be implemented so that when the system founds the optimal code; the fuse will be blown off ensuring that the circuit cannot be used.

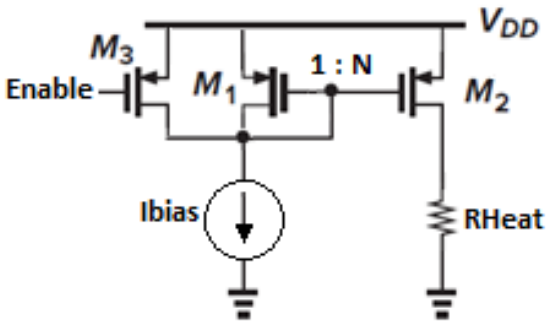

Figure 17. Heating Element.

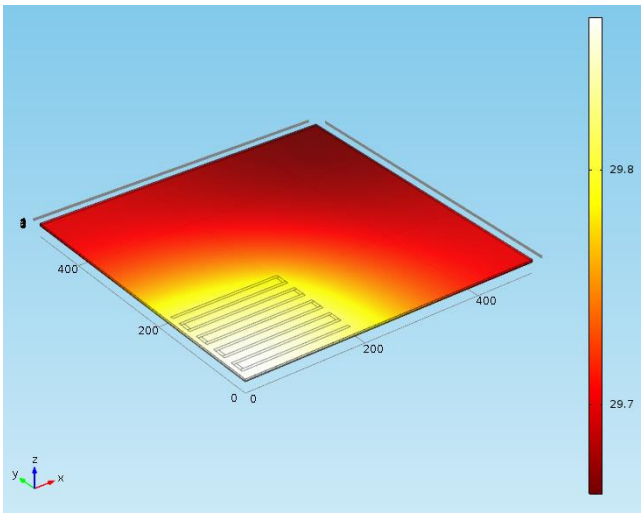

Figure 18. Serpentine layout of the heating resistance simulated in Comsol.

5.6. Logic Circuits

The logic circuits or digital circuits that are in the system are: the main logic circuit, the memory for the optimal code and a digital part of the slope detector. The main logic circuit is where all the decisions are taken and decides which circuit to activate and which to deactivates. The logic circuit implements a trimming algorithm, the flowchart can be found at appendix C. It's a state machine that the code of the block has been implemented in VerilogA, these codes can be found in appendix D. These VerilogA blocks implement the same behavior of the actual digital circuit.

5.7. Trimming Algorithm and Timing Diagram

The trimming algorithm is based in all the blocks that are used for the automated temperature trimming circuit. The algorithm functions this way, after the circuit is been turned on for the first time it will check if a fuse in the circuit has been burned. The fuse is only burned once the optimal code has been stored in memory. If the fuse is not burned, the heating element will start heating the IC. Then the counter will start, just right before that moment the slope detector will store the voltage reference value V1. When the counter reaches a 100 mS it means that the circuit temperature is near 47º C this value is V2, and it will compare it with V1. Then it will detect if the slope is positive or negative. It will then check if the slope was negative or positive with the previous slope value stored. If the slope was the same or this is the first time storing the slope value, it will change the trimming code to the next code. It will repeat the process again heating the device, storing the values, detecting the slope sign until the slope on the previous code its different form the next code. Once that happens it will store the trimming code in memory and will burn the fuse. The next time the circuit is on it will use the code stored in memory that will give a more accurate first order cancellation, achieving from 20 to 30 ppm theoretically of TC. Appendix C contains a flowchart that describes the algorithm explained here.

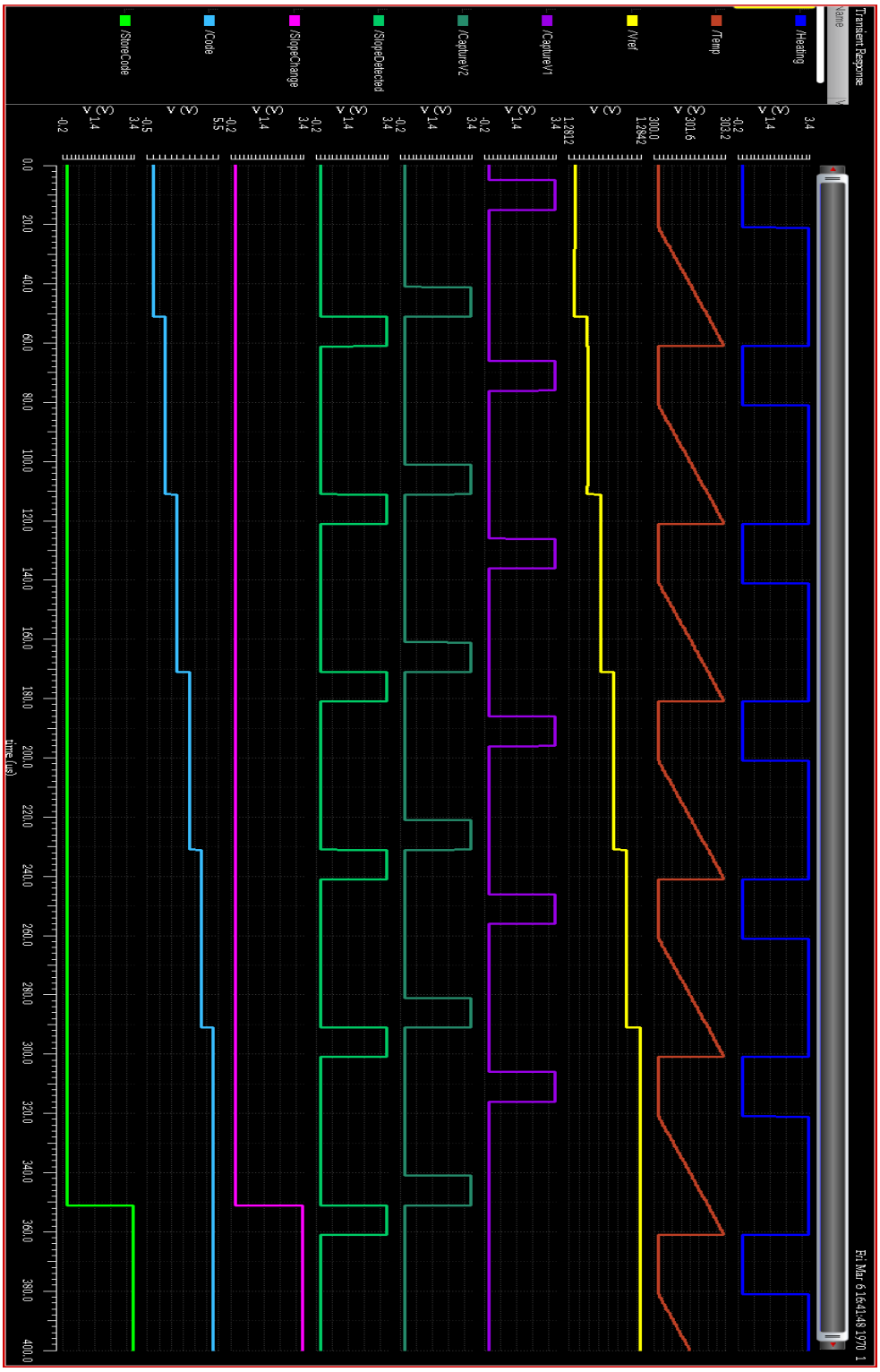

Figure 19. Timing Diagram of the signals.

The signals showed in figure 19, from top to bottom are: Heating, Temperature, Vref, CaptureV1, CaptureV2, SlopeDetected, SlopeChange, Code, StoreCode. The Heating signal goes high to indicate that the circuit is being heated, and low when the temperature is at nominal value. The Vref signal is the output of the BGR that is being monitored by the slope detector. CaptureV1works as a pulse goes high when the circuit is being started to heat as the Heating signal rises. CaptureV2 is also a pulse that goes the desired heating temperature has been reached. These two signals will store two different voltages of the BGR into the capacitors of the slope detector. Once the slope detector has the values, the SlopeDetected signal goes high for an instant. Then the Code signal will go high changing to the next code, repeating this process until the SlopeChange goes high. When this happens the StoreCode will go high, and the circuit will store in memory that code.

CHAPTER 6
RESULTS AND ANALYSIS

This chapter shows the results of the simulations done to validate the system. The first part shows BGR simulations, implemented first in code using only the bandgap equations. Then using a BGR without any mismatch, and then simulations to show how the BGR is affected by mismatch and process variations. The second section discusses the slope detector circuit and offset cancellation simulations which is a critical part of the design. The last section shows the system simulations, first ideal simulation, then using a BGR with mismatch and process variations correcting the first order cancellation errors.

6.1. BGR Monte Carlo Simulations

To validate the hypothesis the first step was to develop a code in Matlab (Appendix B), to see how the slope changes vs the codes. This code was developed using the equations 4, 16 and 20 from chapter 2. The first equation being the Bandgap Voltage Reference, then the equation for the first order coefficient as function of the trimming codes and the equation for delta Vref which is the slope normalized to a known change of temperature (20º C). The change in Vref needs to go from negative to positive, this indicates that the maximum value of Vref has been crossed, at that point the TC will be the lowest. It can be seen in figure 20 it can be observed that delta Vref crosses the y axis at code 15, meaning that it has crosses from negative to positive. On top graph the TC of Vref is the lowest, in this case 15.6 ppm at code 15.

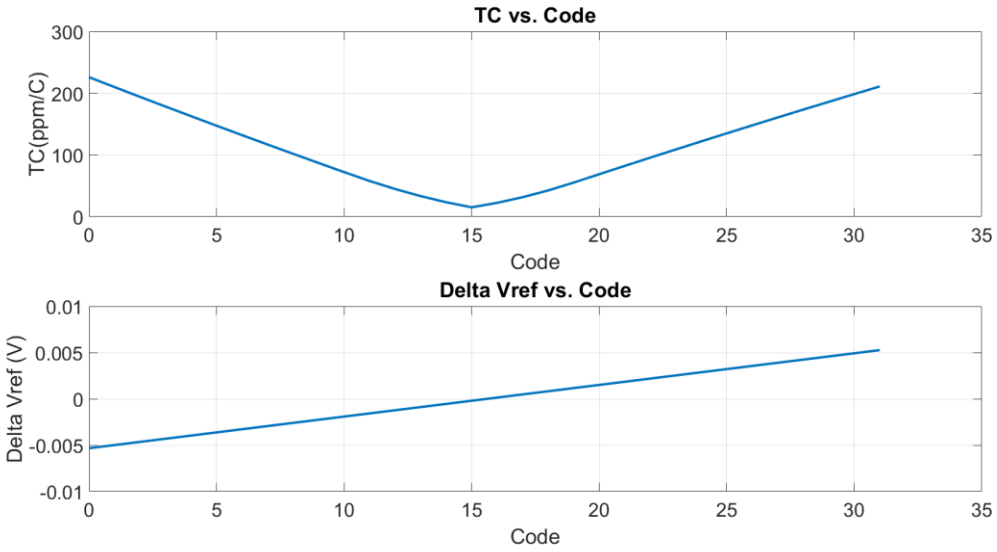

Figure 20. Top graph shows the TC on y axis. Bottom shows Delta Vref on y axis. In both graphs the x axis represents the trimming code.

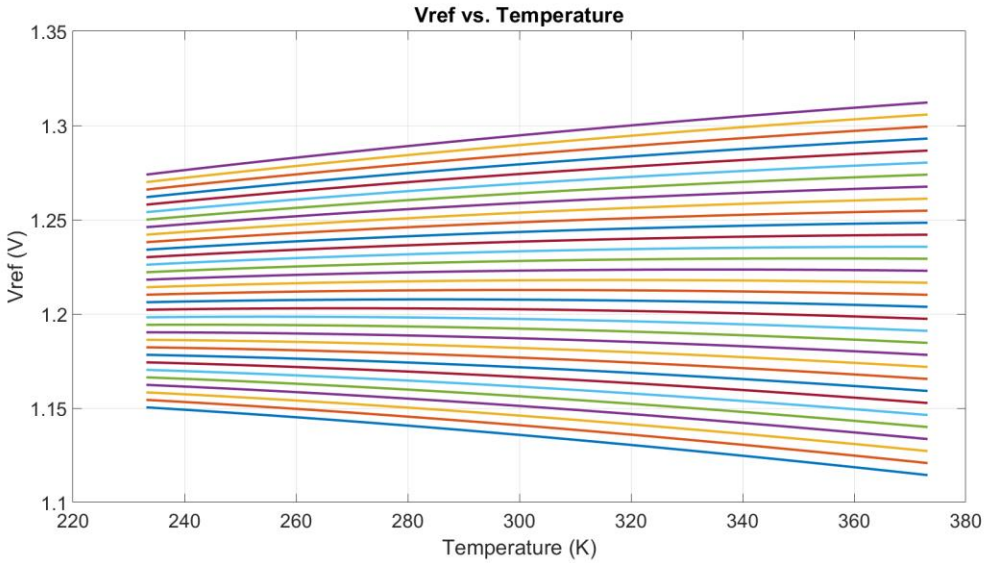

Figure 21. Vref with different trimming code vs the temperature in Kelvin.

Now that hypothesis has been validated using the equations on chapter 2.

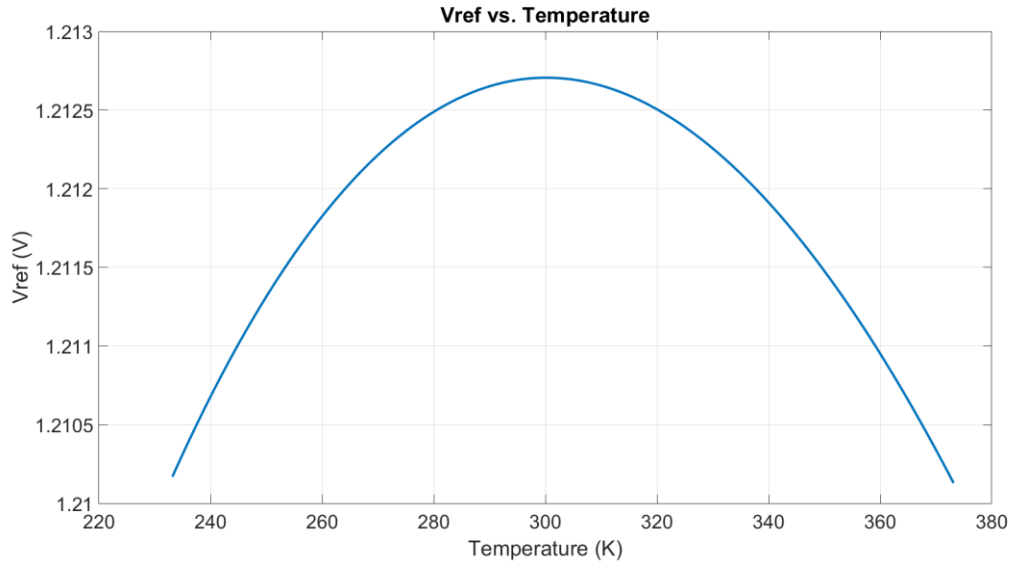

Figure 22. Vref vs Temperature with trimming code being 15.

The TC was calculated for each of the 32 Vref using equation 8. Figure 21 shows the family of curve of Vref by changing the trimming code from 0 to 31. Figure 22 shows the curve of Vref using the code with a more accurate first order cancellation. With the hypothesis validated, a BGR circuit is developed to see the same behavior. This circuit is found in appendix E.2.

The circuit was simulated using Cadence Virtuoso with a 130nm process technology and the simulations from figure 20 to 22 were done using a DC analysis sweeping the temperature from -40º to 100º C. Figure 22 shows the same behavior as described by the Matlab code, the optimal code for a first order cancellation gives a TC of 14.48 ppm. The negative to positive transitions occurred on code 15 and code 15 gives the lowest TC. Figure 23 shows the family of curve of Vref with different trimming codes in cadence simulation and figure 23 shows Vref using the trimming code 15, which is the code with the lowest TC.

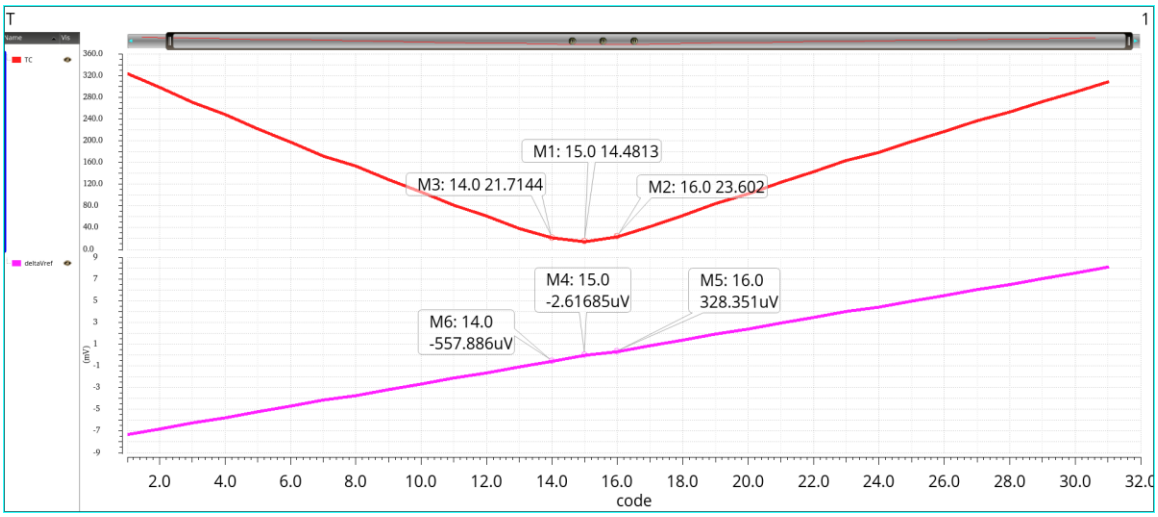

Figure 23. Cadence BGR temperature sweep DC simulation top TC vs Code, bottom delta Vref vs Code.

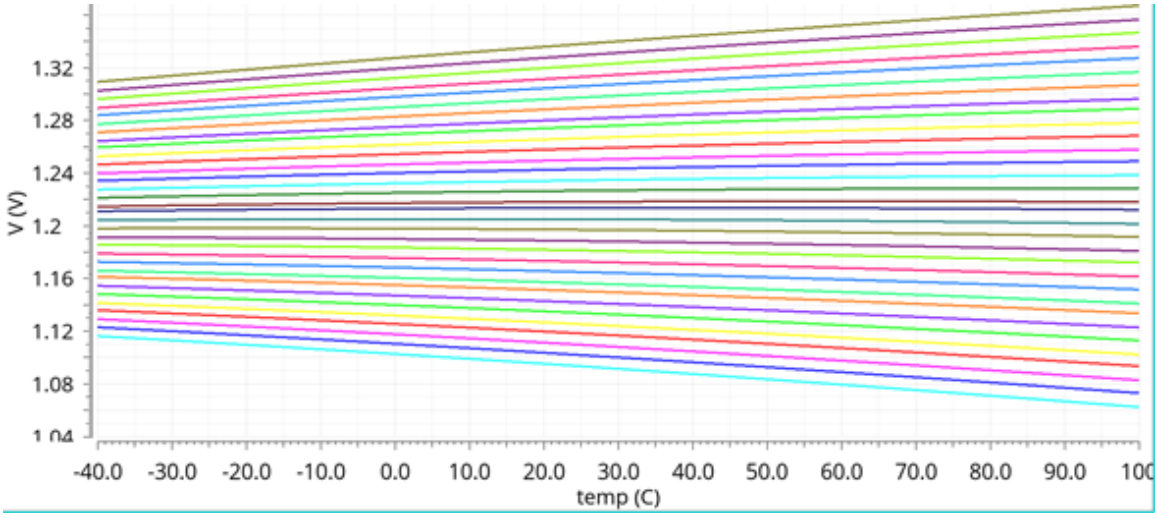

Figure 24. Cadence BGR temperature sweep DC simulation, Vref with different trimming codes.

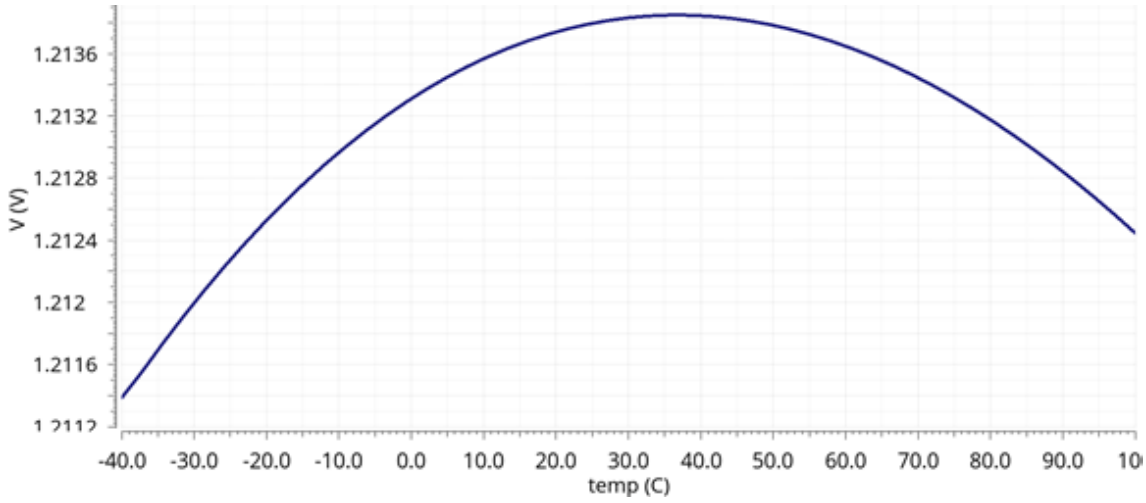

Figure 25. Cadence simulation, Vref vs Temperature with trimming code being 15.

6.2. Slope Detector and Offset Cancellation Simulation

To most critical part of the slope detector is the op-amp. The offset will decide how precise the detection is going to be the offset needs to be lower than 100 µV. The change of Vref when is sampled by the slope detector will have values ranging from values close to 0 up to millivolts. The voltages that are close to zero, can be smaller than 1 µV, this value will occur when the BGR is having an accurate first order cancellation, the next code will give a voltage difference greater than 100 µV. In the case of having a voltage less than the offset voltage, the op-amp will go high or will go low. So, at the point of optimal cancellation it could be detected a negative or positive slope. This doesn't affect because at that point is expected to have a change so there will always be an error of plus or minus one code near the optimal code. A 100 µV offset is desired so that the system doesn't fail by an error of two codes. The circuit used in this simulation is shown on appendix E3. The

offset before using auto zero implementation was from -1.6 mV to 1.7 mV. When using the auto zero technique the offset goes from -50 µV to 50 µV.

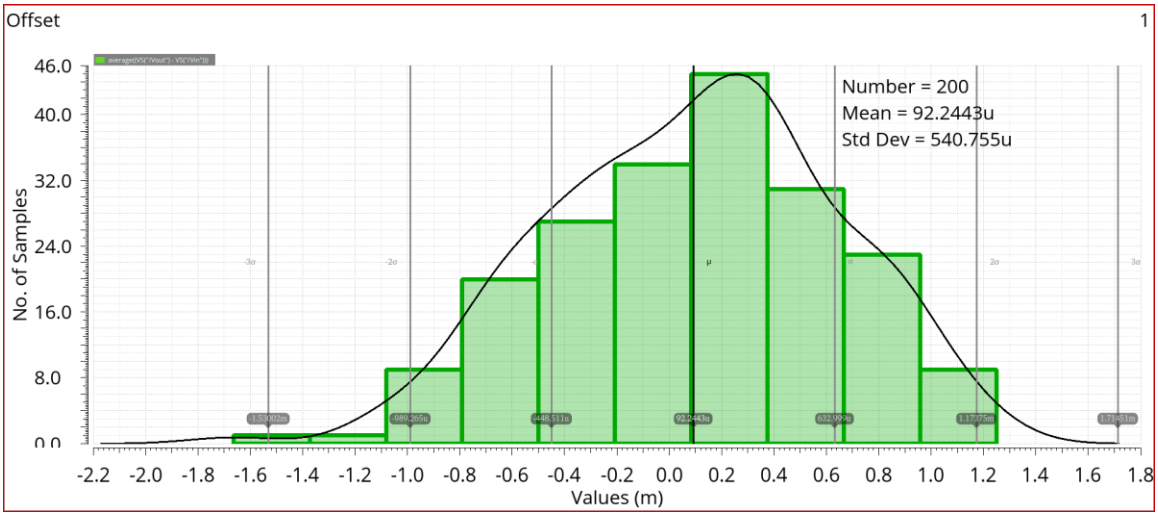

Figure 26. Normal distribution showing offset before correction.

6.3. System Level Simulation

The simulations on the first part proved that the optimal first order cancellation occures when the change in slope changes sign. To test the systme the BGR needs to suffer from mismatch and process variations. This is done using a Monte Carlo simulation which will alterate the BGR, as it will happen after fabricating the actual IC. 200 samples were chosen with random mismatch and process variations. For all of these samples a TC was measured before correction and after correction. These two values will be compared to see how the automated trimming temperature trimming circuit is performing. Appendix E.1 shows the circuit that was used for this simulation.

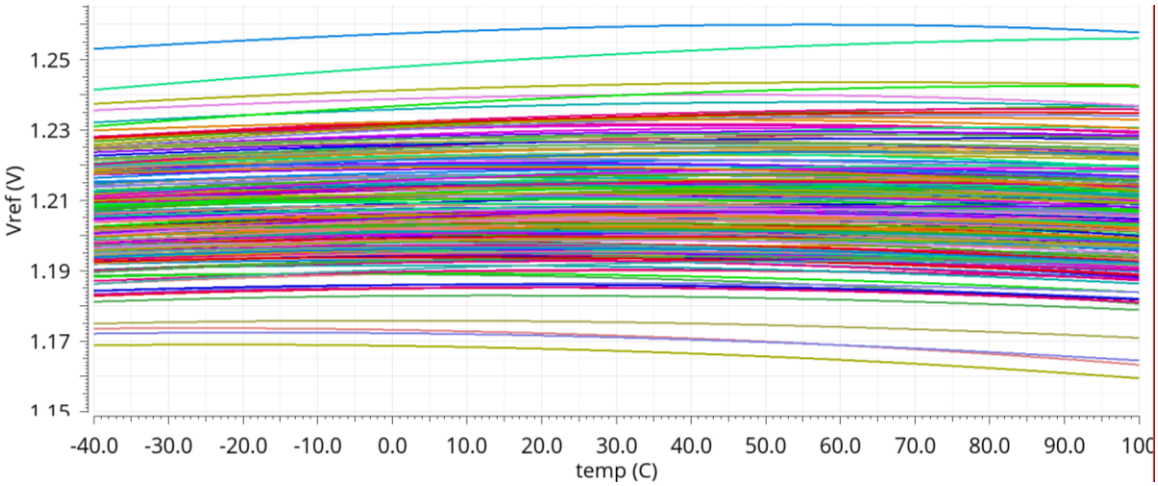

Figure 27. Cadence simulation, Monte Carlo of the BGR, Vref vs Temperature of BGR circuit with no system integration.

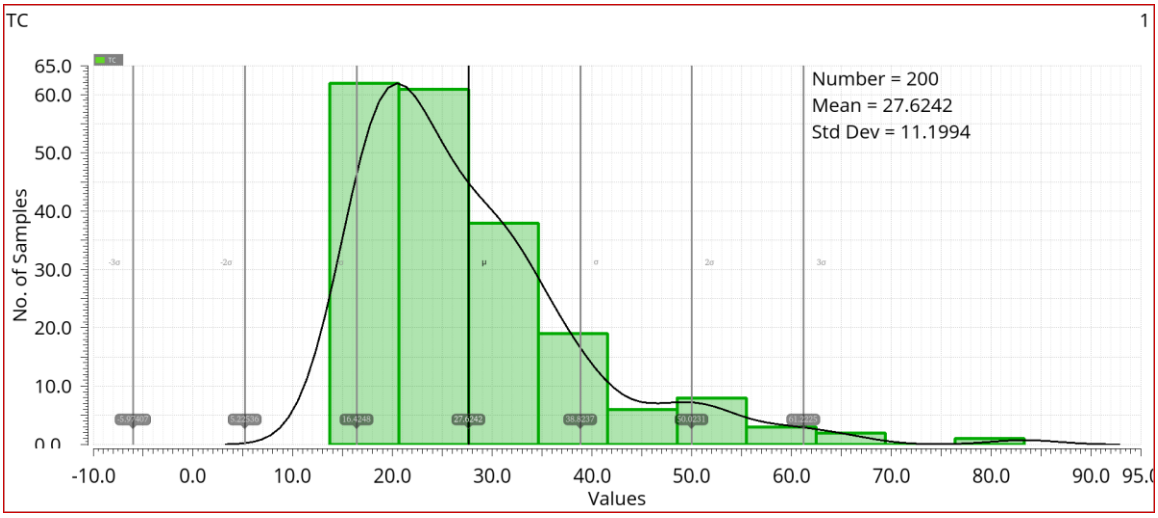

Figure 28. Normal distribution showing TC values of BGR circuit with no system integration.

The family of curves shown in figure 27 show the variation of the voltage reference after being affected by process and mismatch variations. Figure 28 shows the TC normal distribution that goes from 15 to 80 ppm. After the BGR was corrected using the proposed

system, the TC was reduced to 7.207 up to 32.4 ppm. Figure 32 shows the normal distribution of the TC after being correct by the automated temperature trimming circuit.

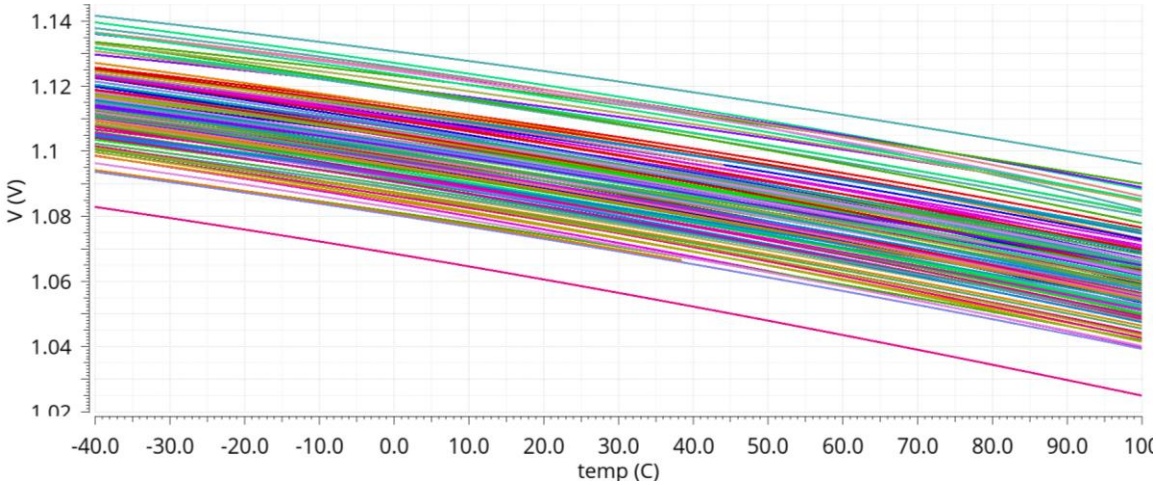

Figure 29. Cadence simulation, Monte Carlo of the BGR, Vref vs Temperature.

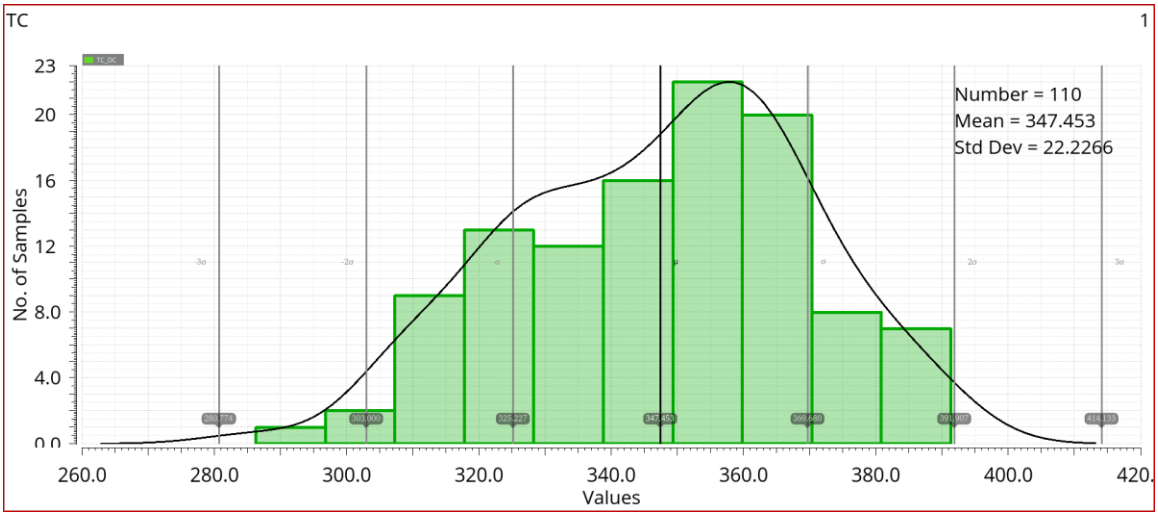

Figure 30. Normal distribution showing TC value before correction.

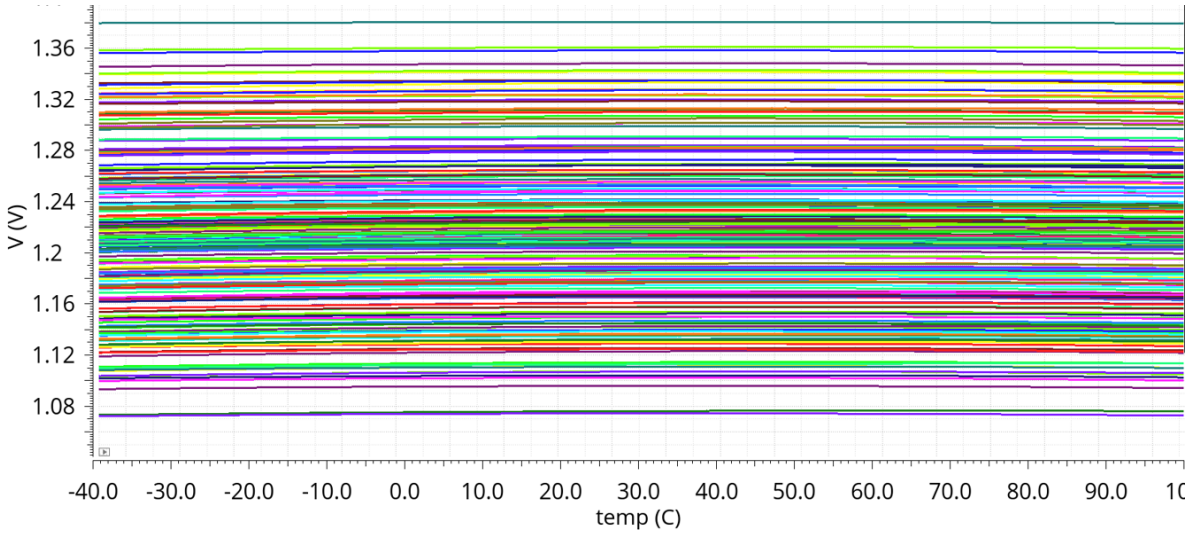

Figure 31. Cadence simulation, Monte Carlo of the BGR, Vref vs Temperature, after being corrected using ideal Slope Detector.

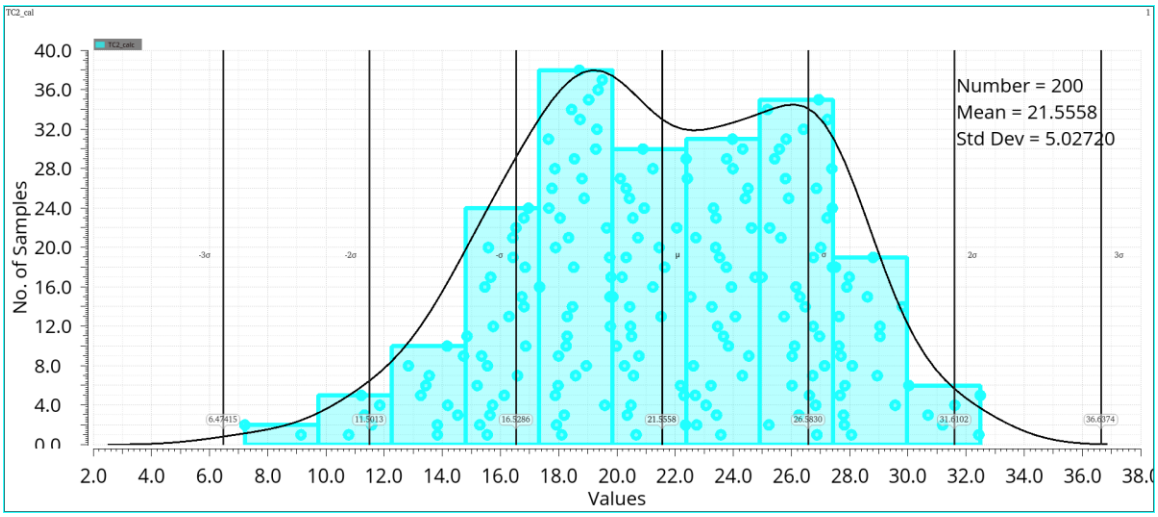

Figure 32. Normal distribution showing TC value after correction using ideal Slope Detector.

The results using an ideal Slope Detector show that the system can correct the first order errors caused by the mismatch and process variations after fabrication. Figure 29 shows that the voltage of *Vref* always had a negative slope this was a desired behavior. By always starting with a negative slope it guaranteed that the design will have trimming codes

to correct the device. When the codes start to the rise the slope of the PTAT component will increment cancelling out this negative behavior of the voltage reference. After being corrected, the same family of curves in figure 29, will be flatter (figure 31). Having flatter lines mean that the voltage reference has less voltage variation across temperature. In this case the TC goes from 6.4 to 36.7 ppm/ºC (using 3σ values).

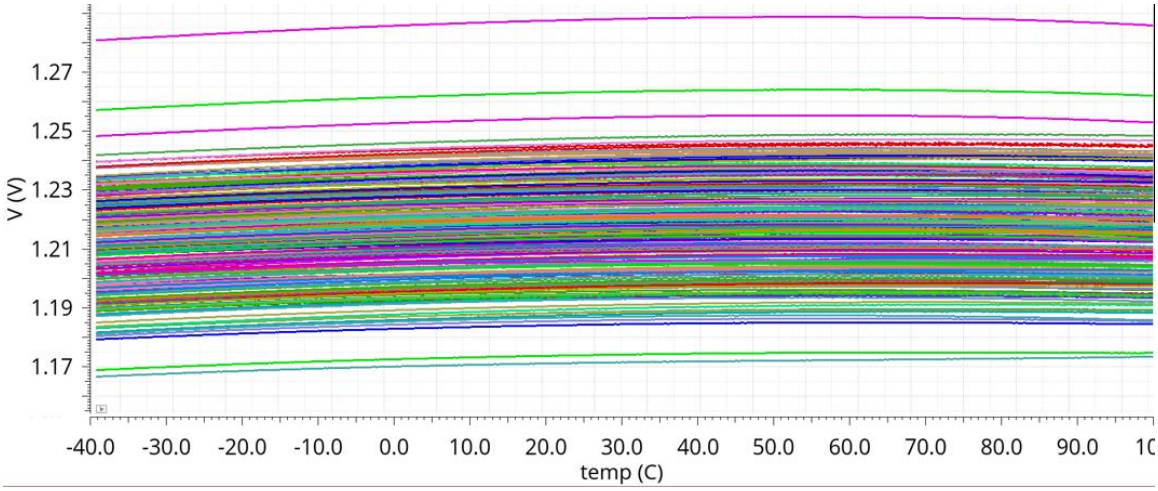

Figure 33. Cadence simulation, Monte Carlo of the BGR, Vref vs Temperature, after being corrected.

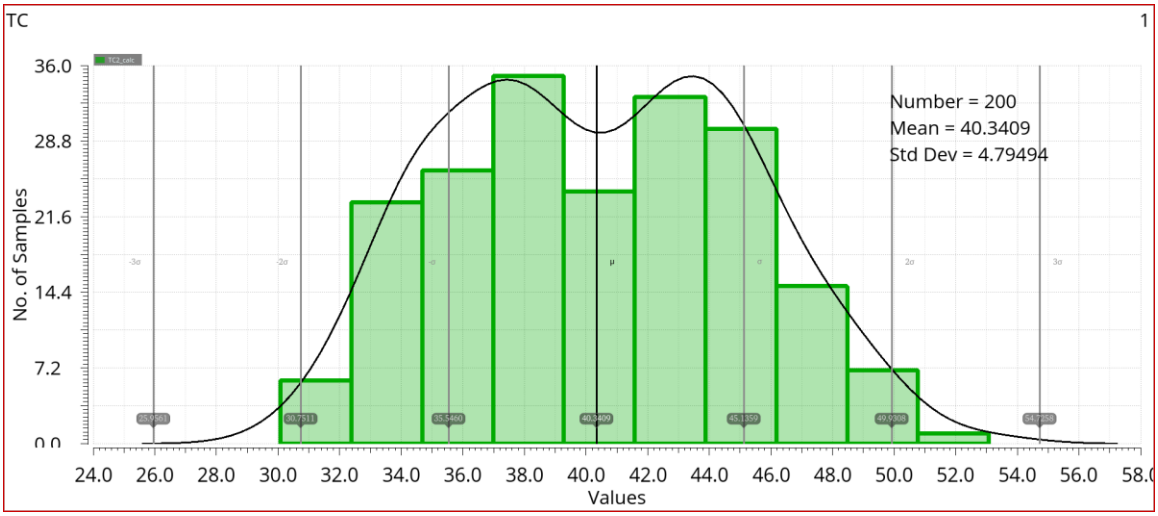

Figure 34. Normal distribution showing TC value after correction.

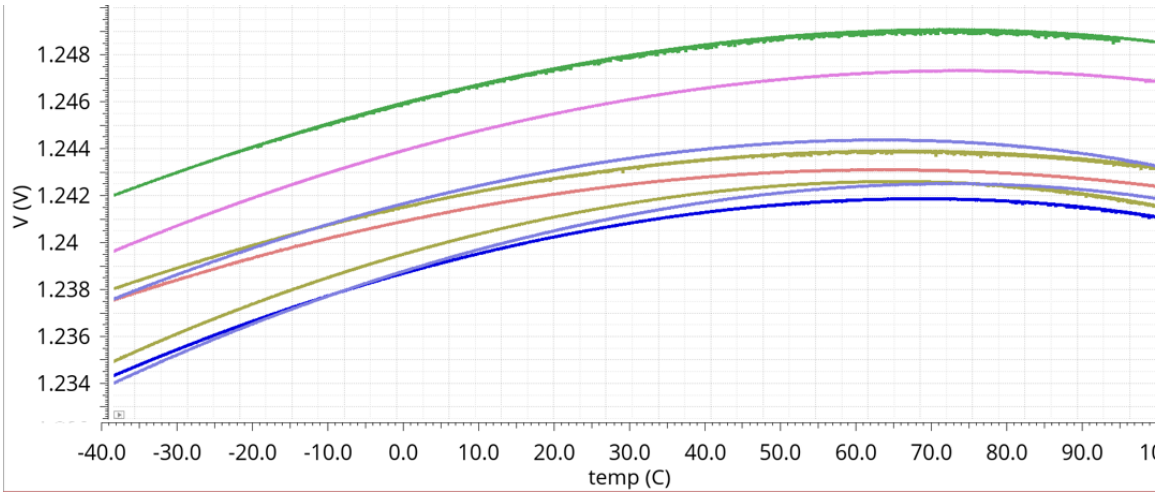

Figure 35. Cadence simulation, Monte Carlo of the BGR, Vref vs Temperature, after being corrected. Maximum shifted due leakage in capacitor.

Using a non-ideal Slope Detector, we can see that the system performance has been affected. In this case the TC goes from 26 to 55 ppm/ºC (using 3σ values). This is due to the leakage in the capacitors of the Slope Detector. Mainly the capacitor that stores the first voltage to calculate the slope sign. The switches storing the voltage, when they are open have a small current (100 fA to 10 pA) flowing through them. This capacitor holds that voltage for 100 mS, enough time for the voltage to drop. After those 100 mS the Op-Amp will compare the voltage reference, with the dropped voltage and it will result in a false detection of the maximum of the slope. This is observed in figure 35 where the maximum has been shifted.

Table I
Literature Review Voltage Reference Comparison

Parameter	[2]	[4]	[5]	This Work	
				Ideal Slope Detector	Real Slope Detector
Year	2015	2013	2010	2018	2018
Process (um)	0.35	0.065	0.16	0.13	0.13
Supply Voltage (V)	3.3	2.5	1.8	3.3	3.3
Current (uA)	53	17.4	55	12	12
Vref (V)	1.220	1.199	1.0875	1.206	1.206
Power Consumption (uW)	64.66	43.5	99	39.6	39.6
Temperature Coefficient (ppm/°C)	3.8	23.6	5 – 12	6.4 – 36.7	26 – 55
Temperature Range (°C)	-40 – 100	-40 – 125	-40 – 125	-40 – 100	-40 – 100
Area (mm^2)	0.437	0.025	0.12	0.08	0.08
Area/Process	1.248	0.385	0.75	0.65	0.65
Trim	digitally	digitally	digitally	digitally	digitally
Samples	N/A	52	60	N/A	N/A

Table I presents the results of this work and is compared with other three publications that use auto correct trimming. In comparison with the other this work has the lowest power consumption; the area was estimated based on literature [4] and [5] that use similar components, so the area will be in that range. This table show the result using an ideal op-amp vs a real op-amp. It shows that with the ideal op-amp the system has better

performance. This is mainly due to the capacitor that is used to sample and hold the first point of the slope. This capacitor suffers from leakage due to the switches. Fixing this problem will give a better performance.

CHAPTER 7
SUMMARY

This chapter discusses the contributions that had been added to the scientific community. The future work that can be implemented to develop a more complete system for the automated temperature trimming circuit for BGRs and a conclusion that summarizes the results and all the work that has been done.

7.1. Contributions

The contributions to the scientific community after being able to complete everything presented in the methodology of this document are:

1. Development of automated temperature trimming circuit capable of reducing mismatch and process variation errors due to fabrication of a Bandgap Voltage Reference.
2. Development of a slope detector circuit.
3. Algorithm to correct BGR errors.

7.2. Future Work

1. Implement fuses so that the memory stores the optimal code.
2. Correct leakage problems in slope detector.
3. Design all digital blocks that were made using VerilogA, at a transistor level.
4. Add multiplexer to the IC output pins so testing is more feasible. This way the multiplexer can be used as a probe to various pins on the circuit.

5. Design the layout of the circuit.
6. Fabricate the IC so that further testing can be done.
7. Compile results, verify errors and redesign.

7.3. Conclusion

This document presents the work achieved to implement a circuit capable of doing automated temperature trimming for a BGR, without requiring use of any external components. This will help reduce cost in manufacturing and will improve the TC of the circuit. This circuit has advantages over other designs because it does not require external equipment for trimming. The overall compensation for the TC is more accurate once the BGR has been corrected with the automated system. The TC goes from 7.2 to 32.5 ppm, which is inside the target range for the first order cancellation of the BGR. The only major concern is the offset of the voltage reference has large variation, because the automated trimming circuit does not account for that. In the future the same system can be used to trim the voltage reference to a desired target voltage at nominal temperature, just by adding an offset trimming circuit.

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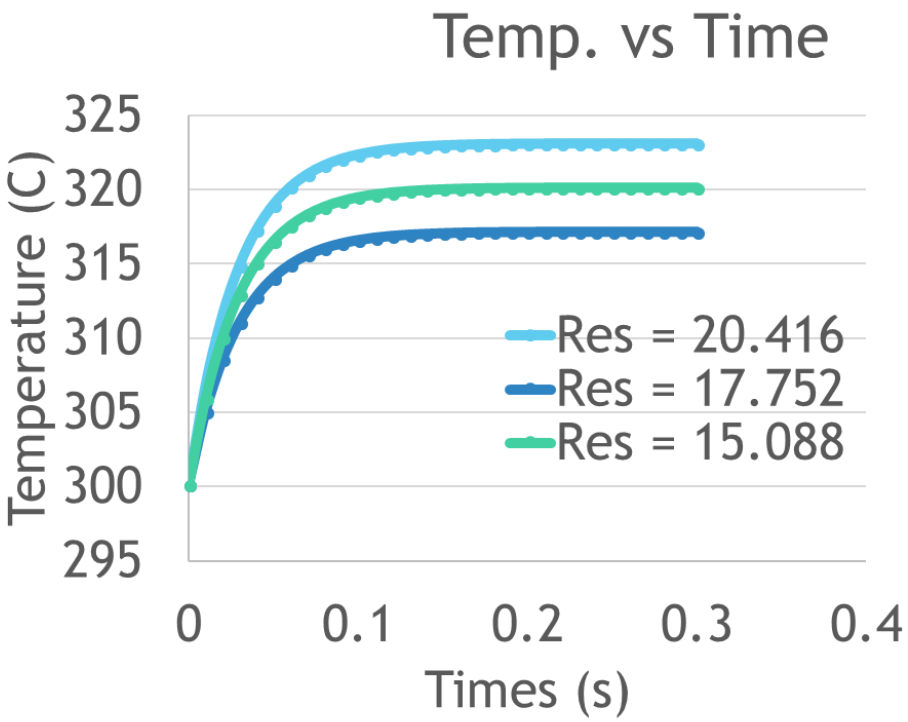
[13] D. Dzahini and H. Ghazlane, "Auto-zero stabilized CMOS amplifiers for very low voltage or current offset," *2003 IEEE Nuclear Science Symposium. Conference Record (IEEE Cat. No.03CH37515)*, 2003, pp. 6-10 Vol.1.

APPENDICES

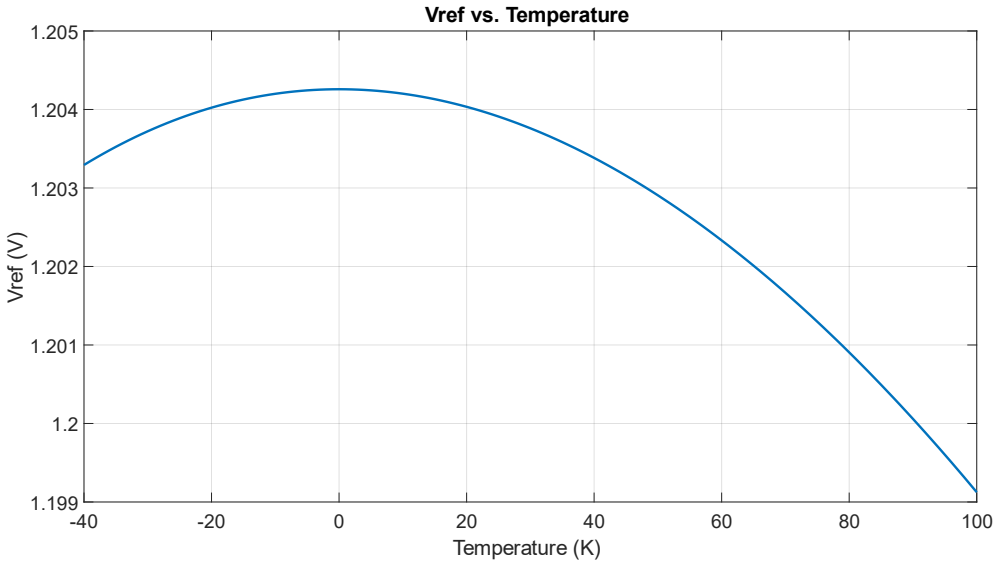
APPENDIX A

SIMULATION DATA OF HEATING ELEMENT

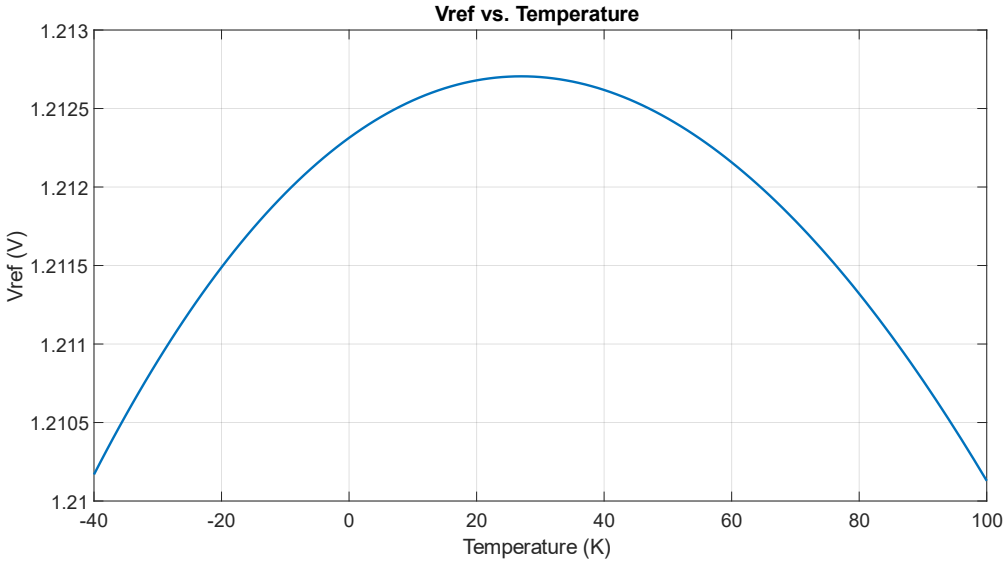
1. **Characterization data of heating element using Comsol**



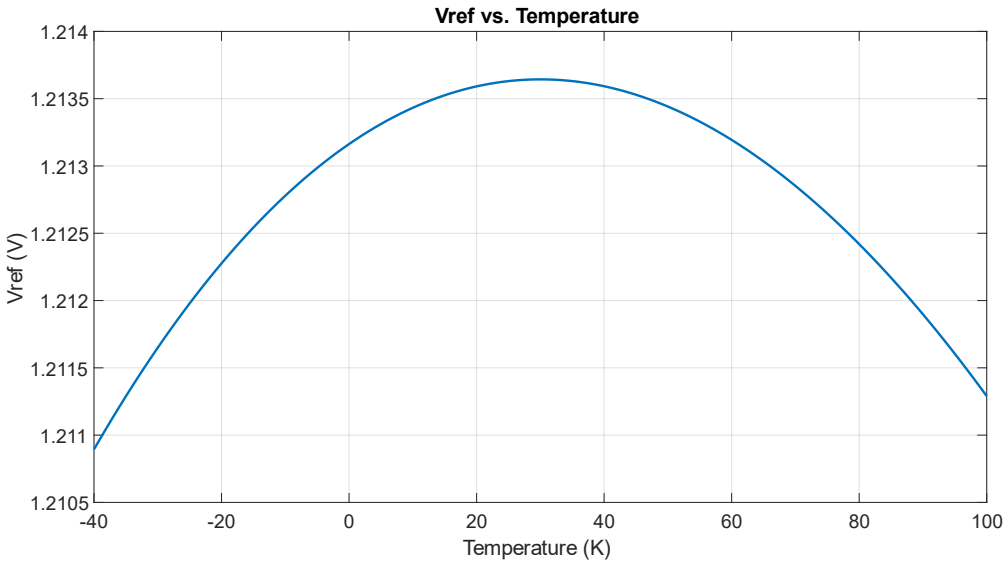
2. **Ideal maximum of the bandgap voltage reference changing the temperature of the device.**



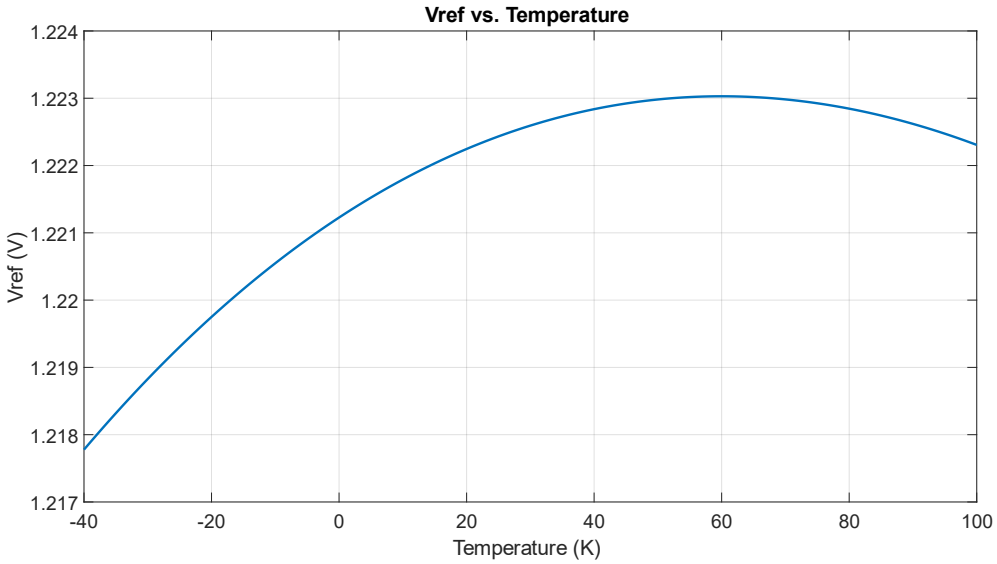
Temperature of device at 0º C, TC = 30.44 ppm/ºC.



Temperature of device at 27º C, TC = 15.17 ppm/ºC.



Temperature of device at 30º C, TC = 16.18 ppm/ºC.



Temperature of device at 60º C, TC = 30.67 ppm/ºC.

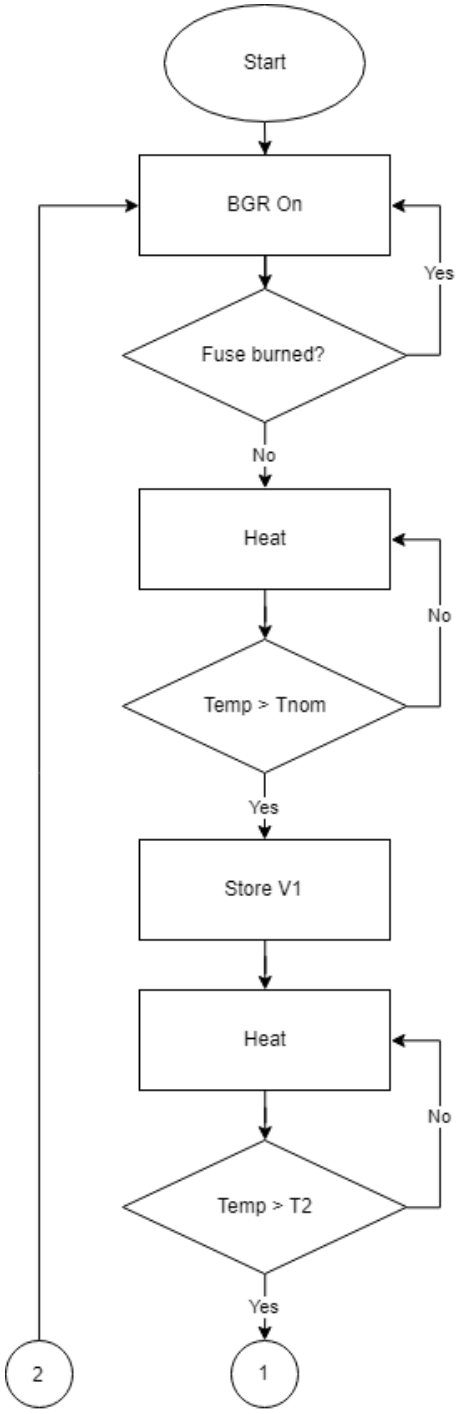
APPENDIX B
MATLAB CODE

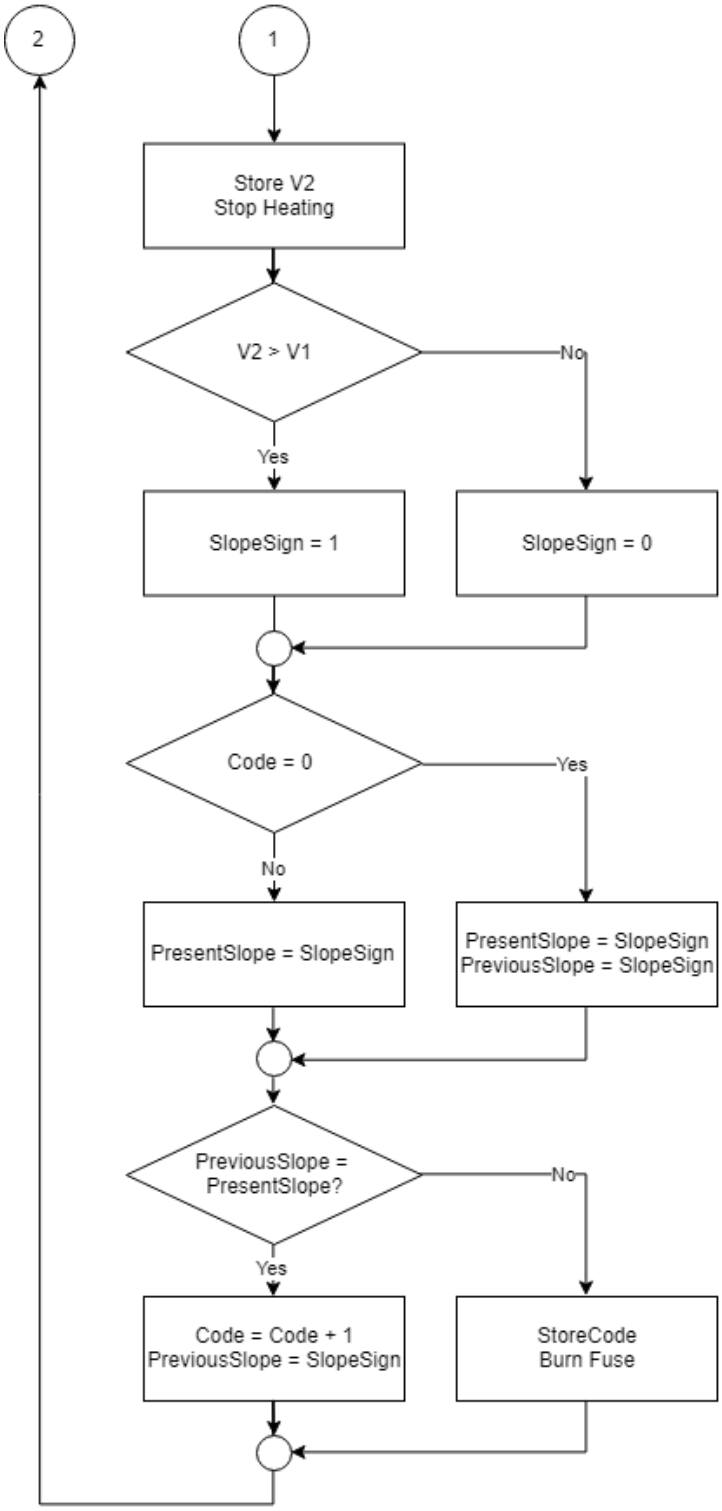
1. Hypothesis validation algorithm

```
clc
close all
clear all

T = -40+273.15:1:100+273.15;
Vgo = 1.1188;
k = 1.38e-23;
q = 1.602e-19;
To = 300.15;
n = 4.6319;
d = 1;
N = 8;
Is = 1.2853e-17;

Rl = 50e3;

Iptat = k*To/q*log(N)/Rl;

Ic = Iptat;

Vbeo = k/q*To*log(N*Ic/Is);

Vbe = Vgo - (Vgo-Vbeo).*(T)/To-(n-d)*k*T/q.*log(T/To);

Vptat = k*T/q.*log(N);

A = ((Vgo-Vbeo)/To + (n-d)*k/q)/(k/q*log(N));

R2 = A*Rl;

DeltaT = 20;

Tl = To + DeltaT;

al = 10.81; %9.2*1.17;

a0 = 7.97; %9.2*0.866776;

bits = 5;

change = floor((2^bits-1)/2);

Rstep = 1/change*(((Vgo-Vbeo)*DeltaT/To+(n-d)*k/q*Tl*log(Tl/To))*q*Rl/...
    (k*log(N)*DeltaT)-(Rl*A-change*(al-a0)*Rl/31));
%Rstep = (al-a0)/(2^bits-1)*Rl;
Ri = R2 - change*Rstep;
```

```
T1 = To + DeltaT;

for i = 0:1:2^bits-1
    R2 = Ri + i*Rstep;
    Vref1 = R2/R1*k*To/q*log(N)+Vgo - (Vgo-Vbeo).*(To)/To-(n-d)*k*To/...
        q.*log(To/To);
    Vref2 = R2/R1*k*T1/q*log(N)+Vgo - (Vgo-Vbeo).*(T1)/To-(n-d)*k*T1/...
        q.*log(T1/To);
    dT(i+1,1) = 100e-6/(R2/R1*k/q*log(N)-(Vgo-Vbeo)/To-(n-d)*k/q);
    Vref(i+1,:) = Vbe + R2/R1*Vptat;
    TC(i+1,1) = (max(Vref(i+1,:))-min(Vref(i+1,:)))/(max(T)-min(T))*1e6/...
        Vref(i+1,ceil((To-min(T))+1));
    deltaVref(i+1,:) = Vref2-Vref1;
end

figure
hold on
for i = 14:1:17
    R2 = Ri + i*Rstep;
    Vref(i+1-13,:) = R2/R1*Vptat + Vbe;
    plot(T,Vref)
end

figure
stairs(0:2^bits-1,deltaVref)

for i = 1:1:20
    DeltaT = i;
    T1 = To + DeltaT;
    code(i) = 1/15*(((Vgo-Vbeo)*DeltaT/To+(n-d)*k/q*T1*log(T1/To))*q*R1/...
        (k*log(N)*DeltaT)-(R1*A-15*(a1-a0)*R1/31));
    Range(i) = code(i)/R1*31;
end
figure
subplot(2,1,1)
plot(0:31,TC)
grid on; xlabel('Code'); ylabel('TC(ppm/C)'); title('TC vs. Code');
subplot(2,1,2)
plot(0:31,deltaVref)
grid on; xlabel('Code'); ylabel('TC(ppm/C)'); title('TC vs. Slope');
```

APPENDIX C
TRIMMING ALGORITHM FLOWCHART




2
1
Store V2
Stop Heating
V2 > V1
No
Yes
SlopeSign = 1
SlopeSign = 0
Code = 0
Yes
No
PresentSlope = SlopeSign
PresentSlope = SlopeSign
PreviousSlope = SlopeSign
PreviousSlope =
PresentSlope?
No
Yes
Code = Code + 1
PreviousSlope = SlopeSign
StoreCode
Burn Fuse

APPENDIX D

VERILOGA BLOCK CODES

2. Code for Memory Block

```
// VerilogA for THESIS_BGR, TrimCode, veriloga

`include "constants.vams"
`include "disciplines.vams"

module TrimCode(NextCode, Vout, StoreCode, X);
output [4:0] Vout;
output X;
input NextCode, StoreCode;
electrical NextCode, StoreCode, X;
electrical [4:0] Vout;

parameter real Vth = 1.65;
parameter real tr = 100e-6;
parameter real tf = 100e-6;
parameter real ttol = 1e-12;
real rem, div, store,t1;
integer i[4:0];
integer j, code,l;
genvar k;

analog begin
    @(initial_step) begin
        t1 = 100;
        for(k=0;k<5;k=k+1)begin
            V(Vout[k]) <+ 0;
        end
    end
    @(cross(V(NextCode) - Vth, 1)) begin
        code = code + 1;
    end
    @(cross(V(StoreCode) - Vth, 1)) begin
        store = 1;
    end
    div = code;
    j = 0;
    repeat(5)begin
        while(div>0)begin
            rem = div%2;
            i[j] = 0.75*rem;
            j = j+1;
            div = floor(div/2);
        end
    end
    for(k=0;k<5;k=k+1)begin
        V(Vout[k]) <+  transition(i[k], 0, tr, tf, ttol);
    end
    t1 = code;
    V(X) <+ t1;
end
endmodule
```

3. Code for Main Logic Circuit

```
// VerilogA for THESIS_BGR, Logic_Circuit, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Logic_Circuit(CaptureV1, CaptureV2, SlopeDetected, SlopeChange, TrimCode, StoreCode, Heating);
input SlopeDetected, SlopeChange, Heating;
output CaptureV1, CaptureV2, TrimCode, StoreCode;
electrical CaptureV1, CaptureV2, SlopeDetected, SlopeChange, TrimCode, StoreCode, Heating;


parameter real width = 10e-6;
parameter real heatTime = 100e-3;
parameter real delay = 50e-6;
parameter real tr = 10e-6;
parameter real tf = 10e-6;
parameter real ttol = 1e-12;
parameter real Vth = 1.65;
real t0, t1, t2, t3;
real v1Expr, v2Expr, heatExpr, trimExpr;
real store, code;
integer i;

analog begin

    if(i==0)begin
        V(CaptureV1) <+ 0;
        V(CaptureV2) <+ 0;
        V(TrimCode)<+ 0;
        V(StoreCode)<+ 0;
        store = 0;
        code = 0;
        t0 = $abstime+delay;
        t1 = 1;
        t2 = 1;
        t3 = 1;
        i = 1;
    end
    @(timer(t0))begin
          v1Expr = 3.3;
    end
    @(timer(t0+width))begin
          v1Expr = 0;
    end
    V(CaptureV1)<+ transition(v1Expr, 0, tr, tf, ttol);

    @(cross(V(CaptureV1) - Vth,-1))begin
        t1 = $abstime;
    end
    @(cross(V(Heating) - Vth,1))begin
        if(store<3.3)    begin
            t2 = $abstime;
        end
    end
    @(timer(t2+heatTime))begin
        v2Expr = 3.3;
```

```
    end
    @(timer(t2+heatTime+width))begin
            v2Expr = 0;
    end
    V(CaptureV2)<+ transition(v2Expr, 0, tr, tf, ttol);

    @(cross(V(SlopeDetected) - Vth,1))begin
        if(V(SlopeChange) < Vth-1)begin
            t3 = $abstime + width;
            code = code + 1;
        end
        elsebegin
            store = 3.3;
        end
    end
    @(timer(t3))begin
          trimExpr = 3.3;
    end
    @(timer(t3+width))begin
          trimExpr = 0;
    end
    @(cross(V(Heating) - Vth,-1))begin
        if(store<=0.0)begin
            t0 = $abstime + delay;
        end
    end

    V(TrimCode)<+ transition(trimExpr, 0, tr, tf, ttol);
    V(StoreCode) <+ store;
end
endmodule
```

4. Code for Heating Element

```
// VerilogA for THESIS_BGR, Heating_Element, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Heating_Element(Heating, Temp);
output Heating, Temp;
electrical Heating, Temp;

real Tempe;
real Result;

analog begin
    @(initial_step) begin
        Tempe = $temperature;
        Result = 0;
    end
    Tempe = $temperature;
    if(Tempe<=300.15)begin
        Result = 0;
    end
    else begin
        Result = 3.3;
    end
    V(Heating) <+ Result;
    V(Temp) <+ Tempe;
end
endmodule
```

5. Code for Slope Detection

```
// VerilogA for THESIS_BGR, SlopeDetection, veriloga

`include "constants.vams"
`include "disciplines.vams"

module SlopeDetection(Vin, CaptureV2, SlopeDetected, SlopeChange);
input Vin, CaptureV2;
output SlopeDetected, SlopeChange;
electrical Vin, CaptureV1, CaptureV2, Reset, Clk, SlopeDetected, SlopeChange;

parameter real width = 10e-6;
parameter real OpAmpDelay = 10e-6;
parameter real tr = 10e-9;
parameter real tf = 10e-9;
parameter real Vth = 1.65;
parameter real ttol = 1e-12;
real positive, positivePrev;
real V1, V2, slope;
real t0,t1;
real slopeExpr;
integer i;
integer j;

analog begin
    if(j==0)begin
        V(SlopeDetected) <+ 0;
        V(SlopeChange) <+ 0;
        slope = 0;
        t0 = 1;
        t1 = 1;
        j=1;
    end
    @(cross(V(CaptureV2) - Vth, 1)) begin
            t0 = $abstime;
    end
    @(timer(t0+OpAmpDelay))begin
            V1 = V(Vin);
            slopeExpr = 3.3;
    end
    @(timer(t0+OpAmpDelay+width))begin
            slopeExpr = 0;
            t1 = $abstime;
    end
    @(timer(t1)) begin
        if (i == 1)begin
            positivePrev = positive;
        end
        if(V1 >= 10e-3)begin
            positive = 1;
        end
        else begin
            positive = 0;
        end
        if(i == 1)begin
            if (positive != positivePrev)begin
                slope = 3.3;
            end
```

```
            end
            i = 1;
        end
        V(SlopeDetected)<+ transition(slopeExpr, 0, tr, tf, ttol);
        V(SlopeChange) <+ slope;
    end
    endmodule
```

6. Code for Slope Detector

```
// VerilogA for THESIS_BGR, MaxDetector, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Max_Detector(Vin, CaptureV1, CaptureV2, SlopeDetected, SlopeChange);
input Vin, CaptureV1, CaptureV2;
output SlopeDetected, SlopeChange;
electrical Vin, CaptureV1, CaptureV2, Reset, Clk, SlopeDetected, SlopeChange;

parameter real width = 10e-6;
parameter real tr = 10e-9;
parameter real tf = 10e-9;
parameter real Vth = 1.65;
parameter real ttol = 1e-12;
real positive, positivePrev;
real V1, V2, slope;
real t0;
real slopeExpr;
integer i;
integer j;

analog begin
    if(j==0)begin
        V(SlopeDetected) <+ 0;
        V(SlopeChange) <+ 0;
        slope = 0;
        t0 = 1;
        j=1;
    end
    @(cross(V(CaptureV1) - Vth, 1)) begin
        V1 = V(Vin);
    end
    @(cross(V(CaptureV2) - Vth, 1)) begin
        V2 = V(Vin);
    end
    @(cross(V(CaptureV2) - Vth, -1)) begin
        t0 = $abstime;
        if (i == 1)begin
            positivePrev = positive;
        end
        if(V1 <= V2)begin
            positive = 1;
        end
        else begin
            positive = 0;
        end
        if(i == 1)begin
            if (positive != positivePrev)begin
                slope = 3.3;
            end
        end
        i = 1;
    end
    @(timer(t0))begin
        slopeExpr = 3.3;
```

```
    end
    @(timer(t0+width))begin
            slopeExpr = 0;
    end
    V(SlopeDetected)<+ transition(slopeExpr, 0, tr, tf, ttol);
    V(SlopeChange) <+ slope;
end
endmodule
```

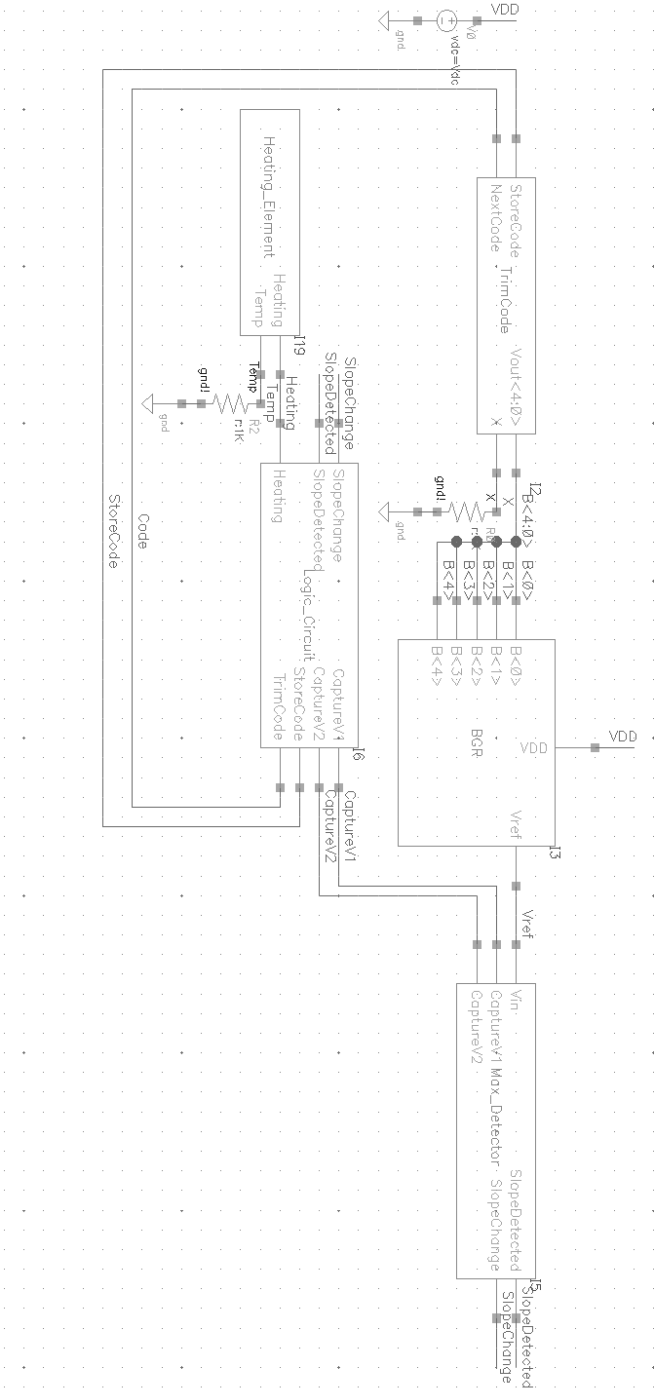
7. Code for ideal BGR

```
// VerilogA for THESIS_BGR, Vref, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Vref(Vout, TrimCode);
output Vout;
input [7:0] TrimCode;
electrical Vout;
electrical [7:0] TrimCode;

parameter real q=1.602e-19;
parameter real K=1.38e-23;
parameter real Vgo = 1.206;
parameter real Vbeo = 0.65;
parameter real To = 300;
parameter real n = 4;
parameter real d = 1;
parameter real N = 8;

real t;
real M;
real T;
real Vptat;
real Vbe;
genvar i;

analog begin
    M = 11.75;
    for (i=0;i<=7;i=i+1)begin
        t = V(TrimCode[i]);
        if(t > 1.65)begin
            M = M + pow(2,i)*0.01;
        end
    end
    T = $temperature;
    Vptat = K/q*T*ln(N);
    Vbe = Vgo - (Vgo-Vbeo)*T/To - (n-d)*K/q*T*ln(T/To);
    V(Vout) <+ M*Vptat+Vbe;
end
endmodule
```

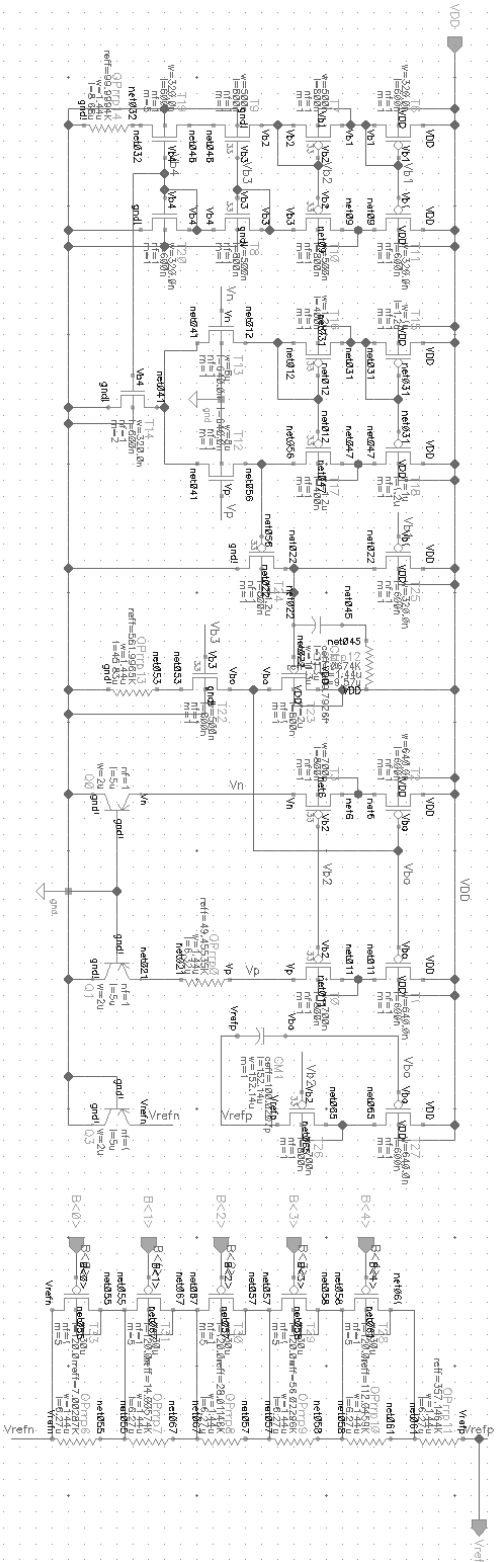
APPENDIX E

CADENCE SCHEMATICS

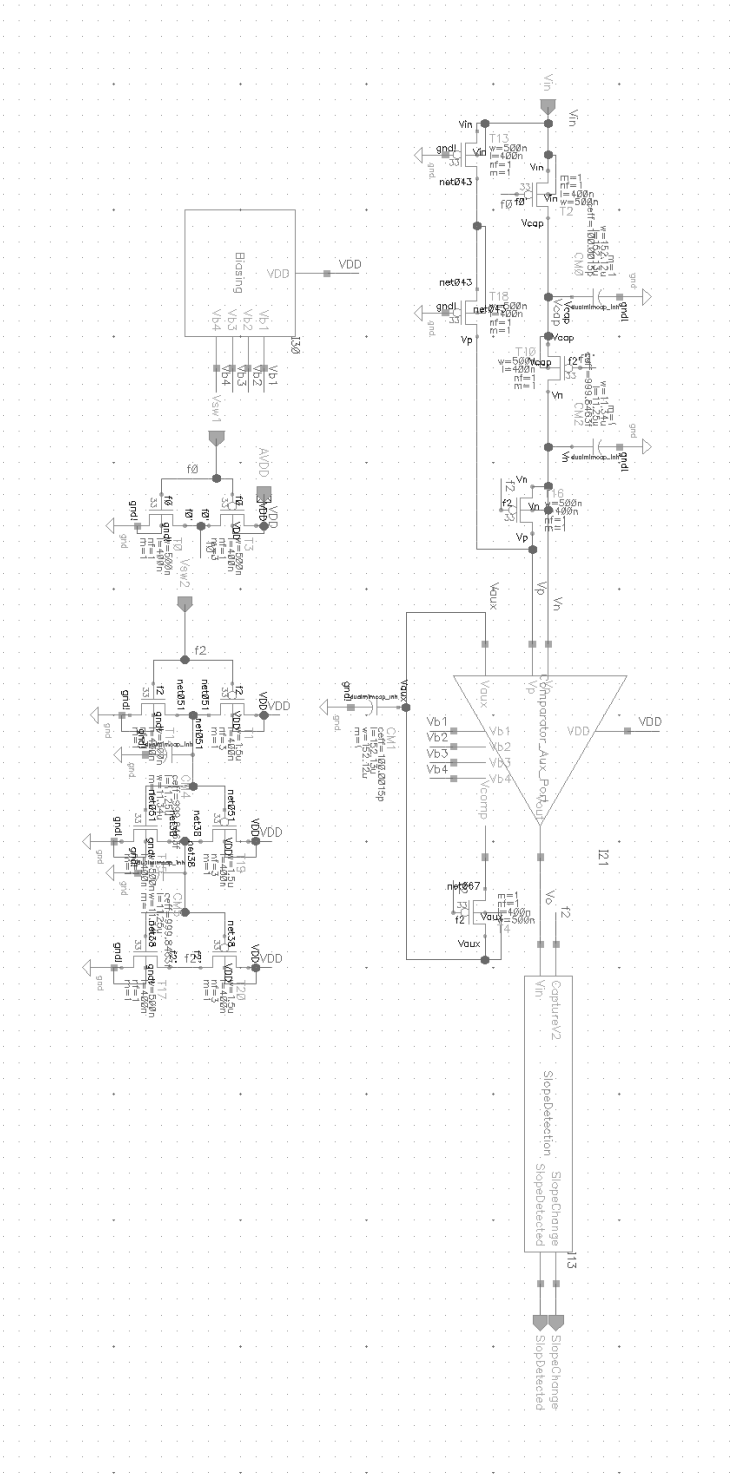
1. Automated Temperature Trimming Circuit



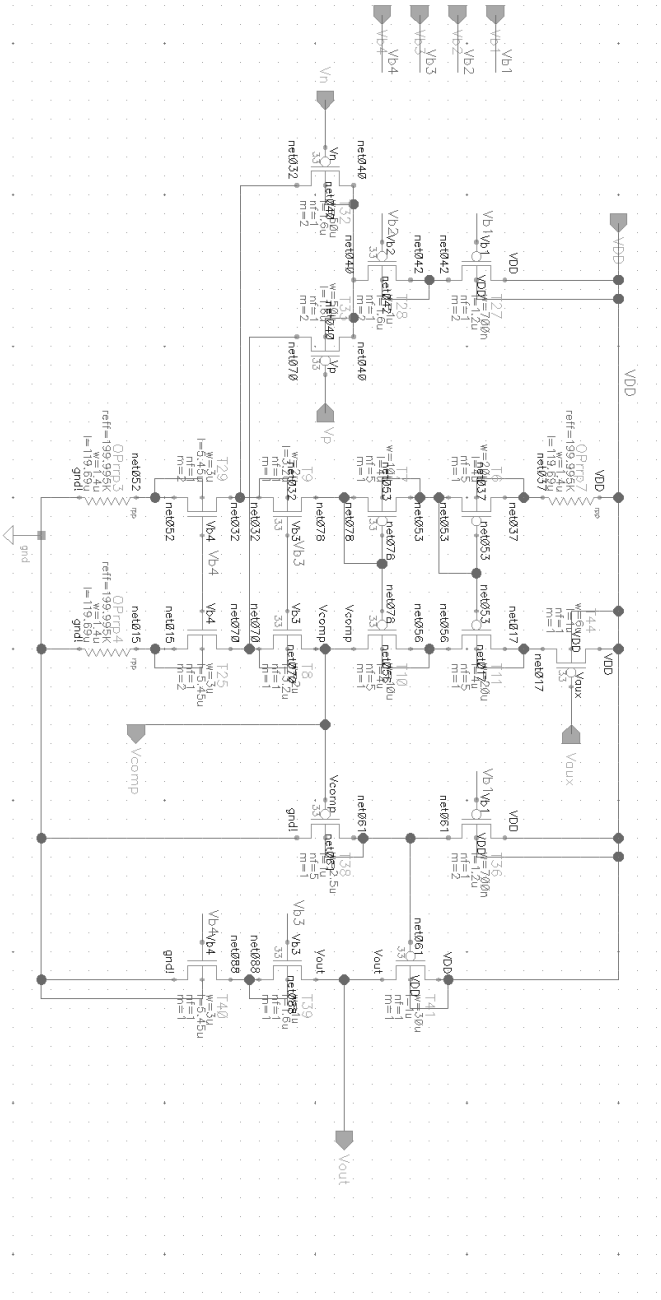
2. Bandgap Voltage Reference



3. Slope Detector circuit



4. Folded Cascode op-amp with second stage with auxiliary input port



5. Biasing Circuit for Folded Cascode