HIGH-PERFORMANCE SELF-REGULATING SELF-BIASING CASCODE CURRENT MIRROR

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2007

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Current Mirrors are one of the most important building blocks in Analog IC Design. They are widely used in all analog and mixed-signal devices. The most important goal in the design of these devices is the accuracy of the current replica. There exists some schemes of current mirrors that have different degrees of accuracy. This work focuses on the improvements of accuracy in one of the architectures of current mirrors by dynamic biasing and regulating the transistor sizes. Results obtained demonstrate that the offset error percent in this work is lower than 0.05%. This system also allows correction of errors introduced by processing. Simulations in Cadence are provided.

Resumen de Informe de Proyecto Presentado a Escuela Graduada
de la Universidad de Puerto Rico como requisito parcial de los
Requerimientos para el grado de Maestría en Ingeniería

ESPEJO DE CORRIENTE DINÁMICOS DE ALTA PRECISIÓN

Por

Laura Elena Sánchez González

2007

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Departamento: Ingeniería Eléctrica y Computadoras

Los espejos de corrientes son unos de los dispositivos más importantes el el diseño de circuitos integrados analógicos. Estos son ampliamente usados en circuitos de señales mixtas. La meta más importante en el diseño de estos dispositivos es obtener la mayor exactitud posible en la replica de corriente. Existen algunas arquitecturas de espejos de corriente con diferentes grados de exactitud. Este trabajo se enfoca en el mejoramiento de la exactitud por medio de polarizacion dinámica y control del tamaño de los transistores en una de las arquitecturas discutidas. Los resultados obtenidos arrojan menos de un 0.05 % de error de "offset". El sistema propuesto también permite corregir errores introducidos en los procesos de fabricación. Simulaciones en Cadence serán provistas.

To my parents Marta and Juan R. and my sister Veronica for all the unconditional love, sacrifice, motivation and support in all my career. To the rest of my family and friends for always believing in me.

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
fig	Figure
eq	Equation
IC	Integrated Circuits
Vgs	Voltage between gate and source of a transistor
Vds	Voltage between drain and source of a transistor
LVCCM	Low-Voltage Cascode Current Mirror
V_T	Threshold Voltage
SBSRDCM	Self-Biasing Self-Regulating Dynamic Current Mirror.

LIST OF SYMBOLS

μA Current (microamps)

CHAPTER 1
INTRODUCTION

1.1 Motivation

Current Mirrors are one of the most important building blocks in Analog and Mixed Signal IC design. They can be used as current sources, biasing circuits and active loads. Their biggest challenge is the current offset in the output node, while maintaining a low-voltage low-power consumption, and high current range.

Biasing conditions are one of the factors that determines the accuracy of the current replica. As the input range increases the accuracy of a current copy in a self-biasing current mirror decreases. Several self-biasing techniques have been published and are explored in this research. This work presents a dynamic biasing scheme that improve the accuracy of a high dynamic bias current mirror. The Self-Bias Self-Regulation Dynamic Current Mirror (SBSRDCM) is presented and its high accuracy will be demonstrated in the following chapters.

This research focuses in the design, simulation and test SBSRDCM that minimizes current offsets in current mirrors, focusing in the self-biasing and self-regulating techniques. This work attempts to follow the trend in Integrated Circuit(IC) which are smaller features size, higher functionality, low power consumption at high speeds, design portability and design programmability.

This scheme has the potential to improve a myriad of the analog circuits. Also attempts to minimize errors introduced during fabrication process.

1.2 Organization

The chapters of this document are organized as follows:

- Chapter 2 explores the principles of current mirrors. Various commonly used architectures of current mirrors are discussed, also some dynamic biasing techniques explores in the literature.
- Chapter 3 introduces the system proposed in this research.
- Chapter 4 presents theory and small signals analysis of some key nodes in the system presented.
- Chapter 5 presents simulations and test of the system introduced in chapter 3
- Chapter 6 present conclusions and the future work that can introduced to improve the proposed work.

CHAPTER 2
LITERATURE REVIEW

Current mirrors are employed in many applications such as operational amplifiers, Analog to Digital and Digital to Analog Converters. Current mirrors mimic the performance of an ideal current source. Therefore their design must fulfill the following requirements: (i) low input impedance, (ii) small voltage swing in the input node, (iii) large output impedance, (iv) accurate input current copy [1].

On an IC chip with a number of amplifier stages, a constant DC current is generated at one location and replicated at various points [2]. In this application, the biasing of the current mirror doesn't need a dynamic biasing scheme. Having a DC voltage to bias the circuit provides the desired range and accuracy. In the case of current sensors the input of a current mirror is an AC value. For this a DC biasing will affect the accuracy of the current copy. As the input current increases the voltage needs of the current mirror changed, that is why is necessary a self-biasing scheme, where the biasing of the transistors depends of the input conditions.

One of advantages of using self-bias [1] or dynamic-bias current mirrors is that their polarization varies with changes in Vdd.

An ideal current mirror should have an infinite input swing and its biasing should be dynamic. The current replica should have zero offset. Current mirrors

[1] A system that has the capability to supply itself with the biasing voltage necessary using the input conditions

are designed to try to achieved the ideal characteristics. A current mirror of a high input range is very useful in data converters, as the works done in [3], [4], [5], [6].

A challenge in the design of a high input range current mirror with low-voltage characteristics is the dynamic biasing. So as it is mention there is a trade off between input range and the biasing conditions. This affects their accuracy. In this chapter some of the most important architectures of current mirrors are explored to understand the need of a self-bias dynamic scheme.

The basic NMOS current mirror is shown in figure 2–1, the diode connection in transistor M1 guarantees operation in saturation mode. The voltage between gate and source (V_{GS}) in both transistors should be the same, thus Iout is a replica of Iin.

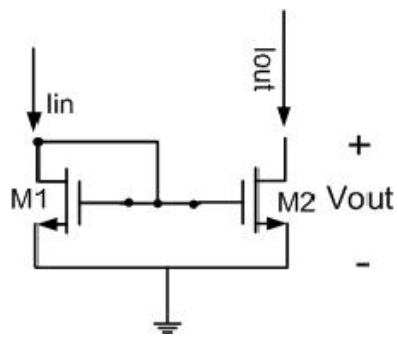


Figure 2–1: Simple Current Mirror

There are some disadvantages to this configuration. First, it is very vulnerable to mismatch between transistor M1 and M2, caused by process errors. If transistor mismatch could be regulated this would aid in the reduction of current offset. Some layout techniques used to minimized mismatch in size are common centroid and interdigitation. The output current value of the transistor M2 is shown in eq. 2.1.

$$Iout = (\frac{W/L_2}{W/L_1}) \times Iin \tag{2.1}$$

A second disadvantage of this structure is that no diode connection exists for the transistor M2. This does not guarantee the following relation relation:

$$Vout \geq V_{GSM2} - V_t$$

Another disadvantage of the Simple Current Mirror is that V_{DS} on the output is not equal to V_{DS} input. This introduces a current offset[2] . Equations 2.2 and 2.3 show the saturation equation for both transistors in the mirror. They show that the current offset is due to the difference between V_{DS1} and V_{DS2}.

$$I_{DSM1} = (\frac{\beta}{2})(V_{GS1} - V_{th})^2(1 + \lambda V_{DS1}) \tag{2.2}$$

$$I_{DSM2} = (\frac{\beta}{2})(V_{GS1} - V_{th})^2(1 + \lambda V_{DS2}) \tag{2.3}$$

The small-signal output impedance of this current mirror(CM) is is relatively low, (see eq 2.4), typically hundreds of $K\Omega$. This factor contributes greatly to the current offset in the output node of this current mirror.

$$r_0 = r_{0M2} = \frac{1}{\lambda \times I_{D2}} \tag{2.4}$$

The simple current mirror is a self-bias architecture. The diode connection in the input transistor allows changes in the biasing node to be proportional to changes in the input current. One of the advantage of this architecture is that it is low input requirement ($Vdd_{min} = V_{GS}$). However, the disadvantages mention before do not make it suitable for many applications.

Improvements to the simple CM in terms of its output impedance, is achieved by cascoding [3] the transistors, see figure 2–2. This architecture is know as a Cascode

[2] Difference of current or voltage between two signals

[3] Put a transistor over other one connecting the drain of one with the source to the other one

Current mirror (CCM). The output impedance of this architecture is shown in eq. 2.5.

$$r_0 = g_m \times r_0^2 \tag{2.5}$$

The disadvantage of this new architecture is that the minimum Vdd is $2 \times V_{GS}$. This architecture's self-biasing conditions increases the voltage supply needs, so this architecture also is not suitable for low-voltage applications.

For low voltage solutions, the Low-Voltage Cascode Current Mirror(LVCCM) shown in figure 2–3 is introduced. The LVCCM has the same output impedance than the CCM shown in figure 2–2, but it can be used for low-voltage application because its minimum voltage supply needs is V_{GS}. This current mirror needs a external polarization. Thus it sacrifices the self-biasing conditions for a lesser voltage supply. Having a fixed DC voltage in the polarization node, affects the accuracy of the current mirror as the input range increases.

Design a dynamic biasing scheme for the LVCCM has generated a abundant research. For example, a straightforward way to obtain the biasing voltage is to generate a replica of the input current and use this to bias [4] the cascode [7] as shown in fig. 2–4.

As mentioned before, one of the most important goals in the design of current mirrors is the accuracy of the output current replica and the value of the output impedance. Another concern is that in most current mirrors the transistors are in saturation region to maintain a constant r_0. In the triode region of operation, the transistor behavior is like a variable resistor, which means that for small variations in the drain-source voltage there can be big variations in the drain current. This is why

[4] Supply a transistor the necessary voltage for stay on or in the operation region that is needed

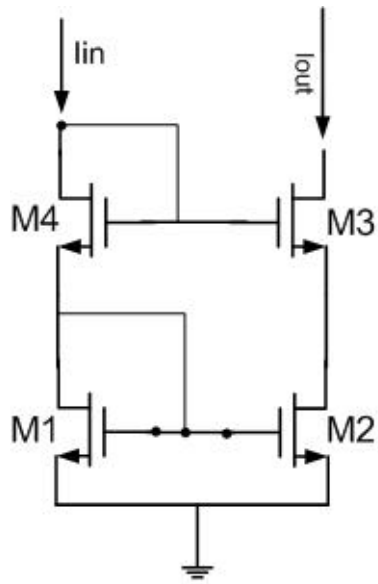


Figure 2–2: Cascode Current Mirror [8]

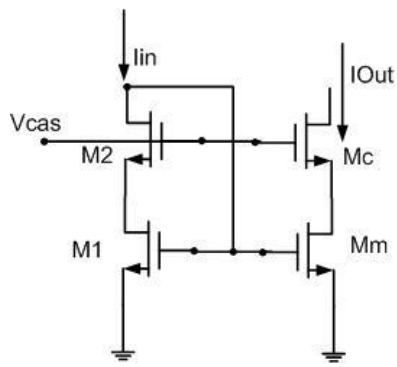


Figure 2–3: Low Voltage Cascode Current Mirror [8]

in most dynamic current mirrors the transistors operate in the saturation region. However there exist some current mirror architectures where some of the transistors are in triode region. The self-biasing Prodanov[9] current mirror shown in figure 2–5 is an example. This structure improves the output impedance of the output node, thus improving the accuracy of the current replica. This architecture operates with transistors either in saturation or triode, allowing the circuit to operate at higher frequencies.

The disadvantages of the Prodanov CM are that the transistors M1 and M2 are in triode region, therefor it suffers from:

- Vulnerability to geometric mismatches

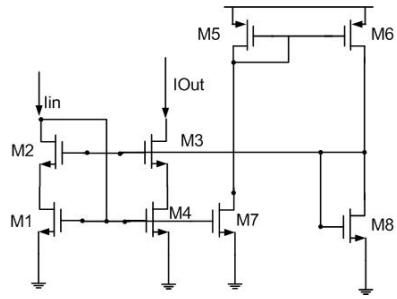


Figure 2–4: Self Biasing Cascode Current Mirror

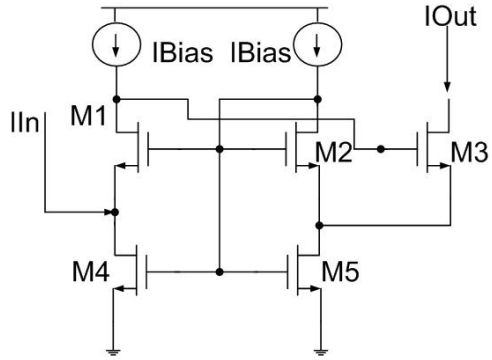


Figure 2–5: Prodanov Self Biasing Cascode Current Mirror

- Vulnerability to V_{th}
- Small variations in drain-source voltage can produce large variations in the drain current.

The Prodanov current mirror has two advantages over the fully cascoded current mirror, lower voltage supply needs V_{GS} and it greatly increases its output impedance of:

$$r_0 = (g_{mM1} \times r_{0M4}) \times (g_{mM3} \times r_{0M3} \times r_{0M1}) \tag{2.6}$$

To overcome the large variations in drain current caused by small variation in voltages an external biasing can be used to polarized the gates of the transistors M1 and M2 see fig 2–6. This architecture as the Geiger Cascode CM. This scheme needs external biasing, but all the transistors operate in the saturation region. This improves the unwanted variations in the drain current, while maintains then high input impedance achieved with the Prodanov architecture. Due to the fact that the

transistor M1 and M2 are operating in saturation region the output impedance if greater. This circuit has an input impedance show in eq. 2.7.

$$r_0 = (g_{mM1} \times r_{0M4}) \times (g_{mM3} \times r_{0M3} \times r_{0M1})[10] \tag{2.7}$$

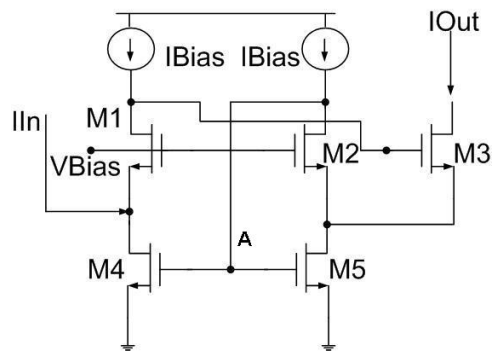


Figure 2–6: Geiger Cascode Current Mirror

Using the biasing techniques demonstrated in [7], it is possible to bias the current mirror in figure 2–6. Designing a dynamic biasing scheme for this mirror has an extra level of complexity when compared to the cascode current mirror of the figure 2–4. The biasing and the input current have to be copied. This is presented in [10]. The result is a circuit that consumes more silicon area but it's dynamically biased and increases the accuracy in the output current copy.

The Self-Biasing Current Mirror shown in figure 2–7 reported in [10] a maximum error percent of 0.1% and minimum error percent of 0.05%. This current mirror was simulated using parameter from the $0.35\mu m$ technology. Biasing the gates of transistors M1 and M2 was achieved by making copies of the input and output stages following the same principle of the current mirror shown in fig 2–4.

The Self-Biasing Current mirror shown in the above figure (known as the Geiger-Cong CM) has the advantage of being a dynamic self-biasing CM. This architecture is reported as the scheme with the highest accuracy of the once presented in this chapter. The accuracy is best if the current input values are close to the current for which the transistor was designed. To increase the accuracy throughout the

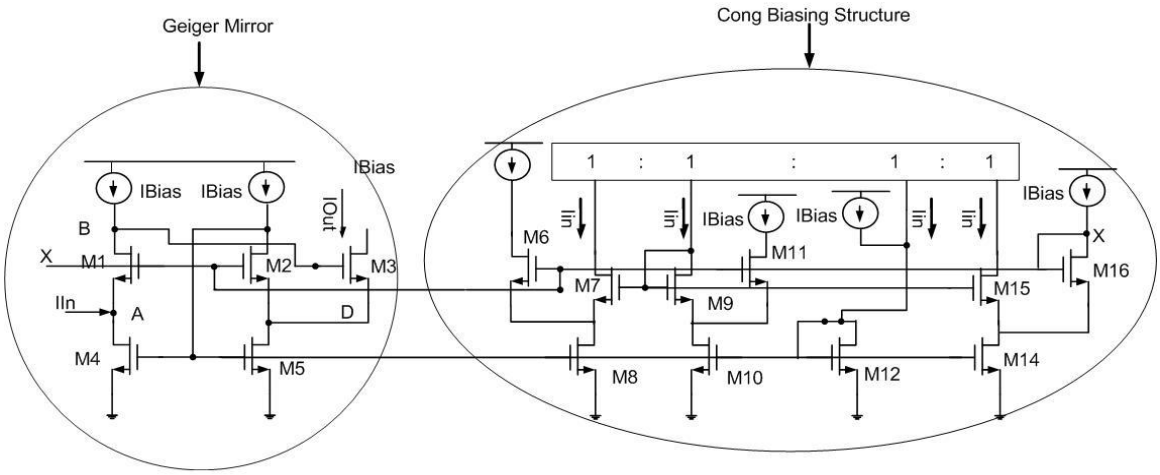


Figure 2–7: Geiger Self Biasing Cascode Current Mirror

whole input range, the polarization scheme should regulate itself according to the input current. This research presents a controller for the circuit presented in figure 2–7. It compensates the offset error according to the input current by continuously comparing input and output current, compensated the current offset when is needed.

The accuracy of proposed system depends of the precision of the current comparator. Several current comparators were studied and compared to be used in the proposed system. Next section discusses several current comparator found in the literature.

2.1 Current Comparators

Current comparators are important building blocks in mixed signal circuits specially in ADCs. Their performance imposes a direct limitation to the achievable resolution and speed [11]. The simplest current comparator is shown in fig. 2–8. It is composed of two transistors M1 and M2, connected as a CMOS inverter. The input current is integrated by parasitics capacitances C_{gs1} and C_{gs2} and there is no DC offset. The problem with this architecture is that the input voltage can have almost rail-to-rail swing and therefore the time it takes for a weak Iin to trip the comparator limits the speed. [11]

The current comparator compares if the input current is positive or negative. If it is negative the current flows out of the circuit through C_{gs2} and the output node goes to ground. The contrary behavior happen if the input current is positive.

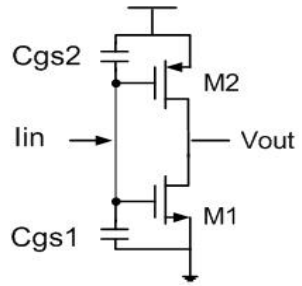


Figure 2–8: Simple Current Comparator [11]

An also widely used architecture is the circuit shown in Figure 2–9. In this schematic the comparison works in the following way, if $Iin < Iref$ then the Out node will toggle high, in this case Vdd, if the contrary happens the Out node will toggle low.

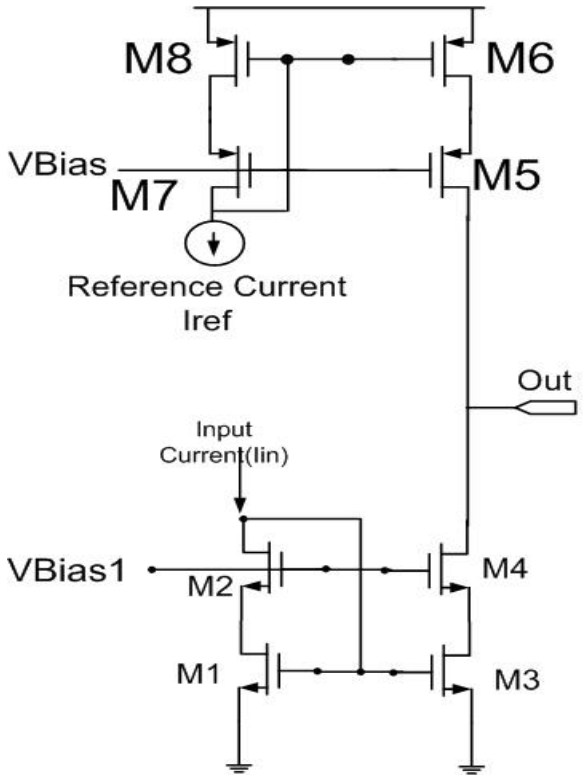


Figure 2–9: Current Comparator

The current comparator shown in fig. 2–9 is one of the most commonly used, due to its low propagation delay time (10ns), which is quite fast for the majority of the applications [12]. It uses high output impedance current mirrors connected as a class AB stage, to amplify small differences in input current to large variations in output voltage [12].

Another important current comparator is the Traff comparator presented in [12] (see figure 2–10). This architecture has an input impedance of $r_{PMOS}||r_{NMOS}$. The input state of a Traff comparator has a source follower input stage, which introduces feedback into the gates. A positive feedback from an inverter is used to achieve enough gain to amplify small voltage variations at the input stage node [12].

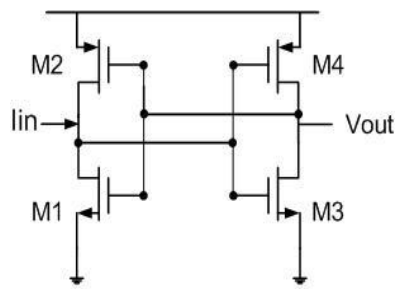


Figure 2–10: Traff Current Comparator

Another architecture used is the current comparator shown in figure 2–11 is another architectures used. This architecture is known as the Wang Current Comparator. The difference between the two input currents is converted to the voltage V_y. This voltage is applied to a regenerative latch that determines the digital output. The regenerative latch is used as an offset compensation circuit, which increases the sensitivity [5] of the current comparator.

In figure 2–11 the uncompensated comparator is composed of transistors M1, M3, M4, and M5. The diode connection in transistors M4 and M5 causes the node to have a very small input impedance and a very small input voltage variations. The

[5] Smaller current step that a current comparator can detect to change of state

offset compensation circuits comprised of a current copier with a negative feedback amplifier and a bias current source I_b. The bias current I_b is equal to the difference between I_{d3} and I_{d1}. The current copier includes transistor M2, the operational amplifier, the holding capacitor and the switch S1. [13]. This offset compensation scheme helps to achieve a sensitivity of 80nA reported in [13].

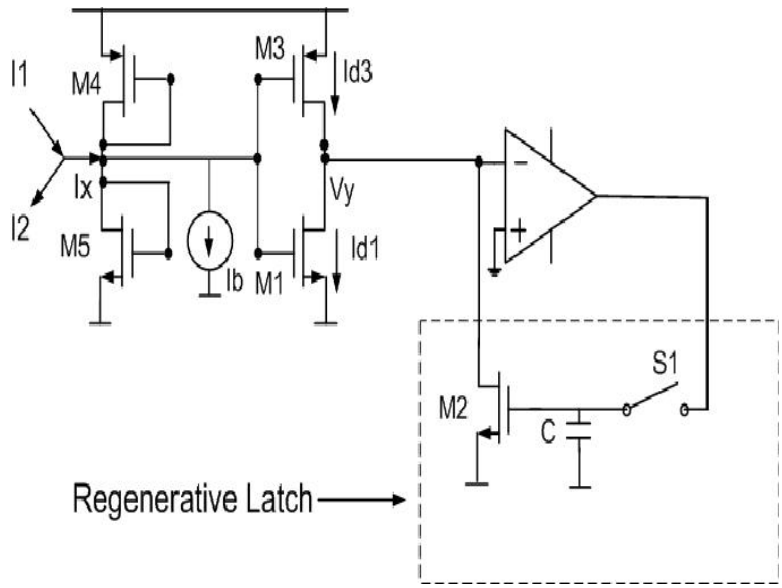


Figure 2–11: Wang Current Comparator [13]

This section presented some of the most relevant current comparator architectures, the most important once are presented in 2–9 and 2–10. Those current comparators achieved the highest sensitivity and also less silicon area consumption, because the comparison does not rely on the use of capacitors. A disadvantage of the Traff architecture is that it only determines if the current is been sourced or sinked. For comparison between two currents, a substraction must be made at an earlier stage. This mirror is useful for determining the direction of the current.

In the system proposed in this work (SBSRDCM), a comparator architecture that consumes a small silicon area is needed. This scheme must be based in a current subtractor structure. Architecture shown in figure 2–9 is used with some modifications and improvements.

The Self-Biasing Self-Regulating Dynamic Current Mirror takes the current mirror architecture proposed in 2–7 and with the design controller minimizes the offset obtained between the input and output current. Next chapter explains the operation of the circuit and provides simulations for each module.

CHAPTER 3
HIGH-PERFORMANCE SELF-REGULATING SELF-BIASING CASCODE CURRENT MIRROR

Chapter 2 discussed some of the current mirrors architectures and the advantages of a current mirror that is self-biasing and self-regulating to improve accuracy. The most accurate architecture that was presented in the Literature Review chapter was the Geiger-Cong architecture shown in figure 3–1. This self biasing current mirror is composed of the Geiger mirror connected to the Cong-biasing architecture. It reports a very small current offset error percent.

This work focuses on the Geiger-Cong architecture because of the difficulty of increase its high accuracy. The increase in accuracy is possible through the control of the *node X* of the circuit [14](see figure 3–1).

It is still possible to achieve more accuracy controlling the *node X* of the circuit. That is why our work is based, in the hypothesis that if the voltage in *node X* is slightly varied for different currents (see fig. 3–1). The accuracy of the current replica reported in [10] is improved. The objective of this work is designing a controller capable of supplying the voltage needed on that node depending of the offset with a change in input current value.

As mention before, the architecture shown in figure 3–1 was chosen because is the most accurate found in the literature. If the system is capable to compensate the offset of this architecture, it potentially could compensate the current offset in less accurate current mirrors.

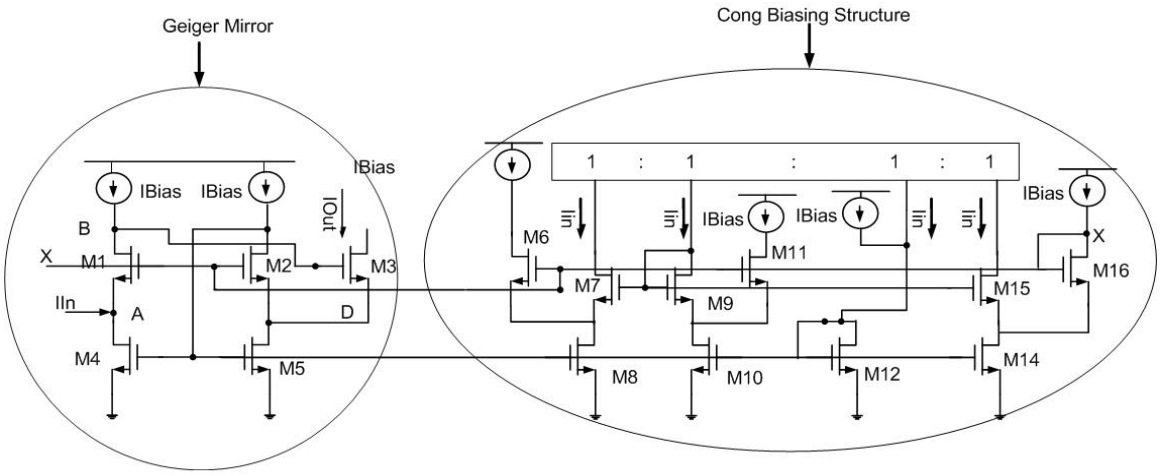


Figure 3–1: Geiger Self Biasing Cascode Current Mirror

This work is based in the biasing of *node X* for two reasons. First, node X is the only node in the Geiger Mirror that is not dynamically biased. Secondly, the biasing of the output transistor is in directly control by node X.

To analyze how the node X influences the output current, the effects of changes in Iin on different nodes must be studied. The current in the transistor M1 must be equal to I_{Bias} regardless of the input current. Changes in Iin will cause voltage changes in node A. This changes must be compensated by changes at node X and/or node B. To increase the output current node B must increase. When the input current increases, voltage in node A increases. If the V_{GSM1} is further decrease, this will cause a significant voltage increase in node B. The opposite will happen decreasing Iin.

One of the challenges of this approach is that the changes in voltage needed at node X for changes in input current are considerably small. Thus the control circuit has to be accurate enough to provide the small changes needed. To properly bias the node X, a comparison between the input and output current must be establish. This comparison must determine if the current offset is positive or negative. Also the magnitude of this offset must be establish.

The behavior of the system is as follows, first the system compares the input and output current of the Self-Biasing Current Mirror. If the magnitude of the difference falls within region of tolerance, the system remains in the same state. If the current offset sensed, is outside the region of tolerance the controller of the SBSRDCM must supply a different voltage to *node X*.

When the input current is lower than the output current, the controller supplies a higher voltage to *node X*. However if the input current is higher than the output current then the voltage at *node X*. This compensates the current offset in the current mirror.

A SBSRDCM block diagram is shown in figure 3–2. It shows how all the modules of the circuit are connected. In the center of the circuit is the Self-Biasing Current Mirror, module 1 (Cong-Geiger architecture). It receives an input current (Iin), voltage for *node X* and it has 4 outputs:

- I_{Out}
- I_{Out} Replica
- Two Iin Replica

Those signals are connected to the Current Comparator(module 2), and the Path Selector Circuit(module 4).

The Current Comparator module (module 2) compares input and output current replicas. The Flag Comparison signal determines if the input current is lower than the output current by toggling low, and toggling high if the opposite is true. If the two currents are equal (or closely matched) The Flag Comparison signal will remain in the transition region.

The Flag Comparison signal is fed to two modules, the Window Detector(module 3) and the Logic Controller (module 4). The Window Detector detects if the Flag Comparison signal of the module 2 is within the tolerance. If the latter is true Vout toggles high. As mention before the Flag Comparison signal is sensed also by the

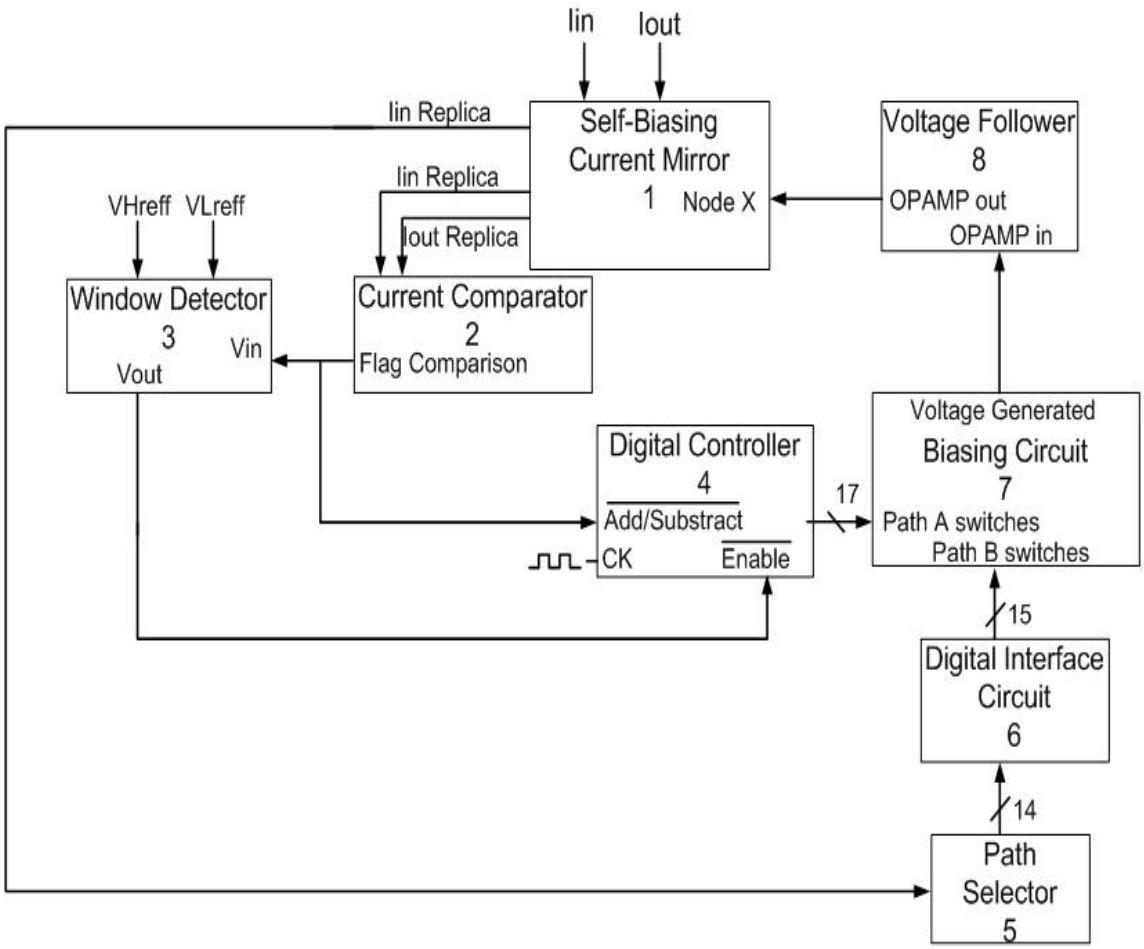


Figure 3–2: System Block Diagram

Digital Controller. It selects the appropriate contains the logic needed to regulate possible offset cause by mismatch. This logic is controlled by the Flag Comparison signal and the output of the Window Detector. If the output of the Window detector is high, the Digital Controller remains in its current state. If not, it will change its state according to the Flag Comparison Signal. The seventeen outputs of the Digital Controller are sensed by the Biasing Circuit (module 7).

The Path Selector (module 5) senses a Iin current replica and determines if it is less than or biggest than various reference currents. Module 5 has fourteen digital outputs. These outputs are fed to Module 6, the Digital Interface circuit, which decodes the signals into fifteen digital output signals that selects the proper switch in the path B of the Biasing Circuit.

Module 7 generates the appropriate voltage needed at *node X* of the Self-Biasing Current Mirror Module, using the information from Module 4 and 6. The voltage generated is controlled by 2 sets of switches, Path A and Path B. Also the output of this circuit, is connected to the Voltage Follower Module (module 8), this prevents current loading in *node X* of Module 1, and finally the output of Module 8 is connected to *node X* of the Self-Biasing Current Mirror

This system contributes to the current offset compensation and minimize the mismatch effects introduced by the mask and lithographic process. Minimizing mismatch effects helps to reduce random errors in a fabrication process.

The next section of this chapter explains the different modules of the system proposed.

3.1 Self-Biasing Current Mirror

The architecture used for the regulated self-bias CM was the Geiger-Cong structure shown in figure 3–1. The accuracy of this circuit is improved by changing the voltage at *node X*. The design of the Geiger-Cong circuit was adjusted for the technology AMI06.

The Geiger-Cong Mirror receive an input current, which is replicated in transistor M3, transistors M1 and M2 maintain transistors in the current mirror always on. Then currents in transistors M4 and M5 should be $I_{Bias} + I_{In}$. Gates of transistor M4 and M5 are biased dynamically by M2 drain. Node X is biased by the Cong biasing architecture. That circuit takes the input and output stages and replicate it, biasing node X.

For this work, the design was replicated for the available technology that is AMI06, and also the operational current of the transistor used was $50\mu A$, having transistors 3 times smaller than in [10]. Table B–1 in Appendix B shows the dimensions of the transistors of the current mirror in [10].

One of the disadvantages of the afore mentioned current mirror is that it is very vulnerable to changes in technology. Transistors M10 and M14 don't have the same geometry that the others N-type transistors in the rest of the circuit [10]. This circuit reports in [10] has a minimum offset error percent of 0.05%. Due to the changes in technology, that error percent never was obtained in $0.5\mu m$ technology.

Transient simulations were done to compare the Geiger-Cong circuit with the proposed circuit, because it has an AC voltage source (Clock signal in Digital Controller Module). So it is impossible to do a DC sweep analysis.

The behavior of this circuit is shown in figure 3–3. The figure shows the transient of the input and output currents, plus the offset found. It is possible to observe that the current offset error percent is between $+0.7\%$ to -10%. But in input currents lower than 100uA the error percent is between $+0.7\%$ to -2.5%, but this error increases in currents higher than 100uA to -10%. The goal of this work is to increase the accuracy reported in [10]. This circuit has the potential to improve the performance of devices such as operational amplifiers and data conversion circuits like ADC and DAC.

The controller proposed for this circuit improved the error percent obtained under the technology available and also improve the error percent reported in [10].

Current Replicas of input and output current are connected to the Comparator circuit, to be compared. Also, other replica of the input current is supply to the Path Selector circuit, to determine the range the input current.

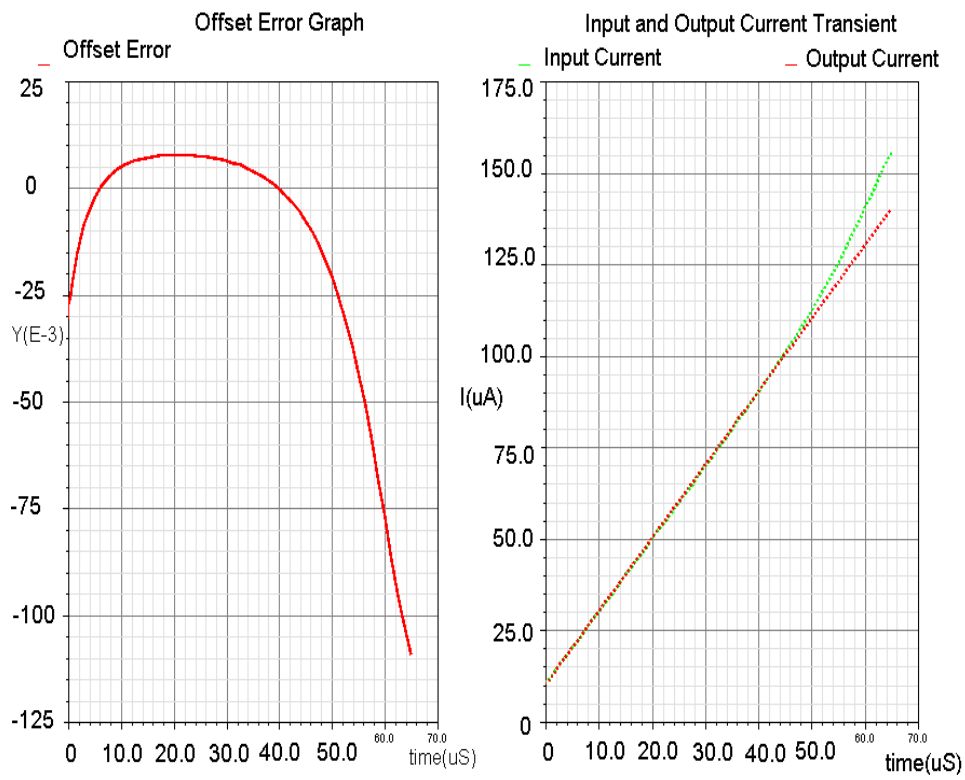


Figure 3–3: Transient Response of Self-Biasing Cascode Current Mirror in [10]

3.2 Comparator

The current comparator is one of the basic blocks of the system proposed. It compares the input current with the output current and it toggles high if the input current is higher than the output current. It toggles low if the opposite is true. This determines which switches are activated in the Path A of the biasing circuit.

From the discussed current comparators the circuit shown in figure 3–4 was selected. The circuit was redesigned to increase the sensitivity of the comparator. A voltage comparator was added, see 3–5.

For the analysis of this circuit is important to explain how nodes X1 and X2 are biased. Node X1 is polarized according to the Iin value, if the current Iin is increases. Node X1 has to decreases. If the contrary behavior occurs node X1 will increase. Node X2 will fluctuate near $\frac{V_{DD}-V_{SS}}{2}$ for similar current currents. However for significant difference between Iin and Iout the node will toggle high or low. To

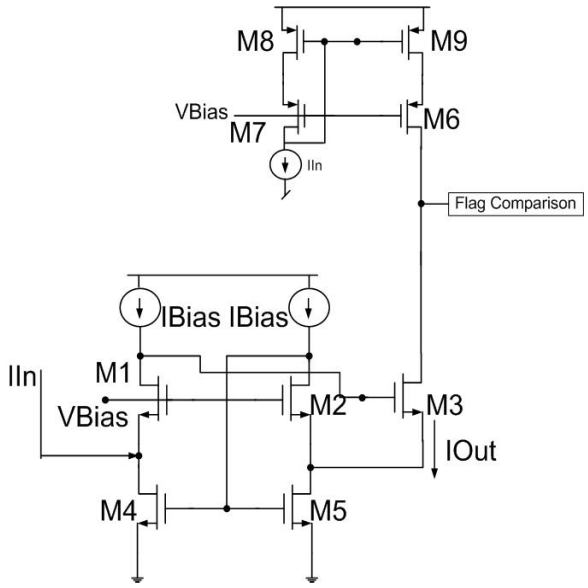


Figure 3–4: Current Comparator

create a signal that toggles high or low, for unacceptable differences in current the sensitivity must be increased.

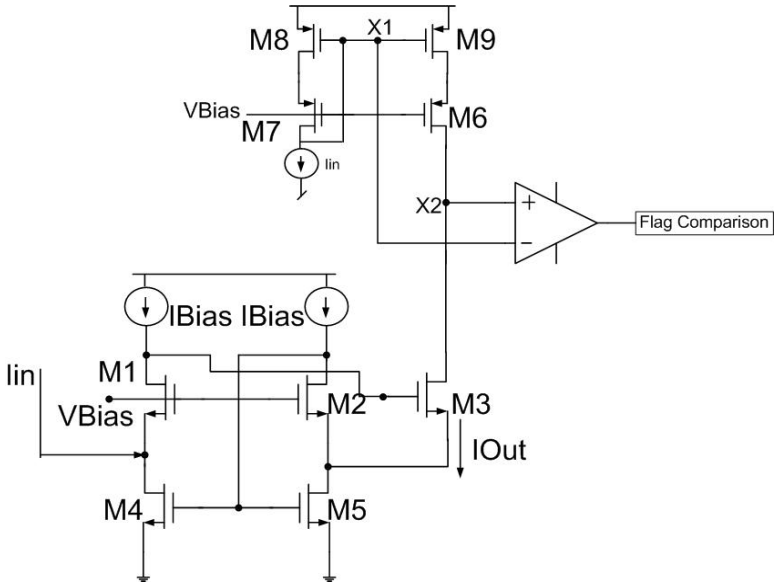
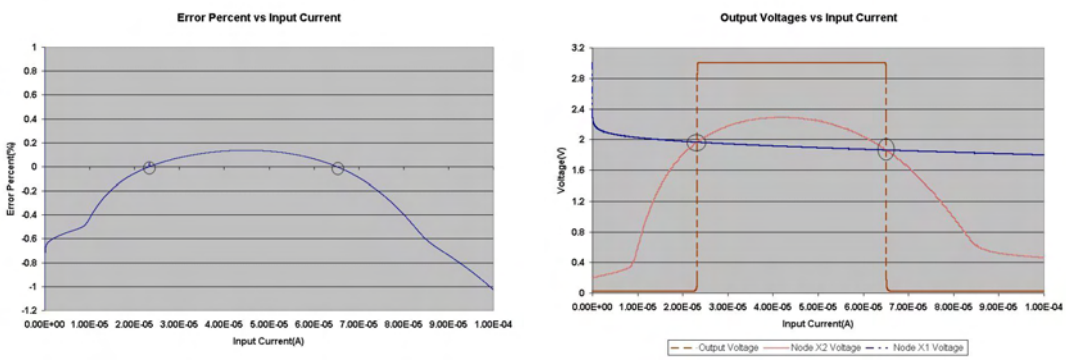


Figure 3–5: Current Comparator

The solution for sensitivity enhancement was connecting the Operational Amplifier between nodes X1 and X2. This architecture was implemented because when both currents are equals (offset error percent 0%) the voltage between those nodes equals zero. Otherwise if $Iin > Iout$, the voltage in node X1 is smaller than the

voltage in node X2. If the opposite behavior occurs, the voltage in node X1 is bigger than the one in node X2. This triggers the Flag Comparison signal. This is why the voltage comparator is connected between these two nodes. This connection guarantees a virtual diode connection in the output PMOS branch of the current comparator, when the OPAMP is in linear region. This occurs when both currents are within the tolerance region (the error percent is lower than 0.05%). This method has a maximum sensitivity of 50nA. This sensitivity was measured using DC current. For the values tested, the sensitivity varied from 35nA to 50nA. At higher frequencies the constraining factor is the operational amplifier bandwidth. This method does not introduce changes in the impedance of the node X2, so it does not affect the values of the currents that are being tested.



(a) Current Error Percent vs Input Current (b) X1, X2 and Output node vs Current Input

Figure 3–6: Current Comparator Circuit Behavior

Figure 3–6 shows an error percent between the input and output current (see equation 3.1). It is observed that there are two points where the error curve reaches the zero percent error.

$$ErrorPercent = \frac{(InputCurrent - OutputCurrent)}{InputCurrent} \times 100\% \tag{3.1}$$

Figure 3–6 shows the curves of nodes X1, X2 and Flag Comparison signal. That graph shows that there is a point where both voltages are equals. As mentioned before, the point where the two voltages are equal is the point where the system

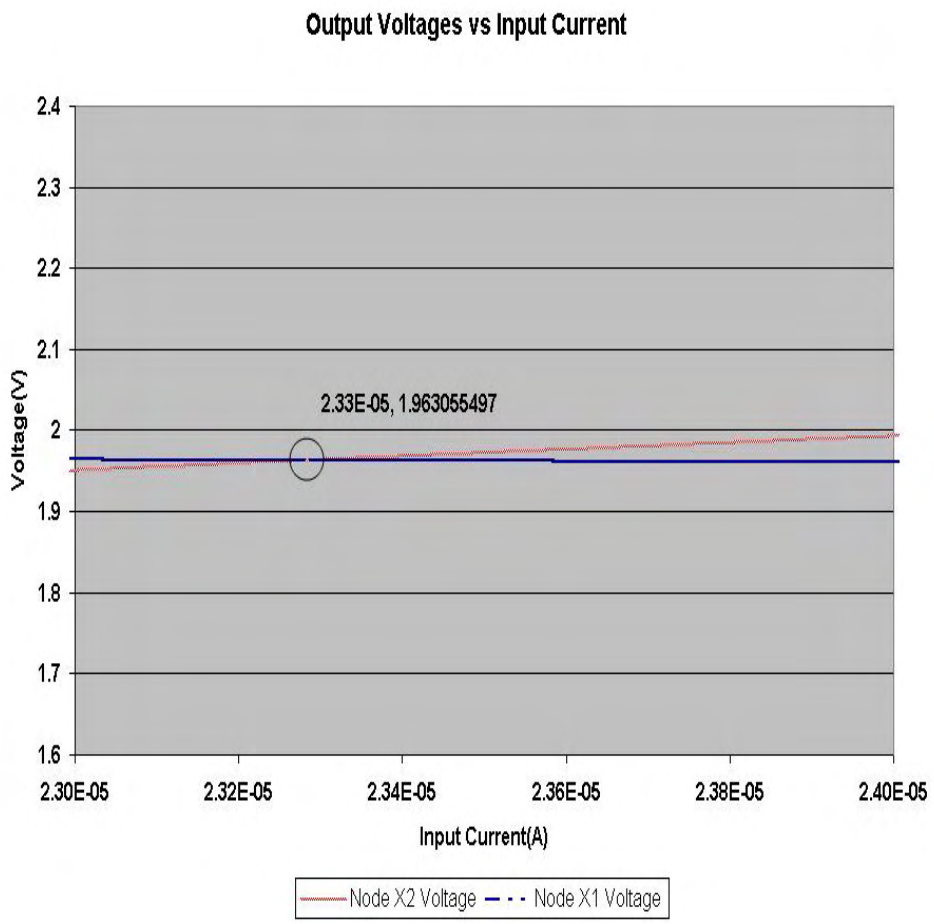


Figure 3–7: Zoom of Voltages in X1 and X2 vs Input Current

reach the zero error percent in the figure 3–6. In the curve of Flag Comparison signal in figure 3–6 is shows that adding the operational amplifier increases the sensitivity to current differences of the circuit. Figure 3–7 shows one of the instances where the voltage value of in node X1 and X2 are equal. The error percent is exactly zero for an input current equal to 23.3uA.

The output of this module, the Flag Comparison signal is inputted to the Digital Controller. It can select the size of the transistors in Path A that will will supply the correct voltage in the *Node X*. Also, this module feeds the Window Detector Module. It determines if the Comparator is in the transition region.

Table B–4 in Appendix B shows the dimensions of the transistors used it in the Current Comparator.

3.3 Window Detector

The proposed system already has a current comparator that determines if the input and output currents are different. It is still necessary to detect when both currents are in the region of acceptance to determine the best path to increment accuracy.

To relate the acceptable current error to the output voltage, a voltage region of acceptance must be selected. The region of acceptance is equal to the transition region of the current comparator circuit. The output of the Window Detector [15] is necessary toggles high if the Flag comparison signal is in the transition region. The Window Detector used in the proposed circuit uses two operational amplifiers, and an XOR gate. Each one of these operational amplifiers compares the voltage of the output of the comparator with V_{OH} and V_{IL}, which represents the limits of the transition region. So if V_{in} is is lower than Vref+ (V_{OH}), then the output operational amplifier A1 will be a logic "0", otherwise will be a logic "1". Analyzing the other side of the circuit if V_{in} is greater than Vref-(V_{IL}), the output of operational amplifier A2 will be a logic "1", otherwise it will be a logic "0". The output from Amplifiers A1 and A2 are sensed by the XOR gate to determine the flag signal. If the output is a logic "1" the currents are within the appropriate tolerance region.

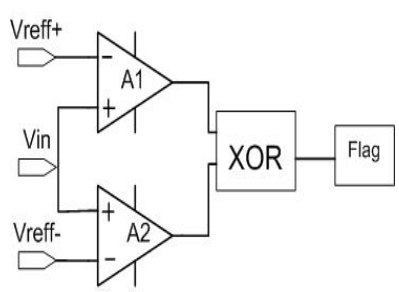


Figure 3–8: Window Detector

Figure 3–9 shows the transient response of the Window Detector. An input sinusoidal waveform with a DC value of 1.5V, an amplitude of 1.5V and frequency of 10KHz was introduced in V_{in} pin, and the reference for the high and low voltages

was 2V and 0.5V. Figure 3–9, shows that in areas where the voltage is between 0.5V and 2V the output voltage of the circuit goes to Vdd, otherwise goes to ground.

This output signal called Flag is inputted as the Enable signal of the Digital Controller Module. If the signal is low the Enable signal is asserted.

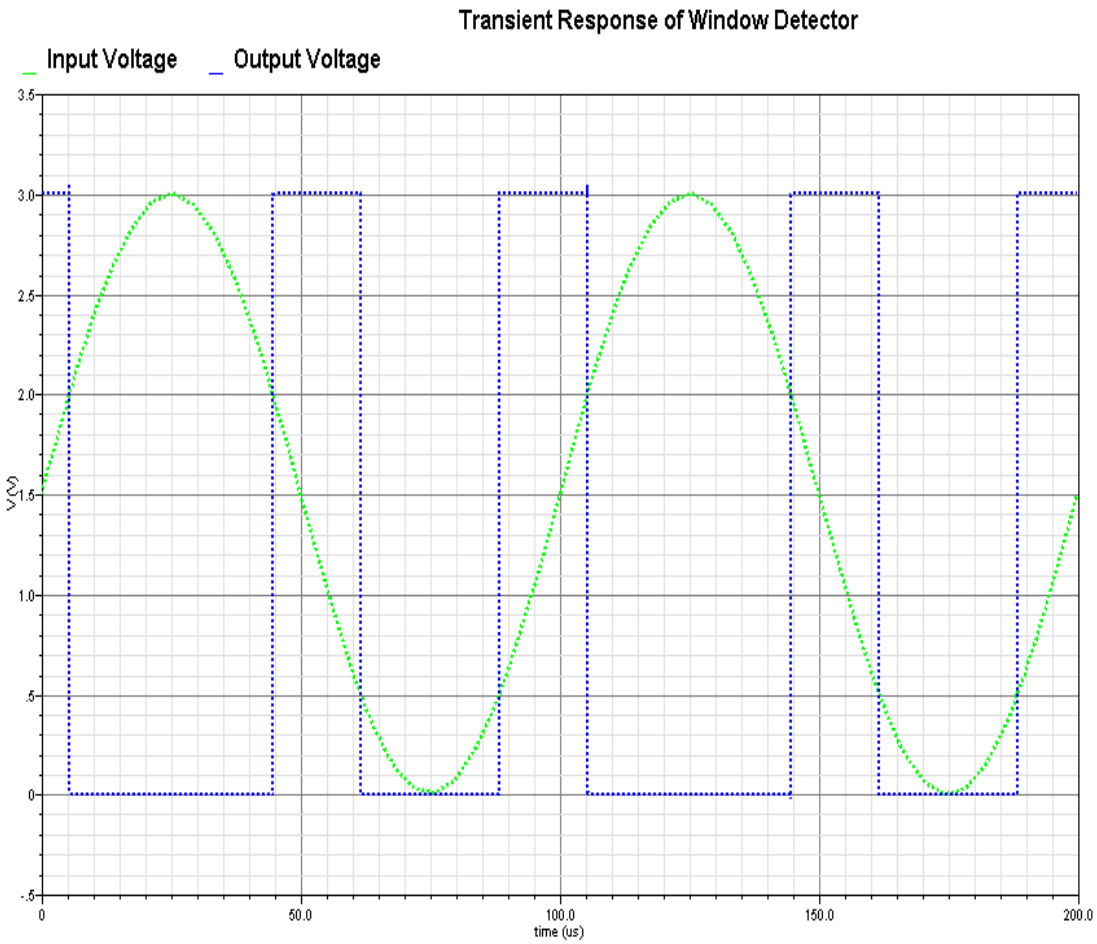


Figure 3–9: Window Detector Transient

3.4 Digital Controller

This section explains how to select the proper switch in Path A of the Biasing Circuit.

The Digital Controller circuit is the link between the current comparator, the window detector and the Biasing Circuit. It activates the correct switches to select the transistor in the Path A. This circuit shown in fig. 3–10, is composed of a decoder, a set of registers and an adder/substractor circuit.

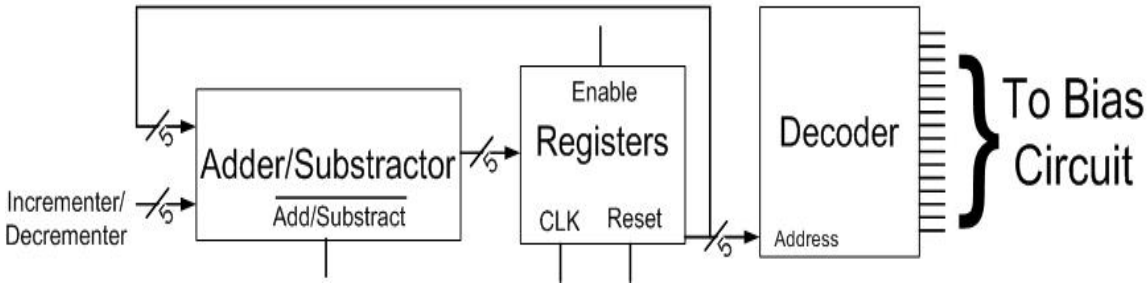


Figure 3–10: Digital Controller Circuit

The inputs of this modules are:

- Flag signal from the Window Detector Circuit
- Flag Comparison from Current Comparator
- ClK signal
- Reset

The circuit is started after the signal Reset is deasserted. The circuit takes an initial 5 bits address of a predetermined Path A. If the Flag signal from the Window Detector is high the circuit is disabled and the initial address remains.

If the Flag signal from the Window Detector is low, the Digital Controller circuit is enable. When the Flag Comparison circuit is set to a digital "1", the initial address, different from zero, will be decremented by one with each clock cycle. This process will continue until the circuit is disabled.

If the Flag Comparison signal is a digital zero, the input current is less than Iout. Thus the address must be incremented to allow the proper biasing to be implemented. Incrementing the address is achieved by adding a digital "1" to the saved address.

The Registers take the address that was incremented by the Adder/Subtractor circuit and store it at the falling edge of the clock. The output of this circuit feds to the Decoder and the Adder/substractor circuit as the address that should be incremented or decremented in the next clock cycle. The CLK signal in the register is the clock signal sensed by the D Flip-Flops. The Enable signal on the DFF is the

output signal of the Window Detector Circuit. When the Window Detector toggles high it is not necessary to increment or store a new address, because the circuit reaches the appropriate offset error percent. So the Registers will remain on the same state until the Window Detector toggles low.

The other part of the circuit is the Decoder. The decoder takes the address stored in the registers and activates the correct switch out of 17 possibilities of the output. Finally the bit that toggles high activates the correct switch in Path A of the Biasing Circuit.

The Adder/Substrator circuit is presented in figure 3–11. This circuit is composed of five 1-bit full adders with carry(see fig. 3–12), where the carry out of one module is the carry in of the next one. The XOR gate is used for the substraction operation. The XOR gate allows the implementation of a two's complement algorithm for subtraction (see Table 3–1).

Table 3–1: Truth Table for 2's Complement Numbers

Inputs	Two's Complement	Unsigned Decimal	Signed Decimal
00000	00000	0	0
00001	11111	1	-1
00010	11110	2	-2
00011	11101	3	-3
00100	11100	4	-4
00101	11011	5	-5
00110	11010	6	-6
00111	11001	7	-7
01000	11000	8	-8
01001	10111	9	-9
01010	10110	10	-10
01011	10101	11	-11
01100	10100	12	-12
01101	10011	13	-13
01110	10010	14	-14
01111	10001	15	-15
10000	10000	16	-16

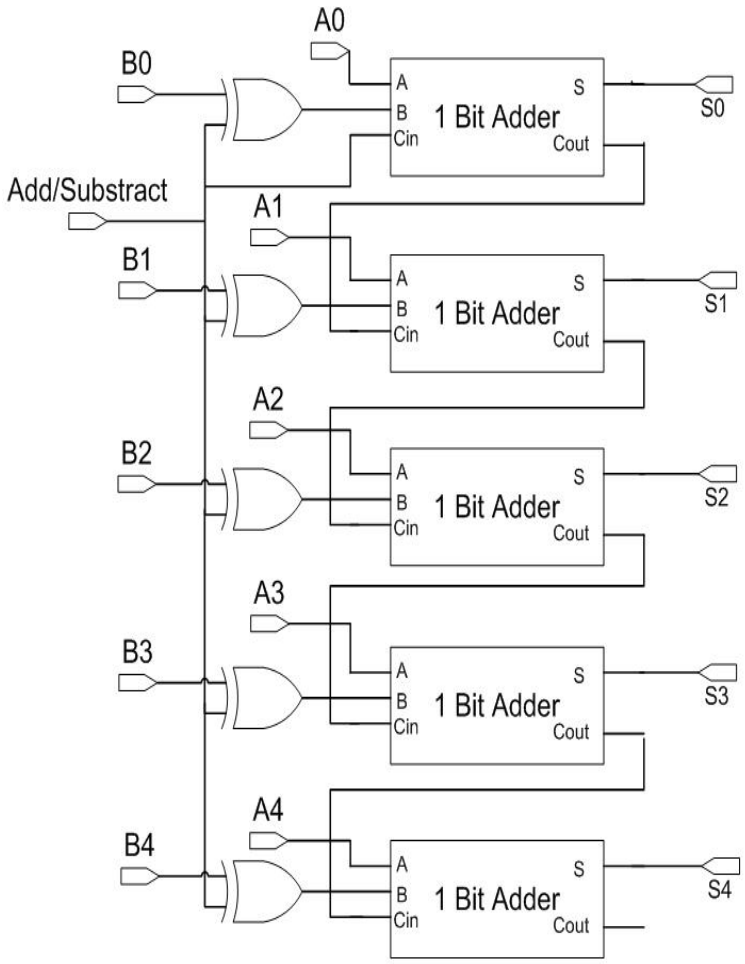


Figure 3–11: 5 Bits Full Adder

A Full Adder of one bit is shown in figure 3–12. This logic circuit adds 2 bits of information. This circuit connects this 1-bit full adder in cascade with another and carry out of the least significant bit to the carry in of the next(see figure 3–11). The 1-bit full adder is cascaded 5 times to compute any of the 5 bits of the binary number.

The 5-Bit register, is used to store the state of the switches. To store the data 5 D-Flip-Flops were used. The D-Flip-Flop used is seen in figure 3–13. This circuit has an Enable signal, a Clock signal and an Data(D) signal, and the output signal is Q. The truth table for this circuit is shown in table 3–3.

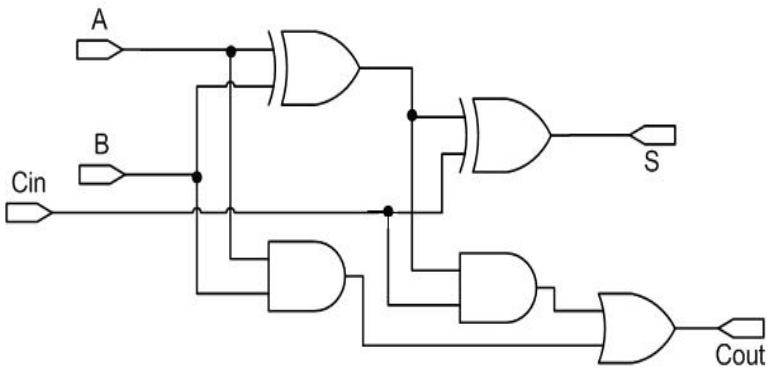


Figure 3–12: 1 Bit Full Adder

Table 3–2: Truth Table for the 1-Bit Full Adder

Inputs			Outputs	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The digital controller was simulated two times. First, the Digital Controller received a clock signal with of a frequency of 500KHz and an enable signal that remained active. Figure 3–14a shows the input signals and figure 3–14b shows the output signals of the circuit. When one of the outputs is asserted a transistor is activated in Path A of the Biasing Circuit. In figure 3–14b the sequence at which the different paths are activated is shown. Signals O0 to O16 are the outputs of the decoder.

For the second simulation the Enable signal was toggled. The transient simulation is shown in figures 3–15a and 3–15b. The Enable signal is toggle low at 8.5μs and again toggle high at 15μs, the signal add/substract is low the first 8.5μs and then goes high. In figure 3–15b the outputs are increasing from O0 to O4. When the Enable signal toggles low, the circuit will remain at the present state. In this

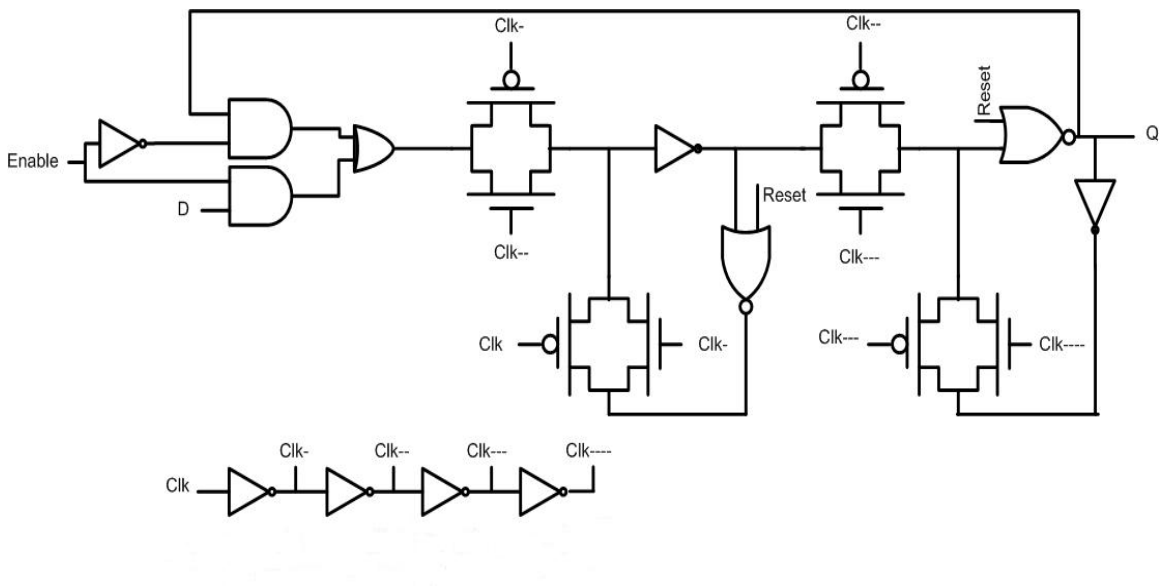
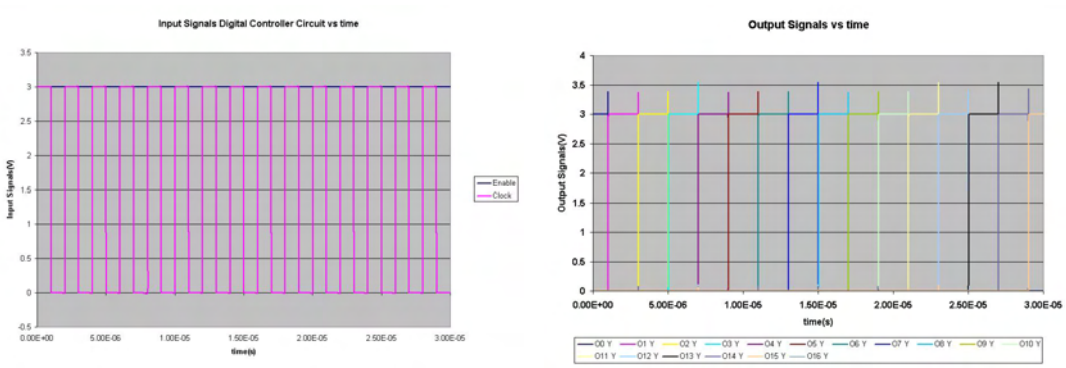


Figure 3–13: D Flip-Flop

Table 3–3: D Flip-Flop Truth Table

Inputs				Outputs	
D	Enable	Reset	Clk	Q	$\bar{Q}$
0	1	0	Falling Edge	0	1
1	1	0	Falling Edge	1	0
X	0	0	Falling Edge	Last Q	Last $\bar{Q}$
X	X	X	0	Last Q	Last $\bar{Q}$
X	X	X	1	Last Q	Last $\bar{Q}$
X	X	1	X	0	1

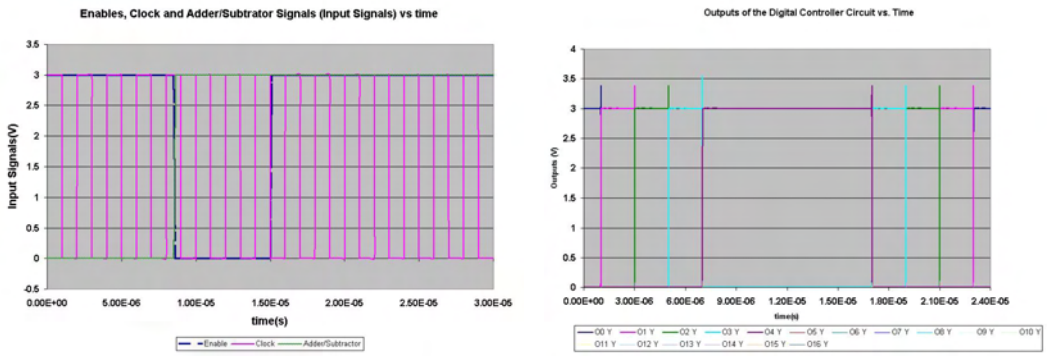


(a) Input Signals vs time (b) Output Signals vs time

Figure 3–14: Behavior of the Digital Controller

case the O4 output will remain high until at 15us the Enable signal again toggles high, and as the add/substract signal is high. Then the circuit should decrement

the state of the outputs, that is why the remaining time of the simulation the circuit decrements the states from O4 to O0.



(a) Input Signals vs time (b) Output Signals vs time

Figure 3–15: Behavior of the Digital Controller, Second Simulation

This outputs allows fine tuning of the biasing voltage by selecting different size PMOS transistors. Still an approximetion of the input current is needed to select a starting biasing point. To determine the range of the input current a Path Selector Circuit is introduced.

3.5 Path Selector and Digital Interface Circuit

As mentioned before the Path Selector circuit senses the input current and outputs 14 digital bits. The outputs carry information about the amount of current inputted. The Digital Interface decodes the 14 bits into 15 non-overlapping digital signals. This signals determine the transistor selected for Path B.

The Path Selector works in parallel to determine the amount of current that is inputted in the circuit. There are 15 different current ranges, and 14 stages of comparison (see Table 3–4). In each branch the current is compared with a different value to determine if Iin is bigger or less than the reference range current. The digital data obtained is inputted to a decoder that selects the best path.

For turning on each one of the switches a comparison between the input current and the limit current ($Range_i$) is done (see table 3–5) . For this purpose 14 input current replicas are generated and compared with 14 replicas of a current references

of 100uA, but with different gain. These gains generate the values of the limit currents that are needed. This circuit is shown in figure 3–16. This figure presents the circuit that generates a high signal for every $I_{refi} < I_{in}$ turns on only two of the switches.

The first range has a gain of 0.25 which means that the current limit here is 25uA, the second one is 0.41 which means that current limit to be compared the input current is 41uA. Using this pattern there are 12 more comparison stages all with different gains which are shown in table 3–4. For the generation of the current gains, the NMOS transistors were size accordingly. If the wrong switches are activated, a correction connection can be made using Path A. The dimensions of the transistors are shown in tables B–5 and B–6 in the Appendix B.

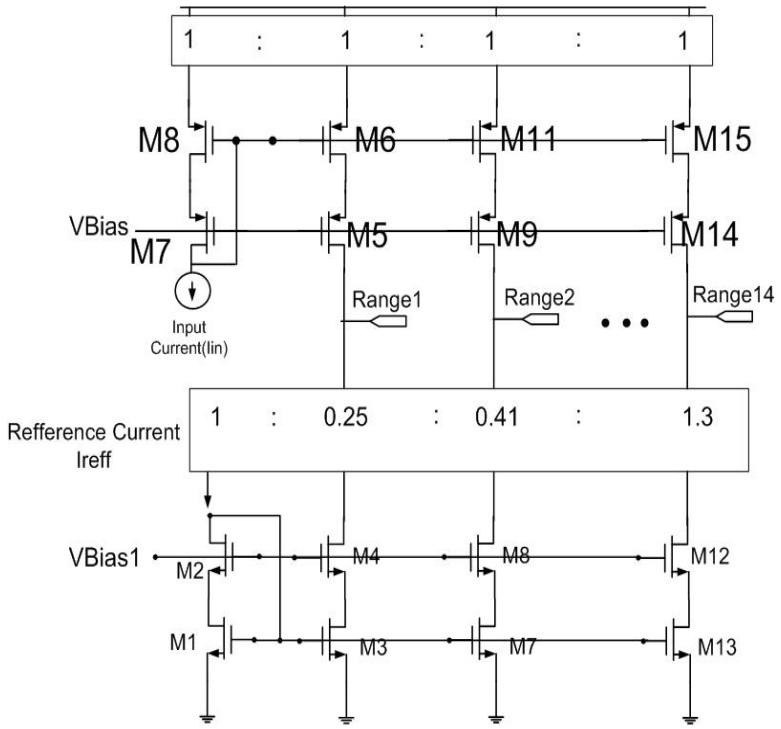


Figure 3–16: Path Selector Circuit

Figure 3–17 shows the behavior of the range generator circuit. When the input current is equal or higher than the limit value of current, the corresponding output

Table 3–4: Gain and Current to be Compare of the Current Stages Comparators

Range	Gain	Current to be Compare with
1	0.25	$25\mu A$
2	0.41	$41\mu A$
3	0.56	$56\mu A$
4	0.68	$68\mu A$
5	0.80	$80\mu A$
6	0.9	$90\mu A$
7	0.97	$97\mu A$
8	1.03	$103\mu A$
9	1.07	$107\mu A$
10	1.11	$111\mu A$
11	1.15	$115\mu A$
12	1.20	$120\mu A$
13	1.25	$125\mu A$
14	1.30	$130\mu A$

node goes high. For example, the behavior of the *Range1* output node (see figure 3–16, it goes high(see fig 3–17) when the input current is higher than 25uA, otherwise the output is low. Same behavior is observed in the other outputs.

The circuit in figure 3–16 determines the correct current range. It indicates if the input current is higher or lower than a reference current. A digital circuit, shows in figure 3–18 was design as an interface between the range generator and the biasing circuit. This circuit, a decoder avoids the simultaneous activation of two biasing switches.

Figure 3–19 shows the output of the range generator with the Decoder connected. It shows a non overlapping response of the switches is non overlapping. For example, the switch 1 is only activated when the input current is less than 25uA, switch 2 is activated when the input current has a value between 25uA and 41uA. The same behavior is observed for the rest of the switches.

Table 3–5: Switches Activation According to Input Current Ranges

Switch Activated	Current Range
SW1	less than 25uA
SW2	between 25uA and 41uA
SW3	between 41uA and 56uA
SW4	between 56uA and 68uA
SW5	between 68uA and 81uA
SW6	between 81uA and 90uA
SW7	between 90uA and 97uA
SW8	between 97uA and 103uA
SW9	between 103uA and 107uA
SW10	between 107uA and 111uA
SW11	between 111uA and 115uA
SW12	between 115uA and 120uA
SW13	between 120uA and 125uA
SW14	between 125uA and 130uA
SW15	greater than 130

3.6 Biasing Circuit

The center of this control system and its motivation is the Biasing Circuit. This circuit supplies the voltage needed at *node X*. The Biasing circuit (see fig 3–20), is a modification of the Regulated Current mirror. *Node A* supplies the voltage needed to *node X* of the Self-Biasing Current Mirror (see figure 3–1) using the Voltage Follower Module. The transistors (Path B) that supply current to transistor M2 are selected depending of the range of Iin (see table 3–5). The current ranges were chosen to achieve its best performance.

In this circuit, transistors M1, M2 and M15 in Path B, have a different sized. In the actual circuit there there are 15 different size transistors, each 0.3um wider than the other. These transistors produce different voltages in *node A*, so it is possible use the path B by closing corresponding switches which are SW1, SW2... SW15, for different quantities of current. There exist one problem with this scheme, in $0.6\mu m$ technology, it has a very small current range where the appropriate accuracy

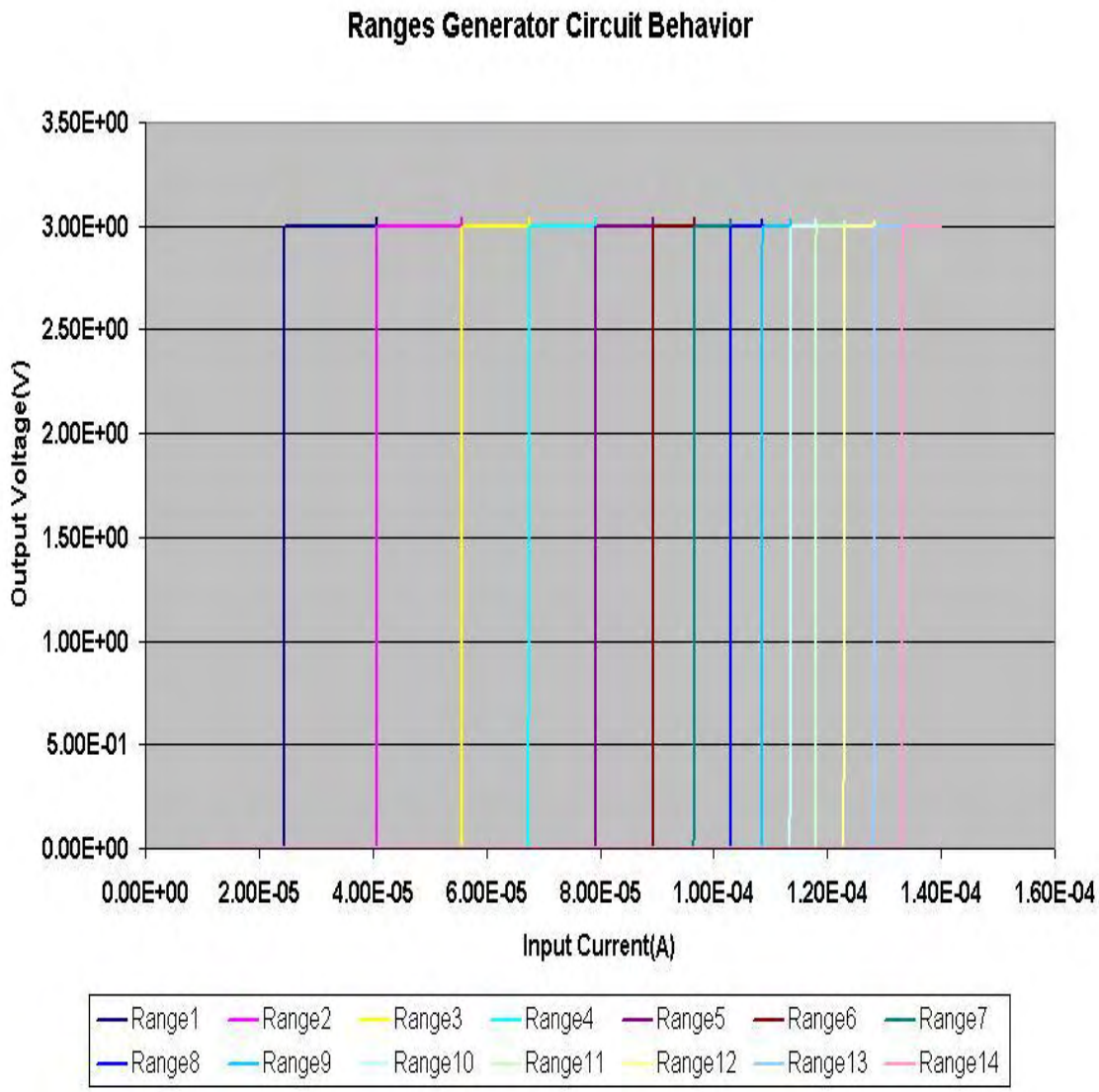


Figure 3–17: Path Selector Circuit Behavior

is achieved, because the voltages quantities produced are not close enough to compensate the offset in continuous current values. Due to the reason exposed before the Path A is introduced.

The main function of those transistors is to allow smaller variations for the output node voltage, thus making a more accurate current copy. The complete system has 15 possible choices in Path B, and other 17 possible choices for Path A. The reason for 17 possible transistors in Path A and and 15 in B that as much transistors would be put it more voltage values it will be possible to produce. With

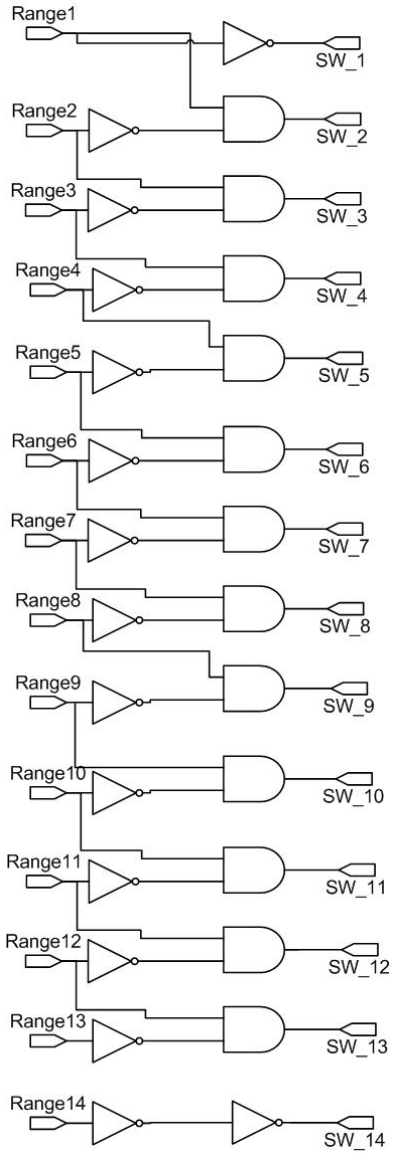


Figure 3–18: Decoder

the addition of Path A, the circuit is able to generate 255 different voltages, because for each transistor chosen in Path B, there are 17 possibilities for transistor size to choose in Path A.

It is important to discuss how the voltage is generated in node A. If one of the transistors of the path A is fixed, depending of the transistor chosen in Path B, the current I_{Out} will change proportionately to the aspect ratio of the transistor chosen. Nodes A and B will polarized according to the transistor size selected. The size of the transistor selected in Path A is proportional to the voltage in Node A. In Path

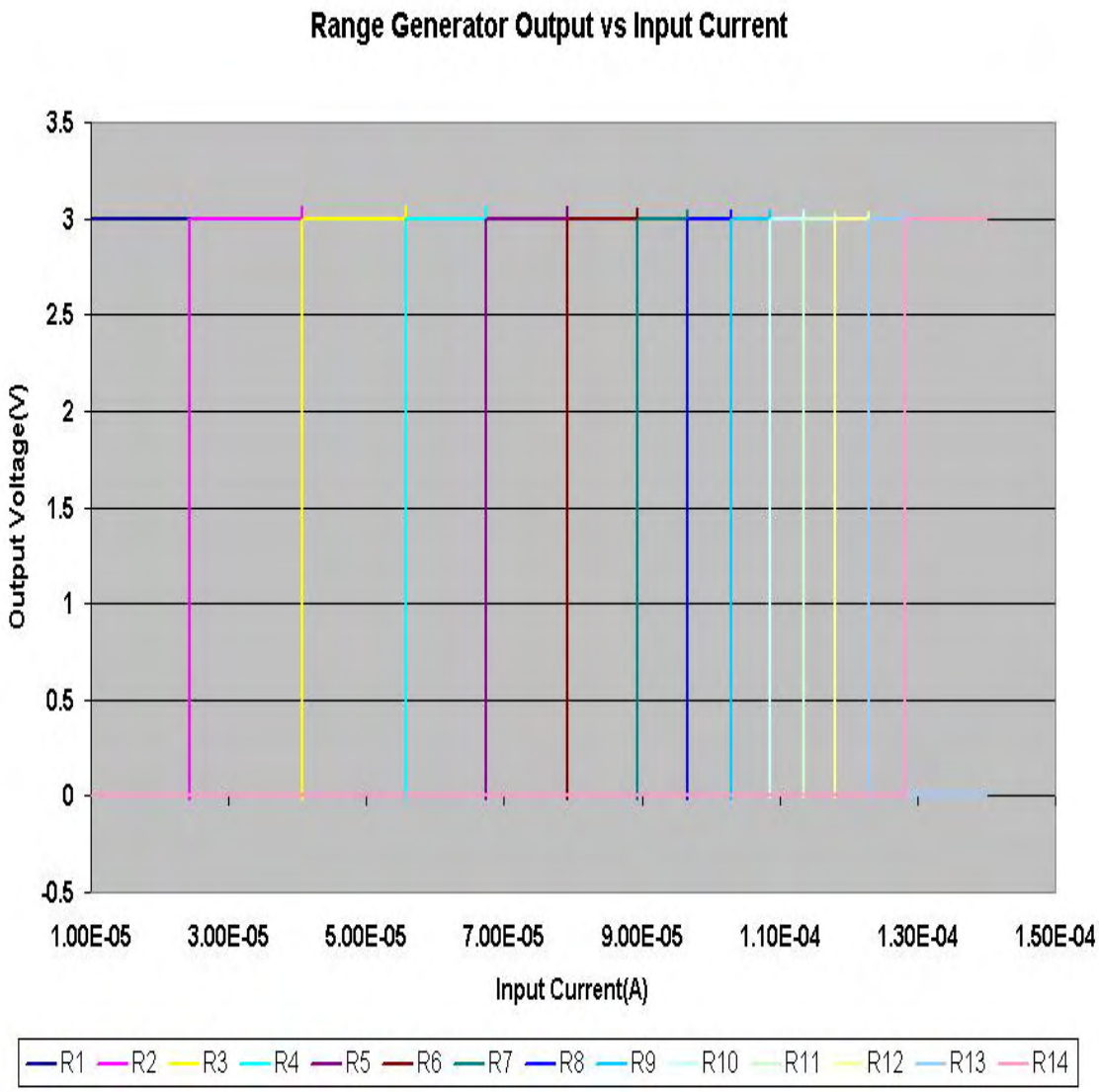


Figure 3–19: Path Selector with Digital Interface Circuit Behavior

B the larger the transistor selected, the lower voltage in node B. Path A permits a fine tuning of the voltage selected for the current range.

Figure 3–21 shows a transient simulations of the Biasing circuit. The transient simulation allows toggling of the clock signals. It covers all the output voltage range that the circuit is able to supply. Switch behavior was simulated with piece wise linear voltage sources. This circuit is capable to supply the Cong-Geiger Mirror with voltage values that range from 1V to 1.6V. As the circuit regulates and selects the transistor for the path the figure shows several glitches. Those are due to the

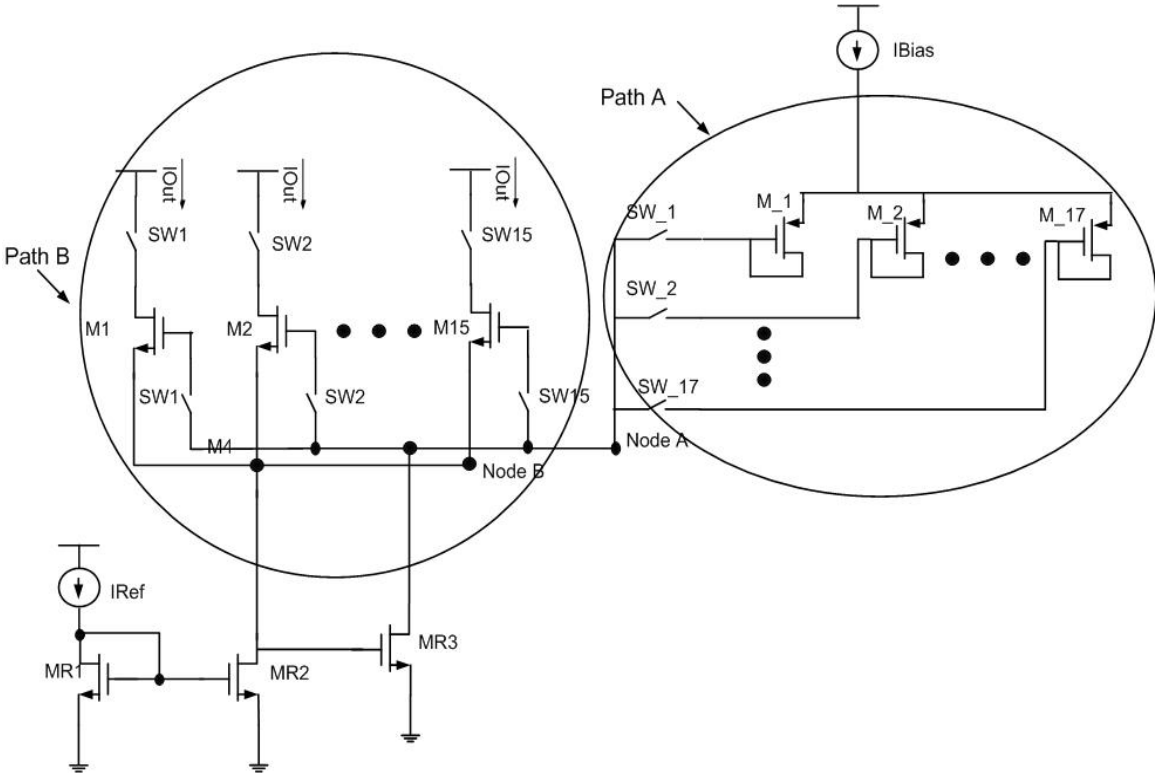


Figure 3–20: Biasing Circuit

switching operation, the largest ones are the ones produced by the switches in Path B, and the smaller ones are due to the switches in Path A.

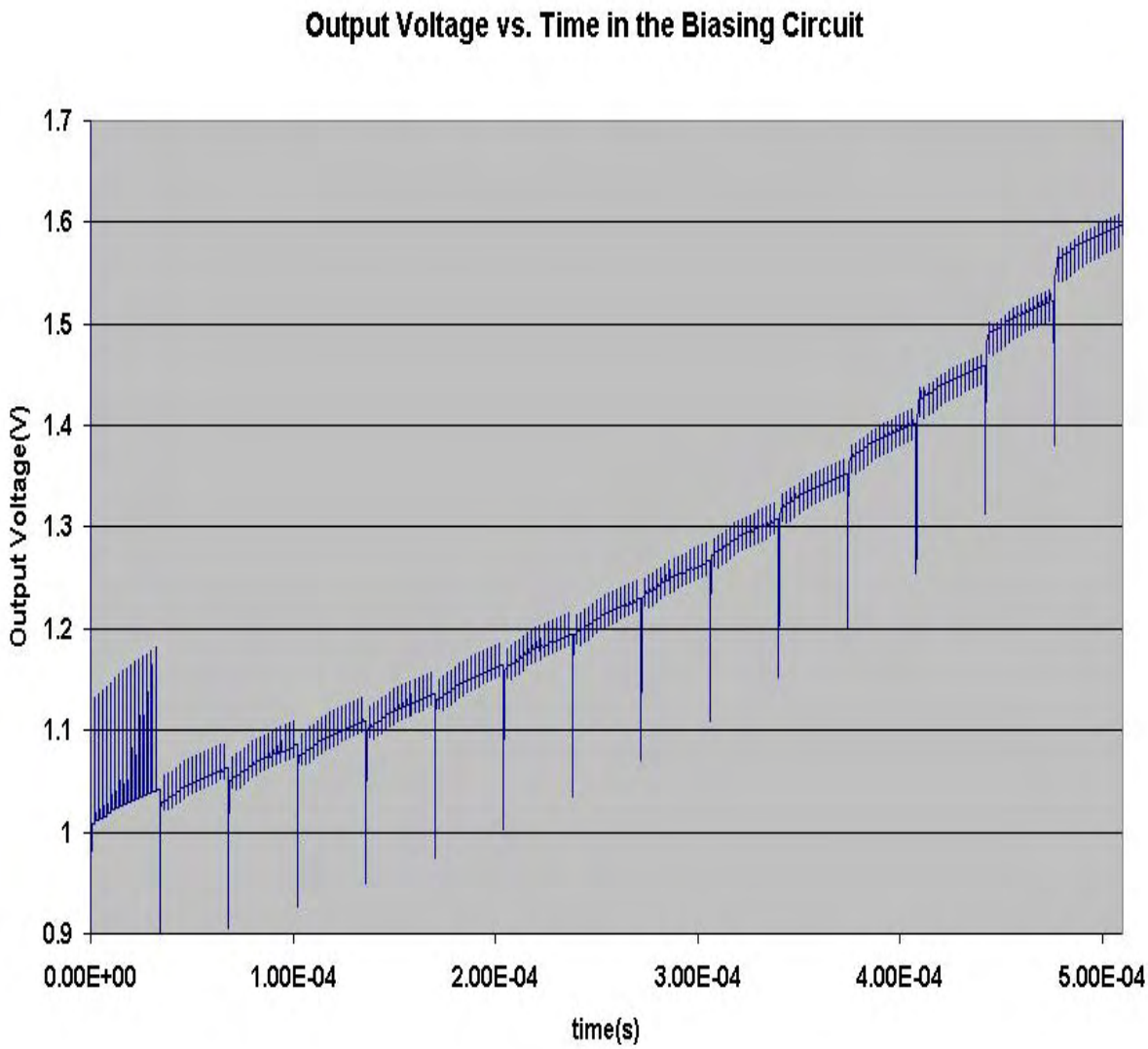


Figure 3–21: Complete Voltage Range of the Biasing Circuit

Figure 3–22 is zooms a range of values found in figure 3–21. In this graph, one of the transistors in path B was selected. All the transistors in path A are changing each $2\mu s$. This allows a selection of 15 possibilities for the output voltage value. This graph also shows that the Bias Circuit can produced values very close one to the other. In the graph, the voltage values vary from 1.01V to 1.04V for the one of the transistors in path B that is on.

The dimensions of the transistors on the Biasing Circuit are shown in Table B–2 in Appendix B.

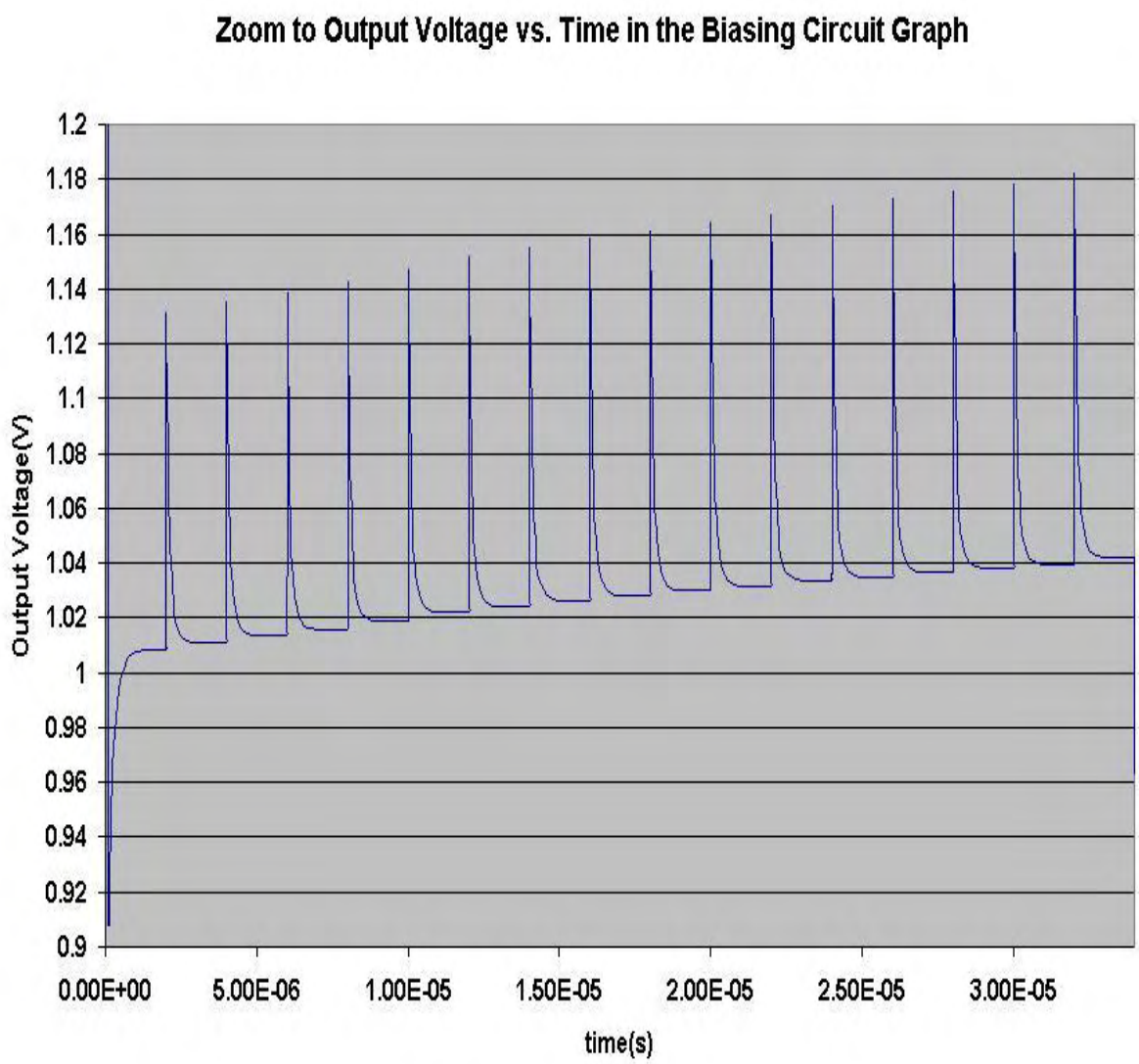


Figure 3–22: Complete Voltage Range of the Biasing Circuit

3.7 Voltage Follower

The output of this circuit is connected to a operational amplifier in voltage follower configuration. This isolates the biasing circuit currents from the Geiger-Cong circuit. The operational amplifier used is shown in figure 3–23. It is important to have a very low voltage offset on this operational amplifier, due to the performance of the system depends on the accuracy of the voltage injected on the node X. The operational amplifier was design to operate in the the range needed with less offset.

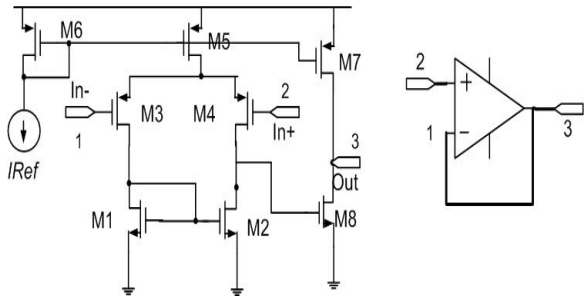


Figure 3–23: Operational Amplifier

Table B–3 in Appendix B shows the dimensions of the transistors use it in the operational amplifier. The layouts of the most important components and the complete system is shown in Appendix C.

This chapter presented the operation of the system design in this research. The results of the simulations of this system is shown in chapter 5.

CHAPTER 4
SMALL SIGNALS ANALYSIS

4.1 Small Signal Analysis of the Output Node in the Geiger Mirror

This section presents the small signal analysis of the output node of the current mirror(see fig 4–1) used in this work. In this analysis, the values of the input and output resistance are calculated. For the small signal analysis the DC current sources I_{bias} are an open circuit and the constant voltage V_{bias} goes to ground.

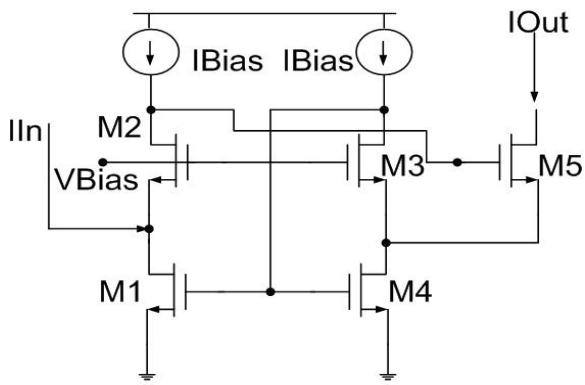


Figure 4–1: Geiger Current Mirror Circuit

Figure 4–2 shows the small signal model of the stage that involves the transistors M3, M4, M5. For this analysis a test voltage source, V_T, is introduced, and the current flowing out of the voltage source called I_T. The current flowing through r_{03} is equal to the current source $g_{m3}V_{gs3}$, this means that the current flowing through M5 is the same current flowing through M4, so eq. 4.1 and eq. 4.2 represent the values of the current flowing through both transistors.

$$I_T = g_{m5}V_{gs5} + \frac{V_T - V_X}{r_{05}} \tag{4.1}$$

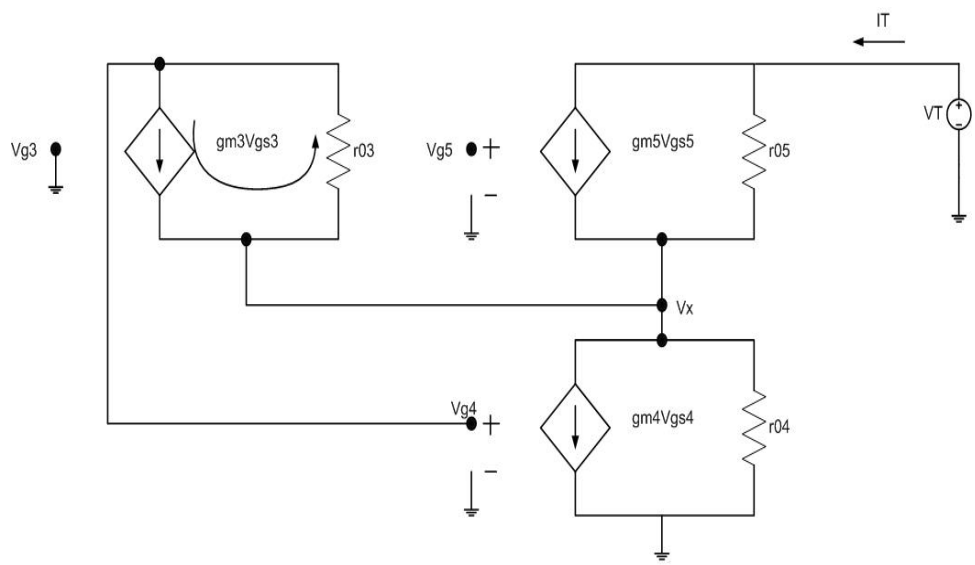


Figure 4–2: Small Signal diagram of the connections between transistors M3, M4 and M5

$$I_T = g_{m4}V_{gs4} + \frac{V_X}{r_{04}} \tag{4.2}$$

Solving eq. 4.2 for V_X it is obtained that

$$V_X = (I_T - g_{m4}V_{gs4})r_{04} \tag{4.3}$$

$$I_T = g_{m5}V_{gs5} + \frac{V_T - (I_T - g_{m4}V_{G4})r_{04}}{r_{05}} \tag{4.4}$$

Knowing that $V_{gs5} = V_{g5} - V_X$

$$IT = g_{M5}(V_{g5} - V_X) + \frac{(V_T - V_X)}{r_{05}} \tag{4.5}$$

$$IT = g_{M5}V_{g5} + \frac{V_T}{r_{05}} - V_X(g_{m5} + \frac{1}{r_{05}}) \tag{4.6}$$

Substituting equation 4.3 in equation 4.6:

$$I_T = g_{M5}V_{g5} + \frac{V_T}{r_{05}} - \frac{1}{r_{04}}(I_T - g_{m4}V_{g4})(g_{m5} + \frac{1}{r_{05}}) \tag{4.7}$$

In the equation 4.7 there are two unknown parameters, which are V_{g5} and V_{g4}. V_{g4} can be calculated from the following equation in transistor M3.

$$g_{M3}(-V_X) + \frac{(V_{g4} - V_X)}{r_{03}} = 0 \tag{4.8}$$

$$V_{g4} = V_X(1 + g_{m3}r_{03}) \tag{4.9}$$

Substituting the equation 4.3 in 4.9:

$$V_{g4} = \frac{(I_T r_{04}) + (I_T g_{m3} r_{04} r_{03})}{1 + (g_{m4} r_{04}) + (g_{m4} r_{04} g_{m3} r_{03})} \tag{4.10}$$

To solve for V_{g5}. It is necessary to analyze the connection of transistors M1 and M2 to calculate the gate voltage. The small signal model is shown in figure 4–3. There is no current flow through both transistors because the I_{bias} current sources were disconected.

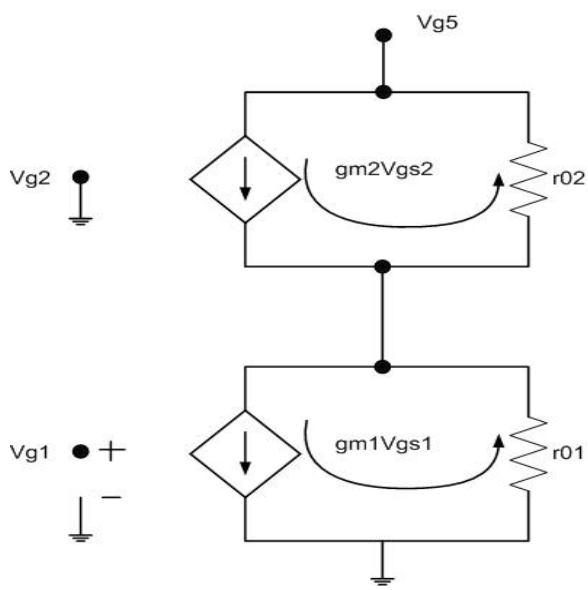


Figure 4–3: Small Signal Diagram of the connections between transistors M1 and M2

From fig 4–3 it is possible to obtain the equation 4.11

$$V_{g5} = -g_{m1}r_{01}(1 + g_{m2}r_{02})V_{gs1} \tag{4.11}$$

The term V_{gs1} is substituted by V_{g4}, because in fig. 4–1 that transistor M1 and M4 share the same gate and source, so equation 4.11 is transformed in equation 4.12.

$$V_{g5} = -g_{m1}V_{g4}r_{01}(1 + g_{m2}r_{02}) \tag{4.12}$$

Substituting equation 4.12 in equation 4.7:

$$I_T = g_{m5}(-g_{m1}r_{01}(1 + g_{m2}r_{02})V_{g4}) + \frac{V_T}{r_{05}} - \frac{1}{r_{04}}(I_T - g_{m4}V_{g4})(g_{m5}) \tag{4.13}$$

$$I_T = V_{g4}(\frac{g_{m5}g_{m4}}{r_{04}} - g_{m5}g_{m1}r_{01} - g_{m2}r_{02}g_{m1}r_{01}g_{m5}) + \frac{V_T}{r_{05}} - \frac{I_T g_{m5}}{r_{04}} \tag{4.14}$$

Equation 4.14 is simplified as follows because the terms $\frac{g_{m5}g_{m4}}{r_{04}}$ and $g_{m5}g_{m1}r_{01}$ are negligible.

$$I_T = V_{g4}(-g_{m2}r_{02}g_{m1}r_{01}g_{m5}) + \frac{V_T}{r_{05}} - \frac{I_T g_{m5}}{r_{04}} \tag{4.15}$$

In equation 4.15 the only unknown parameter is V_{g4}. It is substituted by equation 4.10, thus I_T is equal to:

$$I_T = \frac{I_T r_{04} + I_T g_{m3}r_{04}r_03}{1 + g_{m4}r_{04} + g_{m4}r_{04}g_{m3}r_{03}}(-g_{m2}r_{02}g_{m1}r_{01}g_{M5}) + \frac{V_T}{r_{05}} - \frac{I_T g_{m5}}{r_{04}} \tag{4.16}$$

Arranging the terms of equation 4.16 the following is obtained:

$$\frac{V_T}{r_{05}} = I_T - I_T\frac{r_{04} + g_{m3}r_{04}r_03}{1 + g_{m4}r_{04} + g_{m4}r_{04}g_{m3}r_{03}}(-g_{M2}r_{02}g_{M1}r_{01}g_{M5}) + \frac{I_T g_{M5}}{r_{04}} \tag{4.17}$$

$$\frac{V_T}{I_T} = r_{05}(1 + \frac{r_{04} + g_{m3}r_{04}r_03}{1 + g_{m4}r_{04} + g_{m4}r_{04}g_{m3}r_{03}}(g_{M2}r_{02}g_{M1}r_{01}g_{M5}) + \frac{g_{M5}}{r_{04}}) \tag{4.18}$$

In equation 4.18 the terms 1 and $\frac{g_{m5}}{r_{04}}$ can be neglected because they are smaller in comparison with the other terms of the sum, therefore:

$$\frac{V_T}{I_T} = r_{05}(\frac{r_{04} + g_{m3}r_{04}r_{03}}{1 + g_{m4}r_{04} + g_{m4}r_{04}g_{m3}r_{03}}(g_{m2}r_{02}g_{m1}r_{01}g_{m5})) \tag{4.19}$$

There are some terms in eq. 4.19 that can be neglected, the equation becomes:

$$\frac{V_T}{I_T} = r_{05}(\frac{g_{m3}r_{04}r_{03}}{g_{m4}r_{04}g_{m3}r_{03}}(g_{m2}r_{02}g_{m1}r_{01}g_{m5})) \tag{4.20}$$

Finally having the output value of the output resistance as:

$$r_{out} = \frac{g_{m1}r_{01}g_{m2}r_{02}g_{m5}r_{05}}{g_{m4}} \tag{4.21}$$

Equation 4.21, Geiger Mirror has a very high output impedance, comparable to the triple cascode current mirror.

4.2 Small Signal Analysis of the Input Node in the Geiger Mirror

For the analysis of the input node of the Geiger mirror, the current sources are taken as an open circuit and the DC voltages are ground. Figure 4–4 shows small signal model for the input stage of the Geiger Mirror. In this circuit it can assumed that the gates of both transistors are connected to ground because the gate of transistor M2 is connected to a DC external voltage source, and the gate of transistor M1 gate is connected to a the output stage of the circuit small signal model should be like shown in figure 4–5.

The input resistance (r_{in}) of the node A1 is:

$$r_{in} = r_{top}||r_{bottom} \tag{4.22}$$

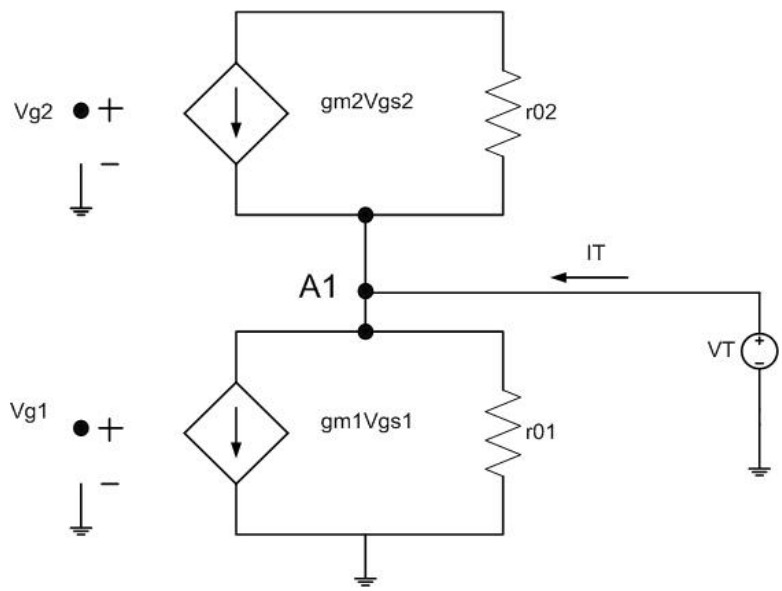


Figure 4–4: Small Signal Model for input stage M1 and M2

To calculate the impedance r_{bottom}, I_T is equal to the current through the transistor M1and M2. The current flow in transistor M1 is modeled by the equation 4.23.

$$I_T = g_{m1} \times V_{GS1} + \frac{V_T}{r_{01}} \tag{4.23}$$

The term $g_{m1} \times V_{GS1}$ gets canceled in the equation 4.23 because $Vgs = 0$. Thus:

$$I_T = \frac{V_T}{r_{01}} \tag{4.24}$$

$$\frac{V_T}{I_T} = r_{01} \tag{4.25}$$

Then as $r_{bottom} = \frac{V_T}{I_T}$ it is possible to conclude that:

$$r_{bottom} = r_{01} \tag{4.26}$$

It is necessary to calculate r_{top}, this is taken as equal to the transconductance (g_m) of the transistor M2. This is supported by the Source Absorption Theorem. Thus the value of r_{top} is given by equation

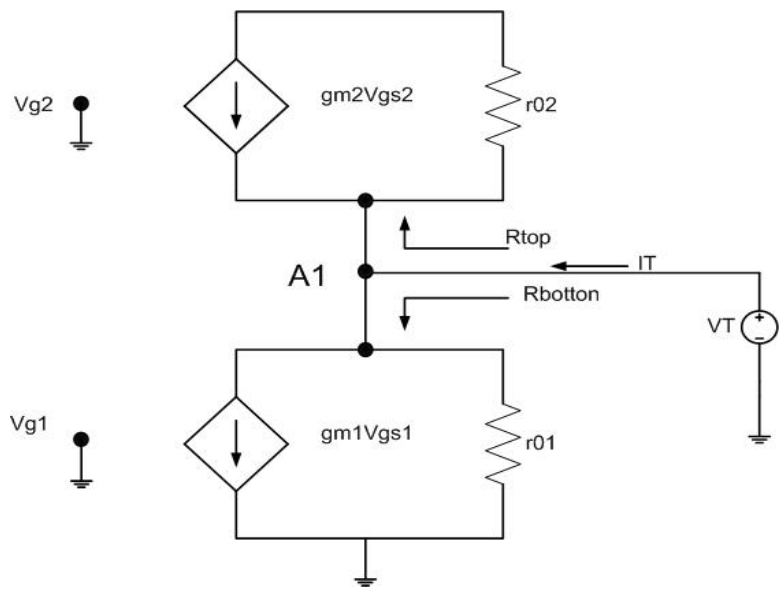


Figure 4–5: Small Signal Model for input stage M1 and M2 simplified

$$r_{top} = \frac{1}{g_{m2}} \tag{4.27}$$

Having the values for r_{top} and r_{bottom} the input resistance of the Geiger mirror is given by equation 4.28.

$$r_{in} = \frac{1}{g_{m2}} || r_{01} \tag{4.28}$$

The input impedance of the Geiger mirror is approximately equal to the transconductance to g_{m2}, which is a very low value of an input impedance.

CHAPTER 5
SIMULATIONS AND RESULTS

This chapter discusses the simulations and results of the proposed system. The first simulations presented, are from the analog part of the system. Secondly, simulations for DC values are provided, and last, simulations of continuous current values. Simulations were done using Cadence Tools with technology AMI06 $0.6\mu m$ technology.

Transient simulations were done to allow the clock signal to be active. It is not possible to run DC sweep simulations because the system relies on the clock signal for circuit biasing and offset correction.

5.1 Analog Circuit Simulations

Simulations of the analog portion where done using data that emulates the control switches response. The simulations used a ramped input current source that goes from $10\mu A$ to $140\mu A$. This is the range of current where the proposed circuit maintains an offset error percent lower than 0.05%.

Figure 5–1 presents the transient response of the proposed circuit. Spikes shown in the output current curve, are due to the toggling of the switches. The time that the switches needs to stabilize is $1\mu s$.

Figures 5–2 and 5–3 present the offset error percent of the output and input current of the figure 5–1. The curve is constrained with in $\pm 0.5 \times 10^{-3}$ which is the same of $\pm 0.05\%$ of offset error. In the error percent graphs, there are some spikes in specific points, (see figure 5–1). Those are due to the switching signals in the analog circuit.

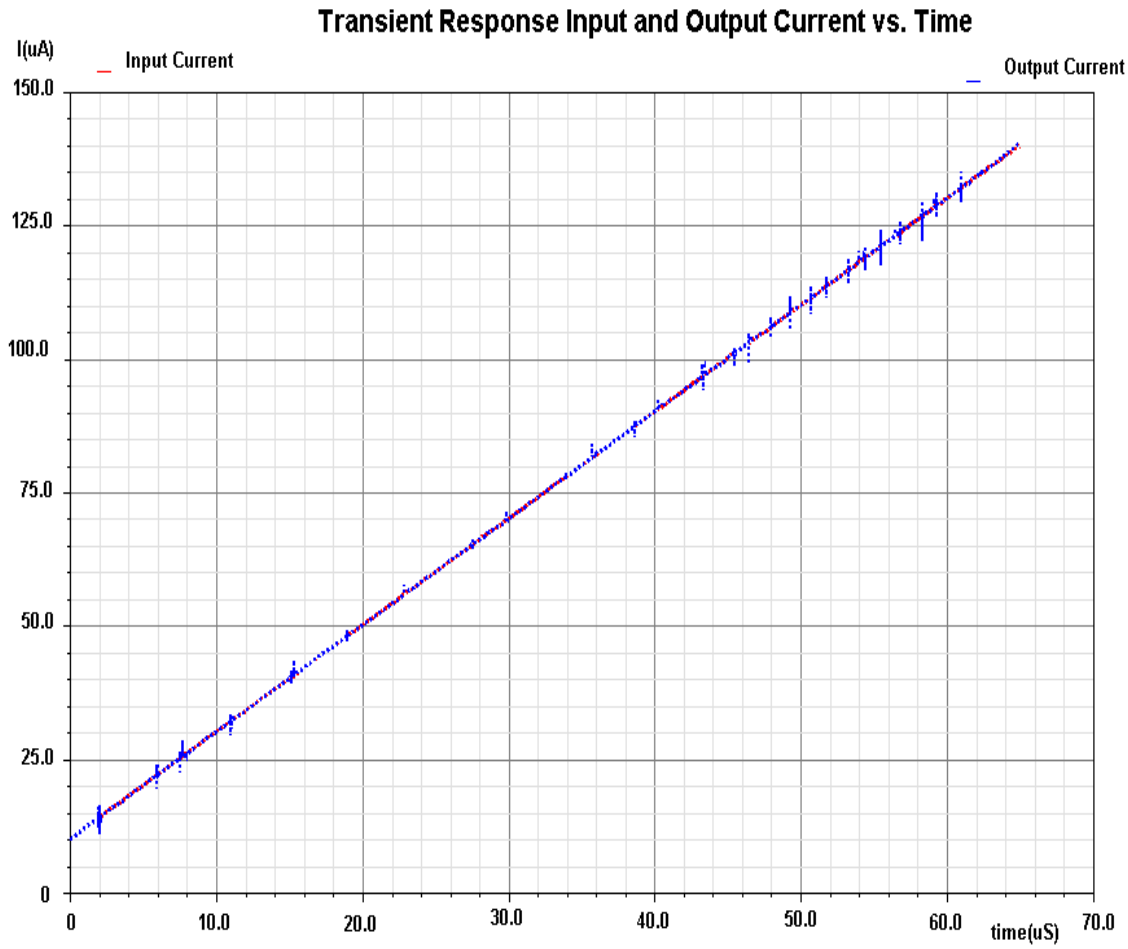


Figure 5–1: Transient Response, Input and Output Currents

Figure 5–4 presents a transient of input output current of the circuit in [10]. This circuit was simulated in technology AMI06, the offset error is shown in figure 5–4. This figure also shows that the minimum percentage error of the current mirror in [10] is 0.7% and the maximum is 11% for the same range that the proposed circuit was tested. Comparing the proposed circuit with [10] a significant decrease in the offset error percent is observed, and the ratio input range vs transistor size is increased. A current of $50\mu A$ is used for design. It has approximately, 3 times the range of current for what the transistors were design for. In [10] the transistors are design for a operational current of $150\mu A$, and a maximum range of $220uA$.

Figure 5–5 shows the behavior of the system proposed in this work. In this simulation the input current is a sinusoidal waveform with a DC current of $45\mu A$

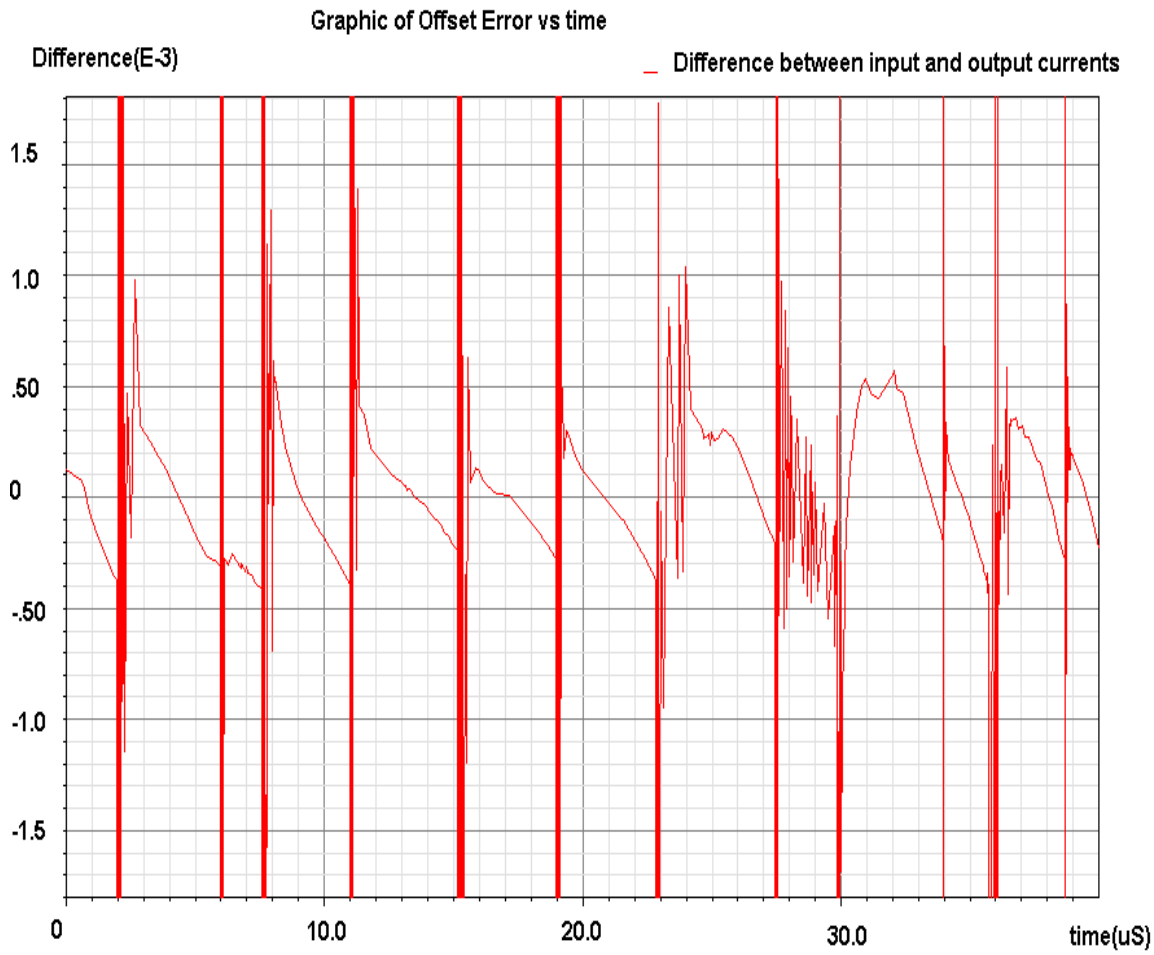


Figure 5–2: Transient Error Percent

and an amplitude of 10uA with a frequency of 10KHz. In that simulation the switches are also controlled, in the same way that in the figures shown before in this chapter. It is possible to observe that our offset error percent ranges between $\pm 0.05\%$. The spikes in the signal are produced by the toggling the switches.

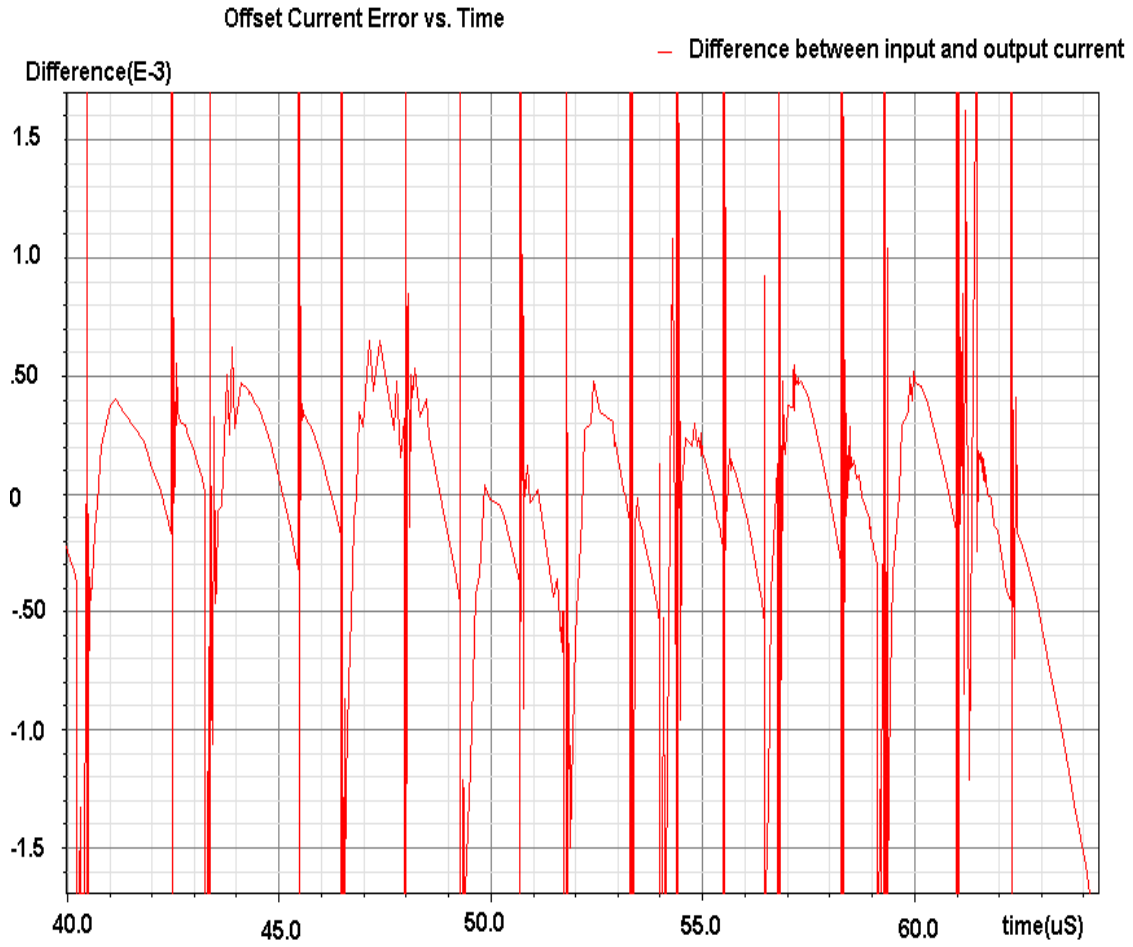


Figure 5–3: Transient Error Percent

5.2 Simulations with DC Values

Last section presented simulations and results of the analog part of the system. This section presents simulations of the complete system. Different DC values were used as input to test the system. The clock signal of the digital controller had a frequency of 500KHz.

The circuit received its input DC values, these values were selected considering the complete range of the system, so the values used for this simulations are 15uA, 70uA and 135.5uA. Those values test the system in the lowest, medium and highest values of the range.

The first value presented, is an input current of 15uA, shown in figure 5–6. In this graph, both current values overlap in the graph. Graph 5–7 presents a zoom

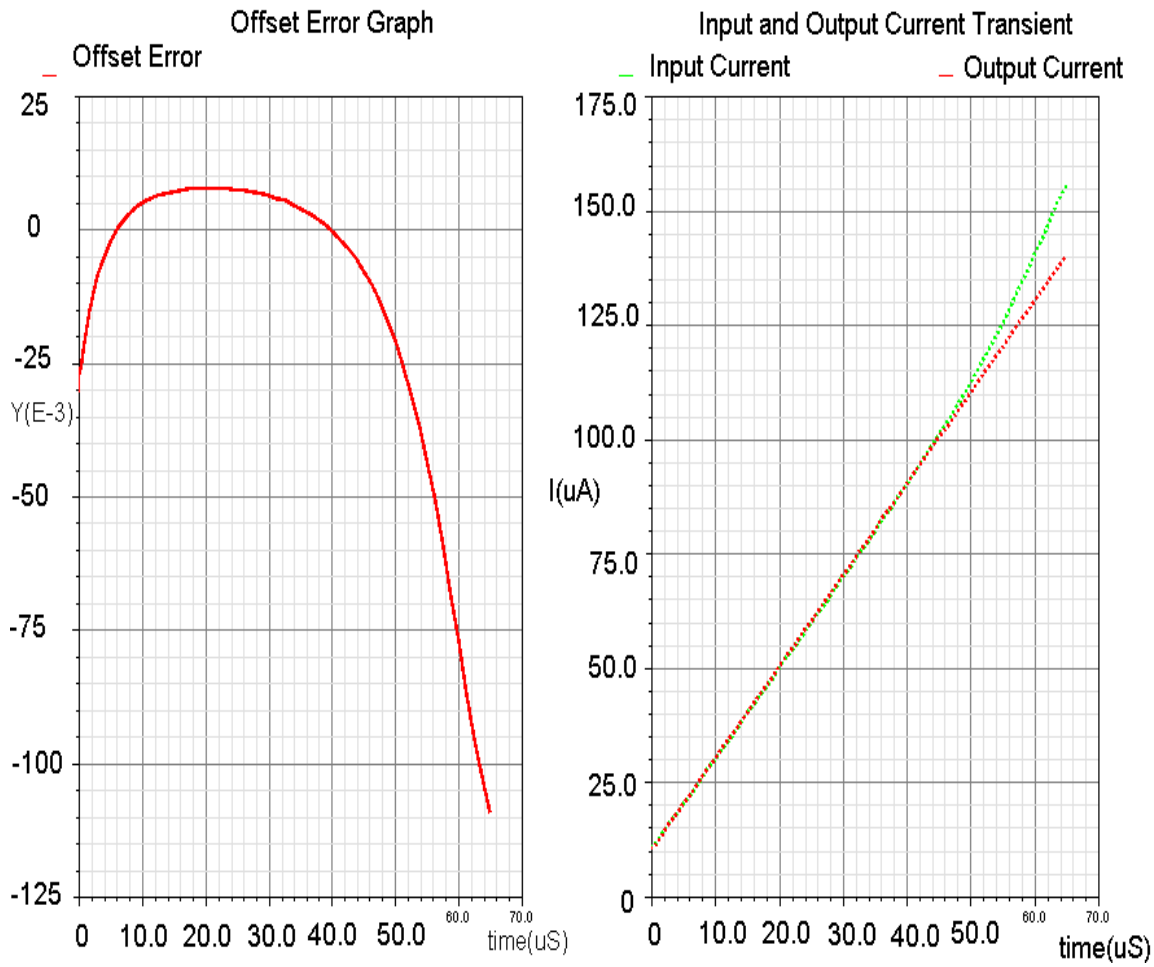


Figure 5–4: Transient of Input, Output Current and Error Percent

of the graph 5–6 around the 15uA value. In that graph, it is observed how the output current is getting closer to the value of the input current while the switches are changing. This supplies the necessary voltage to compensate the offset. After the system reaches a current with an acceptable offset value, the Digital Controller circuit remains in the actual state. In this case after 24μs the system reaches the less offset possible for that value. Figure 5–8 shows the difference between both currents. For determining the difference the equation 5.1 was used.

$$Difference = \frac{(InputCurrent - OutputCurrent)}{InputCurrent} \tag{5.1}$$

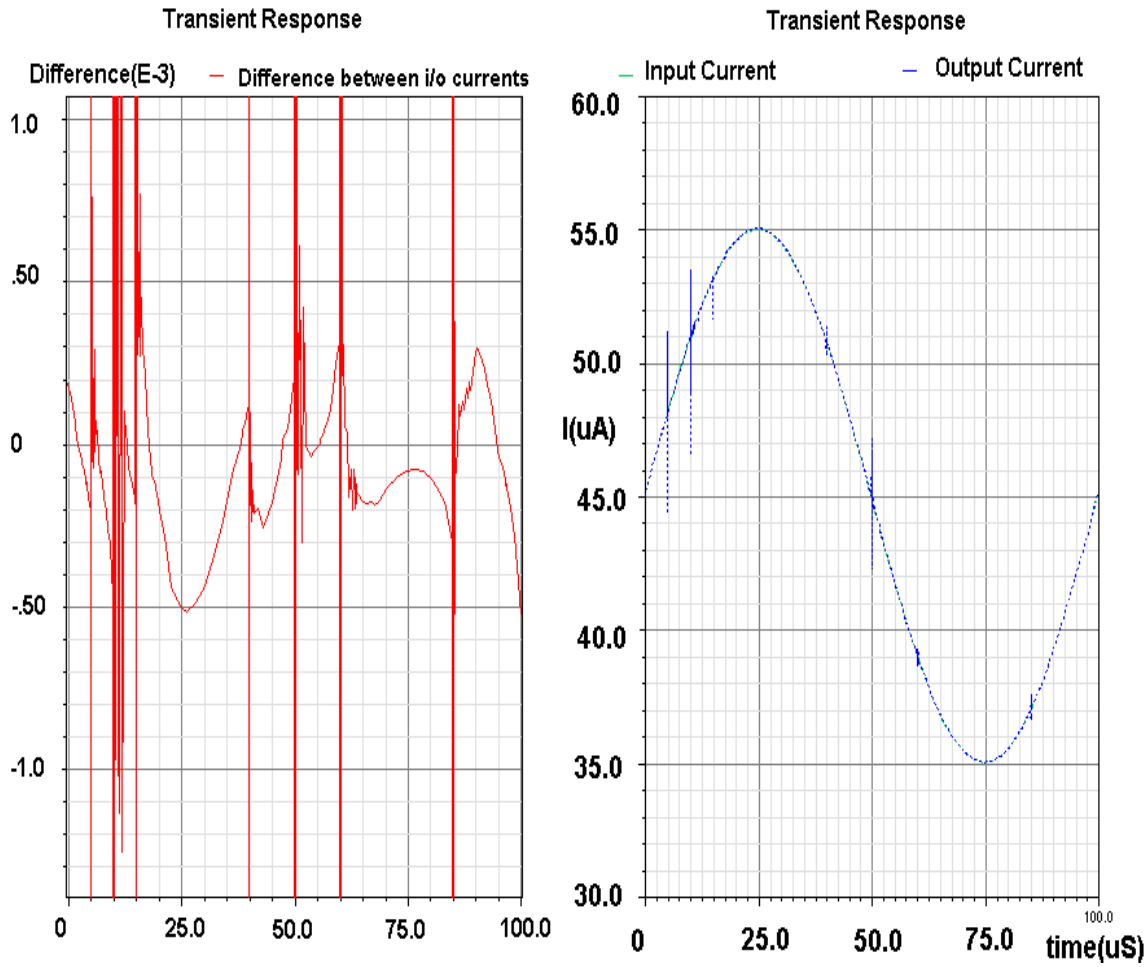


Figure 5–5: Transient of Input, Output Current with a Sinusoidal waveform

In figure 5–8 it is possible to observe that the error percent improve from -0.225% to 0.03%.

Under the same conditions the simulation for an input current of 70uA was made. In this case it took less time for the system reach the offset compensation point. Figures 5–9 and 5–10 present a transient simulations of input and output current. The only difference is that figure 5–10 presents a zooms of figure 5–9 centered around the 70uA value. The system was capable to compensate 100nA of offset. For this value the system only took 12us to reach the desired value.

Graph 5–11 shows the difference between input and output current. In that graph the system improves the current replica, because in terms of error percent, the system improves from an error percent of -0.14% to 0.02%.

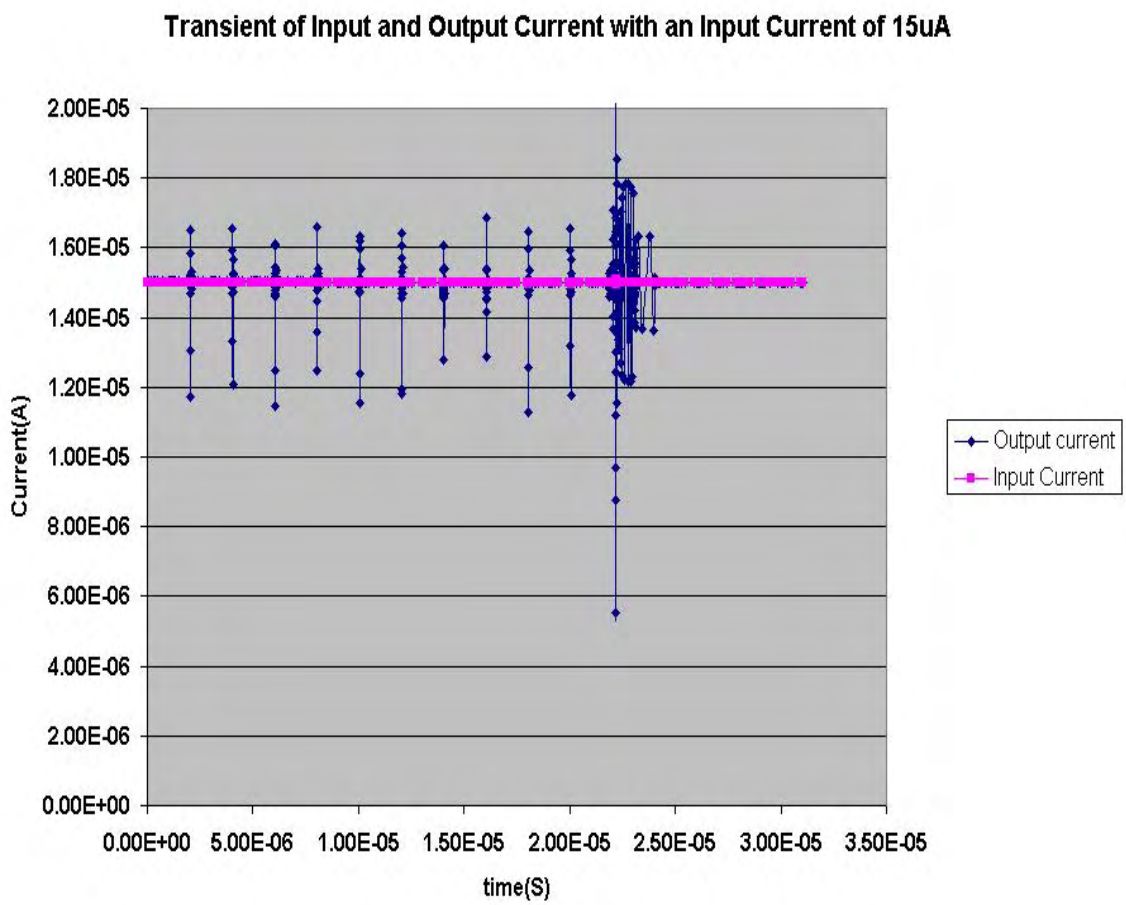


Figure 5–6: Transient of Input, Output Current with a DC value of 15uA

The graphs for the test circuit using input current of 135uA are presented in figures 5–12, 5–13 and 5–14. The graphs in figures 5–12 and 5–13 show the transient behavior of input and output voltage vs time. In this case the system compensate 250nA offset in the output current. Figure 5–14 shows the error percent graph. For this particular current, it shows a 0.03% error. This is the worst case scenario in terms of latency, because the circuit takes 32us to reach the point where the offset is compensated.

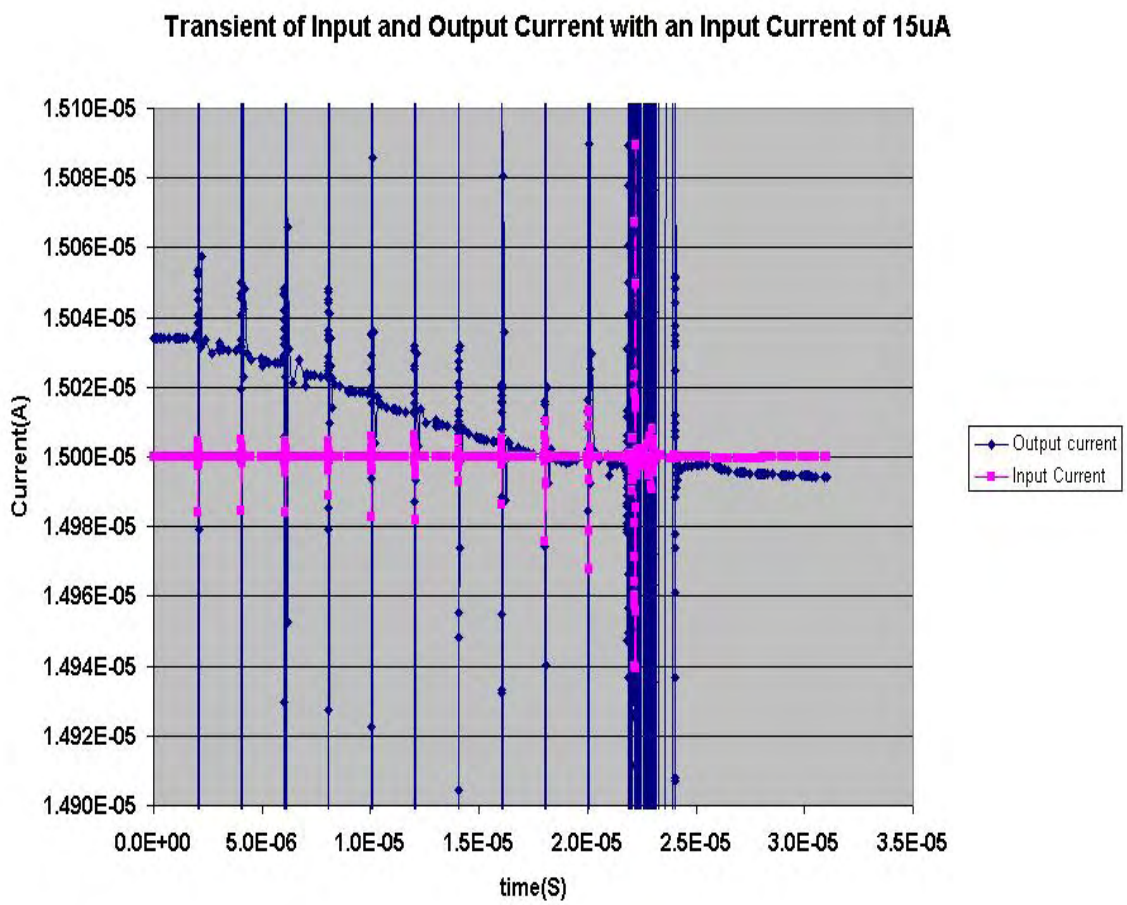


Figure 5–7: Zoom of the Transient of Input, Output Current with a DC value of 15uA

5.3 Simulations with Continuous Values

Last section presented results of the system proposed using DC values, this section presents results for continuous values. Due to the high input current range of the system, the tests was divided in parts, instead of running a complete simulation. There were two reasons for this, first the simulations are time consuming, and the amount of data obtained make small changes of offsets not readily observable.

Figure 5–15 shows a transient for the input and output currents where the input ramp goes from 14uA to 32uA in 185us. In this figure some spikes in the output current are observed when the switches change for one state to the other. This results from the digital controller doing iterations to control the switches that activates the

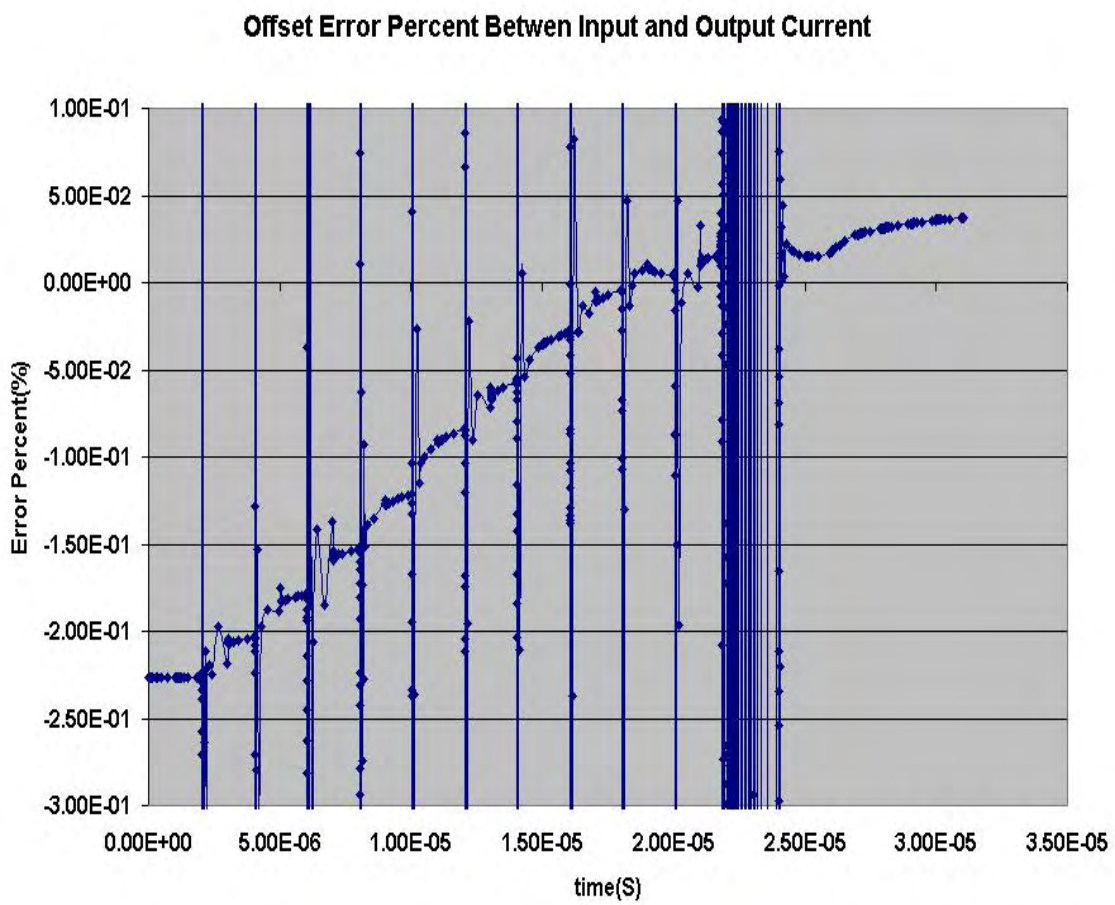


Figure 5–8: Difference of input and output Current

transistors in the Path A of the Biasing circuit. It reaches an acceptable error percent and remains in that state. Additional iterations of paths are made anytime the offset error is not acceptable.

Figure 5–16 shows the behavior of the system when the current ranges from 31uA to 41uA. It shows approximately the same behavior than the one in figure 5–15. It is important to notice that in figure 5–15 and 5–16 the fastest that an input signal can vary is 1.1uA each 10us. It also needs time to stabilize after the circuit reaches the acceptable offset point.

Figure 5–17 shows the transient behavior of the input and output currents ranging from 41uA to 65uA. This is the fastest input range that our circuit operates

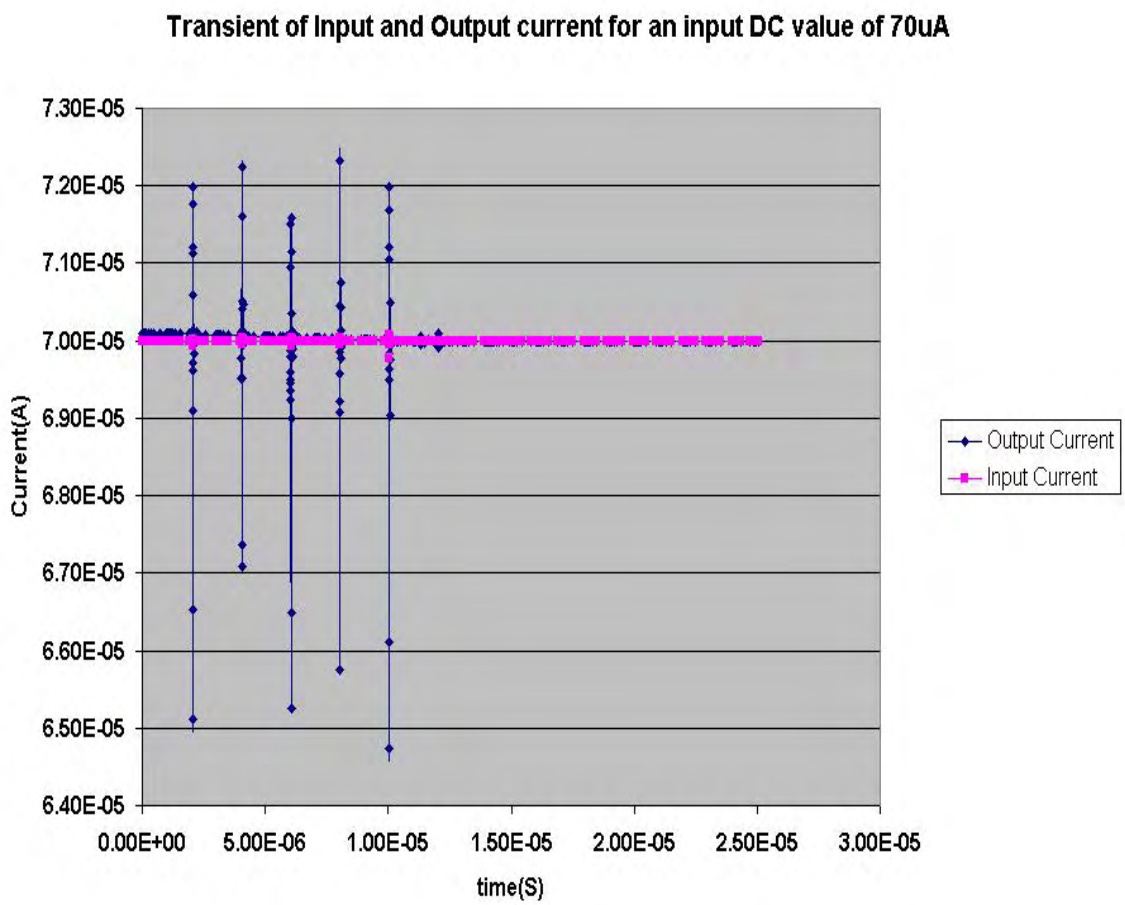


Figure 5–9: Transient of Input, Output Current with a DC value of 70uA

at higher speed. This graph shows a similar behavior to the previous graphs, with the difference that the variation of an input signal can be of 1.67uA each 10us.

Figure 5–18 and 5–19 show the behavior of the system having input current from 67uA to 78uA and from 76uA to 91uA. The behavior of the circuit is very similar to the one shown in the previous graphs.

Figure 5–20 presents the input and output currents. The current range is smaller than the ones shown before, goes from 91uA to 96uA. This graph shows that in this range the input signals needs to be significantly slower than the ones presented before. This is due to the fact that this input ranges approximately 2 times bigger than the operational current.

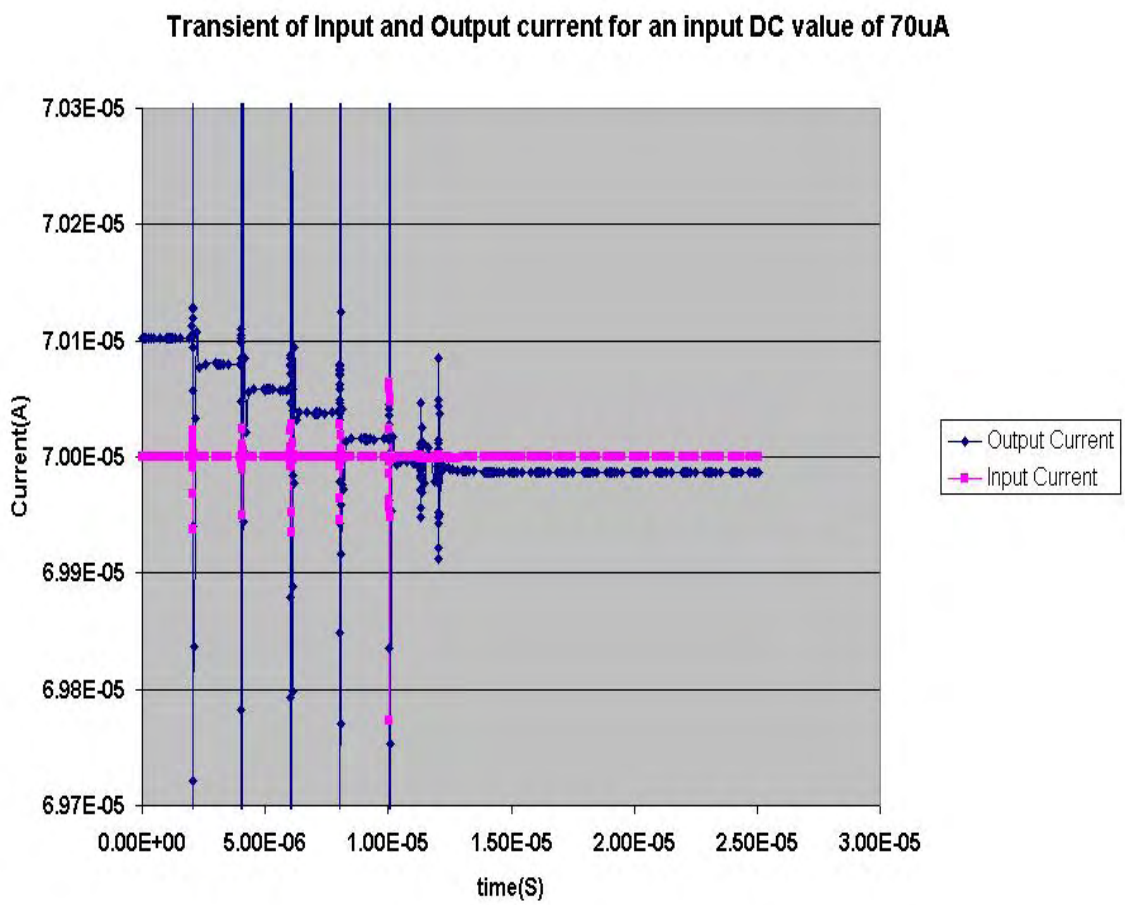


Figure 5–10: Zoom of the Transient of Input, Output Current with a DC value of 70uA

This circuit can be used for low frequency or DC values. But if the user wants to input continuous values, it is recommended that the input current would be lower than 100uA or increase the transistor sizes in the mirror.

A potential problem that can be seen in the proposed system is that for the current values where the switches are changing the systems becomes unstable.

To test this situation the system is supplied with an input current DC value of 41.3uA, this is the value where the switches in Path B changes of state. Results are shown in figure 5–21. System exhibits the same results that the ones shown in last section, a zoom of figure 5–21 is shown in figure 5–22, there the system was capable to compensate the offset even in the worst case scenario.

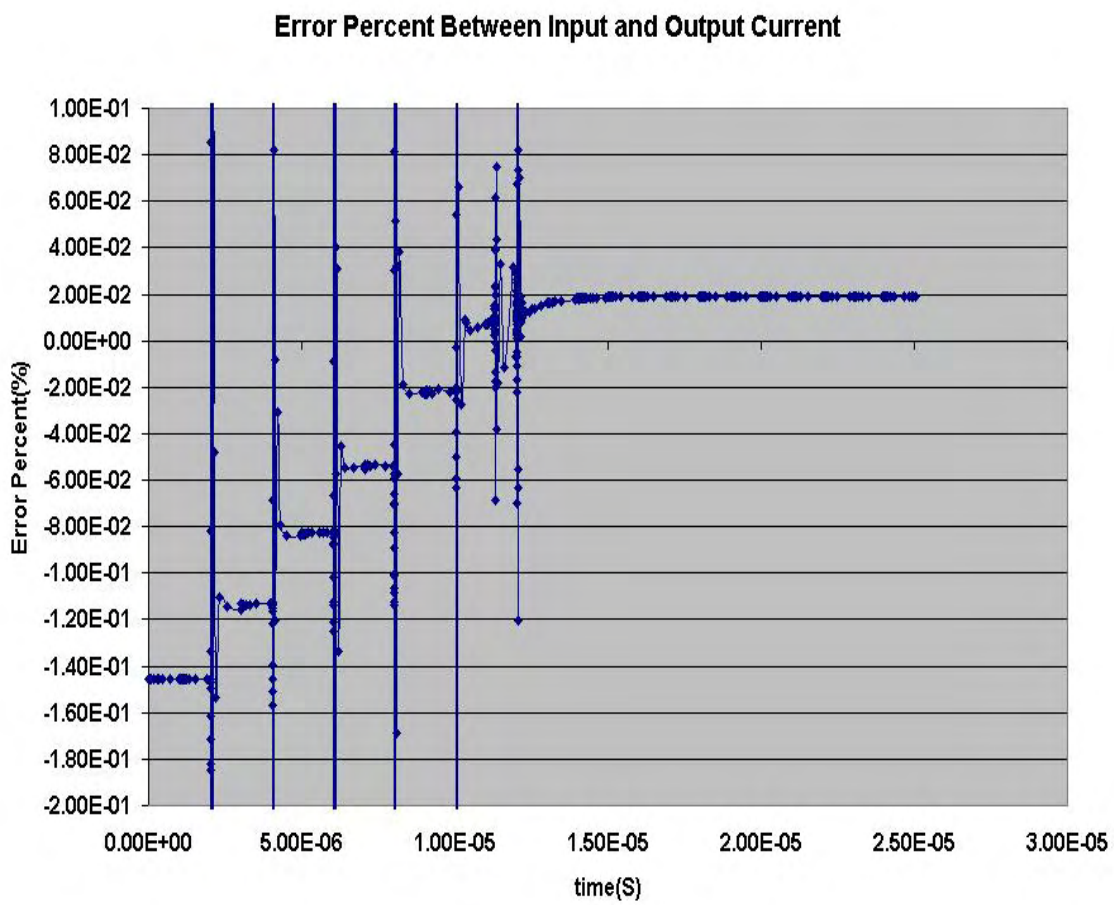


Figure 5–11: Difference of input and output Current

5.4 System Proposed Compared with Related Work

Last sections presented simulations of the system with DC and continuous values. This section presents a comparison of the system proposed versus related work. Table 5–1 presents the offsets error of our system compared with the ones in the literature. It is important to observe that the High-Performance Self-regulative CM has the better offset error percent, thus better accuracy.

It is important to consider that the proposed system makes significant improvements to the work presented in [10]. These improvements are not only in terms of offset compensation. Also the system proposed in this work has a higher range than the one presented [10] because that current mirror is design for an operational current of 150uA, which means that the size of the transistors are bigger. Its

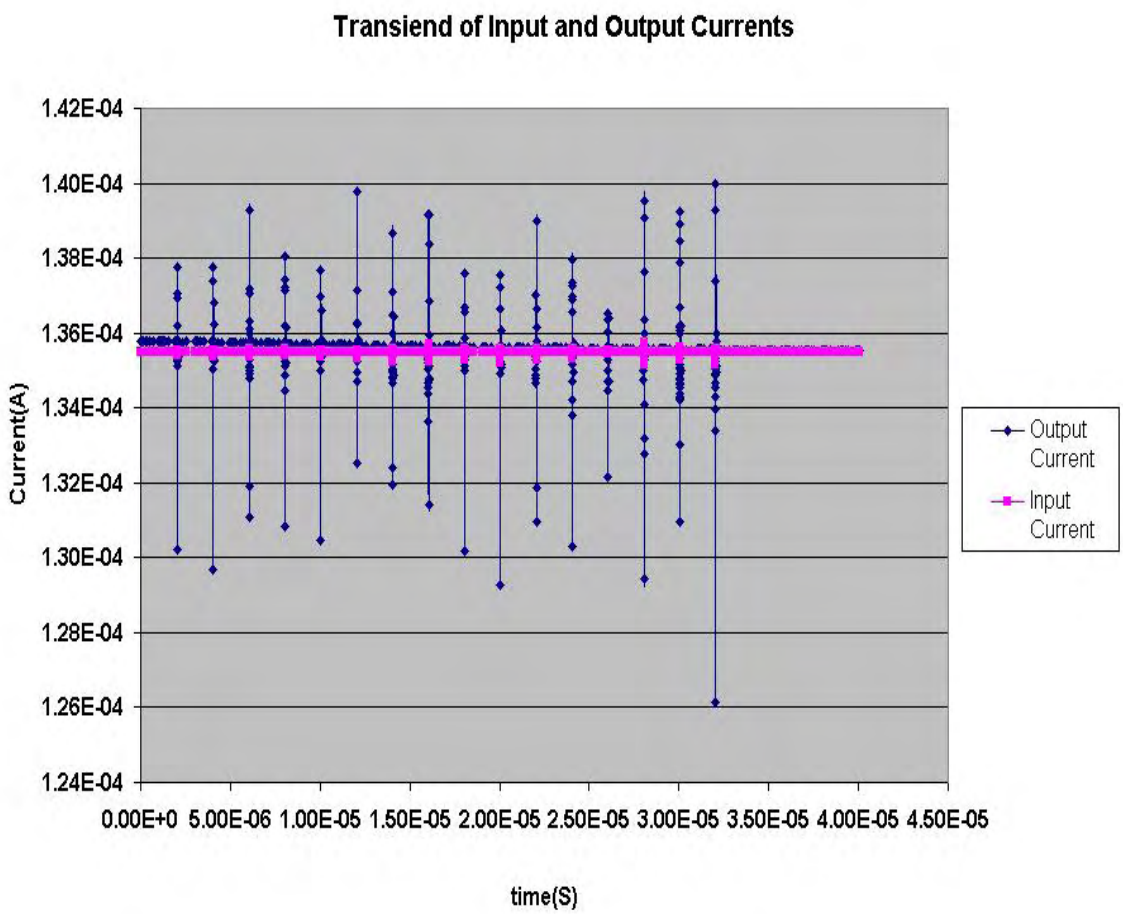


Figure 5–12: Transient of Input, Output Current with a DC value of 135uA

purpose is to minimize offset caused by transistor mismatch. Designing for V_{DSat} ($V_{DSat} = 0.2V$) the transistors in [10] are design optimally for a current of 150uA. This current mirror has a range from 10uA to 220uA. It is possible to observe that this range is doesn't goes much higher than the current operational point. The system proposed in this work was design for an operational current of 50uA, and it has a current input range that goes from 15uA to 135.5uA. This range compared with the operational point current and the size of the transistors is bigger than the one used in [10].

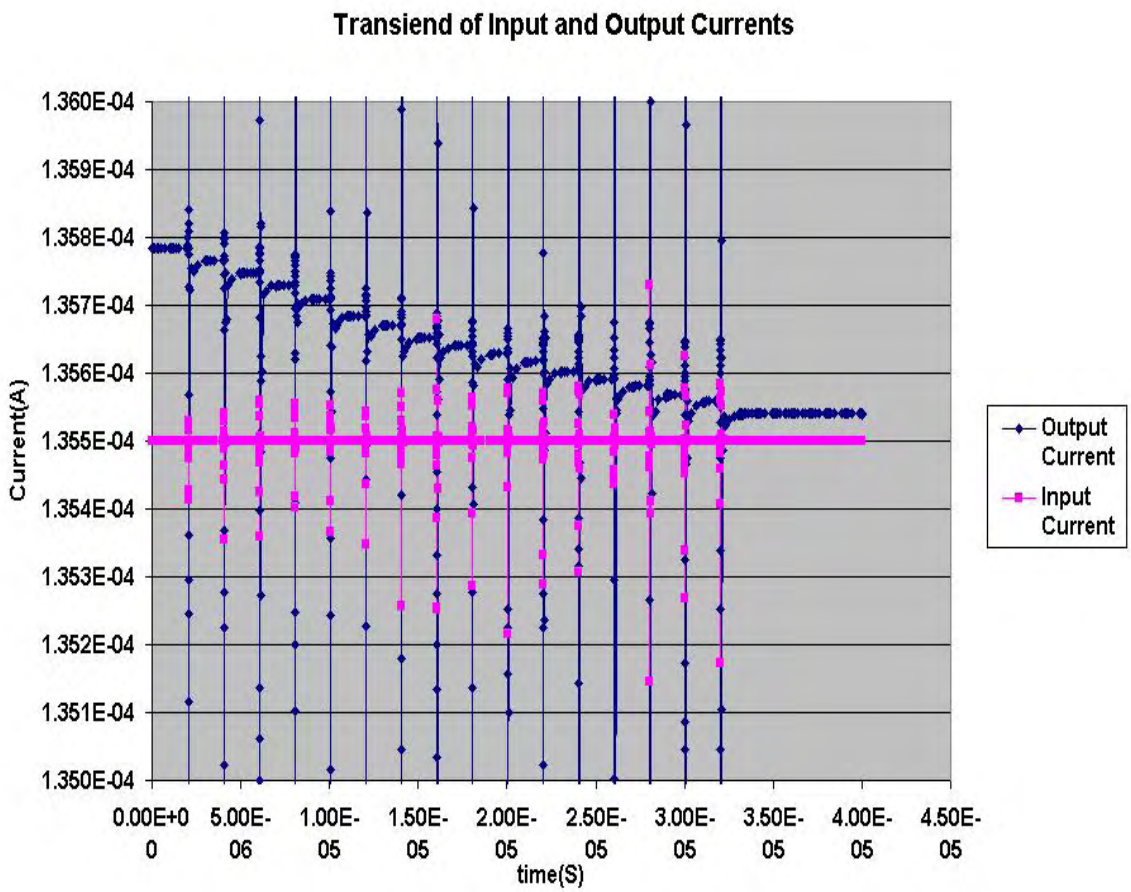


Figure 5–13: Zoom of the Transient of Input, Output Current with a DC value of 135uA

Table 5–1: Comparison of the System Proposed with Related Works

Device	Current Offset Percent of Error
Simple CM [16]	22.5%
Flipped Voltage Follower CM [16]	11.5%
Low-Voltage Cascode CM [16]	0.65%
Low-Voltage Dynamic Current Mirror [10]	0.05-0.1%
Series-Parallel Association Techniques CM [17]	0.33%
Proposed Circuit (High-Performance Autoregulative CM)	less than 0.05%

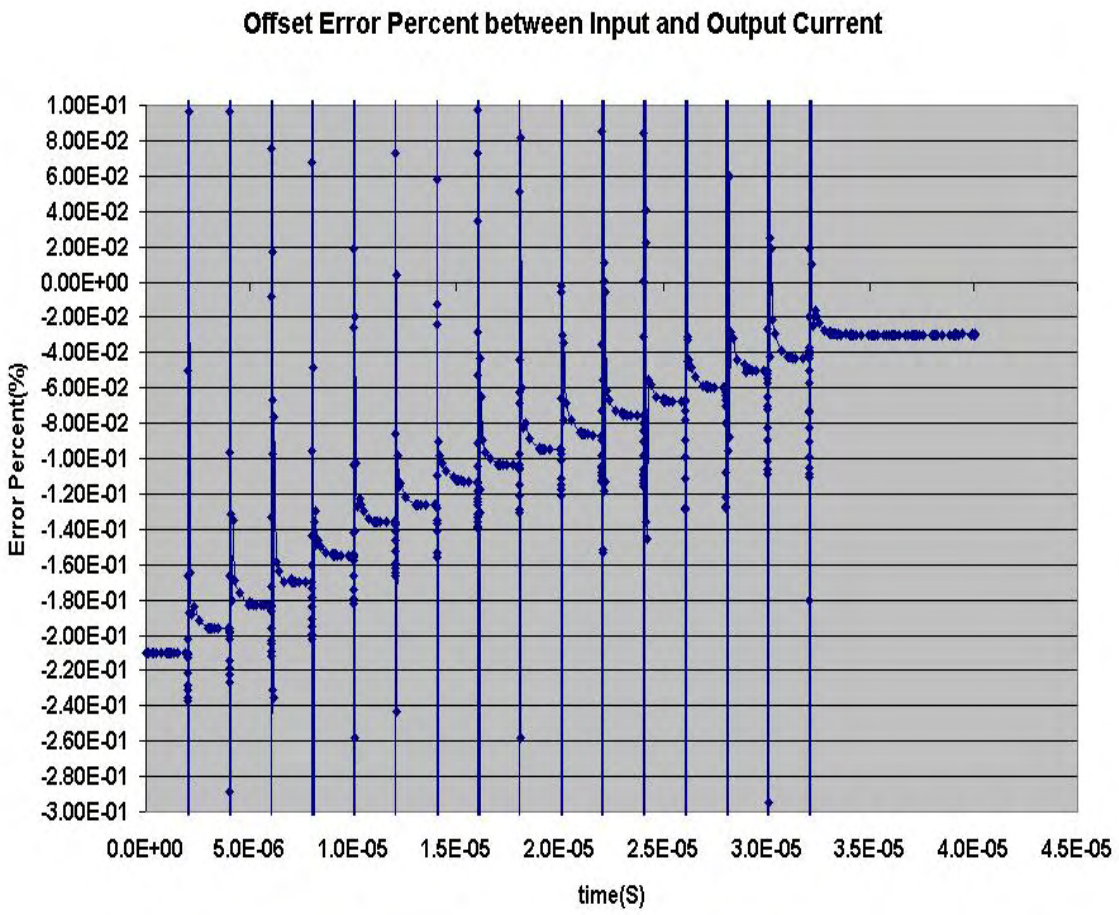


Figure 5–14: Difference of input and output Current

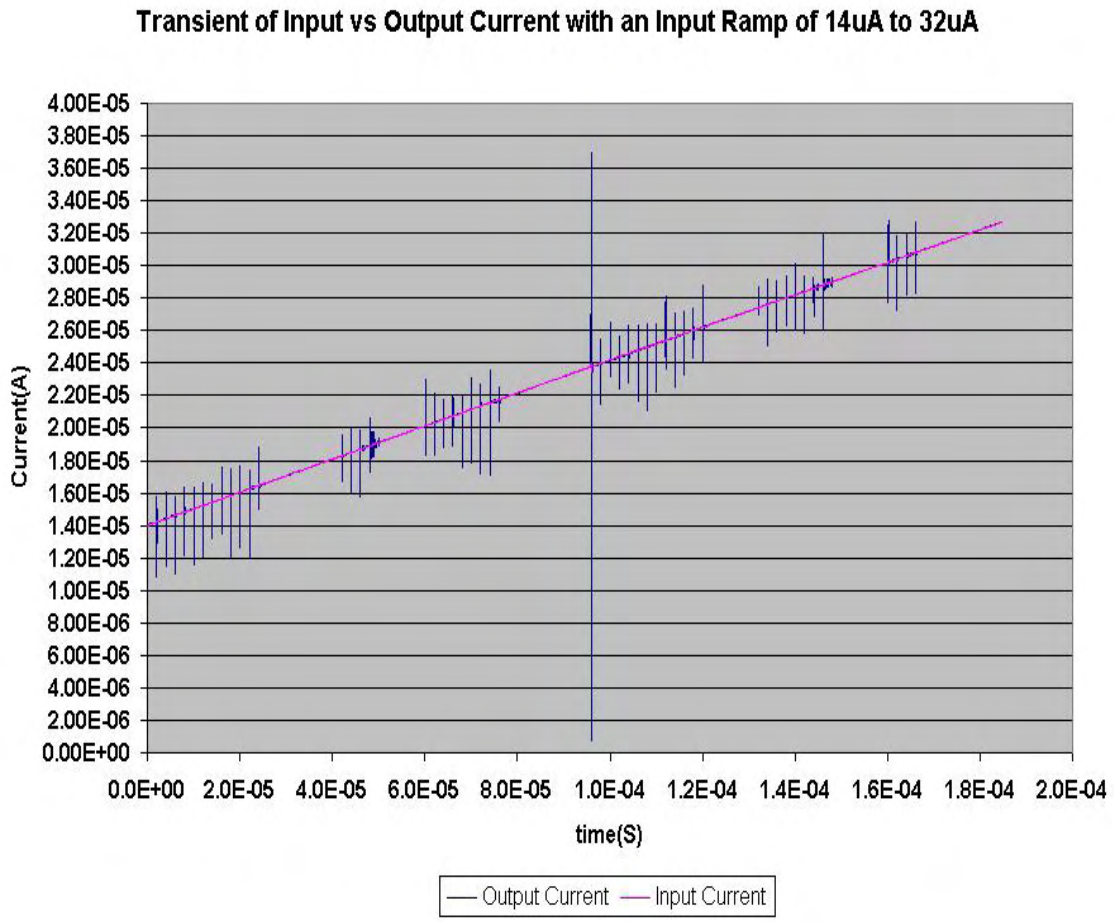


Figure 5–15: Transient of Input and Output Current for an Input Ramp from 14uA to 33uA

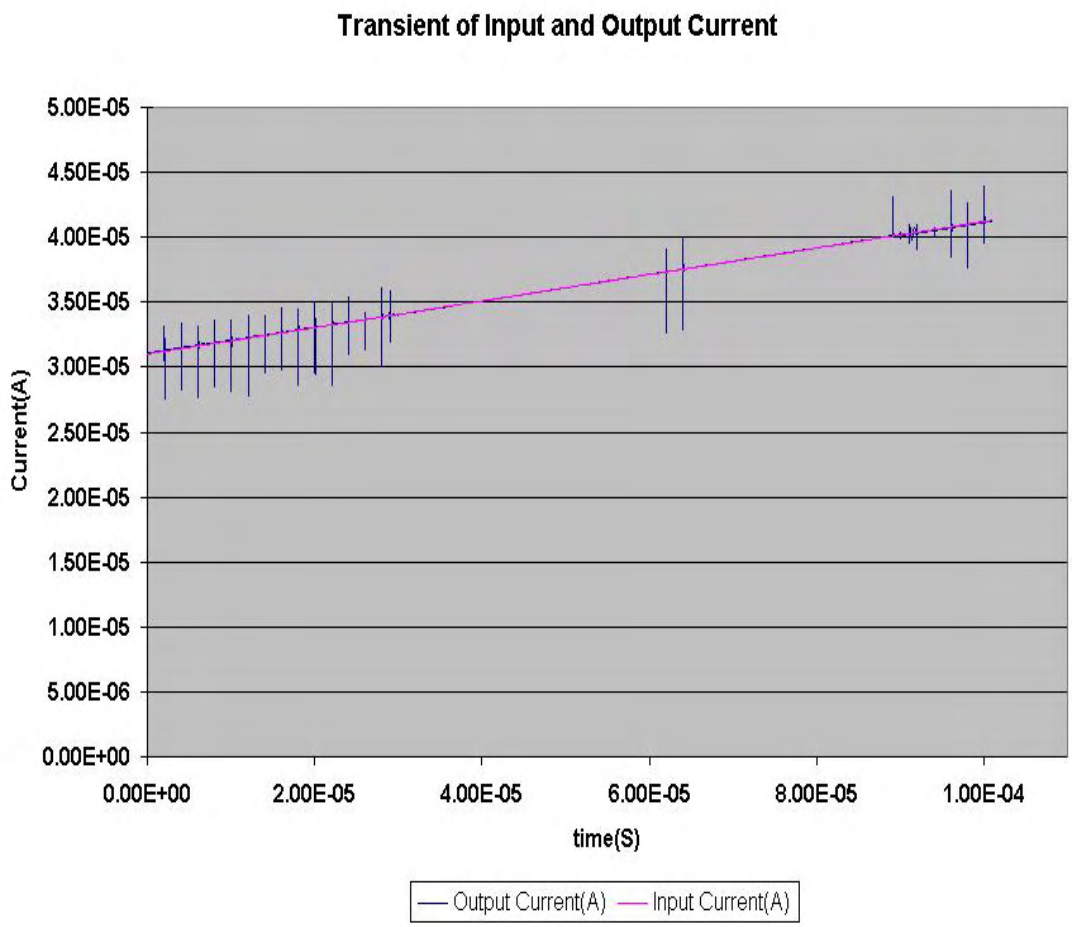


Figure 5–16: Transient of input and output current for an input ramp from 31uA to 41uA

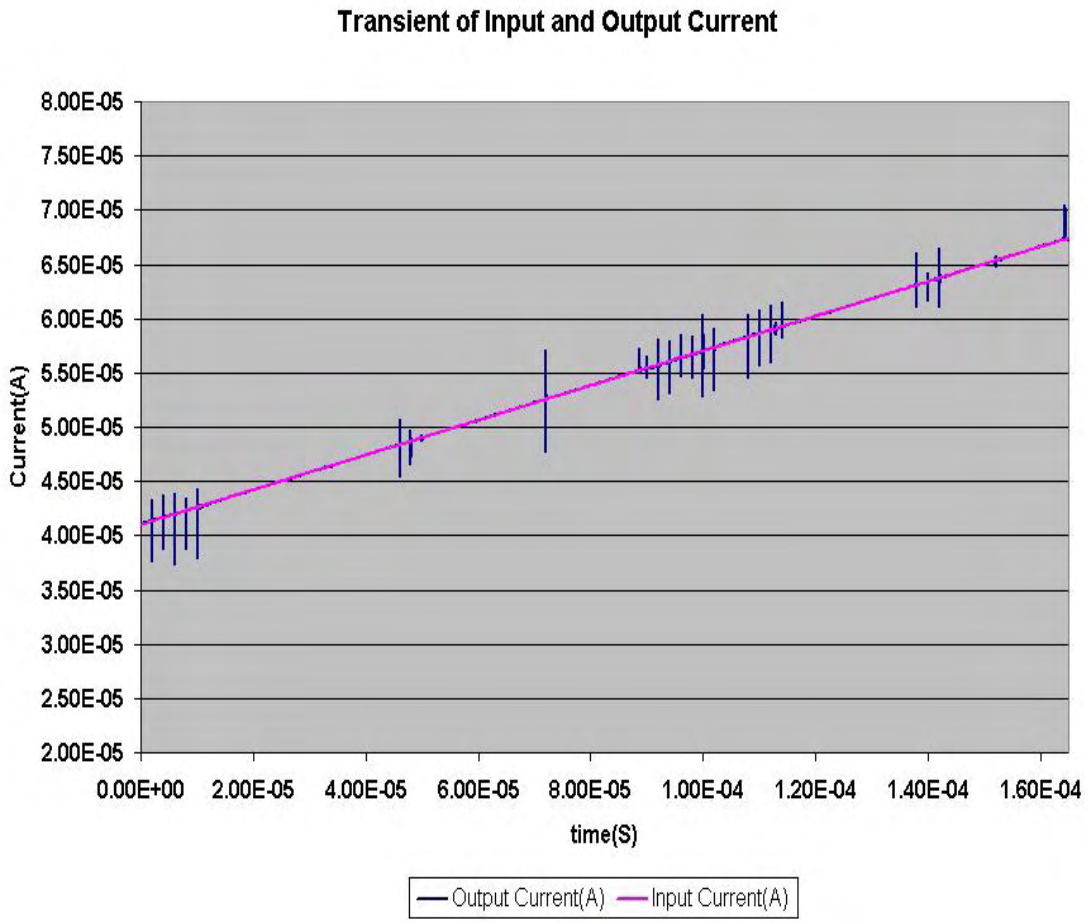


Figure 5–17: Transient of input and output current for an input ramp from 41uA to 67uA

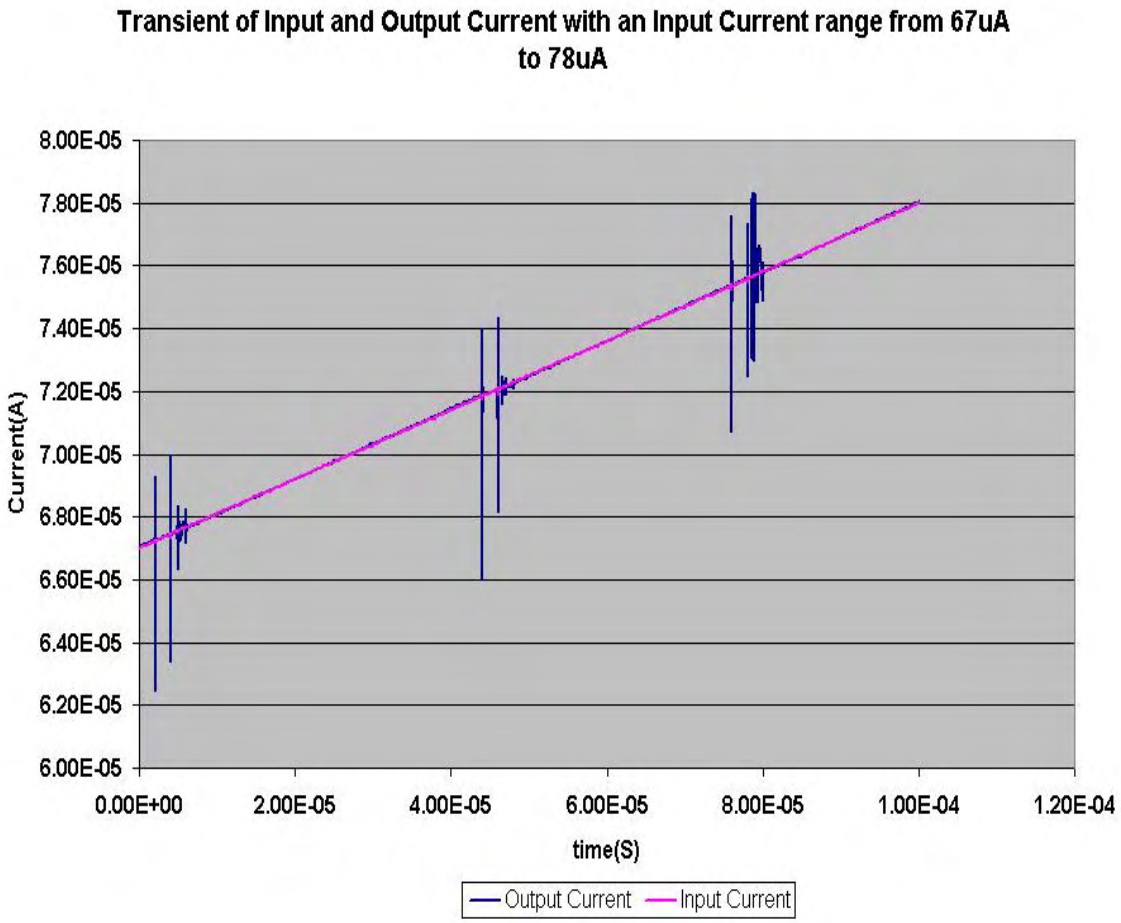


Figure 5–18: Transient of input and output current for an input ramp from 67uA to 78uA

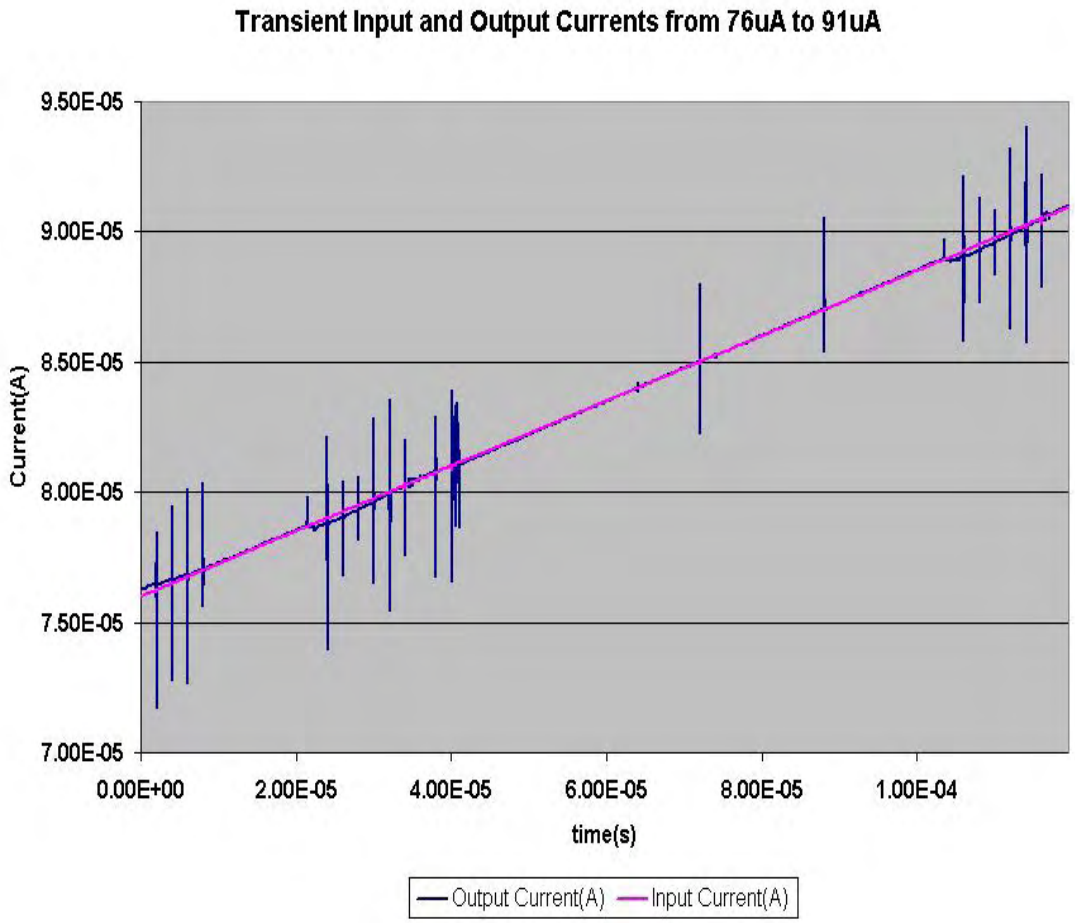


Figure 5–19: Transient of input and output current for an input ramp from 76uA to 91uA

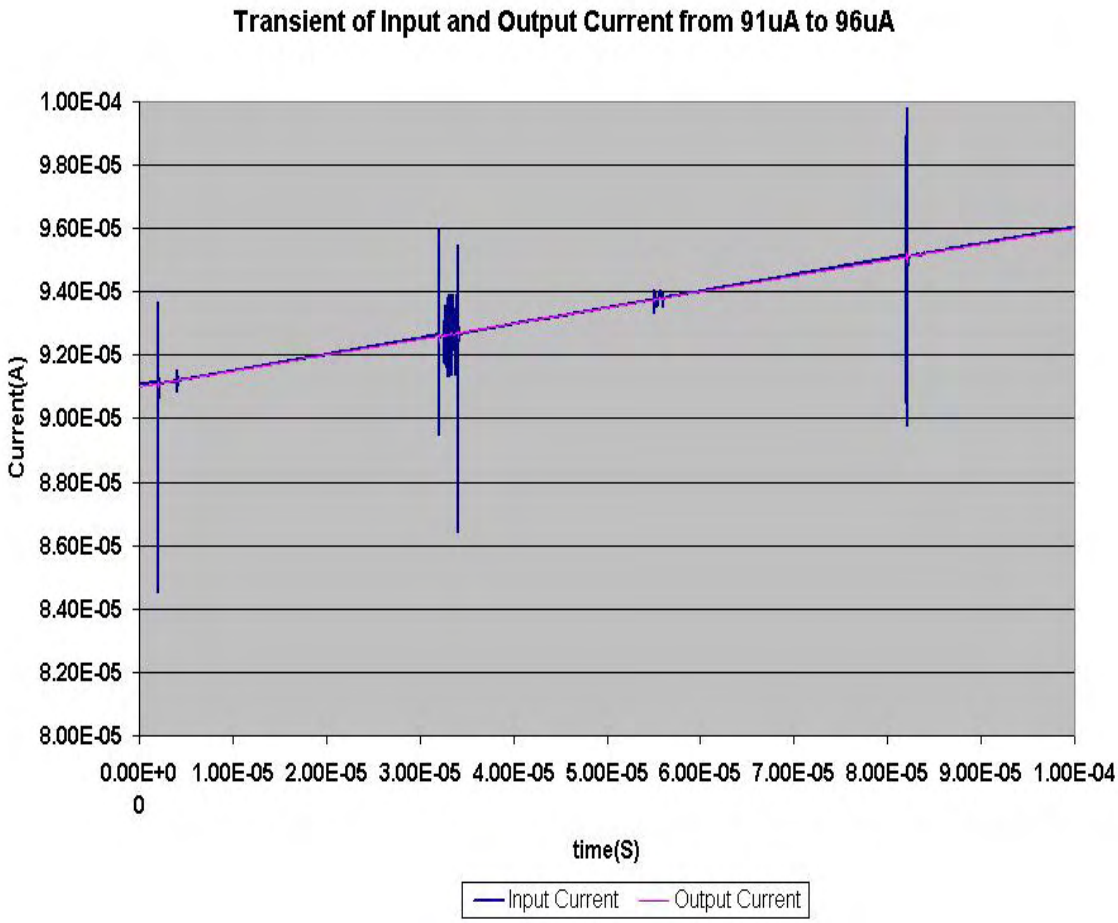


Figure 5–20: Transient of input and output current for an input ramp from 91uA to 96uA

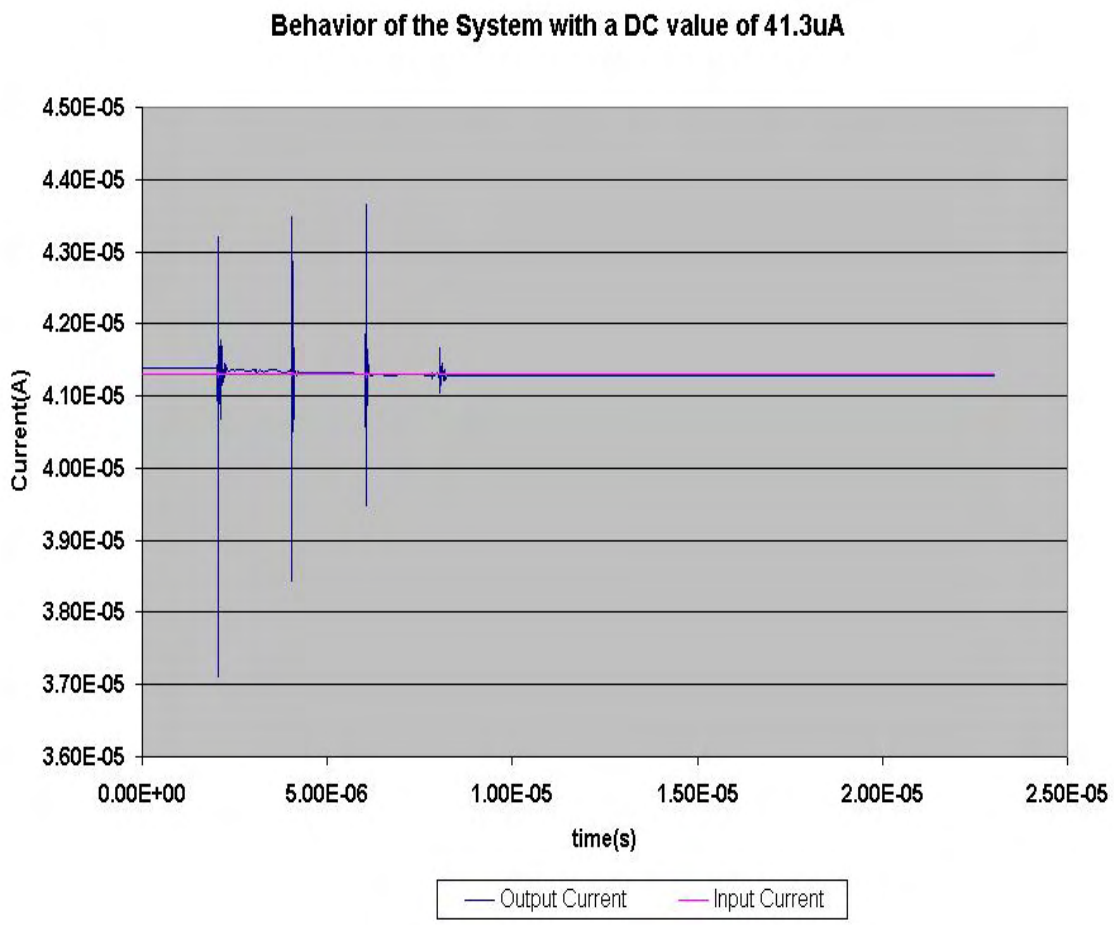


Figure 5–21: Transient of input and output current for an input current value of 41.3uA

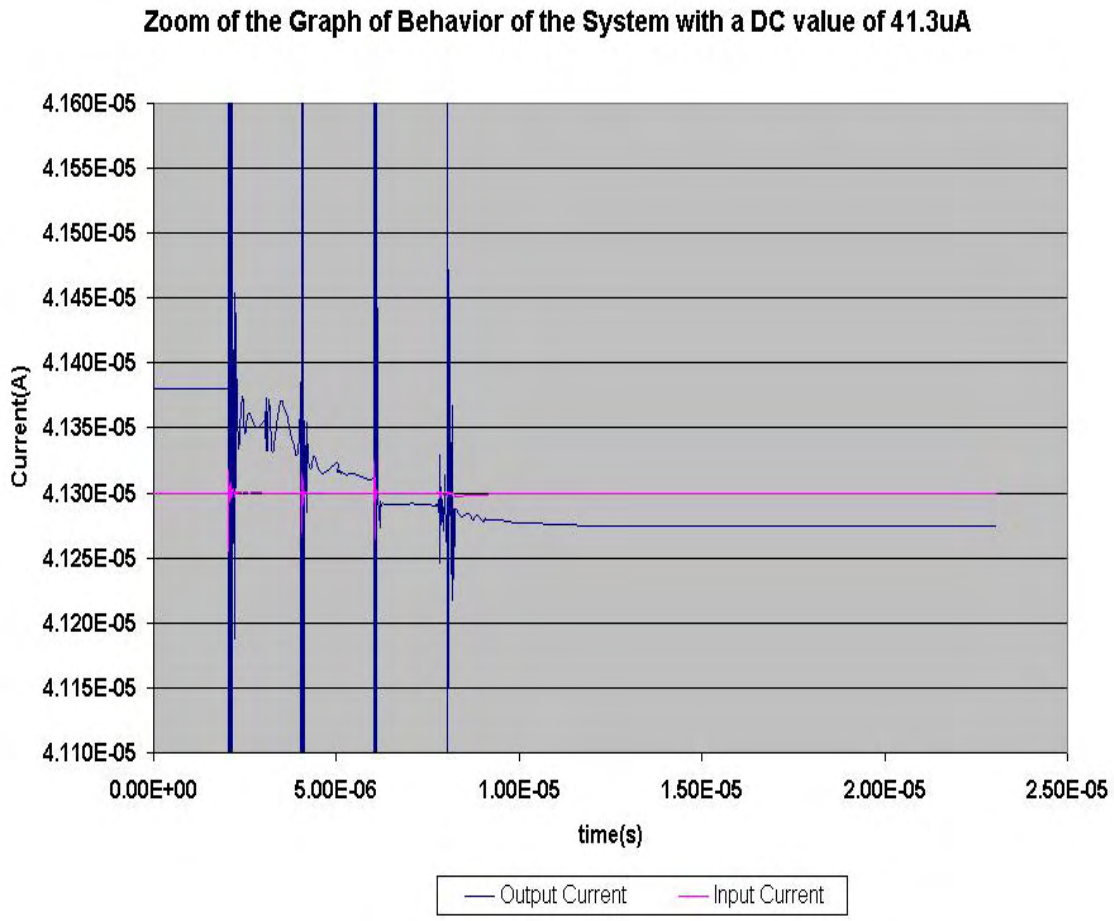


Figure 5–22: Zoom of the transient of input and output current for an input current of 41.3uA

CHAPTER 6
CONCLUSION AND FUTURE WORKS

The design of Current Mirrors is one of the most challenging aspects in the Analog and Mixed signal design. They are one of the most widely used building blocks in analog IC design. They are used as current sources and as active loads in many devices. The most important issue that this document addresses, is the offset in the current replica of the current mirror. As was exposed, this is one of the biggest challenges in the design of these devices.

The purpose of this work was to improve the accuracy of the current replica in the current mirror presented. The approach consists in dynamically controlling a biasing node to cope with changes in current input and reduce the offset. To test this approach the current mirror with one of the highest accuracy in literature was used. Results obtained yield that it is possible to use this kind of scheme because it reduces the offset error significantly. The system proposed here can be used for high precision applications, such as biomedical and instrumentation applications that works at KHz frequencies.

The area consumed by the design presented is significant if compared to simple and cascode current mirror, thus this design is recommended for applications that need high precision. Also this design is potentially immune to changes in technology process, because it is able to correct the offset that the circuit can have due to parameter mismatch in the process fabrication.

6.1 Future Works

In terms of future work the principal improvement can be in the in the implementation of a more efficient search algorithm in the digital controller for example a binary search. This can potentially make the system work faster than with the algorithm that it currently has, reducing the time where the system finds the correct switch for the value of current.

Other possible improvement that can be pursued is to have a better architecture for the operational amplifiers so it will not limit the bandwidth of the system

APPENDICES

APPENDIX A
SOURCE ABSORPTION THEOREM

The source absorption [2] theorem has two dual forms: the voltage source absorption and the current source absorption theorems.

The voltage source absorption theorem establishes that if, in on branch of the circuit with current I, there is a voltage source controlled by I, the source can be replaced by a simple impedance with value equal to the source controlling factor.

The demonstration is trivial. An impedance Z where a current I flows originates the same voltage drop the I source generates at its terminals. See A–2

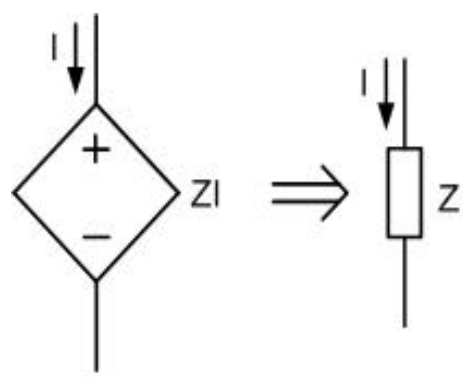


Figure A–1: Figure 1

The current source absorption theorem establishes that if , in one branch of the circuit there is a voltage source submitted to a voltage V and controlled by it, the source can be replaced by a simple admittance with value equal to the source controlling factor.

The demonstration is again trivial. An admittance Y submitted to a voltage V imposes the same current that the source YV provides.

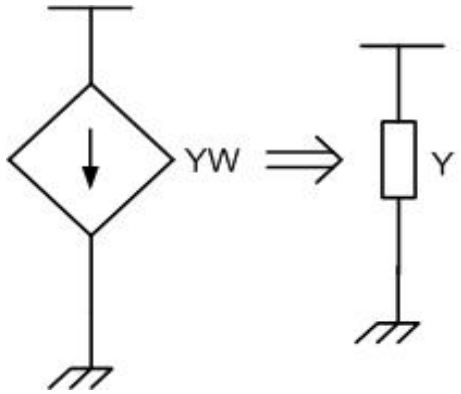


Figure A–2: Figure 2

APPENDIX B
TRANSISTORS SIZES

Table B–1: Cong-Geiger Current Mirror Transistors Dimensions

Device	Dimensions
M1-M9, M11,M14-M16	$\frac{22\mu m}{1.05\mu m}$
M10	$\frac{21.3\mu m}{1.05\mu m}$
M12	$\frac{20.8\mu m}{1.05\mu m}$
IBias	$5\mu A$
Iin	$10\mu A - 140\mu A$
PMOS Current Sources Transistors	$\frac{66\mu m}{1.05\mu m}$

Table B–2: Size of Transistors in Biasing Circuit

Device	Dimensions
NMOS	$W = 22\mu m$, $L = 1.05\mu m$
PMOS	$W = 66\mu m$, $L = 1.05\mu m$
Ireff	$80\mu A$
IBias	$5\mu A$
15 NMOS Transistors Path B	from $W = 2.9 to 4.2\mu m$, $L = 0.6\mu m$, intervals of 2λ
17 PMOS Transistors Path A	from $W = 55 to 112\mu m$, $L = 0.6\mu m$, intervals of $3\mu m$

Table B–3: Operational Amplifier Transistor Dimensions

Device	Dimentions
M0,M1	$W = 22\mu$ $L = 1.05\mu$
M3,M4	$W = 66\mu$ $L = 1.05\mu$
M2	W = 43.95μ $L = 1.05\mu$
M5-M7	$W = 132\mu$ $L = 1.05\mu$
Ireff	$100\mu A$

Table B–4: Comparator Transistors Dimensions

Device	Dimentions
M1, M2, M3, M4, M5	$W = 22\mu$ $L = 1.05\mu$
M6, M7, M8, M9	$W = 66\mu$ $L = 1.05\mu$
Vbias	1.4V
Ibias	$5\mu A$

Table B–5: Size of Transistors in Path Selector Circuit

Device	Dimensions
NMOS	$W = 66\mu m$, $L = 1.05\mu m$
PMOS	$W = 49.45\mu m$, $L = 1.05\mu m$
Ireff	$100\mu A$

Table B–6: Size of Transistors in Range Generator Circuit, Gain Stage

Range	Gain	Transistor Size(NMOS)
1	0.25	$W = 13.65\mu m$, $L = 1.05\mu m$
2	0.41	$W = 20.25\mu m$, $L = 1.05\mu m$
3	0.56	$W = 26.25\mu m$, $L = 1.05\mu m$
4	0.68	$W = 30.9\mu m$, $L = 1.05\mu m$
5	0.80	$W = 35.55\mu m$, $L = 1.05\mu m$
6	0.9	$W = 39.6\mu m$, $L = 1.05\mu m$
7	0.97	$W = 42.25\mu m$, $L = 1.05\mu m$
8	1.03	$W = 45\mu m$, $L = 1.05\mu m$
9	1.07	$W = 47.25\mu m$, $L = 1.05\mu m$
10	1.11	$W = 49.2\mu m$, $L = 1.05\mu m$
11	1.15	$W = 51\mu m$, $L = 1.05\mu m$
12	1.20	$W = 52.95\mu m$, $L = 1.05\mu m$
13	1.25	$W = 55.05\mu m$, $L = 1.05\mu m$
14	1.30	$W = 57\mu m$, $L = 1.05\mu m$

APPENDIX C
LAYOUTS C

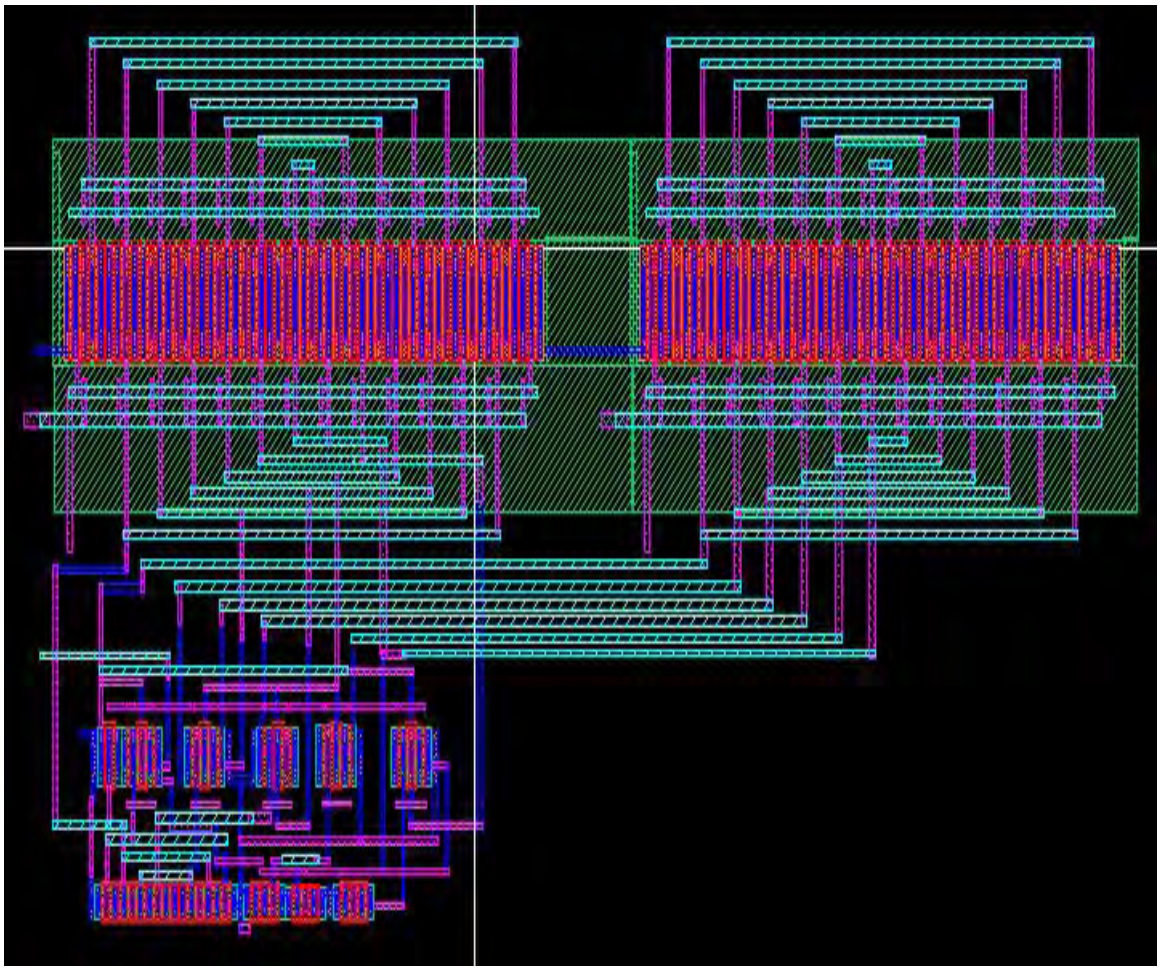


Figure C–1: Self-Biasing Cascode Current Mirror Layout

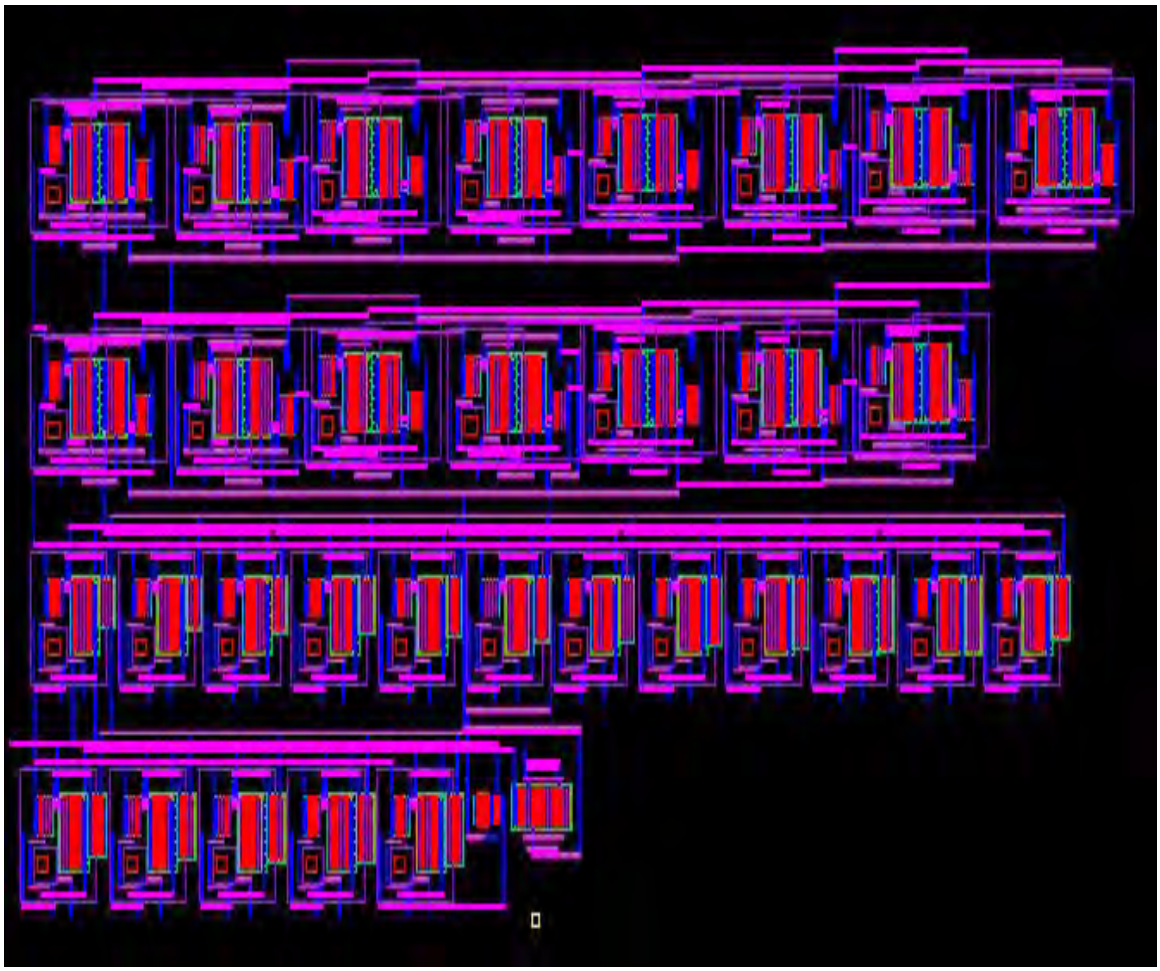


Figure C–2: Biasing Circuit Layout

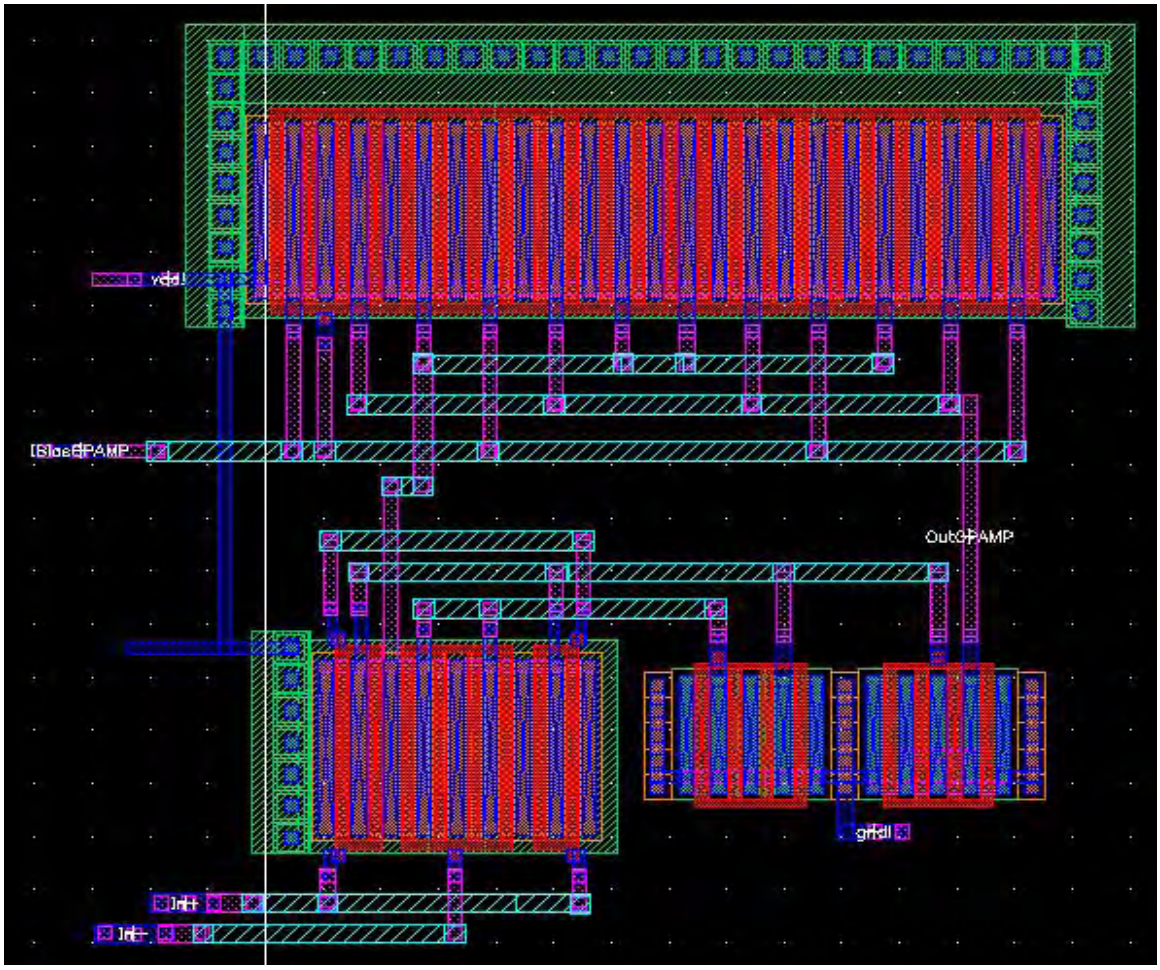


Figure C–3: OPAMP Layout

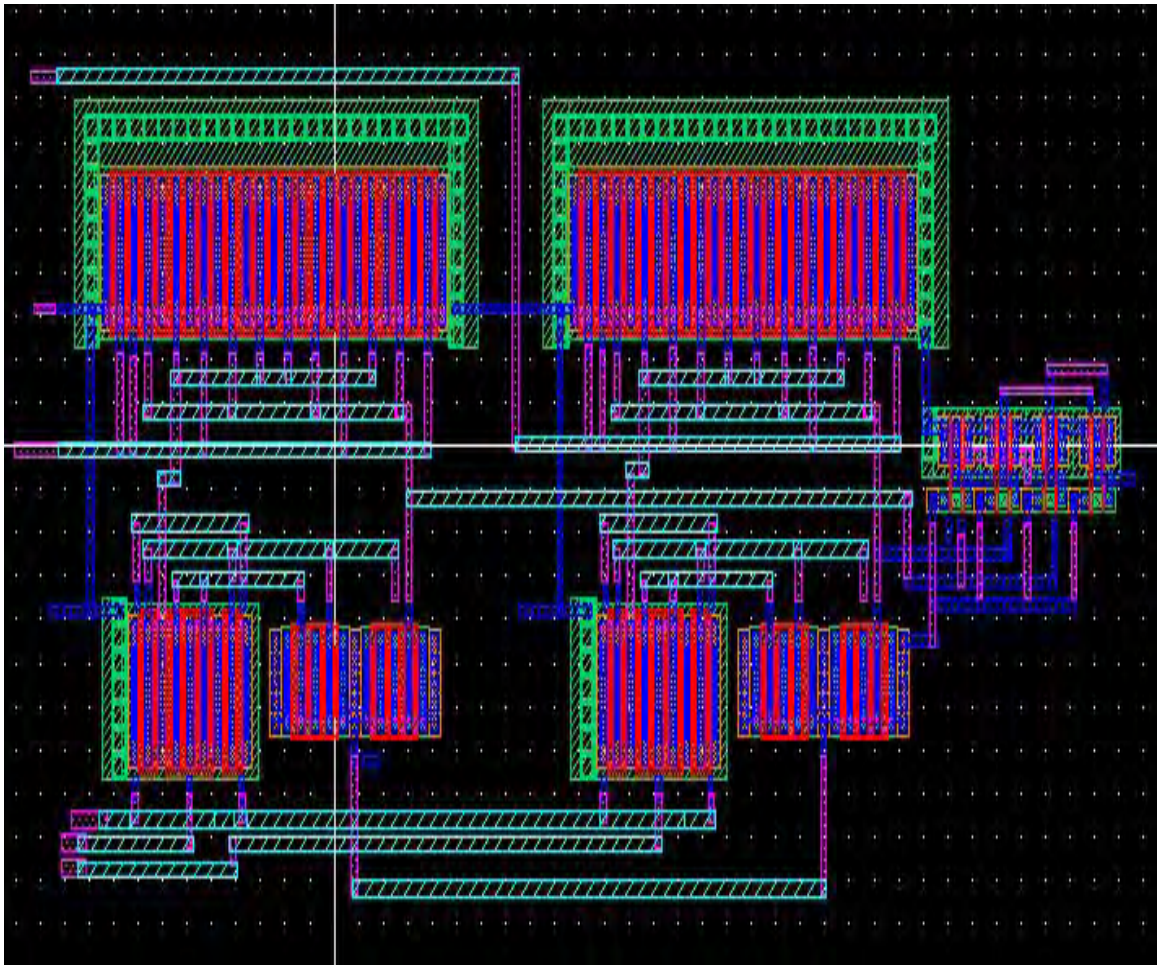


Figure C–4: Window Detector Layout

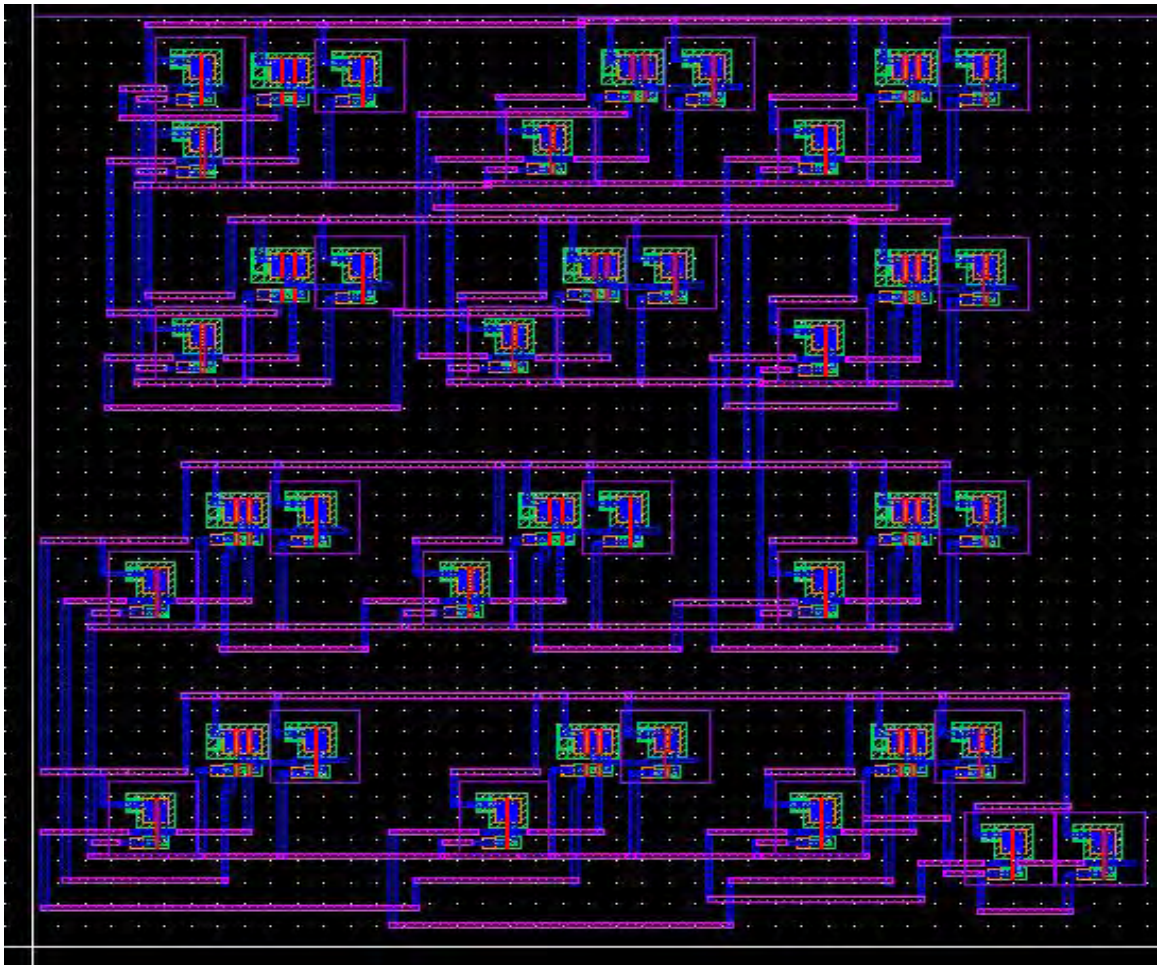


Figure C–5: Decoder Layout

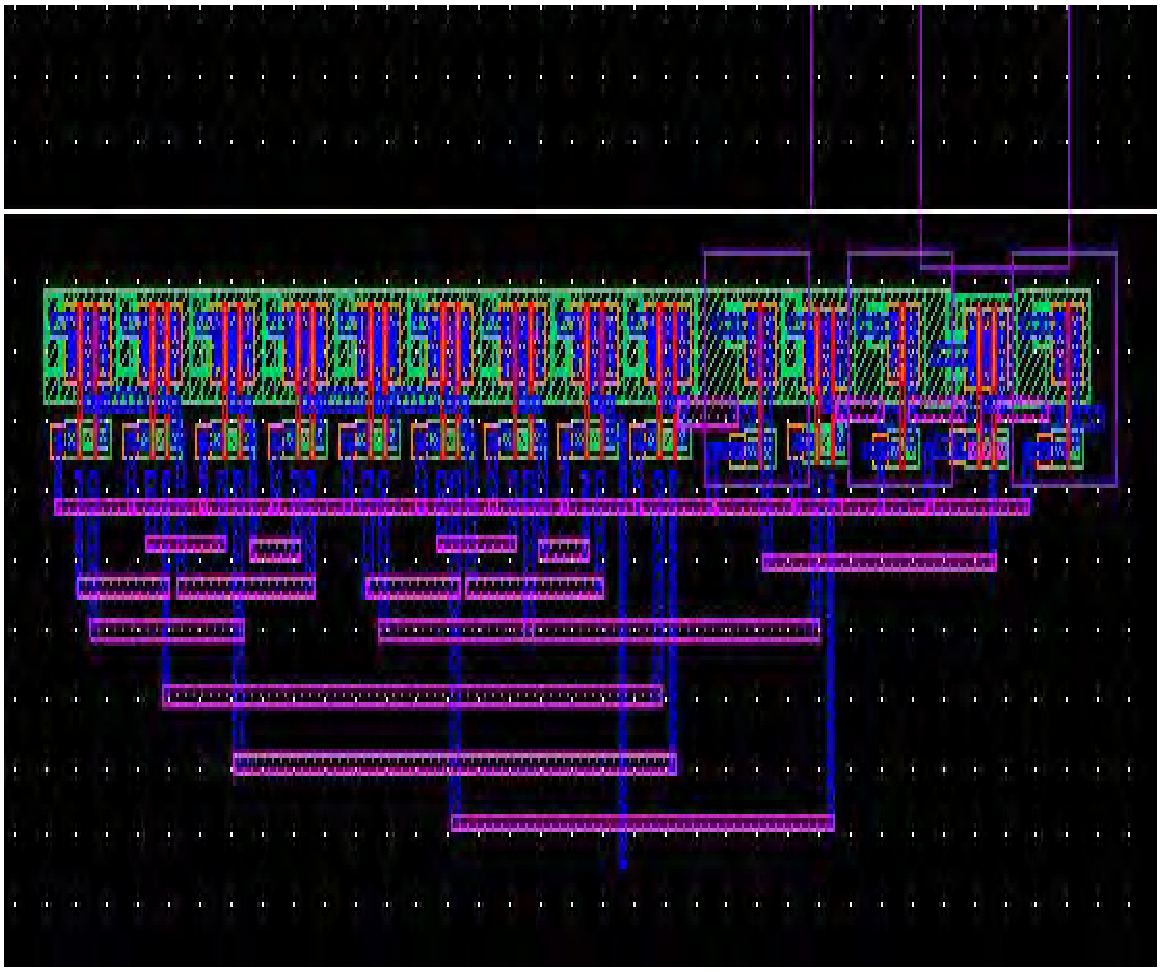


Figure C–6: 1 Bit Adder Layout

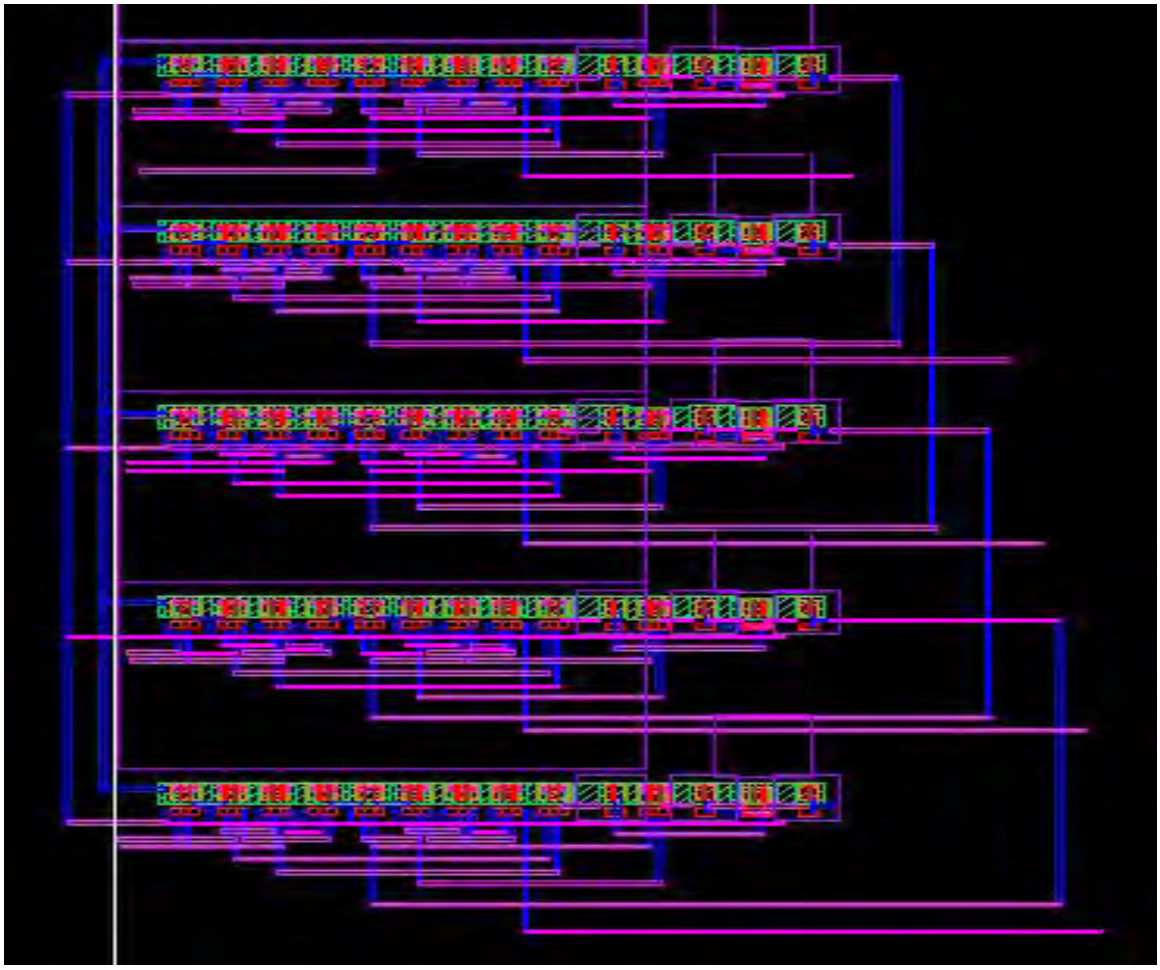


Figure C–7: 5 Bits Adder Layout

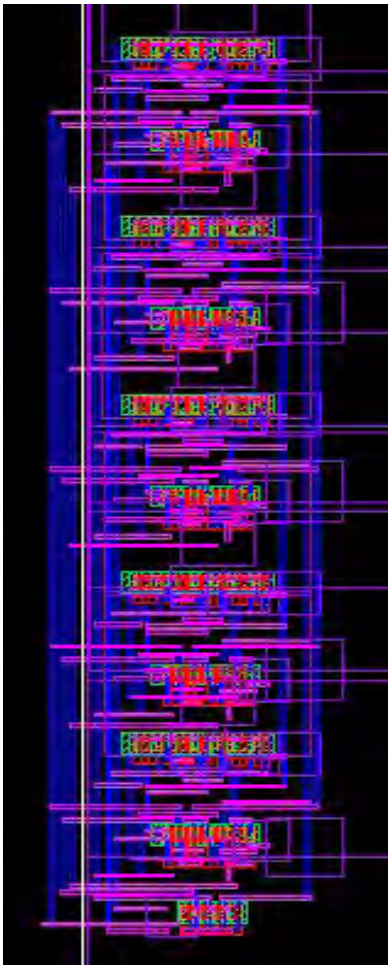


Figure C–8: 5 Bits Registers Layout

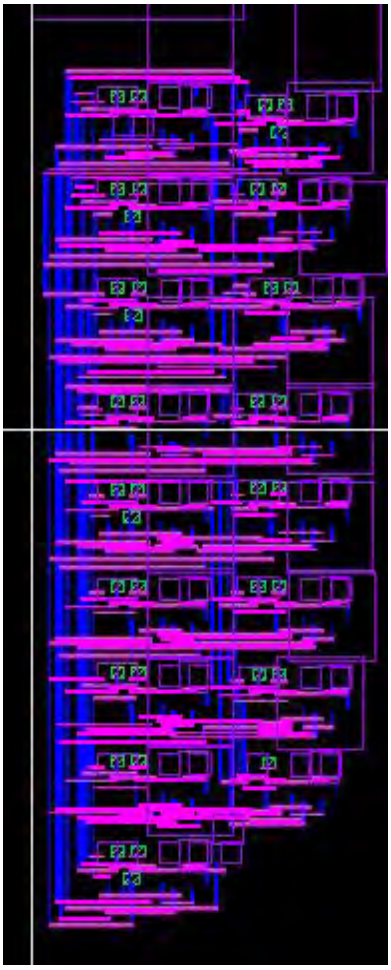


Figure C–9: 16 Bits Decoder Layout

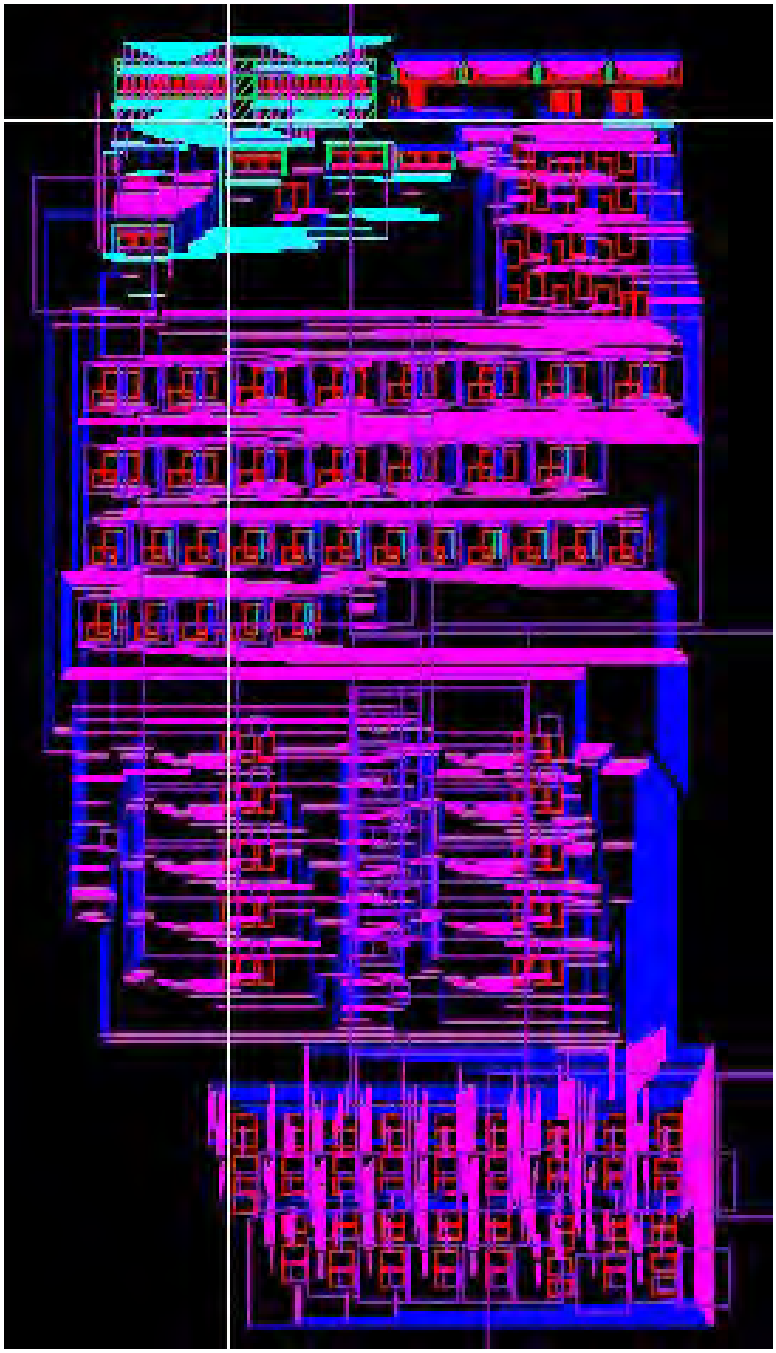


Figure C–10: Complete System Layout

APPENDIX D
DEFINITIONS

Bias Supply a transistor the necessary voltage for stay on or in the operation region that is needed

Cascode Put a transistor over other one connecting the drain of one with the source to the other one

Offset Difference of current or voltage between two signals

Sensitivity Smaller current step that a current comparator can detect to change of state.

Self-Biasing A system that has the capability to supply itself with the biasing voltage necessary using the input conditions.

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BIOGRAPHICAL SKETCH

Laura Elena Sánchez González was born was born in September 18 of 1981 in Havana City, Cuba. Laura is the daughter of Juan Rafael Sánchez Alvarez and Marta González Paz. In December of 2004 she received the Bachelor of Science in Computer Engineer degree from University of Puerto Rico, Mayaguez Campus. In January 2005 she started the M.E studies in Electrical Engineer, at the same university, in the area of Electronic, under the supervision of Professor Gladys O. Ducoudray-Acevedo, PhD.

HIGH-PERFORMANCE SELF-REGULATING SELF-BIASING CASCODE CURRENT MIRROR

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Chair: Gladys Omayra Ducoudray Acevedo
Degree: Master of Engineering
Graduation Date: 2007

Current Mirrors are one of the most important building blocks in Analog IC Design. They are widely used in all analog and mixed-signal, specially in Data Converters. The most important goal in the design of these devices is the accuracy of the current replica. There exists some schemes of current mirrors that have different degrees of accuracy. This work focuses on the improvements of accuracy in one of the architectures of current mirrors. Results obtained demonstrate that the offset error percent in this job is lower than 0.05%. This system also allows correcting of errors introduced by processing. Simulations in Cadence are provided.