DESIGN AND SIMULATIONS OF AN INTEGRATED 9.41 GHZ 24 CHANNELS PHASED ARRAY SYNCHRONIZATION BY PHASE LOCKED LOOP FOR DUAL POLARIZED DOPPLER SOLID STATE RADAR FOR CASA STUDENT TEST BED

by

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Abstract

of Dissertation Presented to the Graduate School
of the University of Puerto Rico in Partial Fulfillment of the
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DESIGN AND SIMULATIONS OF AN INTEGRATED 9.41 GHZ 24 CHANNELS PHASED ARRAY SYNCHRONIZATION BY PHASE LOCKED LOOP FOR DUAL POLARIZED DOPPLER SOLID STATE RADAR FOR CASA STUDENT TEST BED

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The design and simulations of an integrated 9.41 GHz - 24 channel passed array synchronization by phase looked loop for dual polarized Doppler solid-state radar for the CASA student Test Bed is presented in this thesis. The synchronization module is designed using discrete commercial components with low residual phase noise, low current, low power consumption and low cost. Several architectures for Distribution Local Oscillator (LO) based in PLL are analyzed its advantages and its limitations in terms of amplitude, frequency and phase stability, lower power consumption and lower cost. Active filter loop is designed according to the required loop bandwidth and phase margin which are critical factors in the contribution of deterministic phase noise of various sources in the LO generation.

The synchronization module maintain phase, amplitude and frequency stability and purity in a 24 channel system for a dual polarized, Doppler, solid state radar for the Center for Collaborative Adaptive Sensing of the Atmosphere (CASA) Student Test Bed. This is the second stage in building the Solid State Off the Grid radar (SSOTG). The SSOTG is designed to operate at X-band frequency and have a 24 channel system. The full design is completed on a Rogers TMM10i substrate which has a permittivity of 9.8 and a thickness of 0.635 mm. The layout and simulations are carried out using Agilent′s Advanced Design System (ADS).

Resumen

de Disertación Presentado a Escuela Graduada
de la Universidad de Puerto Rico como requisito parcial de los
Requerimientos para el grado de Maestría en Ciencias

DISEÑO Y SIMULACIONES DE UN MODULO DE SINCRONIZACIÓN PARA 24 CANALES A 9.41 GHZ BASADO EN LA TÉCNICA DE LAZO DE SEGUIMIENTO DE FASE PARA UN RADAR DE ESTADO SÓLIDO, DOPPLER DE DOBLE POLARIZACIÓN PARA STB CASA

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El diseño y simulaciones del módulo de sincronización para 24 canales a 9.41 GHz basado en la técnica de lazo de seguimiento de fase para un radar de estado sólido, Doppler y de doble polarización para el lugar de pruebas liderado por estudiantes (STB por sus siglas en Inglés) de CASA es presentado en esta tesis. El módulo de sincronización es diseñado usando componentes discretos comerciales con bajo ruido en fase, bajo consumo en corriente, bajo consumo de potencia y bajo costo. Varias arquitecturas para la distribución de los osciladores locales basado en lazo de seguimiento de fase (PLL, por sus siglas en inglés) son analizadas sus ventajas y limitaciones en terminos de estabilización de fase, frecuencias, y amplitud, consumo de baja potencia y bajo costo. El filtro de bucle activo está diseñado de acuerdo a los requerimientos de ancho de banda de lazo y el margen de fase, que son factores críticos en la contribución del ruido en phase, determinístico de diversas fuentes del PLL. El modulo de sincronización mantiene estable y pura la fase, amplitud y frecuencia en el sistema a 24 canales para un radar de doble polarización Doppler de estado sólido para el lugar de pruebas liderado por estudiantes CASA. Este trabajo es el segundo paso para la construcción del radar de estado sólido fuera de red (SSOTG, por sus siglas en inglés). SSOTG es un sistema de 24 canales y está diseñado para operar a la frecuencia en banda X. El sistema se diseñó sobre el sustrato TMM10i de Roger Corporation, quien tiene una permitividad de 9.8 y un espesor de 0.635 mm. El layout y simulaciones se llevan a cabo utilizando el simulador "Diseño de Sistemas Avanzados (ADS)" de Agilent′s.

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To God, to my husband, to my parents, and in loving memory of my uncle Miguel Sepúlveda and aunt Mireya Lancheros

Chapter 1

Introduction

Continued progress in increasing performance, speed and reliability, and the simultaneous reduction in size and cost in the design of communication systems have resulted in strong interest in phased array antenna systems with components based in solid-state technologies [3, 4]. A solid-state phased array system consists of multiple radiating elements; each of which is driven by a transmitter/receiver (T/R) module [5, 6]. One of the principal difficulties in designing phased array systems is meeting requirements for coherent operation [7, 8]. This is the necessary amplitude, phase [8, 9] and frequency [1] synchronization of each T/R module which is also essential for the electronic beam steering [9]. We propose various architectures to achieve and maintain phase, amplitude and frequency stability and purity in a 24 channel system for a dual polarized, Doppler, solid state radar for the Center for Collaborative Adaptive Sensing of the Atmosphere (CASA) Student Test Bed.

The design of a synchronization module is done in this thesis. The synchronization module is a compact design that provides and maintains the stability and purity of the phase, amplitude and frequency in the system. This is the second stage in building the Solid State Off the Grid radar (SSOTG). The SSOTG is designed to operate at X-band frequency and has a 24 channel system. The full design is completed on a Rogers TMM10i substrate which has a permittivity of 9.8 and a thickness of 0.635 mm. Surface mount components, mainly from Hittite, with solid state technology, will be used for this design because of their greater reliability, superior performance, lower cost and higher factors of availability [10]. The design, layout and simulations are carried out using Agilent′s Advanced Design System (ADS) and Matlab′s. Each channel uses two-step down-conversion and up-conversion. The Phase Locked Loop (PLL) generates 48 Local Oscillator (LO) signals, 24 LO signals at 7 GHz that, divided by 3, generate the other 24 LO signals at 2.33 GHz.

The work presented in this thesis is developed as part of CASA, the objective of which is the development of Distributed Collaborative Adaptive Sensing (DCAS) as a technology to improve monitoring of the earth's lower troposphere. The University of Puerto Rico at Mayaguez campus currently has a network of three radars, located in Cornelia, Aguadilla and the Residential Center of Educative Opportunities of Mayagez (C.R.O.E.M.). These radars operate at X-band frequency with a center frequency of 9.41GHz, have single polarization, are non-Doppler, depend on mechanical parts, and have high power consumption since they operate using magnetrons. These characteristics lead to problems in the network, such as not being able to distinguish moving targets from background clutter and not are able to achieve beam steering, necessary for an accurate scan of weather in the sky. In the future, the sensing network with polarimetric Doppler radars will have the capability to improve data quality by identifying non-meteorological echoes and control in the scanned in the azimuth plane [11]. The proposed work will develop solid-state radar to improve the reliability have better control of the transmitted pulse, and allow the use of electronic techniques for tracing the radiation beam so as to have better control of the address pointed to radar and flexibility when tracking sequences, and can improve the reliability have fewer moving parts and reduce the cost of maintenance. This thesis presents the design and implemention of an integrated 9.41 GHz -24 channel phase array synchronization module by Phase Locked Loop for the dual polarized Doppler solid state radar for the CASA student test bed to be used on the DCAS radar network that is being developed for Puerto Rico.

1.1 Justification

Currently, CASA - UPRM uses marine radars converted to weather radars to aid forecasts in the western region of Puerto Rico. The network has single polarization and is non-Doppler, capable of providing only reflectivity measurements. This thesis presents the second stage for the development polarimetric Doppler solid state X-band radar for precipitation measurements. The design stage of the RF transceiver was completed [12]. This work consists in the design and implementation of synchronization module for the 24 channels of the system. In the future, the new radar design will have the capability to eliminate unwanted clutter. It will diminish attenuation effects and partial beam blocking using differential phase measurements and will shorten data updating time [11]. It will have superior reliability and therefore the availability of the radar network system will improve [11, 13].

1.2 Significance

The reception and transmission of the array radar, smart antenna, wireless communication and other systems of communication, needs to work synchronously [14]. The function of the synchronization module is to distribute the LO signal with the proper frequency and the same phase to each column of the transceiver in order to achieve the desired radiation pattern in the azimuth direction. We propose to study and to examine architectures based on phase locked loop (PLL) techniques to achieve and maintain stability and purity of the phase, amplitude and frequency in each channel. The architectures will be analyzed to provide a better reduction in phase noise, lower power consumption, lower cost, and better stability.

1.3 Objective

The main aim of this project is to design and simulate a synchronization module that fulfills the requirements for the performance and optimal operation of a solid state Doppler X-band weather radar. The function of the synchronization module is distribute 24 LO signals at 2.33 GHz and 24 LO signals at 7 GHz. The LO signals are distributed with the proper frequency and the same phase and amplitude to each column of the transceiver to low power consumption, lower cost and lower phase noise. This work is the second step for the full design of a solid state off the grid radar. The weather radar will be designed to operate in Western Puerto Rico, as part of the CASA Student Test Bed.

The contributions in this work are:

- Our work is to investigate, design and evaluate two architectures for LO Distribution based in PLL. The advantages and limitations are studied in terms of frequency and phase stability, lower power consummation and lower cost.
- Our work will evaluate the effects of different Bandwidths and phase margins in active loop filter designs in order to determine the best phase noise performance in LO generation.
- The design criterion used for selected of component is based on Solid State technology operates, with a low current, low residual phase noise, low power consumption and low cost.

1.4 Work Organization

This thesis is organized as follows: In chapter 2 are discussed in detail generation LO and distribution LO designs. The discussion includes the limitations related to principals and more popular LO distribution architectures. This chapter will also include a literature review about previous works related to some of the alternative solution of the coherence problem that have already been revised. Particularly, the effect of phase noise on Local Oscillator (LO) In the communications system. Chapter 3 presents the overview and modifications on design the RF transceiver module. Subsequently, the methodology used in the design of synchronization module is explained in detail. The simulations the synchronization module and comparative results are presents in chapter 4. According to the results obtained in the simulations, the synchronization module is realized on the Printer Circuit Board PCB by using commercial components. Finally, chapter 5 presents the conclusions and future works.

Chapter 2

Literature Review and Background Theory

2.1 Introduction

The increase of the usage for Dual-polarized weather radars is due to the need of accurate and informative weather measurements. These radars are capable detecting and identifying convective storms and studying the Drop Size Distribution (DSD) [15]. They have the capability to improve data quality through the discovery of non-meteorological echoes (i.e., clutter, insects, airplane, birds, and others.) and to diminish attenuation effects and partial beam blocking using differential phase measurements [16–20].

Additionally, it is a known fact that phased-array technology can shorten data updating time [21]. Phased arrays system are capable moving the beam position with electronic steering by adjusting the relative phases of the signal received or transmitted by each antenna [22]. The principal restriction of phased arrays lies in the difficulty of applying the correct amplitude, frequency and phase to each antenna and the complexity of the electronic hardware required and the resulting cost [23]. The reception and transmission of array radar need to work synchronously [14]. Generally, radiated signal arrives at each element of the antenna at different times [22]. This means that all Local Oscillator (LO) signals be sent out to the transceiver modules at frequency and time precise that are determined by a special signal referred to as the clock; the amplitude, phase and frequency synchronization of each T/R module is therefore critical in ensuring array coherence and is a very important aspect of the distributed controller antenna's beam. With coherent system the phase array combines the signals coherently to enhance the reception from desired directions while rejecting emissions from other directions and compensates the

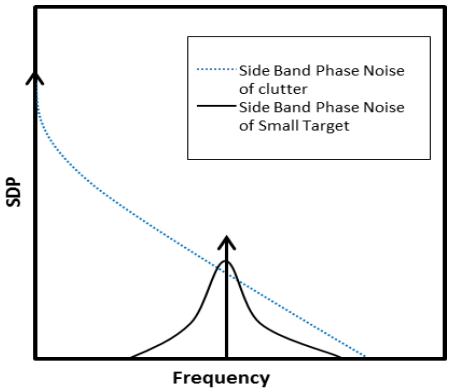


FIGURE 2.1: Phase noise vs. Spectrum Density of Power (SDP) in a radar system

time delay difference between the elements [22]. In general, the functions of the synchronization module are the generation oscillator and distribution the LO signal with amplitude, phase and frequency correct.

Phase noise in communications systems, is a major contributor to generating synchronization problems [24, 25]. The phase noise in a Doppler radar system will broaden all the static target echo received (i.e. clutter), making some portions of power spill to a pass band region limiting clutter cancellation capability which may be a problem in the case of dry weather and light rain situations where the weather signal is much more weaker than the clutter return [26]. This situation in shown in figure 2.1. Phase noise is an undesirable entity that is present in all real world signal generators. It can cause distortion or complete loss of incoming information in traditional receivers.

Regarding the implementation of the system, one of issues in Printed Circuit Board (PCB) construction is contributed by transmission line effects that are getting more prevalent at higher frequency as the circuit length comparable to the signal wavelength. The problems are time delay, reflections, and crosstalk. In microwave circuits, various transmission lines microstrip, stripline and coplanar wave guide are used for PCB implementation. Microstrip is the most popular transmission line [27]. However, microstrip presents several disadvantages at high frequencies since they present a large amount of undesirable inductance. However, coplanar waveguide transmission lines have several benefits like circuit miniaturization [28], immediate access to adjacent power planes provides lower inductance [29], and provide excellent isolation to minimize crosstalk on the same metallization layer [29].

The objective of this chapter is to provide a theoretical foundation for discussions in the following chapters and review of the existing to the design at the LO generation and

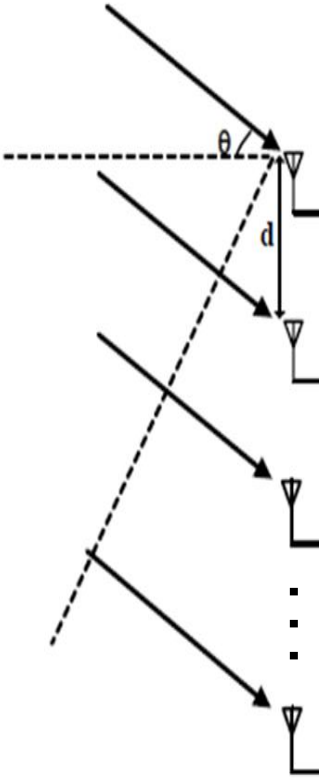


FIGURE 2.2: Phase Array Antenna

LO distribution. The basic concepts in the LO generation are studied in the section 2.5. In the section 2.6 are presented several architectures for the LO distribution in phase array system, that is the main theme of this research. Also the motivations in the use of Coplanar Waveguide CPW transmission line are explained in the section 2.7.

2.2 Phased Array

The phased array system is a special type of multiple antenna system. The operation principles of phased array systems consist in N radiating elements with the same orientation but distributed in the space, and separated each element to a distance,d, as show in the figure 2.2. In general, the phased array in radar applications has many advantages

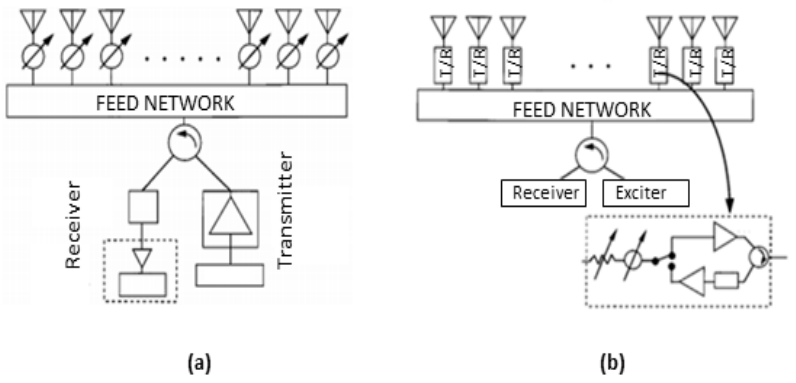


FIGURE 2.3: Types of phase array. (a). Passive Phase Array, and (b). Active Phase Array

[30] as show in the table 2.1. There are two types of phased arrays. These are passive and active as shown in the figure 2.3. Passive array use a central transmitter and receiver, but have phase shift capability at each radiating element. Active phased-array antennas use a T/R module and have phase-shift capability at each radiating element [31]. The principals advantage of an active phase array are: In active array with T/R modules the phase and amplitude can be controlled to generated the radiation patron in the system, and in passive array only the phase in the system is controlled; and other advantage of the active array is that the sensitivity in the receiver is increased due that the RF power is generated at the aperture, and the system noise figure is set [31].

Generally, the radiation patter is determined by changing the excitation phases and amplitude in each element. When the signal, $S(t)$, arriving is distributed to κTh elements, that delay the signal,τ, combined signal in a direction θ, is given by [32] as is illustrated in the equation (2.1). Now, when the electromagnetic wave arriving at the first element array the signal received is showed in the equation (2.2).

$$S_\kappa(t) = \sum_{k=0}^{n-1} A(t - \kappa\tau - \tau_\kappa^{'}) \times \cos[\omega_c t - \omega_c \tau_\kappa^{'} - \kappa\omega_c\tau + \varphi(t - \kappa\tau - \tau_\kappa^{'})] \tag{2.1}$$

$$S_0(t) = A(t)\cos[\omega_c t + \varphi(t)] \tag{2.2}$$

Where A, φ and ω_c are amplitude, phase and carrier frequency respectability. When a plane wave of electromagnetic radiation arrives at spatially antenna element add up coherently in the direction, with progressive time delay, τ, this delay difference between

TABLE 2.1: Advantages in Phase Array Radar

Advantage	**Description**
Agile, rapid Beam electronically steering:	Phase array system not needs mechanically positioning a large and heavy antenna. The beam from an array can be scanned in a determine time by switching speed of the phase shifter. The scan rate is lower at one minute.
Multiple Target tracking	This accomplished either by generating, multiple, simultaneous, independent beams to view more than one target in sequence.
Control of the aperture illumination	Because of the many antenna elements available, the phase array has the ability to quickly go back and look again something of our interest.
Better clutter suppression	Adaptive array has the capability to automatically adjust the aperture illumination to place nulls in the antenna pattern in the direction of the external noise sources as clutter echoes.

two adjacent elements is related to the distance, d, of two adjacent antennas and the signal angel incident with respect to the normal, θ, and the speed of light c, as show in the equation (2.3)[32].

$$c\tau = d\sin\theta \tag{2.3}$$

$$\theta_\kappa = \kappa\omega_c\tau \tag{2.4}$$

Therefore, each element need to compensated for a progressive phase difference θ_κ coherently [see equation (2.4)]. The compensation time delay is inserted in the RF, IF or baseband, digital domain and path LO, as are explained in [22, 32–34]. Additionally, implementing a phased array improves receiver sensitivity, thereby increasing channel capacity [35]. The directivity of the phased-array transceiver system permits higher frequency reuse due to better interference suppression and rejection [35]. If the antennas elements are spaced at a sufficient distance from one another as is reflected in the equation (2.1). Consequently, the coherent addition increases the power radiated in the desired direction for n elements, i.e. the Effective Isotropic Radiated Power (EIRP)as is illustrated in the equation (2.5), while the radiation noise of each antenna is incoherent addition, $10\lg(N)$, for a N elements phase array, improvement in the Signal to Noise Ratio (SNR) [35]. For example, if each transmitter in a 24-element array radiates 14

dBm, the EIRP in the beam direction is increased by 28 dB to 42 dBm.

$$EIRP = n^2 P \tag{2.5}$$

2.3 Phase, frequency and amplitude controls

The phase array transceiver can have errors caused by differences in component tolerances at any point from RF chain in the transceiver to antenna affecting the amplitude and phase of the signal to be transmitted and/or received in each array. Additionally, this system operates at very high frequencies and it can generate errors in the physical construction, caused by mismatches in the length of the transmission lines feeding the different elements introducing significant phase errors. Also, in the phase array can have errors in frequency due to downconversion and upconversion the wanted signal. This error is presented by the phase noise at LO, and this is known as noise frequency translation. Therefore, the phase array radar can have present errors in the phase, amplitude [8] and frequency [1]. In this work we will consider phase, frequency and amplitudes errors that are introduced in the transceiver modules, and assume that the rest of the antenna array operates in an ideal manner. The phased arrays systems use different methods for dealing with these phase, frequency and amplitude errors, as will be discussed in this section. Discussion include the limitations related with principals and more popular architectures, and some of the alternative solution of phase array system problem are revised and compared in terminus of architecture, low power consumption, phase noise, stability and ease implementation. These works summarize the state of the art on the synchronization module design.

2.4 Noise in frequency Translation

In the T/R module the RF and baseband frequencies are downconverter and upconverter respectively. The LO signal used for translation frequency have frequency noise or phase noise and as result is obtained that the downconverter and upconverter signals are corrupt. To understand this, consider that the wanted signal is accompained by interferences and we assumed the ideal case that these signals are impulses as shown in the figure 2.4 part(a)]. Then, the wanted signal is translated to a lower or higher frequency mixed with the Local Oscillator (LO). As the LO exhibits finite phase noise as show in the figure 2.4 part(b), therefore, the output signal consist of two overlapping spectra. One spectra is the wanted signal and other is spectra of interference, as is see in the figure 2.4 part(c). But we obtained the wanted signal suffers from significant

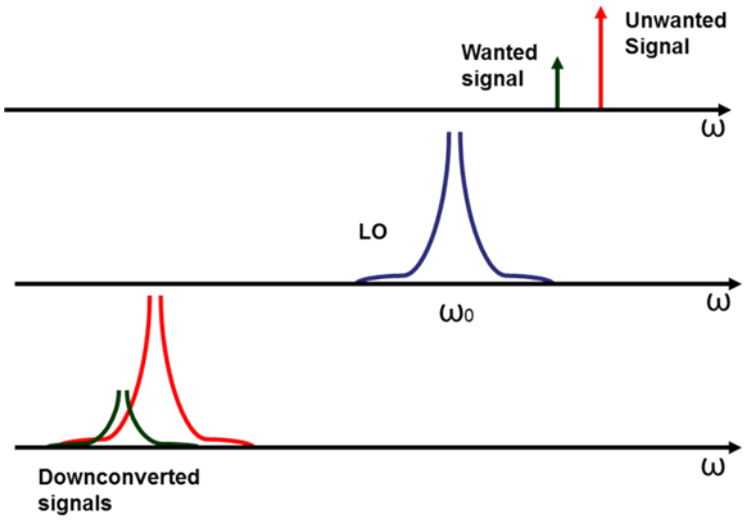


FIGURE 2.4: Noise in frequency translation by effect of phase noise on LO [1]

noise due to the tail of the interferer, this is for the effect the phase noise in the local oscillator.

2.5 Generation RF Local Oscillator

A pure, accurate and stable LO is need for high performance communications systems. Phase locked Loops (PLL) have gained popularity in the used form of Local Oscillator (LO) generation in microwave signals because of low implementation cost, stability and excellent immunity to noise [36, 37]. The concept of PLL was introduced by Appleton in 1923 [38]. In the 1970's the first integrated PLL was designed, this development revolutionized the applications of PLL. Since then, the PLL is used in high-precision apparatuses to improve performance and reliability, especially in modern electronic systems [39]. Recent studies of the impact of Electromagnetic Compatibility EMC on a programmable PLL feature of both Field Programmable Gate Array (FPGA) based Integrated Circuits (IC) and Peripheral Interface Controller (PIC) series microcontrollers (C), have been done by Y. Shih-Yin, W. Cheng-Hsieh, and L. Shry-Sann [40]. The authors analized the impacts Electromagnetic Compatibility (EMC) on a programmable PLL using the TEM-CELL method over two types embedded PLLs. The TEM-CELL method is used to measure the electromagnetic radiation from the circuit board. Their tests were accomplished according to International Electrotechnical Commission (IEC) standard used on Actel FPGA IC. As results they obtained that the different PLL output frequency setups have critical EMC impacts. Based on these results we desired not

to used theses two embedded system (FPGA and PIC) in our design of synchronization module. Instead the application of Gallium arsenide (GaAs) monolithic circuits based on solid state technology in generation clock by PLL provides lower cost, superior performance, higher factors of availability and reliability [10]. These offer lower cost advantages since solid state synchronization modules need neither a high power microwave feed system nor a high voltage DC power supply in order to function. There are many types of PLLs for different applications. Some are designed to handle analog signals and consist entirely of analog circuits. Others are composed only of digital circuits. But most PLLs designed for clock generation and synchronization have both analog and digital circuits.

2.5.1 PLL Basics

Phase locked loop is a simple feedback or control system. The operation principle consist on generating an output signal to a desired frequency, and to a phase stabilized that is related to a stable reference signal. Basic block diagram is shown in the figure 2.5. The PLL are integrated of a Phase-Frequency Detector (PFD), a charge pump, loop filter, a Voltage Control Oscillator (VCO), a feedback multiplier N counter.

The N-counter divides the output frequency by N. The PFD detects the differences in phase and frequency between its reference signal (Fref) and feedback signal (Fout / N), the outputs of the PFD are two signals called Up and Down and it is proportional to the phase-frequency difference of the compared signals. The phase frequency detector and charge pump eliminates the issues of steady state phase error and hold in range. The loop filters eliminate the high frequency components, purifying the tune voltage for Voltage Control Oscillator (VCO). The VCO produce a frequency proportional to its input voltages. The system is stabilized when no phase-frequency difference remains between compared signals. The PFD works is shown in the figure 2.6. The PFD, there are three modes of operation:

1. The phase difference is $+2\pi$; in this model, the charge pump is active only for a portion of the cycle which is determined by the phase difference.

2. The phase difference is-2π ; device is in frequency detect mode and it is continuously sourcing or sinking current depending on which signals frequency is higher, device is in phase detect mode. The charge Pump will be on for a period of τ for every reference period.

3. The phase difference is zero; at the stable point and PFD is in phase-frequency locked mode and the signals are synchronized in frequency and phase.

The major goals in the design of a PLL are to achieve low phase noise, low spurious output, and the ability to change frequencies quickly. These characteristics largely depend on choosing the proper loop filter topology, loop filter order (2nd, 3, 4), loop filter phase margin ($45° - 60°$), loop bandwidth (10 KHz - 50MHz), and loop filter pole ratios [2].

There are two types of topologies of loop filters, active and passive. Active loops use operational amplifiers, which are usually differential as shown in the figure 2.7, and allow the synthesizer to generate tuning voltage levels higher than the PLL IC can generate on-chip. The operational amplifier itself provides the DC amplification necessary to develop a control voltage that is higher than the on-chip supply of the PLL charge pump. Passive filters are mainly R, C (resistor, capacitor) elements that connect directly between the PFD and VCO.

In our design the active loop filter is necessary because the maximum PLL charge pump voltage is lower than the VCO tuning voltage requirements in our system. In terms of filter order, the most basic is the second order filter and can be increased by additional poles. If order of the filter is increased, better filtering of the spurs will occur. When it comes to active loop filters, the third order filter, is generally recommended since the added pole reduces the phase noise of the active device [2]. In practice third order filter active was used for loop filter which was shown in figure 2.7. The phase margin relates the stability and is typically chosen between 40 and 55 degrees [2]. Choosing the phase margin low does results in instability. Choosing higher phase margin results in less ringing in the system. Loop bandwidth is also an important design parameter of the loop filter. It shapes the phase noise characteristic of the PLL. The bandwidth also is related to lock time. The smaller loop bandwidth implies that the reference spurs are smaller, and a larger loop bandwidth implies a faster lock time.

The Impedance of third order active loop filter using differential phase detector outputs is the following [2]:

$$z(s) = \frac{1 + s \cdot R2 \cdot C2}{s \cdot R1 \cdot C2(1 + s \cdot R3 \cdot C3)} \tag{2.6}$$

Where

$$T2 = R2 \cdot C2 \tag{2.7}$$

$$T1 = R3 \cdot C3 \tag{2.8}$$

$$T = R1 \cdot C2 \tag{2.9}$$

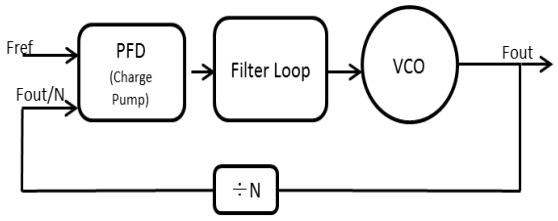


FIGURE 2.5: Basic PLL Block Diagram

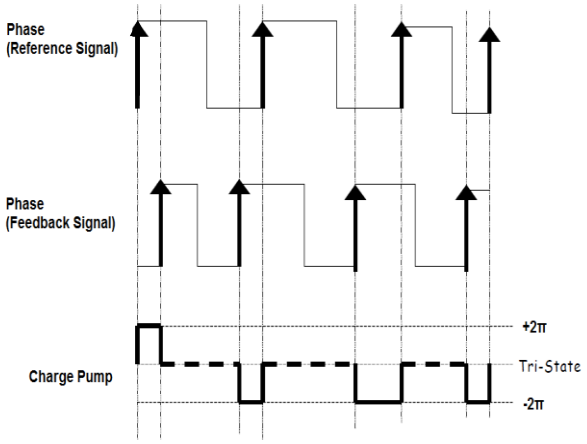


FIGURE 2.6: Phase Frequency Detector Work.

This Expression can be written in a more compact from as in the equation (2.10):

$$z(s) = \frac{1 + s \cdot T2}{s \cdot T \cdot (1 + s \cdot T1)} \tag{2.10}$$

The Pole ratios (T1, T2) should are chosen for lowest spurs. In the figure 2.8[2] show the equations for the time constants and filter components.

The VCO is the component which provides the desired frequency output. Phase noise of the PLL strongly depends on the phase noise of the VCO which is very important for RF applications [41]. An important parameter for low noise phase is the gain of VCO (MHz/V) or Kvco which is a measurement for sensitivity that shows in the frequency on the control voltage. The frequency divider is usually implemented as a programmable

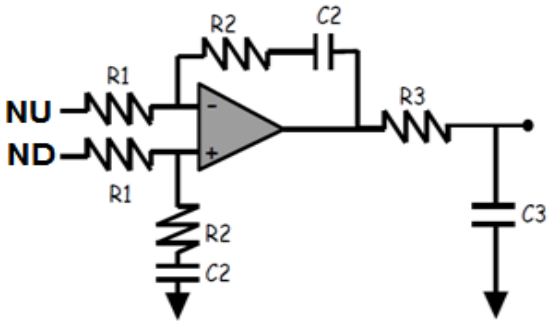


FIGURE 2.7: Active Loop Filter with differential phase detector outputs topology used.

Component	Standard Approach	Alternative Approach
T1	$T1 = \frac{\sec(\phi) - \tan(\phi)}{\omega c}$	0
T2	$T2 = \frac{1}{\omega c^2 \bullet T1}$	$\omega c \bullet \tan\phi$
T	$T = \frac{Kv \bullet Kvco}{N \bullet \omega c^2} \bullet \sqrt{\frac{1+\omega c^2 \bullet T2^2}{1+\omega c^2 \bullet T1^2}}$	$T = \frac{Kv \bullet Kvco}{N \bullet \omega c^2 \bullet \cos\phi}$
C2	Choose this value	Choose this value
R2	$\frac{T2}{C2}$	$\frac{T2}{C2}$
R1	$\frac{T}{C2}$	$\frac{T}{C2}$
C3	Choose this at least four times the VCO input capacitance. Preferably at least 200 pF.	0
R3	$\frac{T3}{C3}$	0

FIGURE 2.8: Time constant and filter Components values [2]

divider allowing the output frequency to move in increments of the reference frequency. The output frequency can be expressed as in 2.11. N value is selected to be as low as possible for optimum noise performance. A programmable divider is usually implemented with dual-modulus prescaler and additional counters to determine how many times to divide by each modulus for a given divider setting.

$$F_{out} = N \divideontimes F_{ref} \tag{2.11}$$

Timing signals as oscillator signals for frequency translation in communication systems use PLL to drive mixing circuits which up-convert or down-convert signals for transmission or reception. Phase noise and spurious tones (due to frequency modulation) in the oscillator signal can limit the selectivity of a radio system.

2.5.2 Phase Noise in PLL

Phase noise, $S(\omega)$, is random fluctuations in the phase of a wave, caused by time-domain instabilities [42], phase noise can be simply expressed as noise power in 1 Hz band at offset from the carrier divided by the carrier power and gives a measure of short term stability of the oscillator [25] as shown in the equation 2.12 and is illustrate in the figure 2.9

$$S(\omega) = 10\log[0.5(S\varphi(\omega)], [dBc/Hz] \tag{2.12}$$

$$S\varphi(\omega) = \frac{P_{SSB}}{P_S} \tag{2.13}$$

Where $S\varphi(\omega)$ is the spectral density of phase fluctuations. When configured in a PLL, the phase noise of a VCO is changed by the action of the loop bandwidth. In addition, the reference input to the PLL has its own phase noise spectrum and the output phase noise depends on this contribution as well. Phase noise of PLL follows voltage controlled oscillator which is the most critical component giving the system output. Therefore, for a low noise system also a low noise VCO is needed.

The output of system is compared to the input through the phase detector, and an error signal proportional to difference is produced. The total phase noise for a PLL can be expressed in terms of the phase noise of the reference, phase noise filter, phase noise loop divider, phase noise PFD and the phase noise VCO.

Noise contributions of individual blocks are shown in the model in angle described by an s-domain model for the phase at various points in the system. If the response of the components in a PLL is linearized, then AC noise model of the PLL in the figure 2.10 can be applied.

Combined forward transfer function of the system is the product of PFD (with charge pump), loop filter and VCO transfer functions which is expressed according to equation (2.14). This is open loop transfer function.

$$G(S) = \frac{I_p F(S) K_{vco}}{s} \tag{2.14}$$

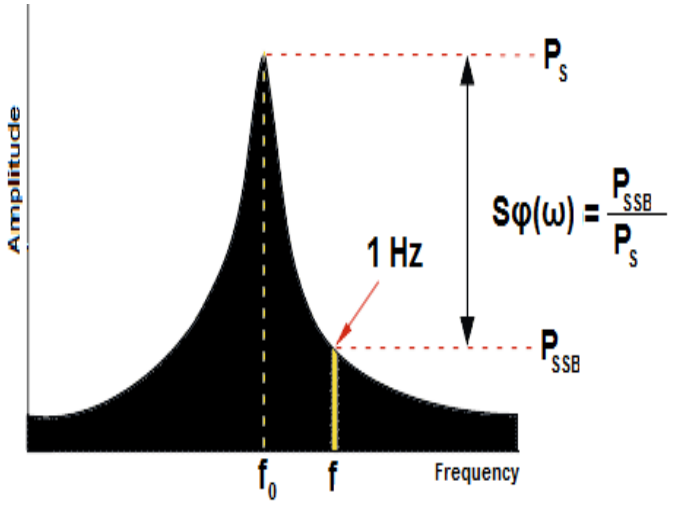


FIGURE 2.9: Phase Noise Definition

Considering the feedback transfer function $H = \frac{1}{N}$, reflections of each noise source to the output can be written as expressed from (2.15) to (2.19):

$$\frac{\Theta_{out}(s)}{\Theta_{div}(s)} = T_{div} = \frac{G(S}{1 + G(S)H} \tag{2.15}$$

$$\frac{\Theta_{out}(s)}{\Theta_{ref}(s)} = T_{ref} = \frac{G(S}{1 + G(S)H} \tag{2.16}$$

$$\frac{\Theta_{out}(s)}{\Theta_{pfd}(s)} = T_{pfd} = \frac{G(S}{1 + G(S)H} \tag{2.17}$$

$$\frac{\Theta_{out}(s)}{\Theta_{vco}(s)} = T_{vco} = \frac{G(S}{1 + G(S)H} \tag{2.18}$$

$$\frac{\Theta_{o}ut(s)}{\Theta_{filter}(s)} = T_{filter} = \frac{2\pi K_{VCO}}{s} \frac{G(S}{1 + G(S)H} \tag{2.19}$$

The equations (2.15) to (2.19) all contain a common factor. This common factor is the expressed in the equation (2.20).

$$\frac{G(S)}{1 + G(S)H} \tag{2.20}$$

The loop bandwidth, ω_c, and phase margin, ϕ, are defined as follows:

$$\|G(j \cdot \omega_c) \cdot H\| = 1 \tag{2.21}$$

$$180 - \angle G(j?\omega_c) \cdot H = \phi \tag{2.22}$$

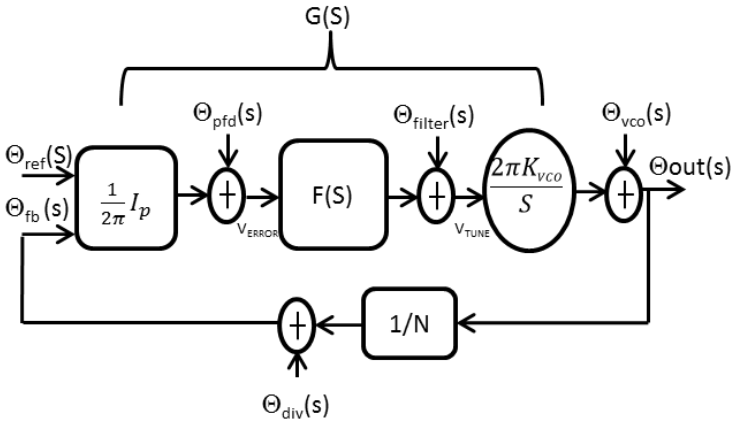


FIGURE 2.10: Model of Phase Locked Loop

$G(S)$ approaches infinity when frequency goes to zero. In such a case expression simplifies to $20 \log N$ in dB scale as is illustrated in the equation (2.23).

$$\lim_{G\to\infty} \frac{G}{1+G\cdot H} = \lim_{G\to\infty} \frac{N\cdot G}{1+G} = N, \omega \ll \omega_c \tag{2.23}$$

Figure 2.11 shown that the noise within the loop ω_c, is dominated by the in-band sources, there may be some slight contribution to this noise from VCO [43].

In case where the loop bandwidth is at least ten times the phase noise offset frequency, the VCO usually does not contribute significantly to the in-band phase noise [43].

The total noise is calculated as RMS sum of these terms according to equation (2.24)

$$\begin{aligned}\Theta_{out}^2 = \\ &(\Theta_{ref}T_{ref})^2 + (\Theta_{div}T_{div})^2 + (\Theta_{pfd}T_{pfd})^2 + (\Theta_{filter}T_{filter})^2 + (\Theta_{vco}T_{vco})^2\Theta_{out}^2 = \\ &(\frac{G(S)}{1+G(S)H(S)})^2.[\Theta_{ref}^2 + \Theta_{div}^2 + \Theta_{pfd}^2] + \\ &(\frac{G(S)}{1+G(S)H(S)})^2.[\Theta_{vco}^2 + (V_{filter}(\frac{2\pi K_{vco}}{s})^2]\end{aligned} \tag{2.24}$$

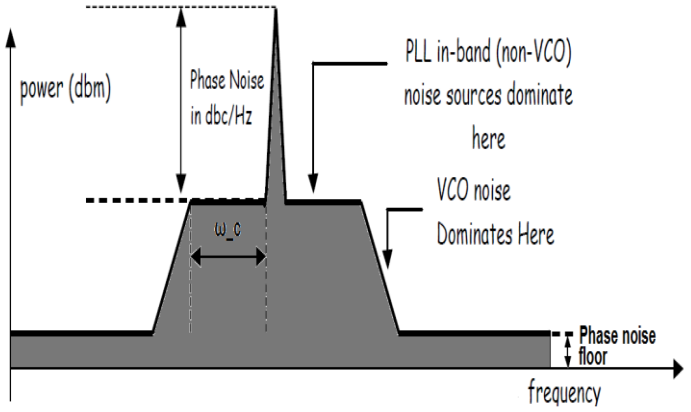


FIGURE 2.11: Typical phase noise spectral plot for a PLL

Resistor and active devices such as operational amplifiers generate noise voltages. The noise voltage in a resistor is the thermal noise. In the case of an operational amplifier, the noise voltage should be specified. The thermal noise generate by a resistor is:

$$V_noise = R_Noise = \sqrt{4T_0K \cdot R}, [\frac{v}{\sqrt{Hz}}] \tag{2.25}$$

Where, T_0, is the ambient temperature in kelvin (300K, typically); K, is the Boltzmans constant equivalent to $1.380658x10^{-23}$ Joule/Kelvin; and R, is the resistor value in ohms. Noise voltage is generated at the VCO input for an open loop system; $G(S)$ is the open loop transfer function. It is necessary to multiply the noise voltage by a factor of $\sqrt{2}$, since these are expressed as RMS.

$$S \approx 20\log(\frac{\rho 2}{2}) for, \rho 2 \ll 1 \tag{2.26}$$

$$\rho 2 = (\frac{\sqrt{2} \cdot V_{noise} \cdot K_{vco})}{f} \cdot \frac{\mid T(2\pi \cdot i \cdot f) \mid}{\mid \frac{1+(G(2 \cdot \pi \cdot i \cdot f))}{N} \mid} \tag{2.27}$$

Today, most of the PLLs are made using synthesizer chips including reference divider, PFD, N divider and charge pump. The chip selects which has lowest noise specifications. The filter loop design is adjustment for low phase noise according to the guidelines mentioned here. The most critical component in phase noise is VCO. Reduction of VCO phase noise directly reduces the PLL phase noise.

2.6 LO Distribution in Phase Array

The key of using phased array antenna is to create a directive beam which can be moved electronically [44]. Phased array coherent radar compared the echo signal with a phase reference in order to be able to use the Doppler frequency. Frequency generation using phased locked loop (PLL) techniques is an interesting approach, particularly at microwave frequencies. Oscillator distribution network is the topology that distribute local oscillator (LO) at microwave frequencies from a common point at all elements that need the local oscillator signal. Numerous architectures for driving synchronous circuits have been devised over years. Many topologies have been developed for the distribution the high frequency oscillator signal in order to synchronize the operation and perform the tasks in orderly manner in a coherent system.

In the literature generally use three types of architectures for the distribution Local Oscillators (LO) signals based on PLL architecture for phase array system [14, 22, 34, 35, 45]. LO distribution by N-VCO using a PLL [45] (see figure 2.12 Part a), LO distribution by N-PLL system using phase frequency detector [14] (see figure 2.12 Part b.), and LO Distribution using a single chip PLL [22, 34, 35, 46] (see figure 2.12 Part c.). In these systems, each LO distribution provides an adjustable phase progression but for our case need studied Local Oscillator (LO) distribution with zero delay. The phase shifting for beamforming on our system is trough of vector modulator on IF signal of the radar.

Due the conflicting requirements of high frequencies for our design of synchronization module, the architecture based in N-PLL is discarded because this topology use extra Phase Frequency Detector (PFD) in the output of each PLL, and the PFD comercial component work at 0.35 GHz as frequency maximum. This implies that we must add the extra frequencies divider to system. Then, the cost is increase in the design of this architecture for synchronization module. Based in low cost the architectures of LO distribution by a single PLL and by N-VCOs are proposed for the studied and analysis in the design of synchronization module. In the following sections are presented work that use the architectures proposed. Generally in the literature reviewed these architectures are studied and treated separately. In this thesis are performed comparative studies of stabilization, cost and power consumption between the two proposed architectures.

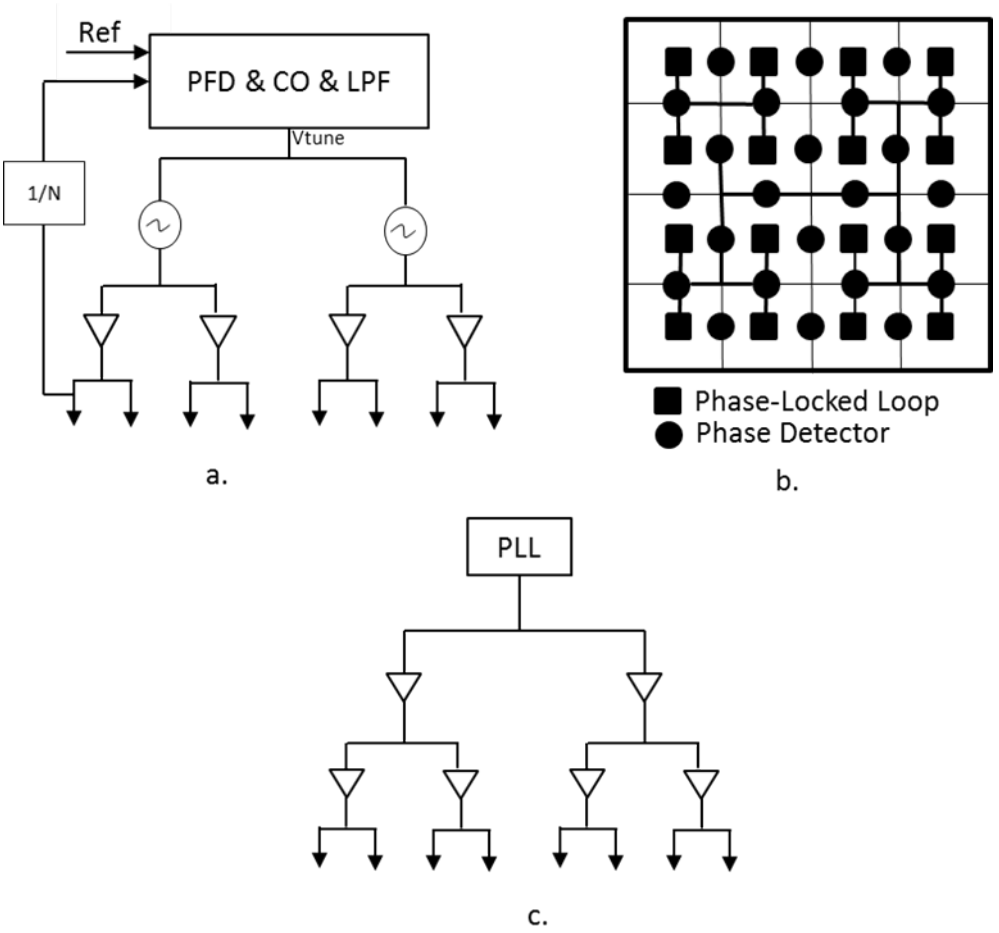


FIGURE 2.12: fig:Architectures for LO distribution based in PLL. a. LO distribution by N-VCO using a PLL. b. LO distribution by N-PLL system using phase frequency detector. c. LO Distribution using a single chip PLL

2.6.1 LO distribution by a single chip PLL

This topology consist in inject a common signal into to T/R modules using a Phase Locked Loop (PLL)as a LO generation followed by N power splitter with amplification levels.

The use of power splitter generate unknown phase shifts, cause errors in the amplitude and phase in the signals distributed. Richard B. Ertel in 1999 [46] proposed a simple procedure for estimate the errors at the system output. The method for estimating the non-ideal amplitude and phase response of the signal splitter consist in the need only find the relative response of the branches of the splitter with respect to a reference branch. The procedure involves taking two measurements for each branch of the splitter. After is estimated the covariance of the measurements and is obtained of eigenvector.

Arun Natarajan in 2005 [35] present a heterodyne transmitter that has a two-step quadrature up-conversion architecture with Local Oscillator (LO) frequencies of 4.8 and

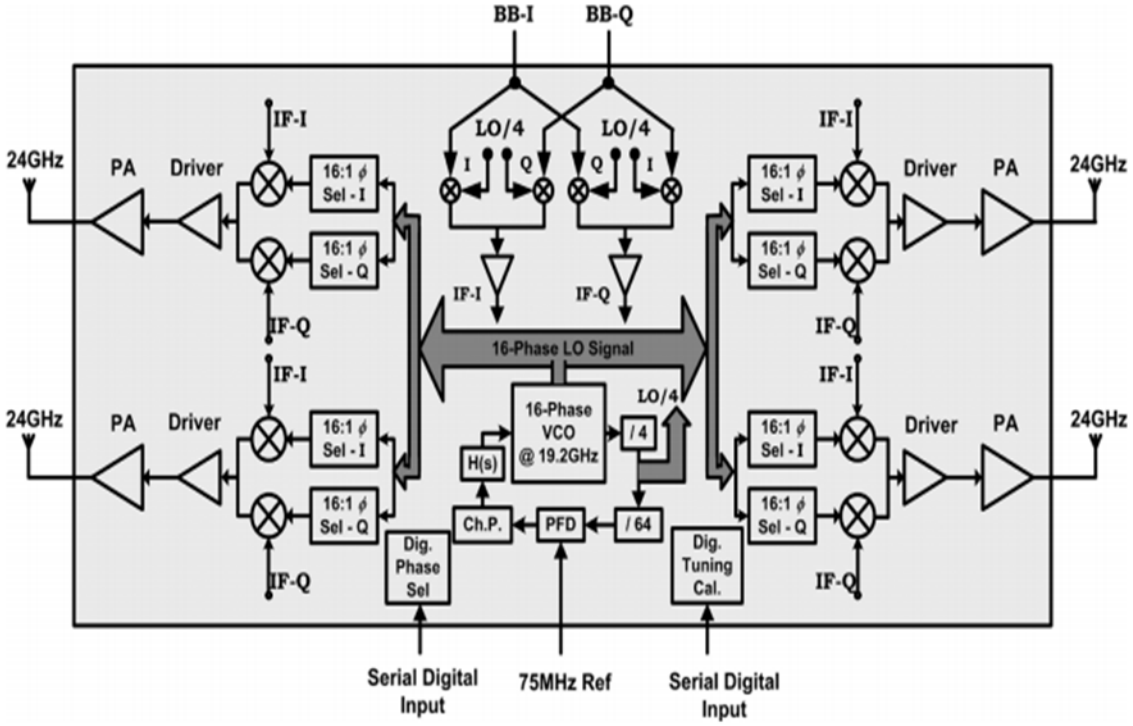


FIGURE 2.13: LO distribution by a single chip PLL **??**

19.2 GHz, which are generated by an on-chip frequency synthesizer as shows of figure 2.13. Our SSOTG radar work at X-band and this is a heterodyne system that need LO frequencies of 2.33 GHz and 7 GHz. One of the objective is generated these two LO frequencies by a chip frequency synthesizer.

2.6.2 Architectures using N-VCOs with a single PLL

A architecture with zero delay for clock distribution networks was published by H. Mizuno in 1998 [47] and consist in comprising a single-PLL with multiple Voltage controlled Oscillators (VCOs). Figure 2.12 Part a. shows the topology used. The PLL is constructed of a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), and voltage-controlled oscillators (VCOs). The outputs of VCOs are connected by equal-length lines of length. These interconnections force all oscillators to oscillate with accurately. The globally-distributed VCOs are synchronized through the feedback signal to the local clock distribution network via short wires.

This architecture is evaluated in stability terms with respect to the architecture LO distribution by a single chip PLL presented in the section 2.6.1.

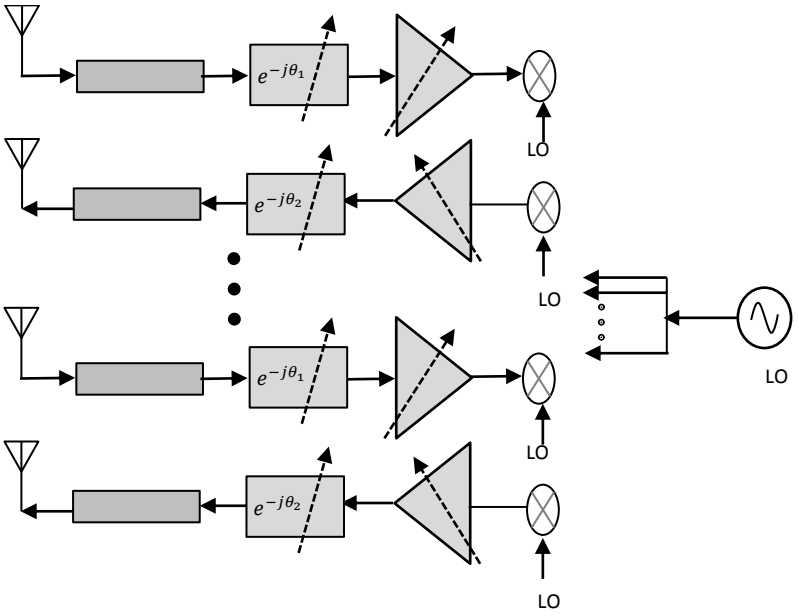


FIGURE 2.14: Phase and amplitude errors introduced in the phase array radar

2.6.3 Amplitude and phase errors in phased array

In the figure 2.14 show the points in the phase array radar where the phase and amplitude errors can be introduced. Errors introduce by feedline lengths due to that this system work at high frequency and small differences in transmission line lengths introduce significant phase errors. Errors introduced in the transmitted and received signals by unwanted phase and amplitud across in the voltage control sections in the components as phase shifter and Voltage Gain Amplifier (VGA). The errors introduced by distribution Local Oscillator (LO), ideally signal with identical phase are injected in each array, however there difference in the signals phase and amplitude at the output power splitter.

The phase and amplitude errors are classified into two groups, static and dynamic [48]. Static errors are caused by differences in component due to manufacturing tolerances and physical construction. Dynamic errors are caused by the fact that the parameters of electronic components vary with temperature. This variation is different for similar components. The static errors, these can be calculated and are relatively stables in the life of components. But the dynamic errors, required be eliminated through periodic recalibrate. In general, phase and amplitude errors in the branches of a phase array radar have negative effect on the system performance's. The accuracy and reliability of these errors in the system, which can solved in several methods of calibration [46, 48, 49]

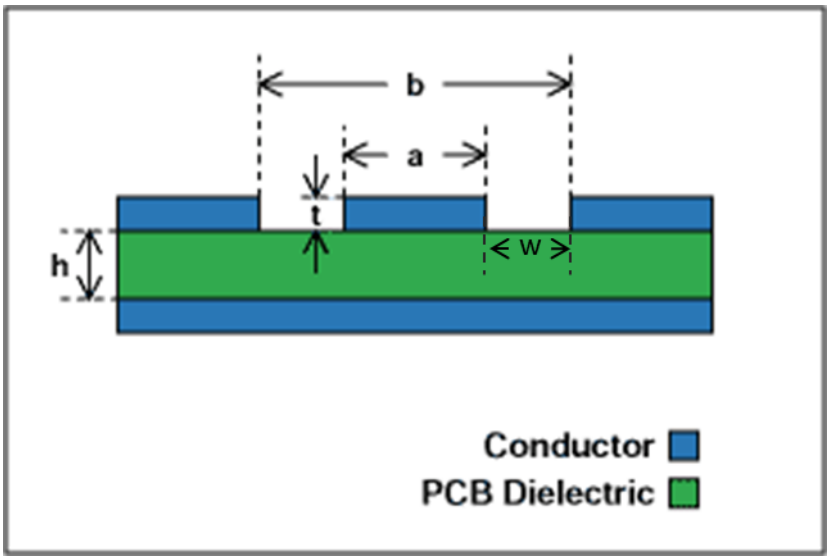


FIGURE 2.15: Schematic of a CPWG

2.7 Coplanar Waveguide Ground Transmission Line

Many studies at high frequencies demonstrate that coplanar waveguides (CPW) provide many solutions to the design of low-loss and compact integrated circuits [50]. The Coplanar Waveguide Ground (CPWG) consists of three conductors printed on a dielectric substrate with thickness h as shows in the figure 2.15; the central conductor width is denoted by a and corresponds to the signal line, and the others correspond to ground. The slots width are denoted by W.

The calculus for characteristic impedance are presented in the equations (2.28) to (2.33).

$$Z_0 = \frac{120\pi}{2.0\sqrt{\varepsilon_{eff}}} \bullet \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k1)}{K(k1')}} \tag{2.28}$$

Where:

$$\varepsilon_{eff} = \frac{1.0 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k1)}{K(k1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k1)}{K(k1')}} \tag{2.29}$$

$$k = a/b \tag{2.30}$$

$$k' = \sqrt{1.0 - k^2} \tag{2.31}$$

$$k1' = \sqrt{1.0 - k1^2} \tag{2.32}$$

$$k1 = \frac{tanh\left(\frac{\pi a}{4.0h}\right)}{tanh\left(\frac{\pi b}{4.0h}\right)} \tag{2.33}$$

The coplanar waveguide ground (CPWG) transmission lines have advantage in the ease in impedance control [51]. Impedance control is facilitated by controlling the spacing and width of the ground traces on either sides of the signal trace without changing the width of the signal trace or its height above the ground plane which are constrained. Syed Bokhari in 2003 [51] shows that the maximum spacing between ground vias on the CPWG transmission line should not exceed a half guide wavelength and also recommend to use either a smaller spacing or two staggered rows of vias to compensate for the via inductance.

Chapter 3

Methodology

3.1 Introduction

In order to design the synchronization of module, first was necessary to revise the radar transceiver design made by [12] and make indispensable modifications, this is explained in details in the section 3.2. The methodology developed for synchronization module design can be summarized through the flowchart showed in the figure 3.1. It consists of two stages. The first stage consist of LO generation by Phase Locked Loop (PLL) and the second stage consist of LO distribution.

For the design of LO generation on need to consider the requirements and specifications of PLL. The specific parameters to define for the design of PLL are the frequency and power of the output signal , the frequency and power of the reference signal, and the N-dividers. This is with the object of obtained two output LO signals with one frequency synthesizer. A LO signal at 7 GHz and other LO signal at 2.33 GHz. Next is the selection of the components to be using on PLL. The design criterion used for selected of component is based on Solid State technology operates with a low current, low residual phase noise and low power consumption and low cost. The active filter loop in PLL was designed and are studied the influence of bandwidth in the phase noise responses. The system is simulated with different bandwidths and phase margin in Advance Design System (ADS) until that is optimized phase noise for system performance. The layout of LO generation is designed. The LO generation design is explained in detail in the section 3.3.

The second stage consist in distributed pure and stable, 24 LO signals at 2.33 Ghz and 24 LO signals at 7Ghz. With the object of have pure and stable signals, are evaluated differents architectures based on PLL. The architectures are analized and studied in phase

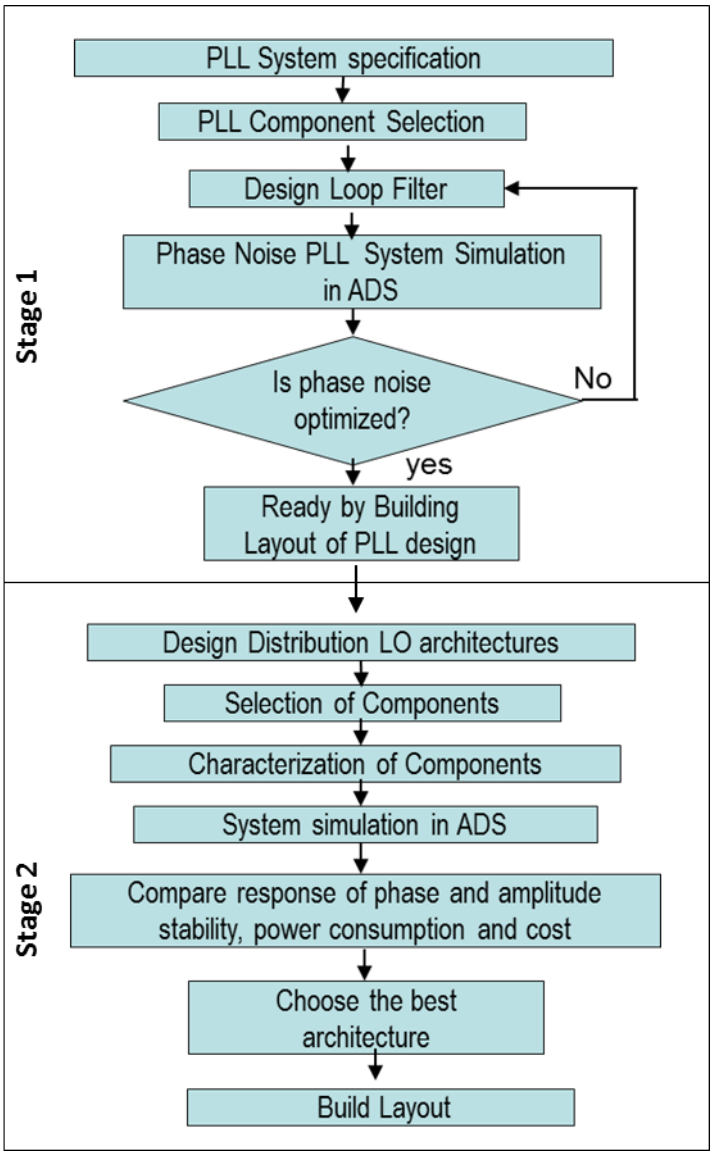


FIGURE 3.1: Synchronization Module Design Methodology Flowchart

and amplitude stability, lower power consumption, and lower cost for the construction of synchronization module. The responses are compared and the best architecture is selected according to the criteria studied and analyzed. The layout of LO distribution is designed. Therefore, synchronization module design is completed.The LO distribution design is explained in the section 3.4.

3.2 System Overview and modifications

In order to start the synchronization module design, there is a need of analysis on solid state transceiver module designed by [12]. The system parameters are shows in the table 3.1. With respect to design by [12] of radar frequency is at 9.5 Ghz and the IF

TABLE 3.1: Radar System Parameters

Parameter	**Symbol**	**Specification**
Radar Frequency	F	$9.41GHz^{*}$
Wavelength	λ	31.88 mm
Peak Transmitter Power	P_t	24 W
H Antenna HPBW	θ_x	6°
V Antenna HPBW	θ_y	6°
Antenna Gain	G	24 dB
Range Resolution	$\triangle R$	1500 m
Radial Resolution	$\tau/2$	$5\mu s$
Unambiguous Range	UR_{max}	15000 m
Noise Figure	F_n	$< 4dB$
Minimum Detectable Signal	MDS	-110 dBm
Intermediate Frequency	IF	$80MHz^{*}$
Maximum Range	R	6-10 Km
Pulse Width	τ	$10\mu s$
Pulse repetition Frequency	PRF	1000 Hz
Sensitivity	Z	3 dBz - 40 dBz
Maximum Winds	w	40 m/s, 89 mph

is at 5 MHz. In the present design these signals are modified at 9.41GHz and 80 MHz, respectively . The center radar frequency was changed for that this system operate the similar frequency the others OTG Radar. The IF frequency was changed so that with a single synthesizer two LO signals are produced and therefore reduce costs. The other parameters of system remain the same.

The new block diagram of transceiver based on modifications of [12] is show in the figure 3.2, where the components mark with "$*$" are modifications made in the selection of components. The modifications and operation of the transmitter and receptor are described as follows.

In the receptor, a three port circulator is used to route outgoing and incoming signals between the antenna, the transmitter and the receive. The circulator was changed of 31MS95-1 from Dorado to 4925- from Narda because the pass selected component is not available. The new circulator selected (4925) provides 20 dB of isolation and has a insertion loss of 0.4 dB. After the circulator, a limiter HMC607 SPDT switch with 60 dB of isolation is followed that can prevent damage on the receiver caused by leakage that comes from the transmitter when the T/R module is in transmit mode. Then a cascade of two Low Noise Amplifiers (LNAs), the HMC564LC4, are needed for amplifier the signal detected by the receiver. The minimal signal detectable for receiver is -110 dBm. Each LNA provides a gain of 17dB and has a low noise figure of 1.8 dB. After the signal at 9.41 GHz from LNA and the LO signal at 7 GHz are mixed and

down-converted, a signal at 2.41 GHz is obtained. The down-converter was change of HMC568LC5 to HMC908LC5 because of HMC568LC5 is a descontinued product. The new down-converter HMC908LC5 selected provides a small signal conversion gain of 10 dB with a noise figure of 2.2 dB and a image rejection of 25 dB. The image reject mixer eliminates the need for a filter following the LNA, and removes thermal noise at the image frequency. i and q mixer outputs are provided and then an external 90 hybrid is needed to select the required sideband. The new hybrid used is the QCC-22+ which provides a low insertion loss of 0.4 dB and high isolation of 28 dB. After a vector modulator HMC631LP3 is used for the reception and transmission of system. The I and Q ports of the HMC631LP3 can be used to continuously vary the phase and amplitude of RF signals by up to 360 degrees and 40 dB respectively for beam forming in the phased array radar. The vector modulator selected have a output noise floor of -160 dBm/Hz at maximum gain setting. The output signal of vector modulator is passed for a new power splitter that feeds the next dual mixer. the power splitter chosen is the GP2S1+ with good isolation of 20 dB and excellent amplitude and phase unbalance of 0.02 dB and 0.9 degrees respectively. The dual mixer used is the HMC340ALP5 for down-conversion of the signal at 80 MHz Intermediate frequency (IF) signal mixed with the LO signal at 2.33 GHz and 2.41 GHz signal output of vector modulator. The LO input need of having a 90 degree hybrid at the end of the LO signal. The hybrid used is the Mini-Circuits QCC-22+ (operating from 1.5 to 2.5 GHz). For the HMC340ALP5 is need filter the I and Q IF signals. These filter are agree for eliminated image frequencies of IF signal. The new filter selected is the ACF321825-152, operating from (60 - 115) MHz.

In the transmitter is need generated 80 MHz IF signal is to be mixed with a LO signal to convert from IF 80 MHz to RF 2.41 GHz needed for the vector modulator. The HMC404ALP5 double mixer is used. The RF signal at 2.41 need be filtered for eliminate image frequencies. The new filter selected is the HMC891LP5. This is a tunable filter, the center frequency can be varied between 2 and 3.9 GHz by applying an analog tune voltage between 0 and 14V. The Vector Modulator used is the HMC631LP3 the same used in the receptor mode and the output and input are operated by switches for selected transmitter or reception mode. The new switch selected is the HMC348LP3 with high isolation major to 55 dB. After the RF signal is phase shifted in the vector modulator it passed through a new component selected that is Mini-Circuit GP2S1+ power splitter that is need for feeds another up-converter. The HMC521LC4 up-converter is changed by HMC924LC5 because the HMC521LC4 have a frequency range of LO at (8.5 - 13.5)GHz out of 7GHz that is our frequency for LO used in the design of system. The HMC924LC5 is responsible of converting transmitted signal from 2.41 GHz to the desired operating frequency at 9.41 GHz. This has amplitude control in the output signal. The LO is

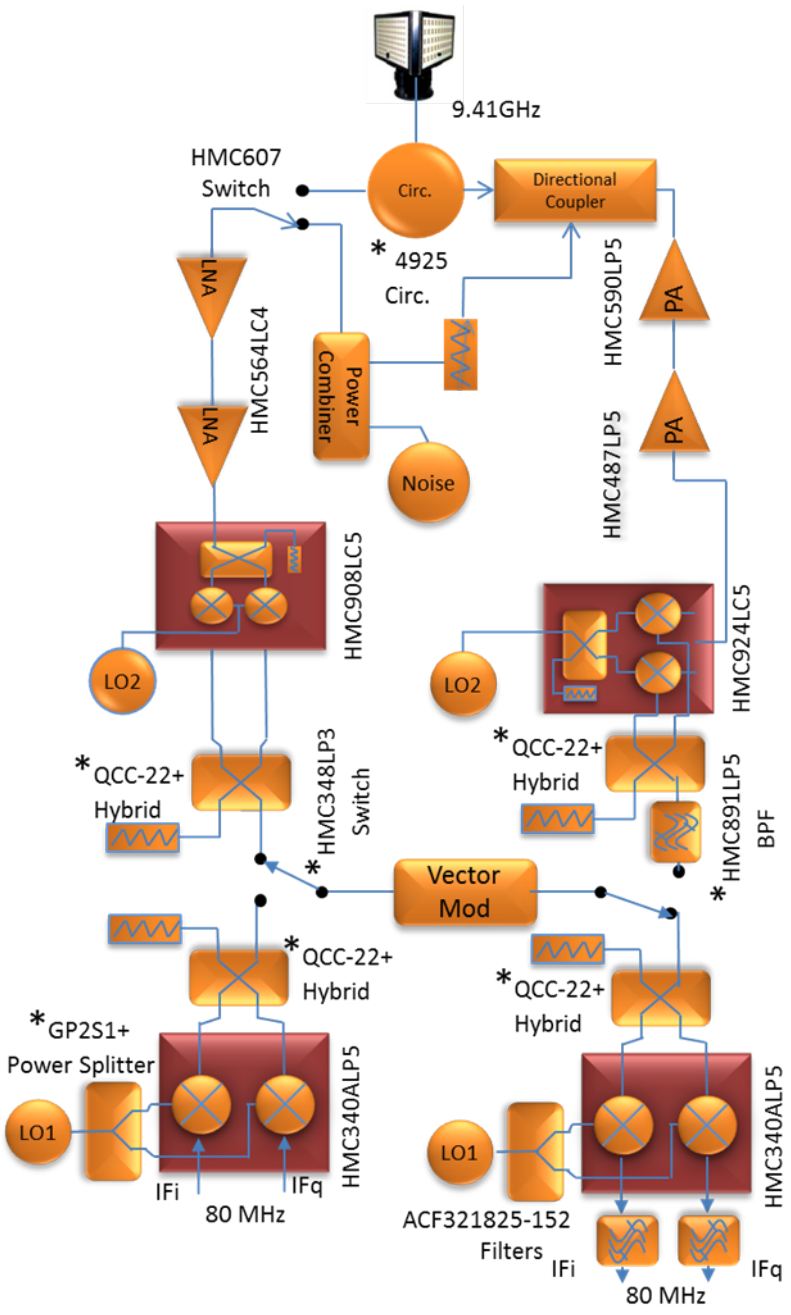


FIGURE 3.2: Block Diagram of Transceiver

placed in conjunction with the dual mixer in order to upconvert the signal. It oscillates at 7 GHz which when mixed with 2.41 GHz will produce the desired frequency of 9.41 GHz. The output of the mixer is fed into to the two power amplifiers that provides necessary power to operate the transmit module. The power amplifier used is the HMC590LP5 with 21 dB gain by the HMC487LP5 with 20 dB gain. Only a string of two power amplifiers are needed in order to amplify the signal at such a level that permits us to have approximately 30 dB signal at the antenna.In Appendix A show the components change and added to design of transceiver made by [12].

3.3 LO GENERATION DESIGN

This radar will haves 24 channels with Transmit/Receive (T/R) solid state modules. For each transceiver it is necessary to generated a LO signal at 7 GHz and a LO signal at 2.33 GHz uses for down-conversion and up-conversion. According to this, a single synthesizer two LO signals are produced and therefore reduce costs in the system.

3.3.1 PLL System Specification

In order to start the design of PLL, it is necessary to consider the following design requirements in the table 3.2.

TABLE 3.2: PLL System Specification

Parameter	Symbol	Specification
Reference Input Frequency	Fin	70 MHz
Output Frequencies	F_{out1}	7 GHz
	F_{out2}	3.5 GHz
	F_{out3}	2.33 GHz
N Divider	N	50
N Divider	N	3
Input Power	P_{in}	0 dBm
Output Power	P_{out}	13.5 dBm

3.3.2 PLL Component Selection

In the Figure 3.3 are showed the devices that make up the PLL. The system uses surface mount and solid-state components with low phase noise, low current consumption and low cost. The oscillator signal provides the reference frequency (Fref)signal at 70 MHz. This signal is the master clock in the system and is used to stabilize the desired phase-frequency of output in PLL. The reference signal into to the HMC699LP5(E) frequency synthesizer have integrated Phase Frequency Detector PFD, charge pump, and N divider. Using this approach eliminates the issues of phase error completely. The synthesizer has ultra-low phase noise -153 dBc/hz, with programmable divider (N = 16 to 519) operating up to 7GHz. Wide loop bandwidth and low N = 50 result in fast setting, very low phase noise, and improved noise performance and frequency resolution. The synthesizer has open collector output buffer amplifiers for interfacing operational amplifier based loop filter. The synthesizer also includes PFD, whose function is to compared the reference signal with output signal of system. The output of PDF is a DC value that is proportional

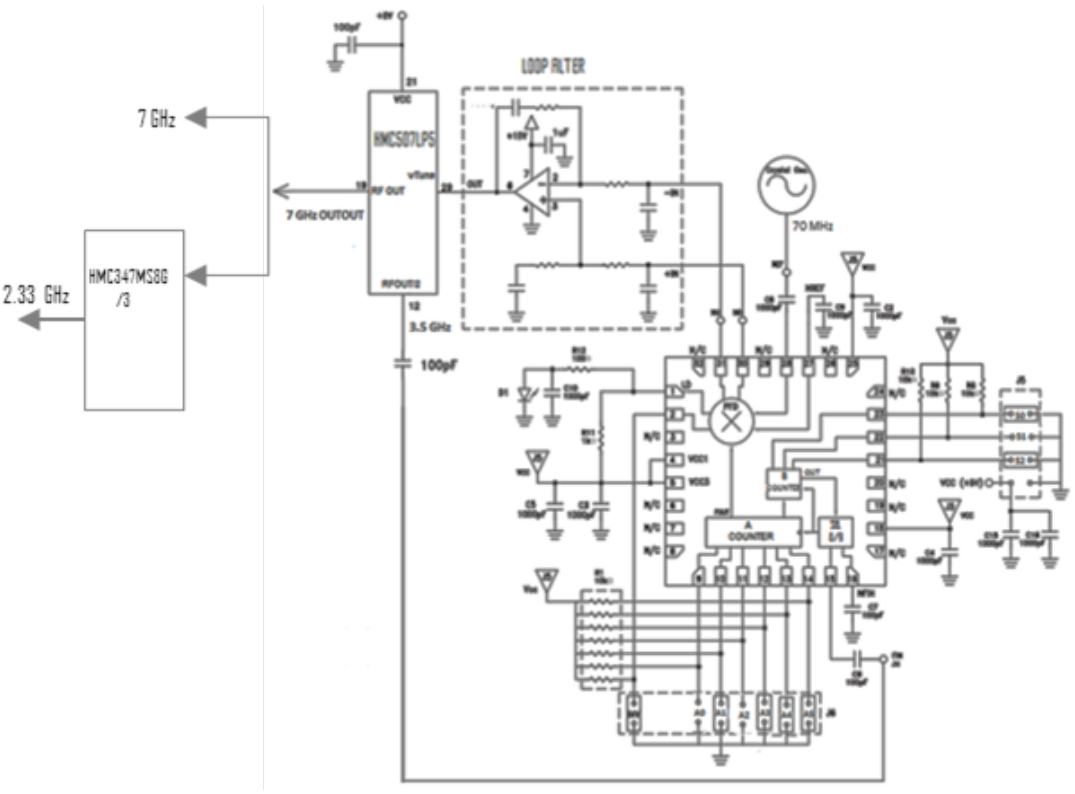


FIGURE 3.3: Circuit Design of PLL

to the phase-frequency difference of the compared signals and produces low and high signals. The PDF has a sensitivity of 0.32 V/rad. The Charge pump converts the digital signal into current. The Filter loop used in this system is active type. This is composed of THS4031CDGN operational amplifier and passive components (resistor and capacitor). The operational amplifier has ultralow $1.6nV/\sqrt{Hz}$ voltage noise, 100-MHz Bandwidth, -90 dBc of total harmonic distortion. The function of the filter loop is to eliminate high signals and deliver pure signal DC to Voltage Controlled Oscillator (VCO). The detailed of design of active filter loop for optimized phase noise are explained in the section 3.3.3.

In the chapter 2 reviews the role of phase-locked-loops (PLLs) for frequency synthesis. Phase noise was shown to be important performance specifications in such systems. Particularly critical in PLL systems is the phase noise of the VCO. Then, the strategy is selected a VCO with low phase noise. The VCO selected is HMC507LP5, which has dual output F_synt (6.65 7.65 GHz) and F/2 (3.325 3.825). F_synt, the output frequency of the synthesizer can be programmed using the following relation (3.1):

$$F_{synt} = F_{ref} * N \tag{3.1}$$

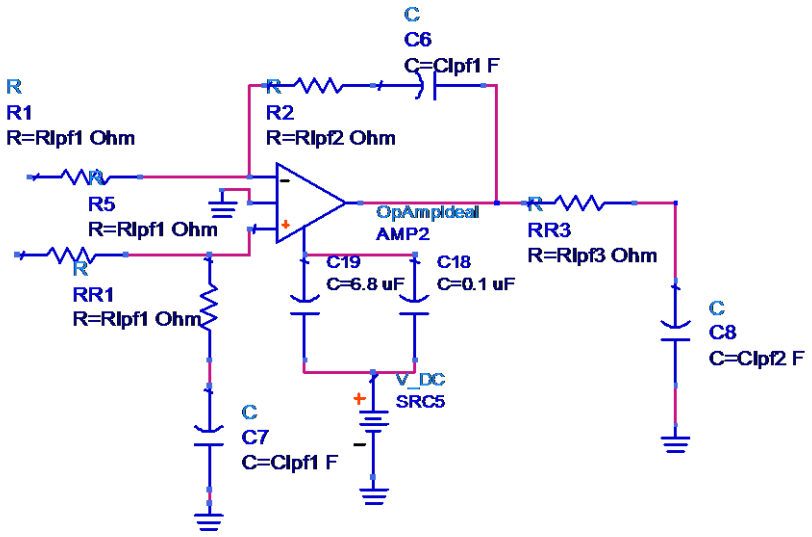


FIGURE 3.4: Active Loop Filter Design

As $F_{ref} = 70Mhz$ and N divider is equal at 50, then $F_synt = 3.5Ghz$. Using HMC507LP5 VCO we can get two outputs at $F_0 = 7Ghz$ and $F_0/2 = 3.5Ghz$. The VCO have good phase noise that is of -115 dBc/Hz and output power is +13.5 dBm. The function of the VCO is generating the oscillator signal of a desired frequency. The output signal at 3.5 GHz is the loop in the PLL. The output signal at 7 GHz is pass by a power splitter GP2X1+ (Mini-circuits, 2800-7200 MHz), obtained two signals at 7 GHz. One of the output at 7 GHz is into frequency divider by 3. The frequency divider selected is the HMC437MS8G for generated the LO signal at 2.33 GHz. In the Appendix B, the details of specifications of the components in the system are shown.

3.3.3 Loop Filter Design

The principal function of loop filter is to eliminate high frequency components to maintain pure DC input to the VCO. Loop filter is important for phase noise response of the PLL therefore it should be carefully designed. In the figure 3.4 the active filter design is shown. The values of active third order loop filter components for different loop bandwidth and phase margins are calculated using MATLAB. The details of calculations by a MATLAB script of the loop filter designed are given in Appendix C. Different loop bandwidths and phase margins are simulated in ADS as illustrated in figure 3.5. The results are compared in relation to total phase noise on PLL as shown in the table 3.3.

Loop bandwidth is an important design parameter in PLL. The Optimum bandwidth is found as the intersection of the noise floor of close-in noise and VCO noise curve which in this case is 2.35 MHz. This is analyzed in detail in Chapter 4. As bandwidth is

TABLE 3.3: Phase Noise for different loop bandwidths and phase margins

Phase Margin	**Loop Bandwidth**	**Phase Noise Total**						
		100 Hz	**1 KHz**	**10 KHz**	**100 KHz**	**1 MHz**	**10 MHz**	**100 MHz**
45°	10 KHz	-89.382	-93.726	-92.607	-93.400	-105.998	-126.410	-153.656
50°	10 KHz	-89.166	-93.002	-91.803	-86.499	-114.920	-134.986	-154.865
60°	10 KHz	-88.593	-91.526	-90.710	-83.205	-114.863	-134.985	-154.865
45°	100 KHz	-90.779	-109.230	-112.749	-103.531	-114.254	-134.979	-154.865
50°	100 KHz	-90.778	-109.122	-112.114	-103.646	-114.159	-134.978	-154.865
60°	100 KHz	-90.778	-109.122	-112.114	-103.646	-114.159	-134.978	-154.865
45°	120 KHz	-90.782	-109.456	-114.065	-104.955	-114.065	-134.977	-154.865
45°	150 KHz	-90.785	-109.632	-115.323	-106.765	-113.752	-134.973	-154.865
45°	250 KHz	-90.788	-109.856	-116.857	-111.697	-112.745	-134.960	-154.865
45°	1.5 MHz	-90.789	-109.984	-117.683	-117.929	-118.137	-134.567	-154.864
45°	2.35 MHz	-90.789	-109.789	-117.689	-117.689	-117.680	-134.535	-154.864
60°	2.35 MHz	-90.789	-109.983	-117.669	-117.841	-119.542	-134.779	-154.781
45°	50 MHz	-90.789	-109.988	-117.713	-117.980	-119.632	-134.758	-154.810
50°	50 MHz	-90.789	-109.985	-117.683	-117.856	-119.541	-134.760	-154.797
60°	50 MHz	-90.789	-109.983	-117.669	-117.841	-119.542	-134.779	-154.781

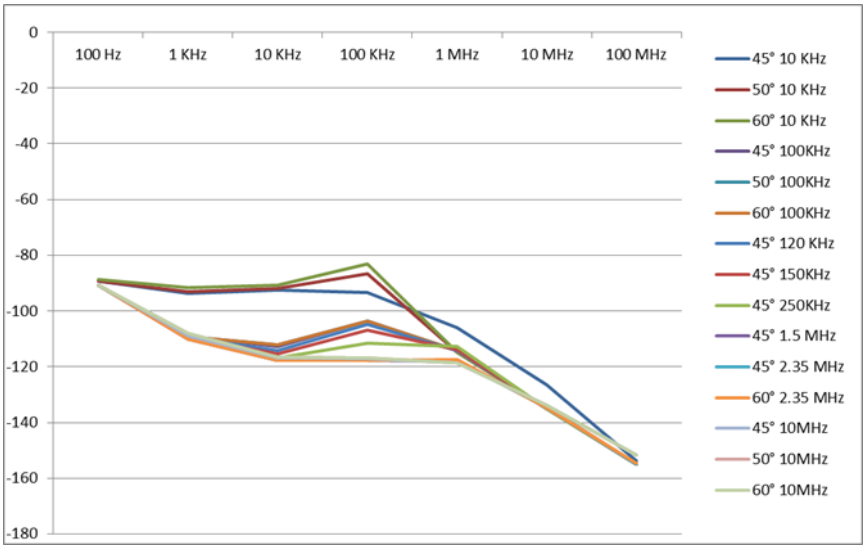


FIGURE 3.5: Phase Noise for Different Loop Bandwidth and Phase Margin

made smaller total phase noise performance approximates ultra-low phase noise VCO performance. The phase margin selected is of 45°. This phase margin reduces the phase noise as shown in the table 3.3.

The filter components values with phase noise performance, i.e with loop bandwidth (BW) of 2.35 MHz and 45° of phase margin (ϕ) are showed in the table 3.4.

TABLE 3.4: Calculated values of Filter Components

Loop Bandwidth	Phase Margin	Components	Values
2.35 MHz	45°	C_{lpf1}	470 pF
		C_{lpf2}	2.0 nF
		R_{lpf1}	318.06 Ohm
		R_{lpf2}	347.88 Ohm
		R_{lpf3}	14.02 Ohm

TABLE 3.5: HMC699LP5 Programming Truth Table

Division Ratio N	**A Counter Decimal Set**	**Swallow S Decimal Set**	**(LSB) A**	**A1**	**A2**	**A3**	**A4**	**A5**	**(LSB) S0**	**S1**	**S2**
50	5	2	1	0	1	0	0	0	0	1	0

3.3.4 Operational Settings Synthesizer

The HMC699LP5 component is programmed with a reference signal of 70 MHz and N = 50. The decimal value of counter A and counter S for N=50 are:

$$A = int\frac{N}{8} - 1 = 5 \tag{3.2}$$

$$S = N - 8(A + 1) = 2 \tag{3.3}$$

Since the calculated value of A and S satisfy the condition of $A + 1 \geq S$ then N=50 is usable division ratio. HMC699LP5 programming truth table, continuous division ratio is showed in the table 3.5.

The analysis on the simulations and results in the design the LO generation circuit are studied in the Chapter 4.

3.4 LO DISTRIBUTION DESIGN

Previous work was presented in the area of LO distribution using synchronous Voltage Control Oscillators or using multiple PLL or a single PLL. This work design with commercial components several architecture for LO distribution in the system for accurately amplitude and phase for each transceiver path in a phased-array radar. The aim of this research is to design and analyze several architectures and chose the best that improves

stability, has lower power consumption, lower cost to be used in solid state X-band Radar.

The proposed architectures based on a single frequency synthesizer for distributes 24 Local oscillator (LO) signals at 2.33 GHz, and 24 LO signals at 7 GHz synchronized. The system is composed of one feedback loop, for correct of phase and frequency of the signals generated. Thus, the LOs signals are distributed with same phase and amplitude to each column of the transceiver in order to achieve coherence in the system. These signals are necessary for the up-converter and down-converter of each column of T/R of dual polarized Doppler solid state radar.

In the next sections first is provides a description on the two design developed for LOs distribution using a single chip synthesizer. After a description in the design for LOs distribution using N-synchronous Voltage Control Oscillators is presented. The power consumption and budget for each design are presented in this chapter.

3.4.1 Architecture One: LO Distribution using a single PLL

The architectures proposed defined the design of the synchronization module for the array of 24 channels. For this architecture was studied two designs.

- The first design consist in taking the output Local Oscillators (LO*'*s)signals provides by the LOs generation circuit. The LOs generation circuit designed provides two LOs signals at 7 GHz and at 2.33 GHz, as was presented in the previous sections. The LO signal at 2.33 GHz have -1 dBm of power after of pass by frequency divisor as shown in the figure 3.6. The signal at 2.33 GHz Requires be amplified and filter for eliminated the image component produced by division frequency with $N = 3$. The amplifier used is a Low Phase Noise Amplifier (LPNA) HMC606LC5, which provides ultra low phase noise performance of -160 dBc/Hz at 10 kHz offset and provides 13.5 dB of signal gain. This signal is then passed to the filter HMC891LP5, which is a band pass filter which a selectable passband frequency. The center frequency can be varied between 2 and 3.9 GHz by applying an analog tune voltage between 0 and 14 V. From this process, a pure and stable LO signal at 2.33 GHz is obtained. The power of the signal at 7 GHz is of 9.8 dBm and 2.5 dBm at 2.33 GHz. Several levels of amplification are necessary to obtained the LO distribution to 24 channels at 2.33 GHz and 7 GHz. The amplifier selected is the HMC606LC5 with 13.5 dB of gain, and has excellent low phase noise of -160 dBc/Hz at 10 KHz . The signal at 7 GHz amplified is into to power divider (GP2X1+). The power divider used by distribution at 7 GHz has 3.7 dB of loss.

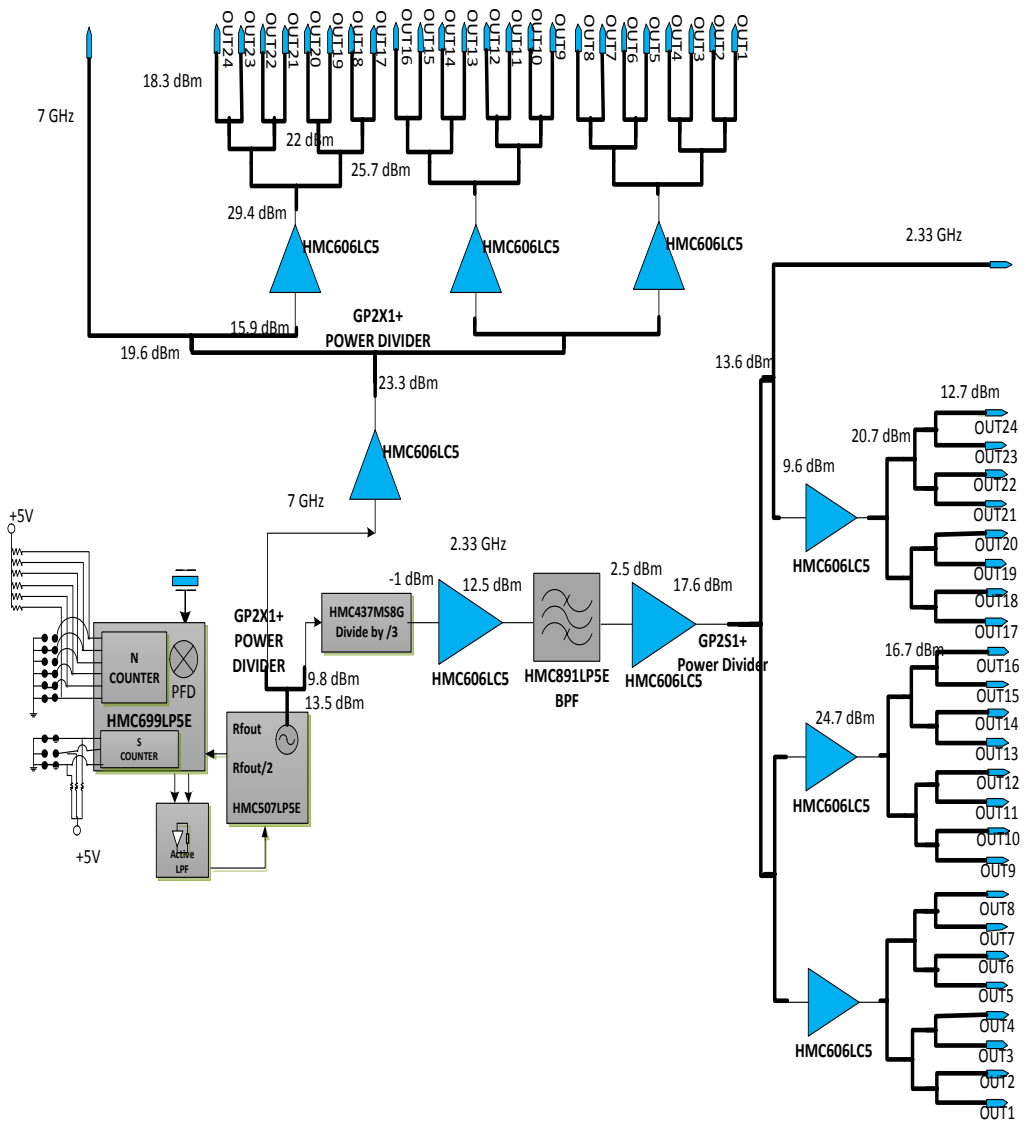


FIGURE 3.6: LO Distribution architecture 1.

Now, we have two signals at 7 GHz with 19.6 dBm of power each one. These two signals are divided by power divider, giving four signals that then amplified by HMC606LP5. Then this continued and divided by power divider (GP2X1+) to obtain 24 signals at 7 Ghz. Each output signal has a power of 18.3 dBm at 7 GHz. The signal of 2.33 GHz is also is divided by power divider (GP2S1+, Mini-circuit). The GP2S1+ has 4.2 dB of loss. Due to this is need amplifier the signal for have 24 LO signals.The amplifier used for the distribution of LO at 2.33 GHz is the same that used for amplifier the LO signal at 7 GHz. It amplifier is the HMC606LP5. Then this signal is divided by power divider (GP2S1+) to obtain 24 signals at 2.33 Ghz with 12.7 dBm of power for each column.

- In the second design is used of same topology of LO distribution using a single PLL.

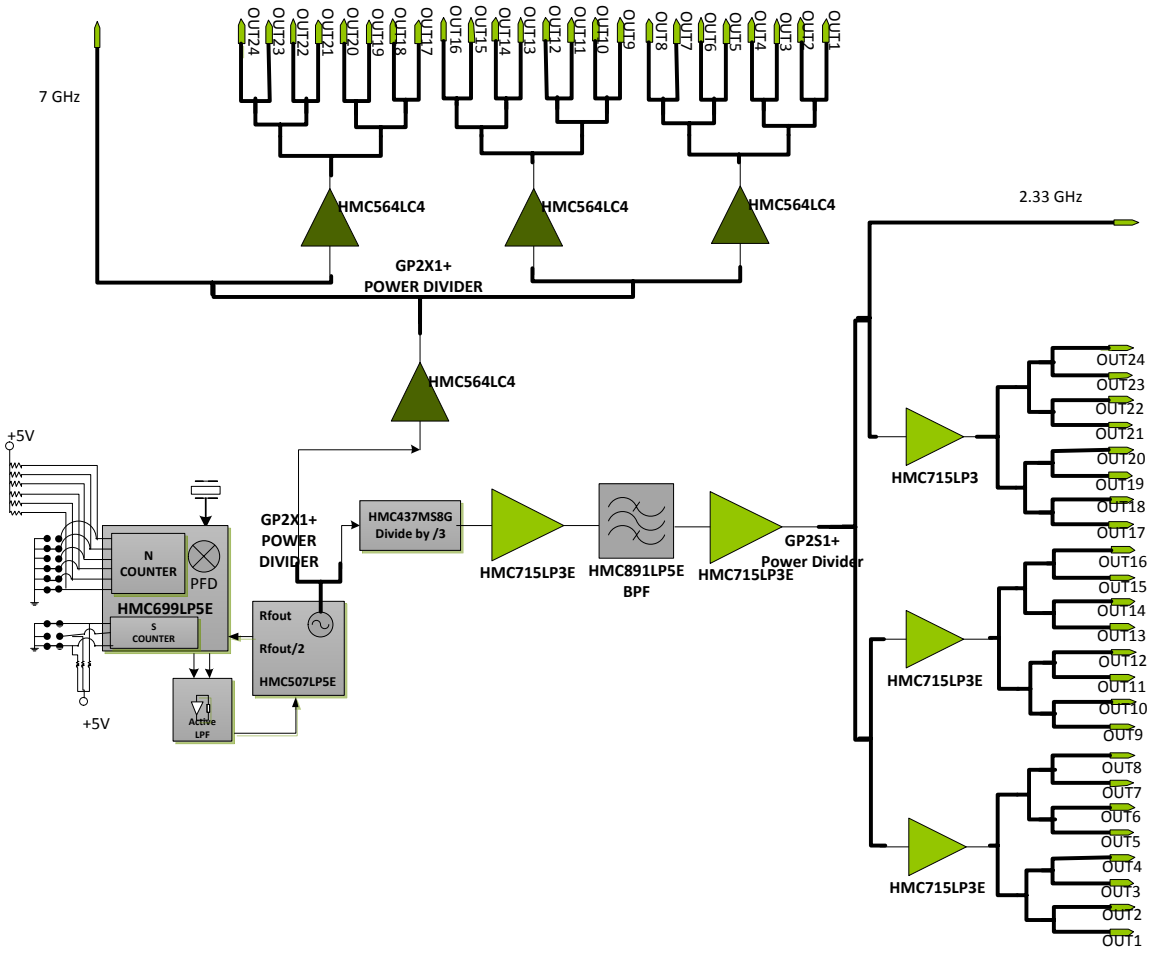


FIGURE 3.7: LO Distribution architecture 1 modified.

The modifications was basically change of amplifier LPNA HMC606LP5 selected by the Low Noise Amplifier (LNA) HMC715LP3 for amplified the signal at 2.33 GHz. The new amplifier selected HMC715LP3 have a noise figure of 0.9 dB and gain of 19 dB. Also the amplifier used on the signals at 7 GHz was changed by the LNA amplifier HMC564LC4 with gain of 17 dB and noise figure of 1.8 dB. The output power of each column for the signal at 2.33 GHz is of 25 dBm and the signal at 7 GHz of output power for each column is of 19 dBm. In the figure 3.7 shown the design, the changes are marked with color green.

- **Power Consumption**

TABLE 3.6: Power Consumption: first design of architecture one based a single PLL.

Architecture One: LO Distribution using only a PLL			
Component	**Current (mA)**	**Vdd (V)**	**Power(W)**
Synthesizer	69 x 8	5	2.76
VCO	225	5	1.125
OPAM	10	3	0.0030
LPNA	64 x 2 x 9	5	5.760
Freq. Div. /3	69	5	0.345
TOTAL			10.02

TABLE 3.7: Power Consumption: second design of architecture based a single PLL.

Architecture One: LO Distribution using only a PLL			
Component	**Current (mA)**	**Vdd (V)**	**Power(W)**
Synthesizer	69 x 8	5	2.76
VCO	225	5	1.125
OPAM	10	3	0.0030
LNA 7 GHz	75 x 2 x 4	3	1.800
LNA 2.33 GHz	47 x 2 x 5	3	1.410
Freq. Div. /3	69	5	0.345
TOTAL			7.47

The power consumption of each active component in the system is shown in table 3.9. The total current draw is 2.008 Amperes, and the total power consumption is 10.020 Watts. It is for the first design as is showed in the table 3.9. In the second design for the architecture one the total current draw is 1.926 Amperes, and the total power consumption is 7.47 watts as is showed in the table 3.7.

- **Costs**

  The following table 3.8 shows the preliminary cost of the components requirement in the design LO distribution architecture with only a PLL. The table includes the cost of LO generation circuit designed in previous sections. This represents the total cost of the components selected for completed synchronization module for the architectures based a single PLL of the Solid State Of The Grid (SSOTG)radar.

3.4.2 Architecture Two:LO distribution using N-synchronous Voltage Control Oscillators

This architecture is presented in the figure 3.8. This architecture consist that the output signal of filter loop is distributed to three Voltages Controlled Oscillator (VCO). The output signal of filter is DC and it is the voltage tune for VCO. The components used

TABLE 3.8: Costs architecture one and architecture one modified.

COSTS							
Architecture 1: based a single PLL							
				Design 1		**Design 2**	
Company	**Description**	**Piece Part**	**Price Per Piece**	**QTY**	**Subtotal**	**QTY**	**Subtotal**
Hittite	Synthesizer	HMC699LP5E	$86.100	1	$86.100	1	$86.100
Hittite	VCO	HMC507LP5E	$31.680	1	$31.680	1	$31.680
Texas Inst.	Opam	THS4031CDGN	$5.420	1	$5.42	1	$5.42
Hittite	Freq. Div. /3	HMC437MS8G	$19.350	1	$19.350	1	$19.350
Hittite	LPN Ampl.	HMC606LC5 (2-18)GHz	$78.720	9	$704.430	0	$0.000
Hittite	LNA	HMC715LP3E (2.1-2.9)GHz	$4.190	0	$0.000	5	$20.950
Hittite	LNA	HMC564LC4 (7-14)GHz	$24.190	0	$0.000	4	$96.796
Hittite	BPF	HMC891LP5E	$98.000	1	$98.000	1	$98.000
Minicircuit	Power Splitter two-way (2.8-7.2)GHz	$GP2X1+$	$1.490	25	$37.250	25	$37.250
Minicircuit	Power Splitter two-Way (0.5-2.5)GHz	$GP2S1+$	$1.490	25	$37.250	25	$37.250
Digikey	Conector SMA	J502-ND	$3.708	72	$266.976	72	$266.976
Digikey	Cap.4.7 μF, Tantalum	399-3696-1-ND	$0.294	20	$5.880	20	$5.880
Digikey	Cap. 2.2 μF, Tantalum	TLCK225M010-PTA	$1.663	3	$4.989	3	$4.989
Digikey	Cap. 100 pF, 0402 PKG	04023A101-FAT2A-ND	$0.400	30	$12.000	30	$12.000
TOTAL				**1,330.050**		**743.790**	

in this architectures are the same as used in the architecture one modified, but the distribution and amounts vary. The output power of each HMC507LP5 VCO is of 13.5 dBm. This signal is divided in two signals by power splitter GP2X1+. Then, to generate a signal at 2.33 GHz it is necessary to frequency divided by 3. The frequency divider used is the HMC437MS8G. This is the same frequency divider used in the others architecture and output is -1 dBm. Next,it is necessary to amplify the signal so that can be filtered and the image component produced by division can be eliminated. The amplifier used is the HMC715LP3, it has low noise figure of 0.9 dB and provides 19 dB of signal gain. Then, this signal is into to a filter HMC891LP5, which is a band pass filter which a selectable passband frequency, as was designed in the previous architecture. From this

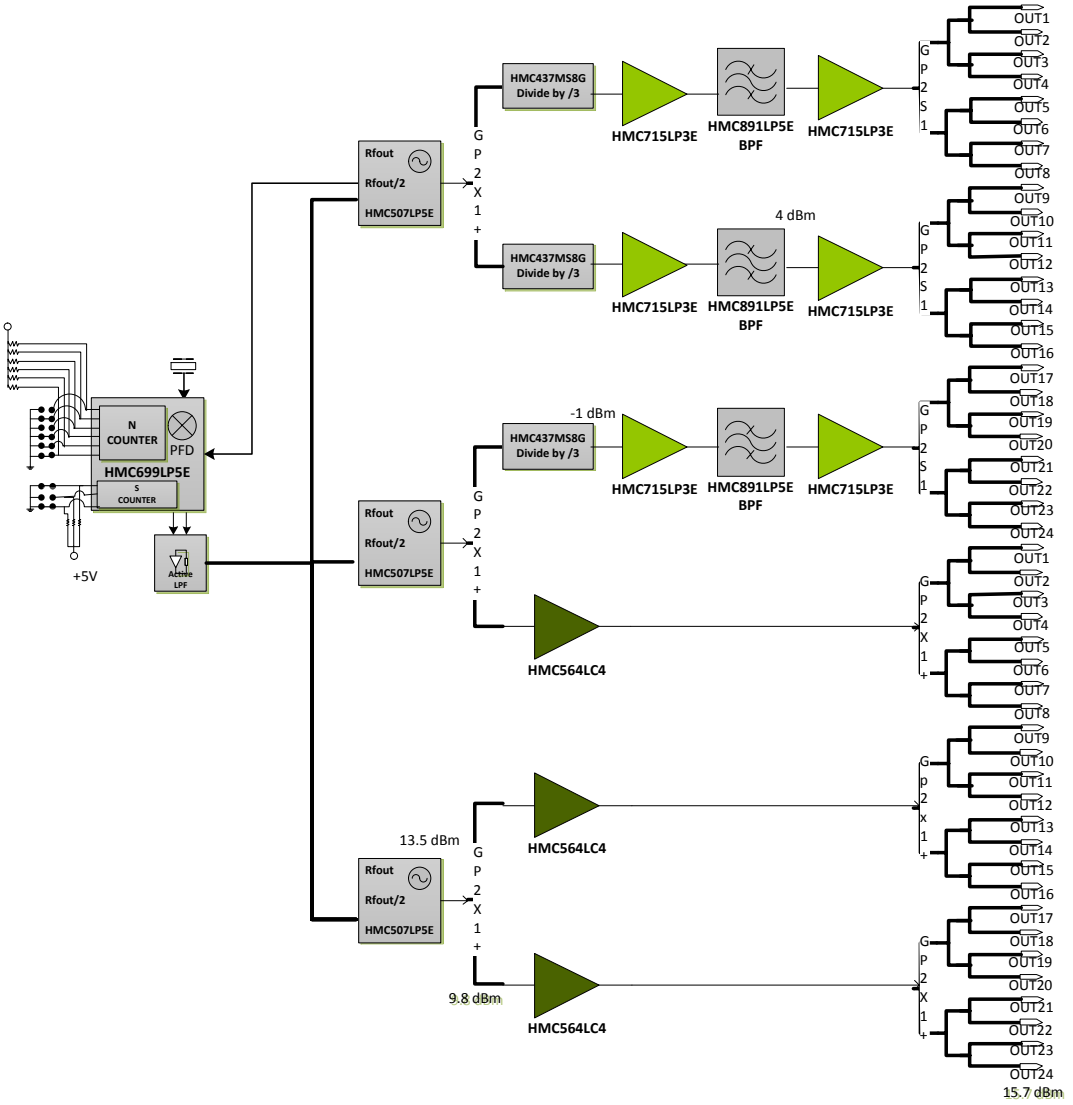


FIGURE 3.8: LO Distribution Architecture 2: LO distribution using synchronous Voltage Control Oscillators

form the other pure and stable LO at 2.33 GHz with 4 dB of power is obtained. It is needed to amplify the signals so that the LO distribution to 24 channels of transceiver. The amplifier used is the HMC715LP3. After, the signal is distributed to obtain 24 signals at 2.33 GHz through of GP2S1+ power splitter. Each output signal at 2.33 GHz has 11 dBm of power. The signal at 7 GHz is amplified first by HMC564LC4 low noise amplifier with gain of 17 dB and noise figure of 1.8 dB. The output signal amplified is distributed through of GP2X1+. Each output LO signal at 7 GHz has 15.7 dBm of power.

- **Power Consumption**

TABLE 3.9: Power Consumption architecture one.

Architecture two: LO Distribution using N- VCO and only a Frequency Synt.			
Component	**Current (mA)**	**Vdd (V)**	**Power(W)**
Synthesizer	69 x 8	5	2.76
VCO	225 x 3	5	3.375
OPAM	10	3	0.0030
LNA 7 GHz	75 x 2 x 3	3	1.350
LNA 2.33 GHz	47 x 2 x 6	3	1.692
Freq. Div. /3	69	5	0.345
TOTAL			9.552

The power consumption of each active component in the system is shown in table 3.9. The total current draw is 2.008 Amperes, and the total power consumption is 10.020 Watts. It is for the first design as is showed in the table 3.9. In the second design the total current draw is 1.926 Amperes, and the total power consumption is 7.47 watts as is showed in the table 3.7.

- **Costs**

  The following table 3.10 shows the preliminary cost of the components requirement in the design LO distribution architecture with three VCOs and only a synthesizer frequency. The table includes the cost of LO generation circuit designed in previous sections. This represents the total cost of the parts in a completed synchronization module for architecture two of the Solid State Of The Grid (SSOTG)radar.

The analysis on the simulations and results in the design the LO distribution circuit are studied in the Chapter 4.

TABLE 3.10: Costs architecture two.

COSTS					
Architecture 2:based N-VCOs					
Company	**Description**	**Piece Part**	**Price Per Piece**	**QTY**	**Subtotal**
Hittite	Synthesizer	HMC699LP5E	$86.100	1	$86.100
Hittite	VCO	HMC507LP5E	$31.680	3	$95.040
Texas Inst.	Opam	THS4031CDGN	$5.420	1	$5.420
Hittite	Freq. Div. /3	HMC437MS8G	$19.350	3	$58.050
Hittite	LNA	HMC715LP3E (2.1-2.9)GHz	$4.190	6	$25.140
Hittite	LNA	HMC564LC4 (7-14)GHz	$24.190	3	$72.750
Hittite	BPF	HMC891LP5E	$98.000	3	$294.000
Minicircuit	Power Splitter two-way (2.8-7.2)GHz	$GP2X1+$	$1.490	25	$37.250
Minicircuit	Power Splitter two-Way (0.5-2.5)GHz	$GP2S1+$	$1.490	25	$37.250
Digikey	Conector SMA	J502-ND	$3.708	72	$266.976
Digikey	Cap.4.7 μF, Tantalum	399-3696-1-ND	$0.294	20	$5.880
Digikey	Cap. 2.2 μF, Tantalum	TLCK225M010-PTA	$1.663	3	$4.989
Digikey	Cap. 100 pF, 0402 PKG	04023A101-FAT2A-ND	$0.400	30	$12.000
TOTAL					**1,021.850**

Chapter 4

Simulations and results

4.1 Introduction

In this chapter will cover the system simulations and results of the synchronization module. The synchronization module performance in terms of phase noise, power consumption, cost, and stability are addressed in detail. The section 4.2 presented the simulations results of LO generation. In the section 4.3 present of results of LO distribution. The general strategy for selected architecture for LO distribution is based in minimize of power consumption, cost, amplitude and phase stabilization .

4.2 Simulations LO Generation

Using the LO generation design described in section 3.3. The three high frequency PLL was designed to operate at frequencies of 3.5 GHz,it is the feedback signal in PLL. The other frequency generated is at 2.33 GHz, it is the LO_1 that required of transceiver radar, and at 7 GHz, that it is the other LO signal that it need for the system.

The loop filter was designed as a third-order active filter as is showed in the Chapter 3. This section analysed the result of the simulations evaluating the system performance in ADS environment. Primary are optimized the components values of filter trough of a loop analysis. For this know that loop bandwidth and phase margin calculated are of 2.35 MHz and 45 degrees, respectively.

For developed the simulation need the specification of VCO sensitivity of HMC507LP5 that is $K_{VCO} = 135MHz$ and the phase detector gain of HMC699LP5 synthesizer selected that is $K = 5/(2\pi)$. The system loops simulation of PLL designed are showed in the figure 4.1. In the part a. shown the model used for simulated close loop and the

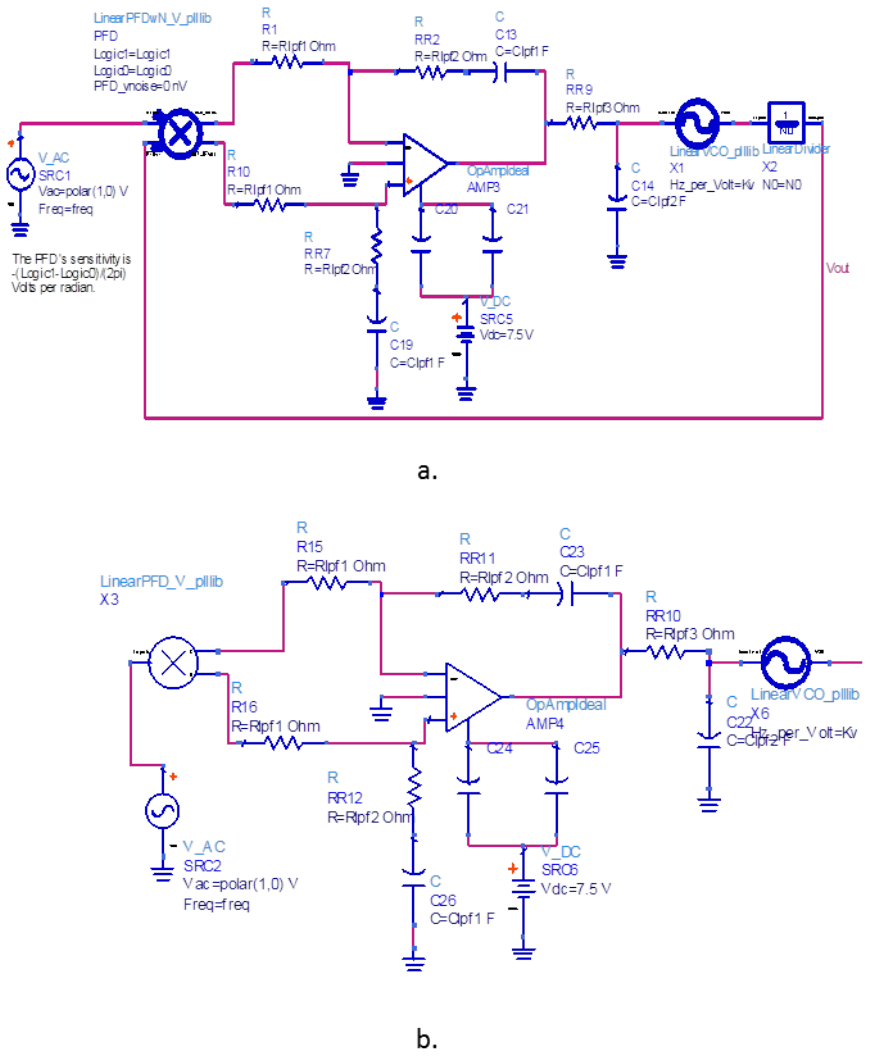


FIGURE 4.1: Loop Simulation a.Closed Loop and b. Open Loop Response

part b. shown of model open loop. The optimized values of the resistor and capacitor for of active loop filter are showed in the table 4.1.

Simulated circuit and filter response are shown in the figure 4.2. Bandwidth and phase margin can be viewed in open loop amplitude and phase plots. Note that at nearly 2.349 MHz offset open loop gain will be 0 dB and phase margin will be approximately 45° in close loop.

To analyse Phase noise contribution of the PLL was realized on ADS as shown the figure 4.3. Through of use of the equations (2.14)to (2.15 showed in the Chapter 2 are consider each contribution of the component. The response of phase noise of each component are observed in the Part a. of the figure 4.4. In the Part b. shown the results on loop bandwidth phase noise, and can be seen that of the reference signal and VCO dominates the characteristics of the noise curve. At loop bandwidth contribution

[h]

TABLE 4.1: Calculated, optimized and realized values of Filter Components

Filter component	Calculated Value	Optimized Value	Realization Value
C_{lpf1}	470 pF	472.7 pF	470 pF
C_{lpf2}	2.0 nF	2.004 nF	2 nF
R_{lpf1}	318.06 Ohm	319.17 Ohm	320 Ohm
R_{lpf2}	347.88 Ohm	348.34 Ohm	348 Ohm
R_{lpf3}	14.02 Ohm	13.96 Ohm	14 Ohm
Loop BW	2.35 MHz	2.345 MHz	2.349 MHz
Phase Margin	45°	45.2°	45.2°

in Part a. approximates to filter and VCO reducing the phase noise in VCO. Therefore a decrease in the slope is observed at the loop bandwidth. After that frequency VCO becomes the dominant factor of phase noise as expected and beyond 2.3 MHz response completely follows the phase noise of the VCO. This is an expected behaviour as analysed previously when of system is optimized.

Simulated transient responses of frequency VCO tune voltage versus time, phase frequency detector outputs and VCO Frequency versus Time with the objective of obtaining frequency stabilization characteristics is as shown (a), (b) and (c)in the figure 4.5. Results show that the system needs less than $2\mu s$ to lock to both frequency and phase. Lock time is a critical issue in high speed circuits which requires switching frequency of oscillation in a restricted time interval as in the radar system.

4.3 Simulations LO Distribution

A group of LO distribution architectures were designed in the section 3.4 . In this section will to investigate stability. The architectures designed were two. Two design were realized for architecture that use a single PLL for LOs distribution as is presented in the section 3.4.1. The second architecture for LO distribution use three synchronous VCOs with a single frequency synthesizer was presented in the section 3.4.2. All the architectures designed were made with commercial components with a low current, low residual phase noise, low power consumption and low cost.

The stability analyses are based on the phase and amplitude characteristics for the 24 LO signals at 7 GHz and 24 LO signals at 2.33 GHz of each architecture proposed. The calculus of errors of phase and amplitude for each channel are based in the average value the N-channels, i.e. the quantity of error is equal a the value phase or amplitude of each channel least the average value of amplitude or phase for the N-channels.

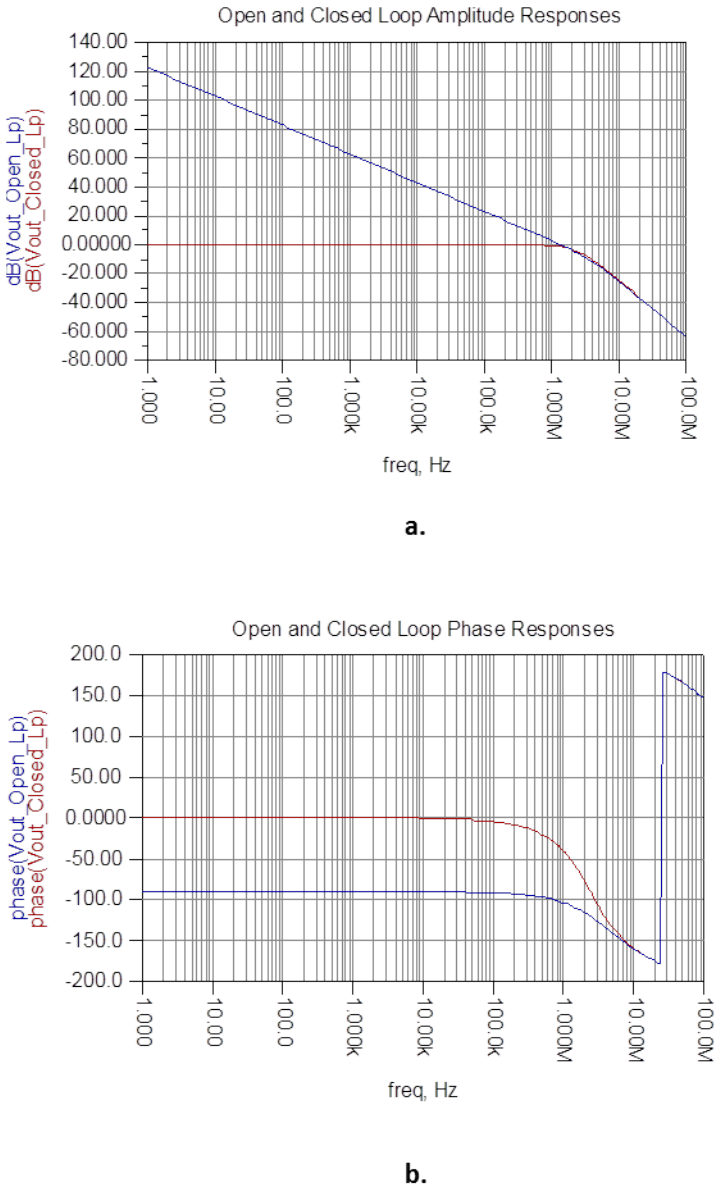


FIGURE 4.2: Closed and Open Loop Response. a. Open and Close Loop Amplitude responses. b. Open and Close Loop Phase Response

The component that integrate the synchronization module are simulated in ADS, using measure SnP data (S2P, S3P)provided by the manufacture. The SnP data file format is also know as Touchstone format. SnP file contained S parameters meters for each data point frequency, with temperature specific and voltages for performance of the system.

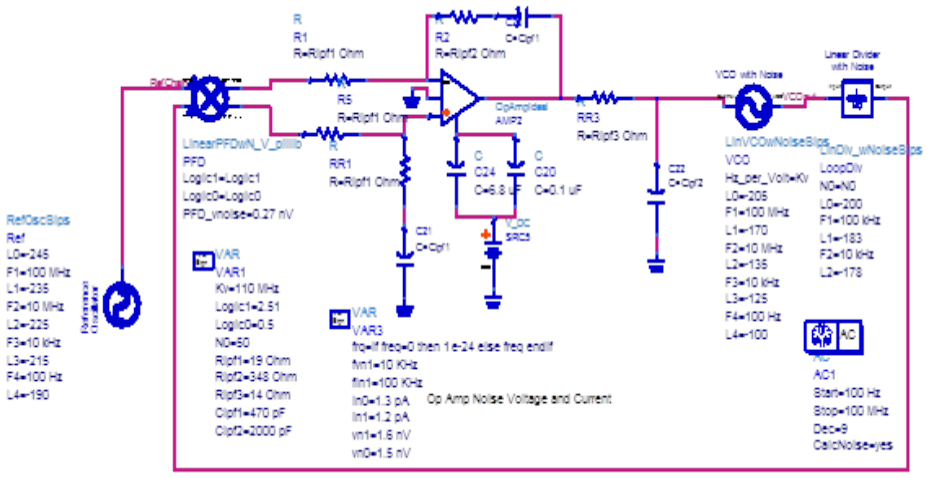


FIGURE 4.3: Phase Noise Simulation in ADS

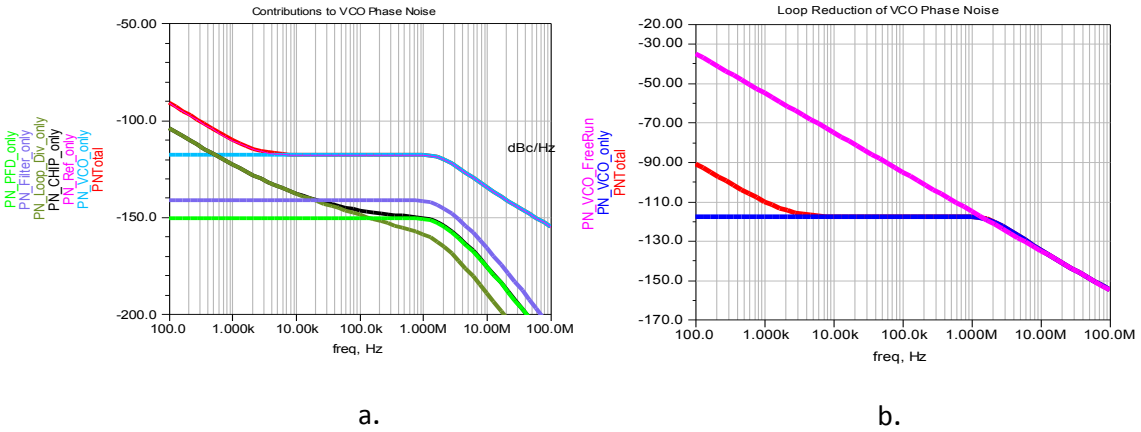
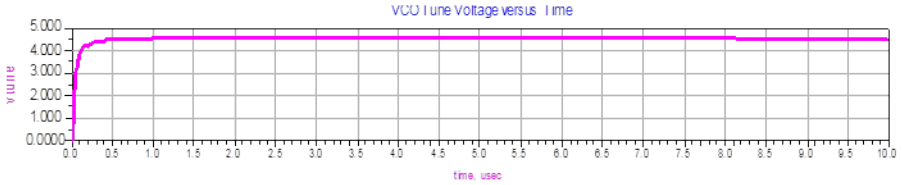
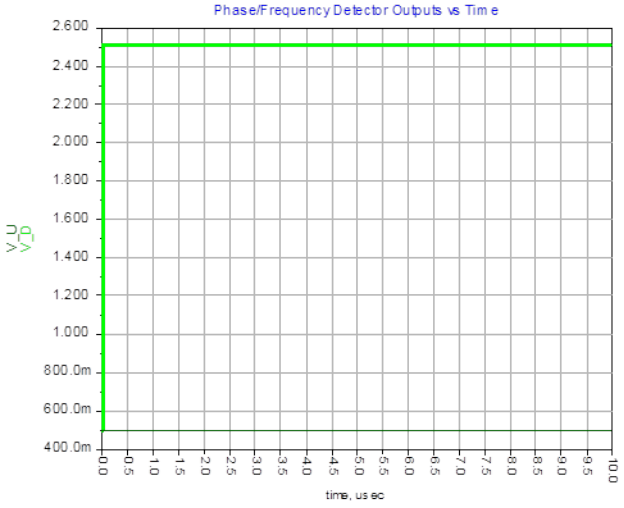


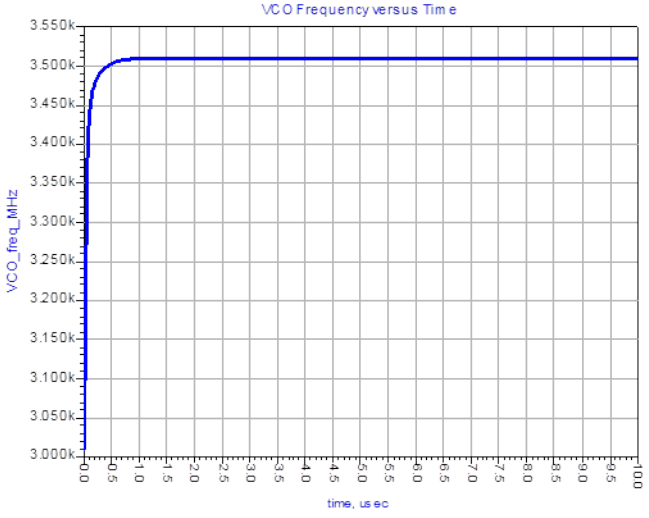
FIGURE 4.4: Response Phase Noise Simulation in ADS. Part a. contribution to VCO Phase Noise and Part b. Loop Reduction of VCO phase noise



a.



b.



c.

FIGURE 4.5: Transient Responses. a. VCO Tune Voltage versus Time. b. Phase/Frequency Detector Outputs vs Time and c. VCO Frequency versus Time

TABLE 4.2: Phase and amplitude errors in the architecture 1 at 7 GHz and at 2.33 GHz

	Architecture 1 at 7 GHz		**Architecture 1 at 2.33 GHz**	
Channel	Phase Error (Degrees)	Amplitude Errors(dB)	Amplitude Errors(dB)	Phase Error (Degrees)
1	−2.354	-0.070	0.129	4.270
2	−2.232	0.009	-0.086	2.973
3	−1.583	0.087	0.215	3.719
4	−1.462	0.166	1.64 E-04	2.422
5	−0.521	-0.035	0.180	1.675
6	−0.399	0.044	-0.035	0.378
7	0.250	0.122	0.266	1.124
8	0.372	0.201	0.050	-0.173
9	−1.523	-0.037	0.109	3.042
10	−1.402	0.042	-0.106	1.745
11	−0.753	0.200	0.195	2.491
12	−0.631	0.121	-0.020	1.194
13	0.310	-0.002	0.159	0.447
14	0.432	0.077	-0.056	-0.850
15	1.081	0.155	0.245	-0.104
16	1.203	0.235	0.030	-1.401
17	−0.212	-0.211	-0.120	-0.647
18	−0.090	-0.300	-0.335	-1.944
19	0.559	-0.143	-0.034	-1.199
20	0.681	-0.063	-0.249	-2.496
21	1.622	-0.265	-0.069	-3.242
22	1.744	-0.186	-0.285	-4.539
23	2.393	-0.108	0.016	-3.794
24	2.515	-0.028	-0.199	-5.091

4.3.1 LO Distribution using a single PLL

Simulations for this array were used to compare of the different phase and amplitude in each column of synchronization module and calculated the errors in each topology used. The phase errors are presented in the table 4.2. The maximum phase for this architecture is of 2.515° present in the channel 24 and the minimum phase error is of 0.09° present in the column 18 of the system. This architecture at 7 GHz present a standard deviation of phase of 1.33°.

In amplitude the system present minimums errors, have been the maximum error in absolute value is equal to 0.3 dB and the minim amplitude error is of 0.002 presented in the column 13 of system. The standard deviation of amplitude in this architecture is of 0.147 dB.

TABLE 4.3: Phase and amplitude errors at 7 GHz and at 2.33 GHz are presented for the second design by the architecture based a single PLL

	7 GHz		**2.33 GHz**	
Channel	Phase Error (Degrees)	Amplitude Errors(dB)	Amplitude Errors(dB)	Phase Error (Degrees)
1	−1.432	-0.095	-0.060	3.763
2	−1.310	-0.015	-0.275	2.466
3	−0.661	0.063	0.025	3.211
4	−0.539	0.142	-0.190	1.914
5	0.401	-0.06	-0.010	1.168
6	0.523	0.020	-0.025	-0.129
7	1.172	0.098	0.076	0.616
8	1.294	0.177	-0.139	-0.681
9	−0.384	-0.046	-0.078	2.072
10	−0.262	0.033	-0.293	0.775
11	0.387	0.191	0.008	1.520
12	0.509	0.112	-0.207	0.224
13	1.450	-0.011	-0.027	-0.523
14	1.572	0.068	-0.242	-1.820
15	2.221	0.147	0.059	-1.075
16	2.343	0.226	-0.157	-2.371
17	−2.209	-0.188	0.256	0.830
18	−2.087	-0.267	0.041	-0.246
19	−1.438	-0.11	0.342	0.279
20	−1.316	-0.030	0.127	-1.018
21	−0.375	-0.232	0.307	-1.764
22	−0.254	-0.153	0.092	-3.061
23	0.395	-0.075	0.393	-2.316
24	0.517	-0.005	0.177	-3.613

The output signal of this architecture at 2.33 GHz are shown in the figure **??**. The maximum phase error presented is of 5.091° present in the column 24 and the minimum phase error is of 0.104° present in the channel 15 as can be observed in the table 4.2. The maximum amplitude error is of 0.335 dB in the column 18 and the minim amplitude error is of 1.64 E-04 dB present in the output 4. The standard deviation of phase is of 2.55° and for the amplitude is of 0.163 dB.

The result of stabilization in amplitude and phase for the second design of this architecture are showed in the table 4.3. The data of phase at 2.33GHz present a standard deviation of 1.9°, and a standard deviation of amplitude of 0.19 dB. The 24 outputs signals at 7 GHz for this design present a standard deviation of phase of 1.24° and a standard deviation on the data of amplitude of 0.13 dB. The second design presented for architecture based in only a PLL have best stabilization in phase and amplitude with respect to the first designed present for this architecture.

TABLE 4.4: Phase and amplitude errors in the architecture 2 at 7 GHz and at 2.33 GHz

	Architecture 2 at 7 GHz		**Architecture 2 at 2.33 GHz**	
Channel	Phase Error (Degrees)	Amplitude Errors(dB)	Amplitude Errors(dB)	Phase Error (Degrees)
1	−1.258	0.032	0.016	4.612
2	−1.137	0.111	-0.199	3.316
3	−0.488	0.190	0.101	4.061
4	−0.366	0.264	-0.114	2.764
5	0.575	-0.067	0.066	2.018
6	0.697	0.146	-0.149	0.721
7	1.346	0.225	0.152	1.466
8	1.468	0.304	-0.063	0.169
9	−0.210	0.081	-0.001	2.922
10	−0.088	0.160	-0.217	1.625
11	0.561	0.318	0.084	2.370
12	0.683	0.239	-0.131	1.073
13	1.624	0.116	0.049	0.327
14	1.746	0.195	-0.166	-0.970
15	2.394	0.274	0.135	-0.225
16	2.516	0.353	-0.080	-1.521
17	−2.621	-0.044	0.101	-0.869
18	−2.499	-0.521	-0.111	-2.166
19	−1.85	-0.363	0.190	-1.421
20	−1.768	-0.284	-0.025	-2.718
21	−0.788	-0.486	0.155	-3.464
22	−0.666	-0.407	0.060	-4.761
23	0.017	-0.328	0.240	-4.016
24	0.105	-0.249	0.025	-5.313

4.3.2 LO distribution using N-synchronous Voltage Control Oscillators

The result obtained for this architecture at 7 GHz is showed in the table 4.4 . In this architecture is analyzed that the signals separated by VCO have large phase differences. 340.885° is of maximum error and the minimum error is of 0.122° as can be observed in the table 4.4. The results of this architecture not has phase stable in the system.

4.3.3 Results

In the table 4.5 are compares the results of three designs for distribution LOs for a phase array radar at X-band.

For the calculus of output power was need characterize of gains and loss each component with S-parameters that provided by the manufacturer or data-sheet. On the calculus

TABLE 4.5: results obtained of each architecture

Parameter	**Freq**	**Architecture 1**	**Architecture 1 MOD**	**Architecture 2**
P_{OUT}	2.33 GHz	12.7 dBm	25 dBm	11 dBm
P_{OUT}	7 GHz	18.3 dBm	19 dBm	15.7 dBm
Cost		$1,330.050	$743.900	$1,021.850
Power Consumption		10.200 W	7.470 W	9.552 W
Phase Error	2.33 GHz	2.558°	1.903°	2.726°
Phase Error	7 GHz	1.330°	1.246°	1.402°
Amplitude Error	2.33 GHz	0.163 dB	0.193 dB	0.127 dB
Amplitude Error	7 GHz	0.147 dB	0.130 dB	0.273 dB

of power consumption, was take the absolute maximum ratings of each component that require a source of voltage, the details of this calculus are presented in the section 3.4 and in the same section the budgets for each architecture are presented detail. In the section 4.3 the calculus of phase and amplitude errors for each column of the architectures design was presented. The variation in phase between columns of synchronization module is due to variations in tolerance manufacture of the components. As each signal is passed through of several components increase the differences and producing errors in phase and amplitude.

In general the results obtained in percentages for the architectures research are as follows:

- The second design for the architecture 1 based in only a PLL for the distribution of local oscillators is best 96.8% that the first design presented for this architecture and a 127% best that the architecture 2 that is the topology based in N - VCOs in power output for each Local Oscillator (LO) signal at 2.33 GHz.
- The second design for the architecture 1 is best 3.8% that the first design presented for architecture 1 and a 21.8% best that the architecture 2 in power output for each Local Oscillator (LO) signal at 7 GHz.
- The second design for the architecture 1 provides 78.79% of reduction in cost that the first design presented for architecture 1 and 37.36% of reduction in cost with respect to the architecture 2.

- The second design for the architecture 1 provides 34.41% of reduction in phase errors at 2.33 GHz that the first design presented for architecture 1 and 43.24% of reduction in phase errors at 2.33 GHz with respect to the architecture 2.
- The second design for the architecture 1 provides 6.7% of reduction in phase errors at 7 GHz that the first design presented for architecture 1 and 12.52% of reduction in phase errors at 7 GHz with respect to the architecture 2.
- The architecture 2 provides 28.34% of reduction in amplitude errors at 2.33 GHz that the first design presented for architecture 1 and 51.96% of reduction in amplitude errors at 2.33 GHz with respect to the second design of the architecture 1.
- The second design for the architecture 1 provides 13.07% of reduction in amplitude errors at 7 GHz that the first design presented of the architecture 1 and 110% of reduction in amplitude errors at 7 GHz with respect to the architecture 2.

Each design of architectures based on PLL for the distribution of LO signals at 7 GHz and at 2.33 GHz was studied it behaviour in phase and amplitude stability, lower power consumption, output power and lower cost. Agree to analysis realized the architecture selected for the build of synchronization module, is the second design for the architecture one based a single PLL. The outputs signal of synchronization module are showed in the figure 4.6

4.4 Layout

Simulated PLL and optimized phase noise in the LO generation circuit and selected the best architecture for the distribution of LOs signals, the following step is generate the layout of synchronization module. The synchronization module present 9 boards as shows the figure 4.7. The LO generation circuit is the central board. For the distribution of the 24-LO signals at 2.33 GHz and was need separated in four board. A board is for the amplifications levels, this board have 3 outputs. The other 3 board are the that distribute the 24 LO signals at 2.33 GHz. Each board of distribution have 8 outputs, these multiplied by 3 board are obtained the 24-LO signals at 2.33 GHz. For the distribution circuit of the 24-LO at 7 GHz was separated in four boards as the distribution circuit at 2.33 GHz.

A 50 transmission line on the board is essential to maximize power transfer. For the selection of material and transmission line was realized several calculus. A small example is observed in the table 4.6.

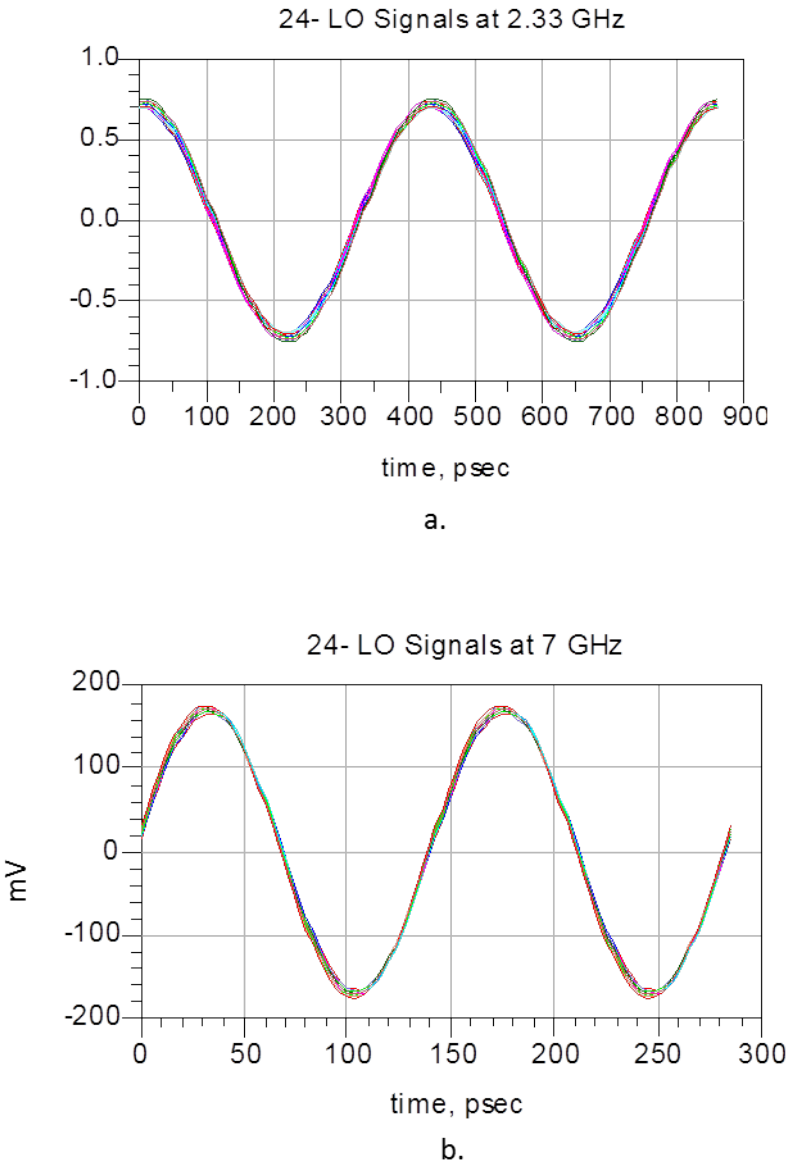


FIGURE 4.6: Output Signal for the design two by the architecture based a single PLL. Part a. LOs Signals at 2.33 GHz and Part b. LOs signals at 7 GHz

The transmission line selected for PCB design was Grounded Coplanar Waveguide (GCPW) because it have approximately 27% in reduction of width with respect to microstrip transmission lines. Also the CPWG present good characteristics such as low dispersion, good control of characteristics impedance [52] as was presented in the section 2.7. The one layer circuit board is implemented by using TMM10i material having 0.635 mm thickness and dielectric constant $\varepsilon_r = 9.8$. The CPWG transmission line with impedance at 50Ω is calculed according to ADS transmission line calculator, the dimension of GCPW can be shown as the figure 4.8. We set the parameters as below:

- Dielectric constant: $\varepsilon_r = 9.8$

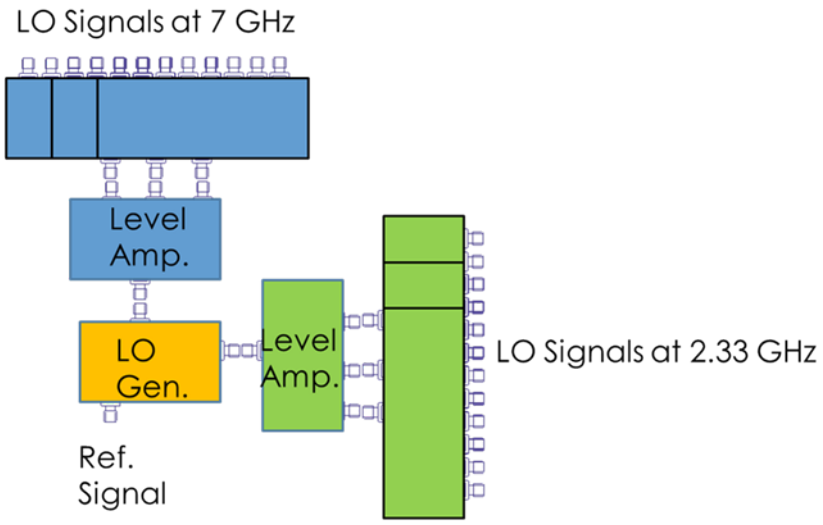


FIGURE 4.7: Synchronization module, board distribution

TABLE 4.6: Material and Transmission Line Selection. The calculus of transmission lines was realized for a impedance at 50Ω

Material	**Dielectric**	**Thickness**		**Microstrip**	**CPWG** (0.127 mm Gap)
TMM10i	**9.8**	**0.635 mm**	**line Width**	0.600 mm	0.254 mm
			1/4 wave length	2.870 mm	3.300 mm
R04350B	3.48	0.762 mm	**line Width**	1.730 mm	2.140 mm
			1/4 wave length	4.470 mm	4.200 mm
R03006	6.15	0.640 mm	**line Width**	0.940 mm	0.400 mm
			1/4 wave length	3.502 mm	4.000 mm

- Substrate High: h = 0.635 mm
- Conductor thickness: $T = 17\mu m$
- Operating frequency: f=7 GHz

The calculation obtained was the ground plane separation of G = 0.127 mm, and the conductor width W = 0.204731. To verify to that bandwidth the transmission line is match at 50Ω is simulated in ADS (see figure 4.9). The result obtained has good line match with a bandwidth of (1 GHz - 10 GHz) as show in the figure 4.11.

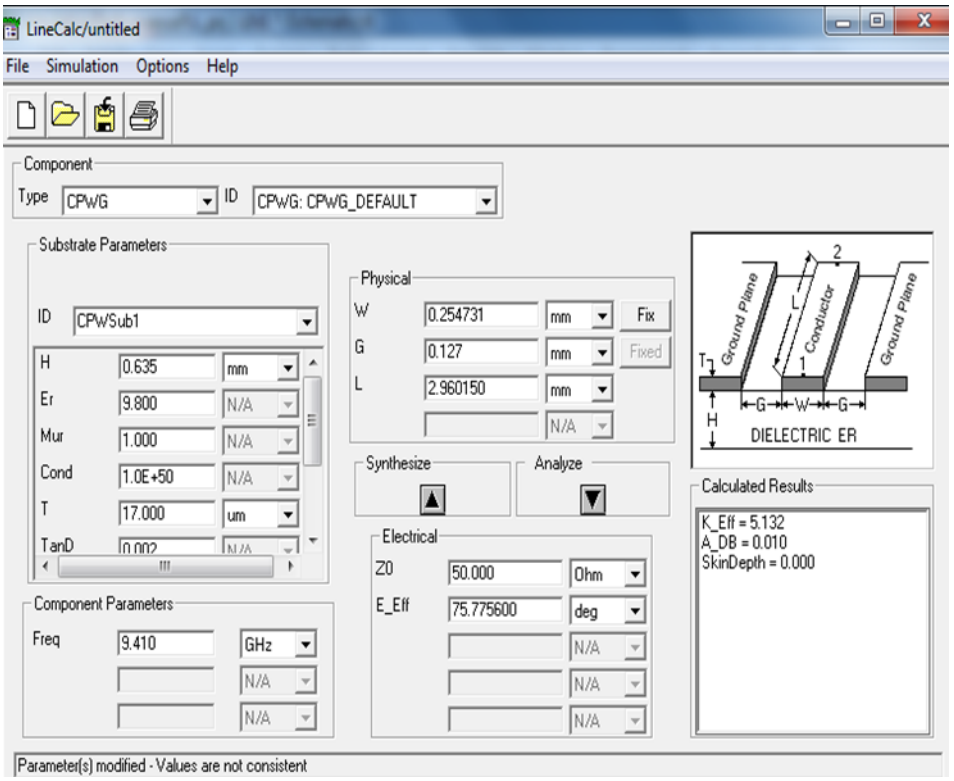


FIGURE 4.8: Line Calculator for CPWG

The synchronization module is designed to be work with 5 V supply and 3 V. The circuit layout PCB has been designed in ADS. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Surface mount components were selected because of the extremely low lead inductance associated with this technology. Also, because surface mount components are physically small, the layout can be very compact. This helps to minimize both stray inductance and capacitance. Tantalum power supply bypass capacitors at the power input pads help supply currents for rapid, large signal changes at the system output. A proper ground plane on both sides of the PCB is used; this provides low inductive ground connections for return current paths. In the area of the each components inputs pins. The board uses plated through vias (holes) to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the path to ground.

Based on the specifications given in the previous section, the first prototype for the synchronization module was made with available surface mount technology mainly from Hittite Microwave Corporation. The dimensions of PCB of LO generation are 12 cm x 8.3 cm (see figure 4.11). The dimensions of PCB active distribution LO at 2.33 GHz and 7 GHz are 1.8 cm x 7.55 cm (see figure 4.13). And the dimensions of LO Distribution for 2.33 GHz and 7 GHz are 12.5 cm x 7.55 cm. The system was realized modular because is necessary spaces between each out-port.

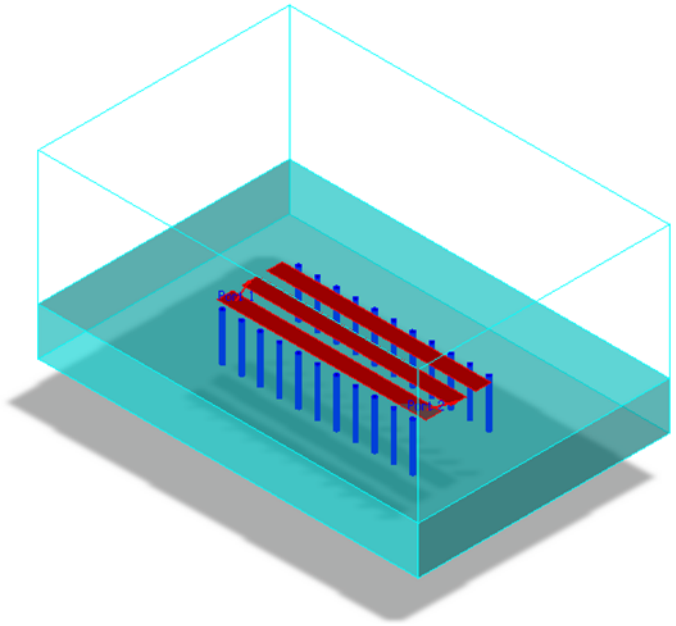


FIGURE 4.9: Coplanar Wave-ground Transmission Line implement

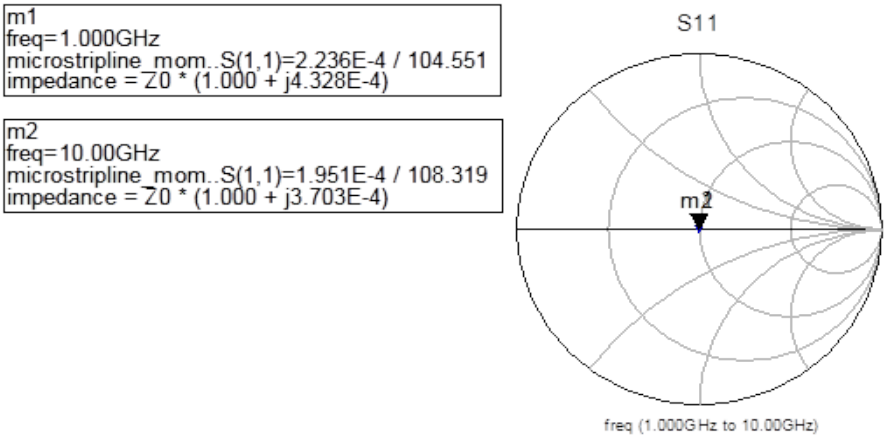


FIGURE 4.10: Results Simulation CPWG Transmission Line

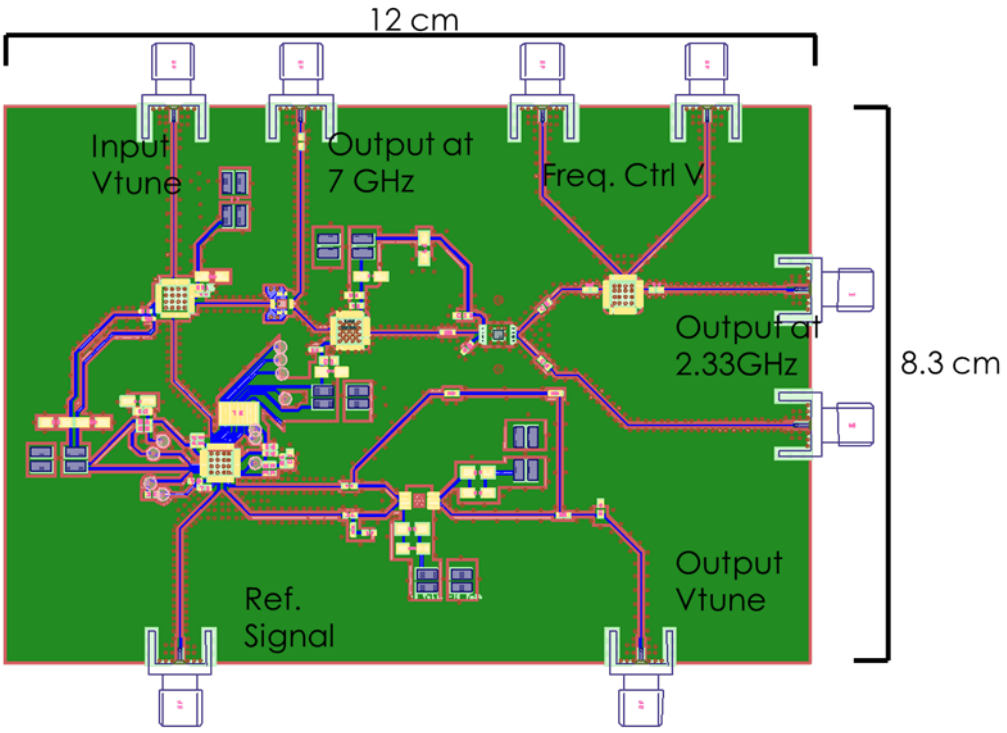


FIGURE 4.11: Layout LOs Generation at 2.33 GHz and at 7GHz

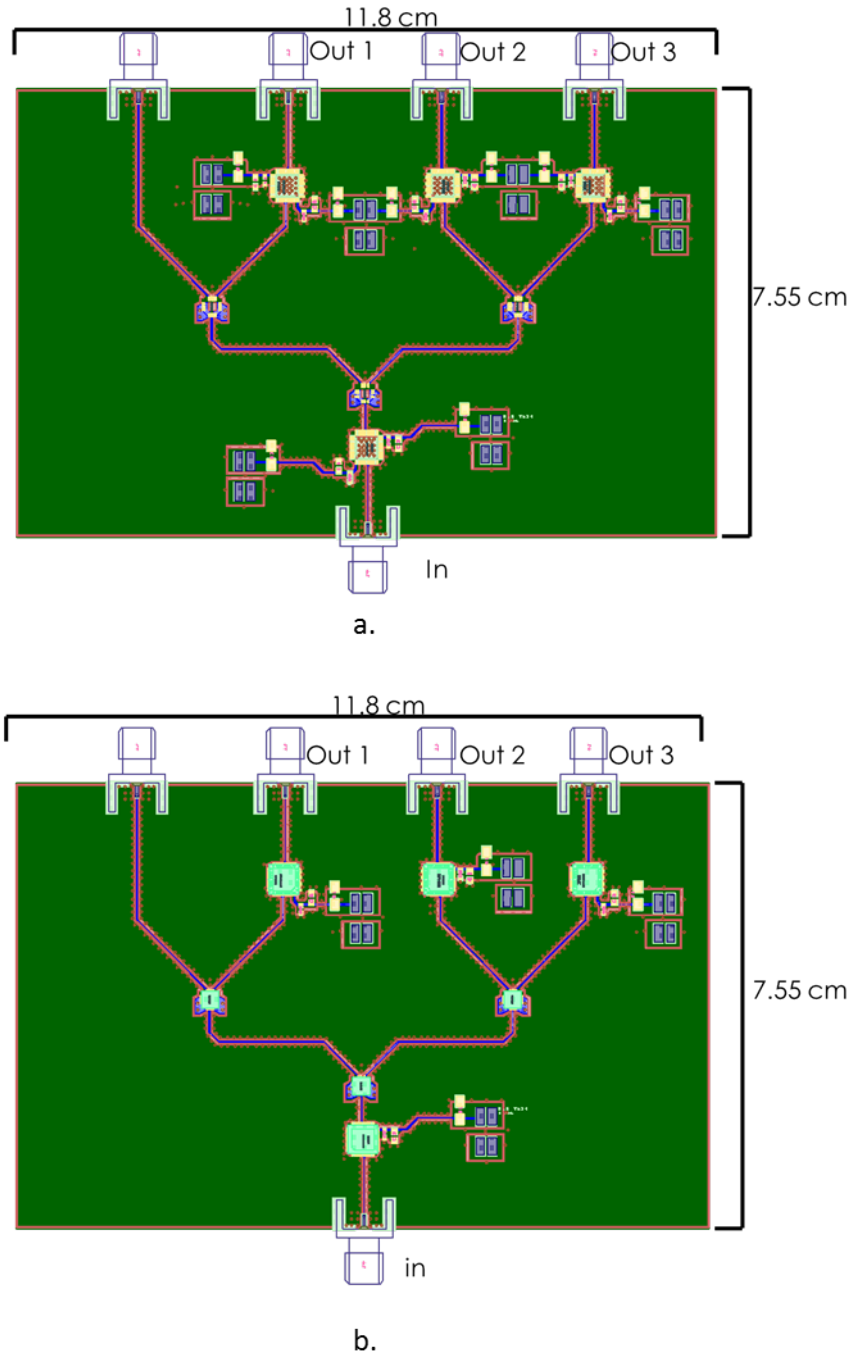
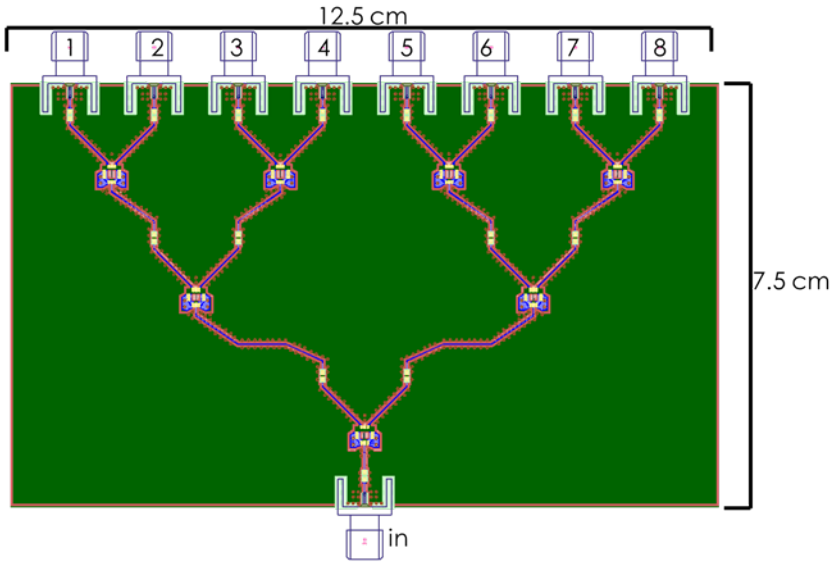
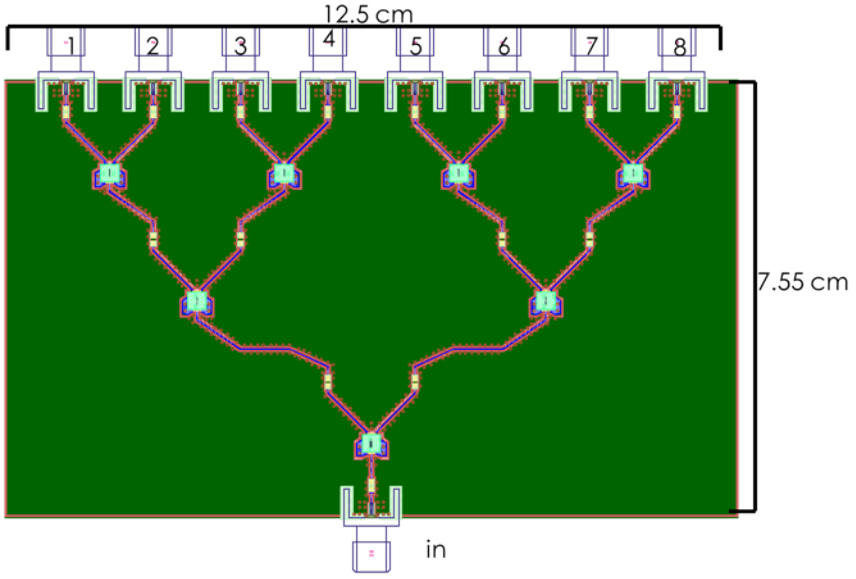


FIGURE 4.12: Layout Amplification Level for LOs Distribution a. board at 2.33 GHz b. Board at 7 GHz



a.



b.

FIGURE 4.13: local Oscillator Distribution. a. Board at 2.33 GHz and b. Board at 7 GHz

Chapter 5

Conclusions and Future Work

A synchronization Module based in phase locked loop for a Doppler weather radar has been designed, simulated (using Agilent Advanced Design System) and generate the layout. This Module is the second stage for the construction of solid state radar. The synchronization module designed provides 24 LOs signal at 7 GHz and 24 LOs signals at 2.33 GHz, with 19 dBm and 25 dBm of power, respectively and the power consumption is of 7.47 Watts.

The Filter design for a LO generation was presented for optimization of phase noise. Also demonstrated in the results of phase noise that the use of a adequate loop bandwidth and phase margin the phase noise in the system is optimized. The loop bandwidth optimum is equal to 2.35 MHz with 45 degrees of phase margin. The total phase noise floor of the local oscillator is -150 dBc/Hz.

Two architectures for distribution LO were studied. For the architecture of LO distribution using only a PLL two designs are developed. And for LO distribution using N-synchronous Voltage Control Oscillators was presented a only design. The selection criterion for choose the best design was based on the analysis to improve stability in phase, amplitude, lower power consumption, and lower cost. The architecture selected was the second design presented for the topology based in only a PLL. This present a phase error maximum of 2.34° and minimum at 0.25°, this is at 7 GHz. The error at 2.33 GHZ was 3.7° as maximum and minimum was of 0.129°. The phase of the signals at 2.33 GHz presented a standard deviation of 1.9°, and a standard deviation of amplitude of 0.19 dB. The 24 outputs signals at 7 GHz for this design present a standard deviation of phase of 1.24° and a standard deviation in amplitude of 0.13 dB. The phase and amplitude error are probably caused by the differences in component due to manufacturing tolerances. The errors in each channel was calculated. The accuracy and reliability of

these errors in the system, which can solved as future work through of analysis of several methods of calibration in phase array for the system performance. For the layout generation the transmission line used is CPWG allows 28% reduction in line width for 50 Ohm lines. With of design of synchronization module, the second step for the design of SSOTG is completed. For future work it is suggested to analyze the effects of the phase and amplitude errors on the radiation pattern of the antenna, and the design and implementation of the digital signal processing and Control Systems.

Appendix A

Appendix A

In the figure A.1 and figure A.2 show a list the changes made on transceiver radar designed by [12].

Component	Modifications			Descriptions
	Change		New	
	Y	N		
Dual Mixer, HMC340ALP5 HITTITE				Dual mixer covering 1.7 - 4.5 GHz RF/LO range.
Power Splitter, GP2S1+ MINICIRCUITS				Power Splitter 2 way 0°, 500 to 2500 MHz
Quadrature Hybrid QCC-22+ MINICIRCUITS				Power Splitter 2 way 90°, 1500 to 2500 MHz
Vector Modulator, HMC631LP3 HITTITE				Vector Modulator, 1.8 – 2.7 GHz
Band Pass Filter, HMC891LP5 HITTITE				Band Pass Filter, 2 – 3.9 GHz
Switch, HMC348LP3 HITTITE				Switch, GaAs MMIC SPDT non-reflective CATV SWITCH, DC - 2.5 GHz
Quadrature Hybrid QCC-22+ MINICIRCUITS				Power Splitter 2 way 90°, 1500 to 2500 MHz
Upconverter, HMC924LC5 HITTITE				GaAs MMIC I/Q UPCONVERTER RF range 9 - 16 GHz, Frequency range oscillator 7 - 16 GHz, IF frequency range 0 - 3 GHz. Conversion gain 14-17 dB
Power Amplifier, HMC487LP5 HITTITE				Surface Mount PHEMT 2 WATT Power Amplifier, 9 - 12 GHz. Gain 20 dB.
Power Amplifier, HMC590LP5 HITTITE				GaAs PHEMT MMIC 1 WATT POWER AMPLIFIER, 6.0 - 9.5 GHz. Gain 21 dB.

FIGURE A.1: Selection of Components Transmitter Radar

Component	Modifications			Descriptions
	Change		New	
	Y	N		
Circulator, 4925	■			Circulator coaxial, 7000 to 124000 MHz Isolation 20 dB.
Switch, HMC607 HITTITE		■		is a broadband high isolation non-reflective GaAs MESFET SPDT MMIC chip. Covering DC to 15 GHz, the switch features >55 dB isolation.
Low Noise Amplifier, HMC564LC4 HITTITE		■		Low Noise Amplifier, operating from 7 to 14 GHz. Gain of 17 dB and 1.8 dB noise figure.
Downconverter, HMC908LC5 HITTITE	■			GaAs MMIC I/Q Downconverter 9 - 12 GHz, Noise Figure of 2.2 dB conversion gain 11dB. Frequency range, LO 5.5 -15.5 GHz, Frequency range, IF DC - 3.5 GHz
Band Pass Filter, HMC891LP5 HITTITE			■	Band Pass Filter, 2 – 3.9 GHz
Quadrature Hybrid QCC-22+ MINICIRCUITS			■	Power Splitter 2 way 90°, 1500 to 2500 MHz
Power Splitter, GP2S1+ MINICIRCUITS			■	Power Splitter 2 way 0°, 500 to 2500 MHz
Dual Mixer, HMC340ALP5 HITTITE		■		Dual mixer covering 1.7 - 4.5 GHz RF/LO range.
Analog to Digital Converter, AD7490 ANALOG DEVICES			■	The AD9637 is an octal, 12-bit, 40/80 MSPS analog-to-digital converter (ADC) operates at a conversion rate of up to 80 MSPS. It Have 8 channels.

FIGURE A.2: Selection of Components Receiver Radar

Appendix B

Appendix B

Company	Piece Part	Description
HITTITE	HMC507LP5	VCO, Vtune = 7.25 V at $F_{0UT} = 7GHz$ and $F_{0UT}/2 = 3.5GHz$, Vcc = 5 V, Icc=[200 - 270] mA, Output Power = 13.5 dBm, Sensitivity = 110 MHz/V
HITTITE	HMC437MS8G	Freq. Div., Input Power Rang [-10 - 10] dBm Vcc = 5 V, Icc = 69 mA, Output Power Range [-4 to -1]dBm, SSB Phase noise (@100 kHz)= -153 dBc/Hz
HITTITE	HMC699LP5	Synthesizer, Reference VCO input [-10 to +5] dBm Reference Sine Wave input [-5 to +5]dBm, PFD Gain = 0.32 V/rad. Output High Voltage, (NU, ND)= 5 V Output Low Voltage, (NU, ND)= 2.9 - 3.1 V $Vcc = Vcc1 = Vcc2 = Vcc3 = Vcc_{pd} = 5V$, Total Supply Current 345 mA,
Texas Instruments	THS4031CDGN	Operational Amplifier, Voltage Noise $1.6nV/\sqrt{Hz}$ Bandwidth = 100 MHz, Gain = -1, 2, 3 dB. Typical Operation $\pm 5Vto \pm 15V$ Supply Current = 10 mA

Table B.1: Component Selection, LO Design

Appendix C

Appendix C

With the following program in matlab is calculated the components values for differents bandwidths and phases margins for active loop filter.

```
%%%%%%% PLL Parameters %%%%%%%
clear all
Kvco=110e6;                  %VCO gain
Kv=0.32;                     %Phase Detector Voltage Gain
Fref=70e6;                   %Reference Frequency
RFout=3.56e9;                %RF Output Frequency
Fc=2.35e6;                   %loop Bandwidth
PhaseMargin=pi*60/(180);     %Phase Margin

%%%%%%% Parameters Calculations  %%%%%%%

N=RFout/Fref;
Wc=2*pi*Fc;

%%%%%%%% LOOP FILTER CALCULATIONS %%%%%%%%

T_1=((sec(PhaseMargin))- (tan(PhaseMargin)))/Wc;

T_2=(1/((Wc^2)*T_1));

A=((Kv*Kvco)/(N*(Wc^2)));
B=(((1+((Wc^2)*(T_2^2)))/(1+((Wc^2)*(T_1^2))))^0.5);
T= A*B;
```

```
24
25 C_1=1000e-12;
26 R_2=T_2/C_1;
27 R_1=T/C_1;
28 C_2=1000e-12;
29 R_3=T_1/C_2;
```

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