MONOLITHIC INTEGRATED SOLAR ENERGY HARVESTING SYSTEM

By

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A system capable of harvesting the solar energy through the use of integrated solar cells is presented. The system consists of a start-up circuit, a maximum power point tracking scheme and a DC-DC conversion stage. The use of floating gate transistors permits the operation of the start-up circuit and charge pumps with input voltages <0.7V. The system was designed, fabricated and tested in a $0.5\mu m$ CMOS technology. Measured results demonstrate an output of 1V for the start-up circuit with an input of 0.3V and the behavior of the complete energy harvesting system.

Resumen de Tésis Presentado a Escuela Graduada
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SISTEMA MONOLÍTICO INTEGRADO DE COSECHA DE ENERGÍA SOLAR

Por

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Un sistema capaz de cosechar la energa solar atravéz del uso de fotodiodos integrados es presentado. El sistema consiste de un circuito de arranque, un esquema de rastreo para mxima potencia y una etapa de conversión DC-DC. La utilización de transistores de compuerta flotante permite la operación de el circuito de arranque y un charge pump con voltajes de entrada <0.7V. El sistema fue diseñado, fabricado y probado en tecnología CMOS de $0.5\mu m$. Resultados medidos demuestran una salida de 1V para el circuito de arranque con una entrada de 0.3V y el comportamiento de el sistema de cosecha de energía completo.

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List of Abbreviations

MOS	Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
N-WELL	Negatively doped well
P-DIFF	Negatively doped diffusion
FGMOS	Floating-gate MOS transistor
MOSCAP	MOS capacitor
IC	Integrated circuit
PV	Photovoltaic
MPPT	Maximum Power Point Tracking
LRCM	Linear Reoriented Coordinates Method
PU	Programming unit
LDO	Low dropout
VCO	Voltage controlled oscillator
PTAT	Proportional to absolute temperature
ASIC	Application Specific Integrated Circuit
FPGA	Field Programmable Gate Array
SOI	Silicon on Insulator

List of Symbols

t	Time (seconds)
μs	Microseconds.
ns	Nanoseconds.
V	Volts.
A	Amperes.
W	Watts.
Hz	Hertz.
LUX	Luminous flux per unit area.

CHAPTER 1
Introduction

Wireless sensor networks have an increasing importance in today's world due to the quantity of applications they have. Some applications of the sensor networks are used for security, surveillance and environmental and health monitoring. These networks are formed by a number of sensor nodes or motes. Each node consists of a power supply, control device, sensor, ADC, memory and transceivers to be able to communicate with other nodes and the server. The data acquired by these sensors over long periods of time can lead to important insights and benefits for science in general. For this reason, they need to be robust and be able to function for the longest periods of time possible.

The sensor nodes, also known as Motes, are usually deployed in hard to reach areas where maintenance is very difficult. These devices are required to have a long lifetime due to the fact that sensor networks last until the sensor nodes have sufficient power to work. Batteries have been for a long time the main source for powering the motes. For this reason the lifetime of the nodes depend entirely on the battery life but batteries are difficult to change in remote locations. To solve this problem recent works have researched the use of ultra-low-power circuits and power-aware systems to increase battery life [1, 2]. However, harvesting energy from the environment has become the new trend to power motes. Combining ultra-low-power circuit design techniques and energy scavenging, the motes have the possibility to achieve longer lifetimes.

Many sources for energy harvesting are being proposed to power sensor nodes from the environment. The most common types of energy used are mechanical, thermal, solar, electromagnetic and chemical. The challenge of harvesting energy from the environment is the low voltage that can be obtained from the environment. With the average threshold voltage of transistors in the range of 0.6V in standard CMOS technologies, different design techniques need to be employed to increase the voltage to power-up the circuits.

Thermo-electric energy can be used as a power source where there exists a temperature gradient, for example, between the heat of the skin and the environment. Using thermo-couples this gradient is capable of producing a voltage in the range of 50mV. In [3] a battery-less thermoelectric harvesting circuit is proposed; the system uses a start-up circuit capable of increasing 35mV to a voltage high enough to power their circuits. After the input voltage is increased it is stored in a capacitor to be regulated and supplied to a load using a buck converter. In [4] a piezoelectric resonator is used to convert vibrational energy from air conditioners to electrical energy. The harvested signal is then rectified and supplied to a voltage management that is in charge of powering a regulator when the voltage is sufficiently large. The system achieves an output of 30mW which can power a sensor node for approximately five minutes at a time.

It has been demonstrated that integrated photodiodes can supply sufficient energy to low power integrated circuits [5]. These photodiodes are based on CMOS passive pixels and use multiple interconnect metal layers for three purposes: connect the terminals of the diodes, store energy, and diffract light to achieve more efficiency. It has been shown that a single diode under 20 kLUX of incident white light intensity can deliver approximately $225\mu W/mm^2$ [6] for a $0.35\mu m$ CMOS process. An integrated solar system has been proposed in [7]. Their system consists of charge pump and a hysteresis comparator to connect and disconnect a LDO regulator to the load.

However, no power efficiency control is used in any part of the circuit. This issue is targeted in [8] by using a VCO to change the frequency at which the charge pump is operating. A control unit using a hill-climbing method monitors the charge pump output current and changes the frequency depending on the desired output. This system is used to charge a battery from an external PV cell.

Although research in energy scavenging systems have been fruitful most of the published work has not been able to develop a single integrated system as they typically use discrete components for step-up conversion [9],external microcontrollers [10] and off chip PV cells [9, 11, 12]. Charge pumps have become one of the preferred methods for DC-DC conversion in energy scavenging systems since it permits voltage conversion in an easy and integrable manner. In [13] a charge pump for energy harvesting systems is proposed. The circuit is capable of working with an input as low as 0.7V and its efficiency is increased by connecting the bulk of the transistors to their source at their higher in-stage voltage. Another charge pump is used in [14] for harvesting energy from a solar cell capable of supplying 2.5V at its optimal point.

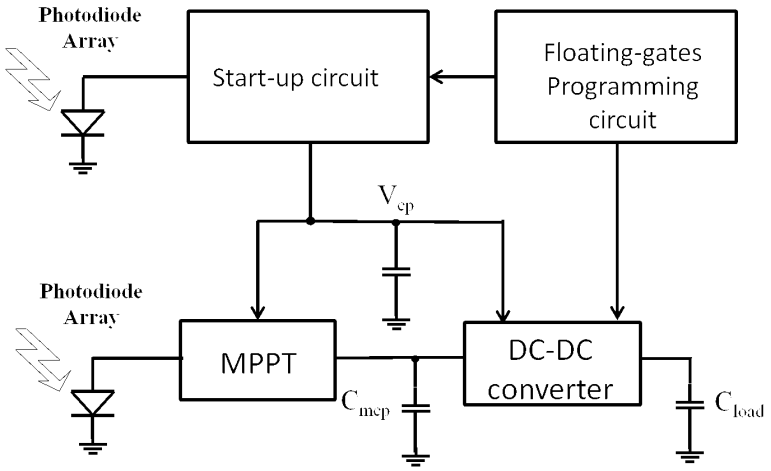


Figure 1.1 : Block diagram of the proposed energy harvesting system

The purpose of this work is to use low power analog design techniques to design a system capable of using the harvested power scavenged from the environment. Moreover, by using photodiodes based on CMOS pixels a complete scavenging integrated circuit is proposed to harvest solar energy. Figure 1.1 presents the main components used to achieve the purpose of this work. A start-up circuit is first used to increase the low voltage provided by the photodiodes to a voltage high enough to power other circuits. Instead of batteries large capacitors are to be used as charge storage. Once the start-up capacitor has reached a certain voltage a Maximum Power Point Tracking (MPPT) scheme is activated to obtain maximum power values for changing light conditions. A DC-DC converter consisting of a charge pump then increases the voltage from the maximum power stage to a voltage high enough to be used by the load. Floating-gate transistors are mainly used as a threshold modification mechanism which permits the transistors to work with voltage inputs well below their threshold voltages. A key objective of this work is to demonstrate the energy harvesting and how MPPT schemes can be achieved in the same chip. With the integration of energy harvesting, the complete sensor nodes can be fabricated on a single chip, making them more portable, cost efficient and capable of having a longer lifetime.

Chapter 2 discusses the design and functionality of the integrated photodiodes. The types of connections for the photodiodes in a standard CMOS process and their advantages are also discussed. The linear reoriented coordinates method (LRCM) is presented as a way of obtaining the photodiode behavior in a simulation environment. Floating-gate transistors functionality and charge modification techniques are presented in the afore mentioned chapter. An automated charge modification circuit for energy harvesting systems to precisely program the floating-gate transistors its also discussed and used through this work .

The detailed circuits that compose the blocks of Figure 1.1 , their behavior, and measured results are presented in Chapter 3. The circuits discussed include a low-power current reference, a floating-gate charge pump, a sample and hold circuit and a low voltage start-up circuit. Each circuit was characterized independently and then tested as a whole system as it is important to understand the behavior of each circuit before connecting them together as a complete system. The results from the energy harvesting system and general testing results are discussed in Chapter 4. Finally, Chapter 5 presents a summary of the results and plans for future work.

CHAPTER 2
Methodology

2.1 Integrated Photodiodes

CMOS imaging pixels have been dominating the digital and video market since the late 90's because of their ease of integration with the CMOS process and low cost. In addition, CMOS image sensors enable high integration of other applications such as automotive, machine vision and biomedical devices among others [15, 16]. An imager pixel is formed by a simple p-n junction, when light hits the depletion region formed by the p-n junction a reverse current is generated proportional to the light intensity. When the pixels are arranged in arrays a projected image can be converted to electric signals which are then read out, processed and displayed.

Using the same layout technique as in imagers, a diode equivalent to a PV cell can be integrated into a CMOS process. A solar cell formed by a p-n junction is able to generate an output current only when the energy of a photon of the solar spectrum has more energy than the bandgap of the cell's material. Photons that hit the solar cell with less energy than the bandgap do not contribute to charge generation while the excess energy of highly energized photons is dissipated as heat. When the photons are absorbed, electron-hole pairs are generated near the p-n junction's electric field. The electric field then forces a current I_L in the reverse direction. When an external current path exists it is capable of generating a voltage given by the built-in potential of the diode. The relationship between the voltage across the diode and its output current is given by

$$I_{ph} = I_s \cdot \left[exp\left(\frac{qV}{kT}\right) - 1 \right] - I_L \tag{2.1}$$

in which the first term of the equation is the forward bias current equation of the diode, I_s is the diode saturation current, V is the voltage across the diode, q is the charge of an electron, k is the Boltzman constant, T is temperature and I_L the maximum current generated by the solar cell defined as

$$I_L(E_g) = Aq \int_{E_g=h\nu}^{\infty} \frac{d\phi_{ph}}{dh\nu}\, d(h\nu) \tag{2.2}$$

As the forward bias increases, the electric field at the junction is reduced but never reaches zero. This is the reason the solar cell will keep providing current in the reverse-biased direction. The fact that the generated current from solar energy is a reversed current is the reason why solar cells are capable of providing such low power and efficiency.

CMOS photodiodes have been studied in previous works where different topologies and techniques have been investigated to increase the photocells' efficiency. In [5] the use of metal gratings as storage capacitance and light diffraction is suggested. Using a six metal process, different metal gratings were done following a quadratic sequence to obtain the best diffraction level. Although diffraction helped increase the photodiodes' efficiency, a solar cell with just one metal layer was capable of providing significant power. Also, both the layout geometry and area of the cells have been found to affect the efficiency. In [17] different layout geometries and areas were used to test the efficiency of solar cells. The best efficiency was obtained from a structure of straight lines of p-diffusion on an n-well. This is because that specific geometry has the largest active area density, demonstrating the linear relation between area and generated photocurrent as in Equation 2.2.

The types of diodes in a standard n-well CMOS process include n-well/substrate, n-well/p-diff, and n-well/p-diff/substrate, Figure 2.1 presents these types of connections. The n-well/substrate is similar to the passive pixel structure used in imagers. The n-well/p-diff, where the cathode is hard wired to the substrate, can be used as a floating diode but suffers from losses caused by the parasitic diode formed between the n-well and the substrate. Finally, the n-well/p-diff/substrate is used to connect the substrate to the p-diff, making this cell the most efficient as the current generated by the parasitic diode is added to the harvester diode current. However, the latter cannot be used in a single n-well process because the substrate has to be connected to the lowest potential available.

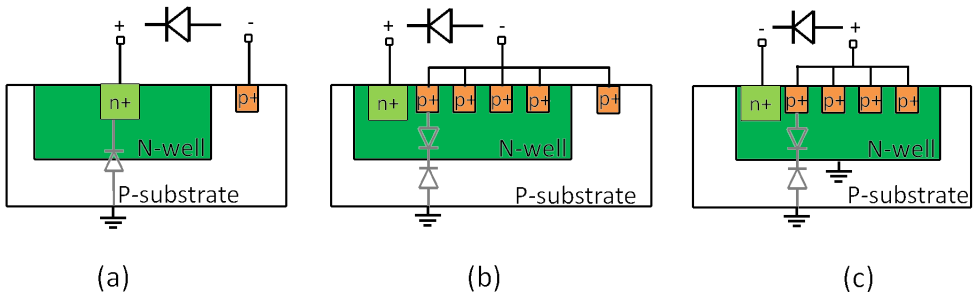
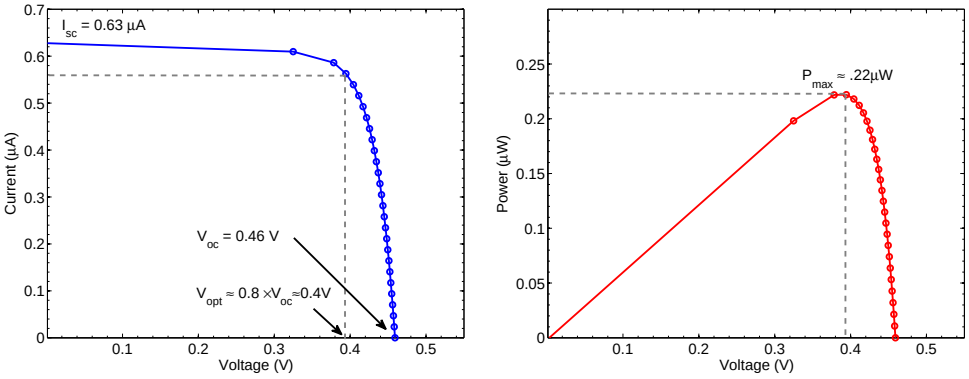


Figure 2.1 : Cross section view of the integrated photodiodes and the types of connections available in a standard CMOS process: (a) n-well/substrate, (b) n-well/p-diff/substrate, (c) n-well/p-diff

A n-well/p-diff floating diode must be used to implement the photodiodes in a single die with the circuits in a standard CMOS single n-well process. In this case the n-well has to be connected to the substrate because it is the lowest potential on the IC. This connection short-circuits the parasitic diode formed by the n-well/substrate junction which limits the efficiency of the cell by decreasing the photo-generated current. In [17] the efficiencies for the different p-n junction connections are shown and for a specific structure the short-circuit connection reduces the current by four times. This value can be taken as an approximation of the effect of this connection in the design and simulations of the PV cells.

In this work, floating n-well/p-diff diodes were designed since it is the only option to make the complete integrated solar system. An IC containing both n-well/pdiff and n-well/substrate diodes was designed and fabricated in a standard CMOS $0.5\mu m$ technology for characterization. Each individual cell has an area of $25\mu m$ x $32\mu m$ and the arrays are composed of ten rows and columns of n-well/pdiff diodes connected in parallel, covering a total area of $205\mu m$ x $271\mu m$.

The solar cells were tested under lab conditions using a lamp at room temperature. The characteristic graph was obtained sweeping a current with Keithley's picoammeter while measuring the voltage at each point. Using a pyrometer the radiation of the lamp on the chip was measured for different light conditions. Figure 2.2 shows the characterization graphs for a single n-well/p-diff solar cell array under these conditions. Figure 2.2 (a) illustrates the measured short circuit current and open circuit voltage of the photodiode which are $0.62\mu A$ and $0.46V$ respectively for an illumination of $1080\ W-m$. Under these conditions the solar cell is able to achieve a maximum power of $.22\mu W$.



(a) Current and voltage graph of the photodiode.

(b) Power graph of the photodiode.

Figure 2.2 : Characteristic graphs of a single $10x10$ n-well/p-diff solar cells array under $1080\ W-m$ of illumination.

2.2 Maximum Power Point Tracking

Maximum power point tracking (MPPT) is a technique utilized to obtain the point where a solar cell can supply its maximum power available. MPPT consists of measuring the open circuit voltage and short circuit current of a PV cell to obtain the maximum power available for different conditions. Different techniques have been used to obtain the the afore mentioned point the most common being perturb and observe [18] and hill climbing techniques [19]. The most common uses for MPPT methods have been for DC-DC conversion [20] and maximum performance of electrical machines [21].

2.2.1 Linear Reoriented Coordinates Method

Integrated photocells have a low and limited power because of the variations of illumination affecting the maximum power that should be obtained at all times. A maximum power point tracking will be used in our design to solve these problems in most efficient conditions.

The most accurate method to obtain the optimum values of voltage and current for maximum power of an integrated photodiode is by using Equation 2.1. Since the power relation is $P = IV$, Equation 2.1 can be multiplied by a variable V and solved for current and voltage when $\frac{dP}{dV} = 0$. However, these equations are difficult to solve and require a large number of iterations to obtain the optimum voltage and current. They also require knowledge of the fabrication process to be able to obtain the current equation. For these reasons another method is necessary to model the photodiode behavior to obtain the maximum power available from it.

The Linear Reoriented Coordinates Method [22] is a method in which the maximum value of a function is approximated when it can not be solved by traditional methods of differential calculus. The LRCM models the behavior of a PV cell where the relation of the current I is related to the voltage V across the photodiode by

$$I(V) = \frac{p \cdot I_x}{1 - exp(\frac{-1}{b})} \cdot \left[1 - exp\left(\frac{V}{b \cdot s \cdot V_x} - \frac{1}{b}\right)\right] \tag{2.3}$$

where I_x and V_x are the short-circuit and the open circuit voltage respectively, s is number of cells in series and p are the number of cells in parallel. The characteristic constant b is calculated using an algorithm based on the Fixed Point Theorem. The LRCM has the advantage that it can work for any type of solar cell and can be applied to integrated photo cells since it doesn't depends on the size and doesn't require specific parameters from the material of the PV cell.

Using the LRCM, a very close approximate of the optimal values of voltage V_{op} and current I_{op} can be obtained using Equations (2.4) and (2.5). The approximate values V_{ap} and I_{ap} are then used to calculate the maximum power of the photodiode.

$$V_{ap} = V_x + b \cdot Vx \cdot ln\left[b - b \cdot exp\left(\frac{-1}{b}\right)\right] \leq V_{op} \tag{2.4}$$

$$I_{ap} = I_x \cdot \left[\frac{1 - b + b \cdot exp\left(\frac{-1}{b}\right)}{1 - exp\left(\frac{-1}{b}\right)}\right] \geq I_{op} \tag{2.5}$$

In this work, the LRCM was used to simulate the diode behavior for simulations. Equation 2.3 was used in a Verilog-A program of the photodiode to simulate the scavenging system. LRCM was also used to obtain the approximate values of the optimal point for the MPPT.

2.3 Floating-gate Technology

Programmability has made Floating-gate MOS transistors (FGMOS) an essential tool nowadays in digital/analog circuit design. Historically, FGMOS have been use as non-volatile digital programmable memories like EEPROMS [23]. Recently, FGMOS have been used as non-volatile analog memories by precisely modifying the amount of charge stored at the floating node. This property permits the use of floating gate devices to compensate for transistor mismatches without the use of techniques such

as laser trimming and large size transistors. Floating-gate transistors have been used in the design of high precision converters [24, 25], voltage/current sources [26, 27, 28, 29], and imagers[REFS] among others. This work exploits the use of FGMOS in the development of low voltage and high efficiency circuits for energy harvesting applications.

2.3.1 Floating Gate MOS Transistors: An Analog Memory

Figure 2.3 (a) presents the schematic and layout of a typical floating-gate transistor. The FGMOS consists of a standard MOS transistor with capacitors C_g and C_{tun} connected to the gate terminal. There is no DC path to this node, hence charge can be stored indefinitely. C_g is usually a poly/poly capacitor and one of its terminals can be used as an input to the floating-gate transistor. On the other hand, C_{tun} is a MOS capacitor and is used to program the floating-gates as a charge extraction mechanism.

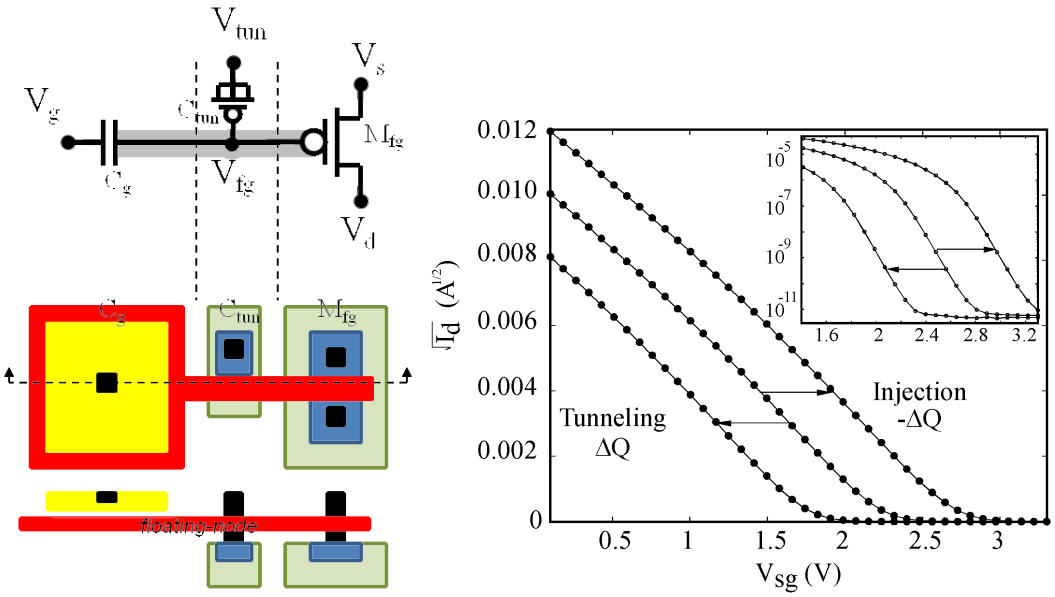


Figure 2.3 : Floating-gate Transistor: (a) Circuit schematic and layout of a floating-gate PMOS transistor. (b) Threshold variation of a PMOS floating-gate.

The gate-source voltage V_{gs} on a PMOS floating-gate transistor is dependent on the capacitively coupled input voltage V_g and the charge stored at the floating node V_{fg}. Additionally, V_{gs} its affected by the voltage at the drain and source coupled by their parasitic capacitances C_{gs} and C_{gd} as described by

$$V_{gs} = V_s \cdot \left(\frac{C_{gs}}{C_{tot}}\right) + V_d \cdot \left(\frac{C_{ds}}{C_{tot}}\right) + V_g \cdot \left(\frac{C_g}{C_{tot}}\right) - \frac{Q}{C_{tot}} \tag{2.6}$$

where C_{tot} is the total capacitance at the floating node, and Q is the charge stored at the floating node. Assuming $C_g >> C_{gs}+C_{ds}+C_{tun}$ the equation can be approximated as

$$V_{gs} \approx V_g - \frac{Q}{C_g} \tag{2.7}$$

The current of the FG transistor is then determined by its gate-source voltage and the transistor's region of operation. For a transistor working in the saturation region the current is given by

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_g - \frac{Q}{C_{tot}} - V_{th}\right)^2 \tag{2.8}$$

where μ is the charge mobility, C_{ox} is the oxide capacitance, $\frac{W}{L}$ is the size of the transistor and V_{th} is the threshold voltage. In the sub-threshold region the current equation is

$$I_d = I_o \cdot e^{\left[\frac{V_g - \frac{Q}{C_{tot}} - V_{th}}{n \cdot U_T}\right]} \tag{2.9}$$

where I_o is the drain current when $V_{gs} = V_{th}$, n is the slope factor and $U_T = \frac{kT}{q}$.

It can be seen in both equations how the effective threshold voltage of the transistors can be increased/decreased depending on the charge stored at the floating node. Also, the coupling of C_g can be used to control the current depending on the voltage applied at the gate of the FGMOS.

2.3.2 Charge Retention

Floating gate transistors have good charge retention capabilities on account of the gate being surrounded by a high quality insulator. This characteristic permits a fairly constant programmed value to be retained for long times. In [30] a conservative estimate of ten years is reported for a FGMOS with a oxide thickness of $70\mathring{A}$. However, retention time depends on the oxide thickness, the value of capacitances at the floating node and the bias voltage of the FGMOS [31].

2.3.3 Automated Charge Modification of Analog Memories

Programming of FGMOS is achieved by modifying the charge on the floating node. The programmed value depends on the quantity of electrons stored at the FG node. The main methods for charge modification of a FGMOS are hot-electron injection [32] and Fowler-Nordheim tunneling [33]. Tunneling is used as a global erase and it's done by applying a high voltage through the CMOS capacitor C_{tun}. When the high electric field is applied across C_{tun}, negative charge in the floating node is capable of crossing through the insulator barrier of the MOSCAP, thus erasing the memory.

On the other hand, hot-electron injection is used to program the FGMOS and occurs when there is a high enough potential between drain and source of the MOS transistor. Electrons acquire energy from this potential, when their energy is higher than the SiO_2 barrier energy hot-injection of carriers occurs at the FG in the form of a current I_{inj}. It is important to note that during injection and tunneling electrons cross the silicon oxide barrier of the MOS transistor and MOS capacitor respectively. The main difference between the two effects is that injection occurs when particles have enough energy to cross the barrier and tunneling is due to quantum phenomenon.

An automated scheme for programming FG devices is used in this work to lessen the programming time and increase accuracy of the programmed voltage. The system

architecture presented in [34] permits charge modification of 25 independent programming units (PU) requiring minimal effort. Figure 2.4 (a) shows the schematic of a single programming unit which includes transistors M_I, M_F and M_{fg} sharing the same floating node. Transistor M_I is used to enable hot-electron injection, transistor M_F allows negative feedback, and transistor M_{fg} represents the target transistor to be programmed.

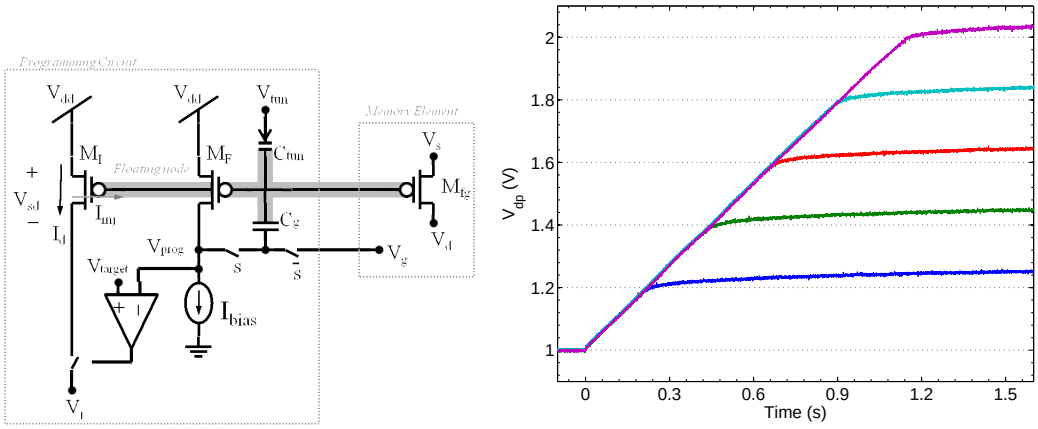


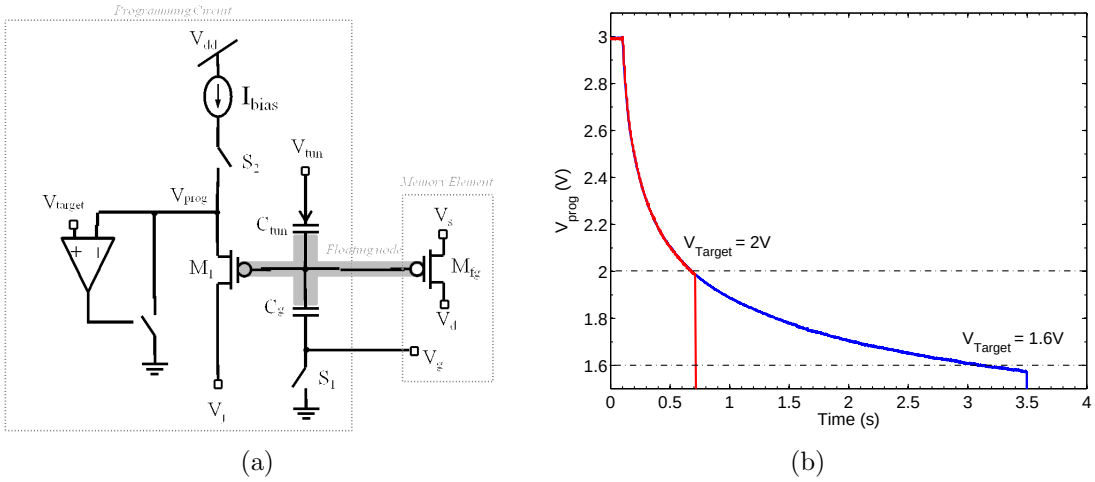
Figure 2.4 : (a) Schematic representation of a single programming unit (PU). (b) Programming of a single PU for different voltages at maximum injection rate.

The circuit operates in two modes: programming mode (s=gnd) and running mode (s=V_{dd}). In running mode, transistor M_{fg} is connected to the analog/mixed-signal system and all the programming circuit is transparent to the rest of the IC.

In programming mode I_{bias} flows through the diode connected device M_F. If M_F and M_I are designed as identical transistors, then I_d will be forced to the constant current I_{bias}. Assuming capacitor $C_g >> C_{tun} + C_{par}$ the voltage at V_{prog} will change linearly with respect to the charge stored a the floating node. When injection starts, V_{prog} is charged/discharged until it reaches the value of V_{target}, which is the desired voltage at the floating note. After the desired programmed voltage has been reached, the circuit stops injection and maintains the programmed value at V_{fg}.

Figure 2.4 (b) shows the programming of a single PU for different voltage values in 0.2V steps with respect to time using the afore mentioned programming system.

2.3.4 Programming circuit for the solar system



(a) (b)

Figure 2.5 : Modified programming circuit for a solar powered system: (a) Schematic of a single programming unit (PU) for the solar energy scavenging system. (b) Programming of a single PU for different two different target voltages.

In the programming circuit discussed in the previous section the switches need a V_{DD} voltage to keep them closed when the FG transistors in their functional mode. Since the solar scavenging system needs to work under the Sun only with the voltage generated by the photodiodes, the programming circuit was edited so it can be functional without any external voltage. Figure 2.5 shows the schematic of the new programming circuit, by closing switch S_1 both V_g terminals are drawn to ground and switch S_2 connects the FG transistor to the current source. At this moment the system is in programming mode and the amount of charge can be monitored by looking at voltage V_{prog}. The expression for the V_{prog} voltage in this circuit is given by

$$V_{prog} = V_{gs} + \frac{Q}{C_g} \tag{2.10}$$

It can be seen that by using this configuration the rate of injection slows down as the voltage at the floating node is more negative. When this happens V_{prog} decreases as described in Equation 2.10. If V_j is kept constant the drain source-voltage decreases, making the rate of injection slower. Figure 2.5 (b) demonstrates the programming of a FG for two different values, in this case 2V and 1.6V. The sudden drop in voltage to 0V is due to the comparator which draws V_{prog} to ground when the FG reaches the desired value of V_{target}.

When in functional mode S_1 and S_2 are open by tying their controlling signal to ground. In this mode both V_q terminals are connected to their respective locations and the PU is disconnected from the supply voltage, making the circuit work when there is no V_{DD} voltage available.

CHAPTER 3
Solar Energy Scavenging System

3.1 MPPT circuits

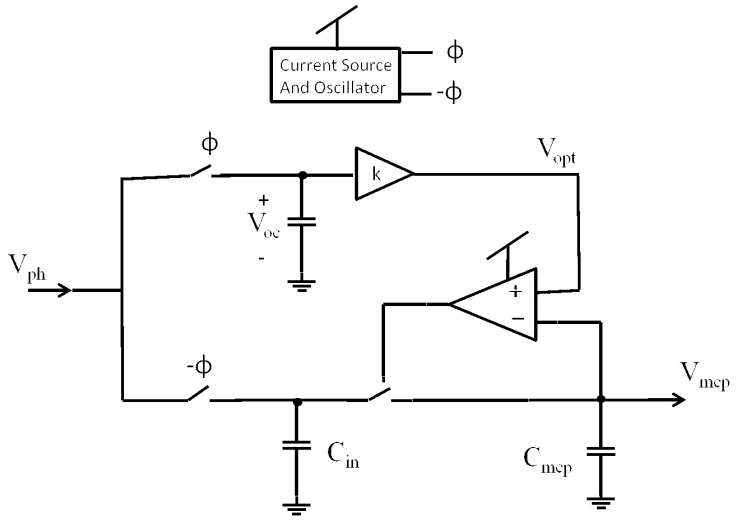


Figure 3.1 : Block diagram of Maximum Power Point Tracking circuit.

Figure 3.1 presents a simple diagram of the proposed MPPT scheme. The circuit is composed of an oscillator to control the open-circuit sampling and maximum power transfer periods. A gain stage is used to obtain the optimal voltage value of the photodiode, which is approximately eighty percent. This voltage value is then feed to a comparator which connects the photodiode to a load and forces it to work at its maximum power point. A current reference is used to provide the bias currents for the amplifiers and oscillator presented in the sections below.

3.1.1 Current Source

The current reference is a very important part of the design since it supplies current to most of the circuits in the energy scavenging system. The reference has to be able to provide currents in the nano scale to keep the circuits working without consuming too much power. The topology used is shown in Figure 3.2 , this circuit replaces the resistance in a common Proportional To Absolute Temperature(PTAT)reference with a transistor working on the linear region. Assuming M_1 and M_2 are working in the sub-threshold region, the differential voltage of their gate-source voltages fixes a voltage at the source of M_3. Since M_3 works in the linear region, its effective resistance can be controlled by its gate-source voltage. Therefore, the generated current can be controlled by the ratio between M_3 and M_4, which is saturated due to the diode connection. This configuration is able to generate small currents given by Equation 3.1, using only a fraction of the area that a resistor based reference would occupy. Furthermore, the reference is almost independent of temperature because of its relationship between the transistor thermal voltage and the mobility temperature dependence [35]. Although the currents through the system do not have to be precise for different temperatures, temperature compensation helps to keep power down and maintain operating conditions fairly constant when the circuits are exposed to the sunlight.

$$I_{ref} = 2K_n \frac{A_3^2}{A_4} (U_T ln(N))^2 \tag{3.1}$$

A_3 and A_4 are the dimension ratios of transistors M_3 and M_4 respectively; N is the ratio $\frac{A_2}{A_1}$, U_T is the thermal voltage and K_n encloses the mobility and oxide capacitance of the transistors.

The current reference was designed with the ratio $\frac{A_3^2}{A_4} = 1.17$ to supply a current of 20nA. Measurements from the fabricated chips demonstrate a current with a variation between 10nA and 12nA. The margin between the designed and measured currents

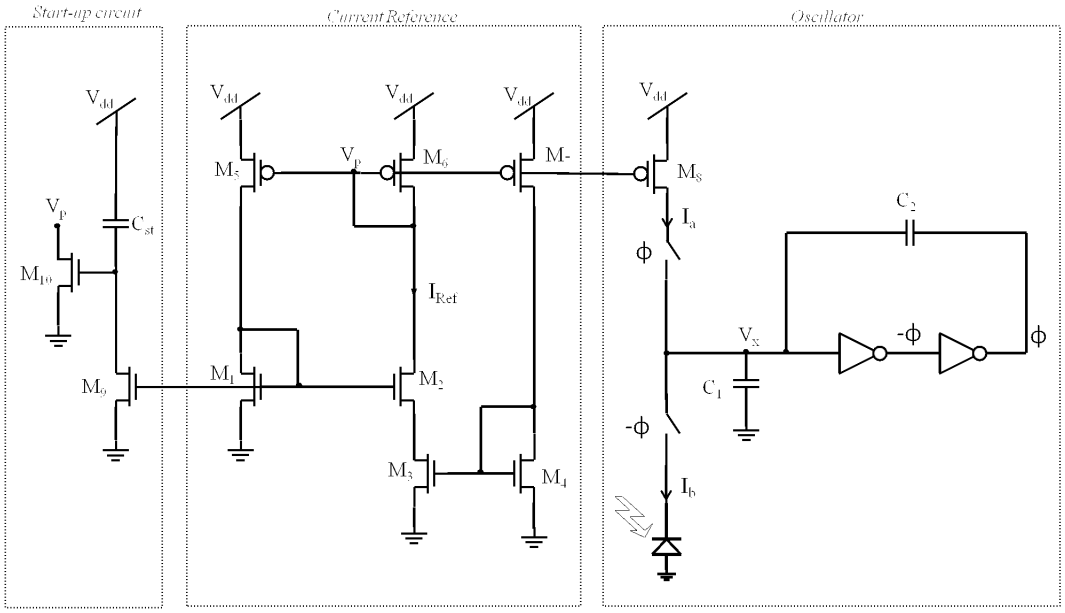


Figure 3.2 : Schematic of the integrate and fire oscillator along with the current reference.

can be attributed to process variation. A mismatch between transistor ratios $\frac{A_2}{A_1}$ and $\frac{A_3^2}{A_4}$ can cause the reference current to change greatly. The sensitivity to process variation is due to the fact that both transistor ratios are squared, which means a slight change in sizes can affect the output current. Different techniques such as the use of operational amplifiers, layout techniques and cascode connections can be used to mitigate mismatch between currents.

3.1.2 Integrate and Fire Oscillator

The MPPT circuit contains a track and hold circuit that constantly takes samples of the input to obtain the optimal voltage of the solar cell under different illuminations. A generated signal activates the track and hold circuit to take a quick sample of the open circuit voltage of the PV cell. The second phase is then held for a relatively longer time so the MPPT circuit can adjust and maintain the desired voltage at C_{mcp}. The circuit to achieve this is based on the integrate and fire neuron oscillator [36]. Figure 3.2 shows the schematic of the oscillator where the sample and

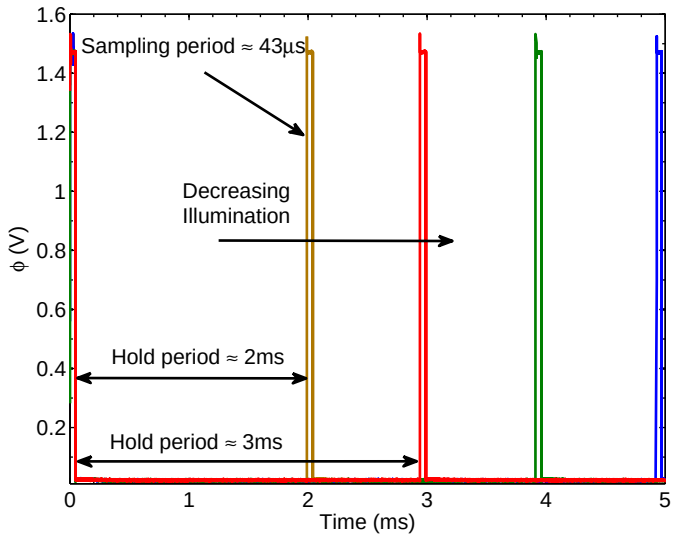


Figure 3.3 : Measured integrate and fire oscillator signal period for different illuminations.

hold periods are determined by the currents used to charge and discharge C_T and the supply voltage V_{DD}. The duration of each of the periods is determined by

$$T_a = \frac{C_T \cdot V_{DD}}{I_a}, T_b = \frac{C_T \cdot V_{DD}}{I_b} \tag{3.2}$$

where I_a and I_b are the currents charging and discharging C_T respectively, and C_T is the sum of $C_1 + C_2$.

Initially C_T is discharged and $\phi = 0$. Then, I_a supplied from the current reference through transistor M_1 starts charging node V_x until it is capable of turning on the NMOS transistor of the first inverter. When this happens, V_x increases rapidly. This increase is determined by the capacitor C_2 and V_{DD}. At the moment this occurs, the switch connecting the current reference opens and the current I_b, dictated by the photodiode, discharges node V_x. After this, the behavior of the circuit is the same, making the oscillation possible with the desired duty cycle.

This circuit was chosen because of its simplistic approach and easy configuration in obtaining the desired frequency and duty cycle. The circuit was designed to have

an asymmetric duty cycle so that the positive part of the cycle would be short and the low cycle long with respect to time. To achieve a longer hold time a small area photodiode working as an imager pixel is used to generate the smaller current. By using the photodiode power and space are saved since no need for extra circuits and connections are needed. Furthermore, current starved inverters are used; this configuration limits the current during switching of the inverters to minimize power consumption. In this case the currents driving the inverters are four times larger than the reference current because a smaller current can cause degradation of the signal.

Figure 3.3 shows the tested signal measured from one of the fabricated chips under different conditions of illumination. Under a supply voltage of 1.5 V, the short positive cycle has a duration of approximately $46\mu s$ while the negative cycle lasts $2ms$ under normal light conditions. Since the positive cycle depends on I_a from the current from the reference, it is not expected to fluctuate with illumination changes. However, it increases moderately when the operational voltage is increased because the inverters in the circuit take a slightly longer time to reach the supply voltage value as given by the delay equation of an inverter. The negative cycle, on the other hand, depends greatly on illumination, causing the sample period to take more time between samples as illumination is decreased. This behavior can be clearly seen in Figure 3.3 where four different measures of the signal period were take for different illuminations. The measurement was done under room illumination, controlling it to achieve approximately 1ms between each period with respect to the other. This behavior also helps power consumption at lower illuminations since switching in the sample and hold and MPPT circuits will happen fewer times, wasting less power. Measured data confirms the functionality of both the current reference and the integrate and fire oscillator with a supply voltage as low as 1.2V.

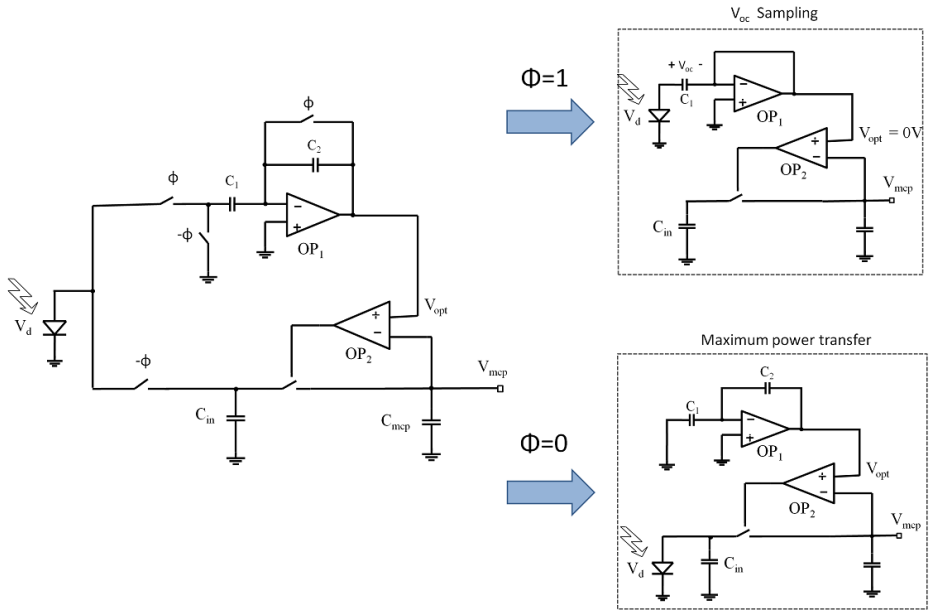


Figure 3.4 : Schematic of the MPPT scheme and the equivalent circuits during the sample and hold cycles.

3.1.3 Sample and Hold Circuit

The MPPT circuit samples the open circuit voltage of the photodiode and multiplies it by a factor that is constant for different light conditions. The implementation of the MPPT only requires the multiplication of the open circuit voltage of the photodiode by a calculated factor to obtain the optimum point of operation. The most common way of obtaining this value is by using an operational amplifier with the desired gain set by the ratio between resistances. However, an amplifier with resistors is not viable in a harvesting system because it consumes power at all times. Even if a typical amplifier circuit was to be used, the resistors would need to be of a considerable size so a small amount of power is wasted. Therefore, a switched-capacitor amplifier with a non-inverting gain was chosen. Many variations of these sample and hold circuits have been used for Analog to Digital conversion ([37],[38],[39]). However, the output voltage of these circuits only follow the input voltage. The topology presented in [40] offers the possibility of multiplying the input voltage by a factor given by the ratio of its capacitive feedback. In this configuration the capacitive feedback

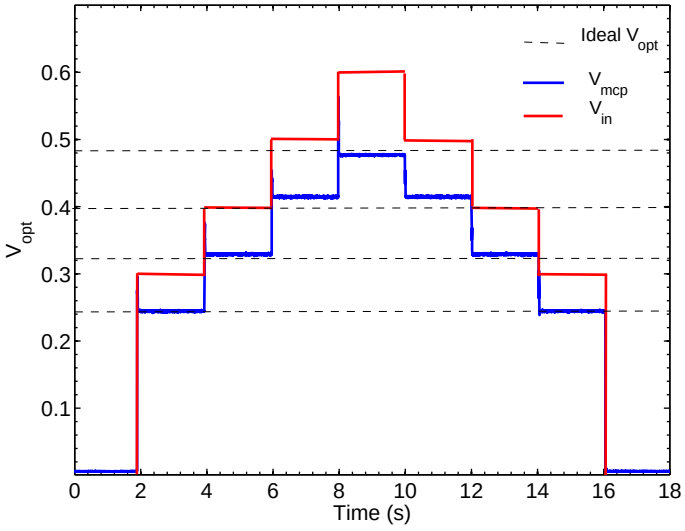


Figure 3.5 : Measured output of the MPPT circuit for input values ranging from 0.3V to 0.6V.

consumes less power and in the hold phase once the charge settles between the two capacitors, C_2 does not load the output of the amplifier.

Figure 3.4 shows the schematic of the MPPT circuit in the top-left, the switched capacitor sample and hold circuit composed of OP_1, C_1 and C_2. The circuit can work with a clock and its inversion to manipulate the switches. In the V_{oc} sample period the ϕ switches are closed and $-\phi$ are open. At this moment OP_1 is working as a unity-gain buffer, its output is at 0V and the voltage across capacitor C_1 is near V_{oc}. In the maximum power transfer phase $-\phi$ closes, connecting the input capacitor to ground, forcing charge transfer between C_1 and C_2. This causes the input to be disconnected from the circuit and the output voltage $V_{opt} = V_{oc} \cdot \frac{C_1}{C_2}$. Then, V_{opt} is fed to the positive terminal of the comparator OP_2, where its output manipulates a NMOS transistor switch to maintain the desired voltage at the output of the MPPT circuit. The switching is dependent of the output capacitor's current load, large current will make the switching faster and the opposite for low currents.

When this circuit is used with a photodiode the switching will maintain the output voltage at the desired value. Due to the previously stated current/voltage relationship of the solar cells, the photodiodes are maintained at their optimal operating point by the switching of the comparator.

The ratio of the capacitors was chosen to have a gain of 0.80 according to the calculations to obtain V_{ap}. One-stage amplifiers with PMOS inputs are used in the multiplication circuit and the comparator. This obtained value is then compared to the voltage at C_{hold} and the voltage is maintained at V_{opt} by turning on and off the pass transistor.

Figure 3.5 presents the output of the MPPT circuit for different input voltages where the red line represent the input voltage variation. The input was swept from 0.3V to 0.6V in a 0.1V step difference starting and finishing at 0V. Dashed lines represent the ideal eighty percent value of the input voltage the blue graph is the measured output voltage of the circuit after the input voltage is multiplied by the 0.8 factor. The data was taken with a supply voltage of 1.5V and using the oscillator presented in Section 3.1.2 under normal lighting conditions in the laboratory to control the switches. It can be clearly seen that the output follows those values every time the input voltage is sampled independently of its variation.

3.2 DC-DC Conversion

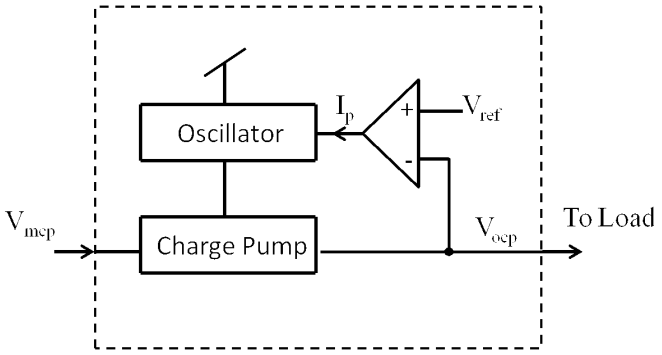


Figure 3.6 : Block diagram of the DC-DC conversion stage.

Figure 3.6 shows the components of the DC-DC conversion stage circuits. This stage increases the output voltage of the MPPT circuit and increases it to a voltage that can be used by other circuits. It consists of a FGMOS charge pump and an oscillator to operate it. A feedback circuit is used to decrease the frequency of operation of the oscillator as the charge pump reaches its maximum voltage value.

3.2.1 Main Oscillator

The main oscillator is based on the circuit discussed in Section 3.1.2 with the addition of a latch and other modifications to improve speed. The first modification is the use of the latch to force faster changes between logic states. The latch signal gets feed again to the inverter chain and to the switches that control the charge and discharge of the capacitor divider from the integrate and fire topology. A current mirror with feedback from the output voltage of the charge pump is also added to the oscillator. The frequency of the oscillator can then be controlled with the feedback and a floating gate transistor.

The tripping point in which the oscillator stops working can be set by floating gate transistor M_1. This transistor has a 0.5 capacitor coupling at the floating node so V_{ocp} can reach a fairly high voltage before turning on M_1. The voltage at which the frequency starts decreasing can be calculated by

$$V_{tp} = \frac{C_1}{C_1 + C_2} \cdot Vocp + V_{fg} \tag{3.3}$$

Initially the output voltage of the charge pump is 0V and the oscillator works at its maximum frequency. At this moment M_1 is off and node V_x has the value of the supply voltage. Transistor M_2 is working as a current source, its bias voltage V_b is obtained from the current reference and is working in the linear region. As the charge pump's output voltage increases and approaches V_{tp}, M_1 starts to turn on, driving node V_x closer to ground and turning off M_3. This causes the V_{ds} voltage of M_2 to

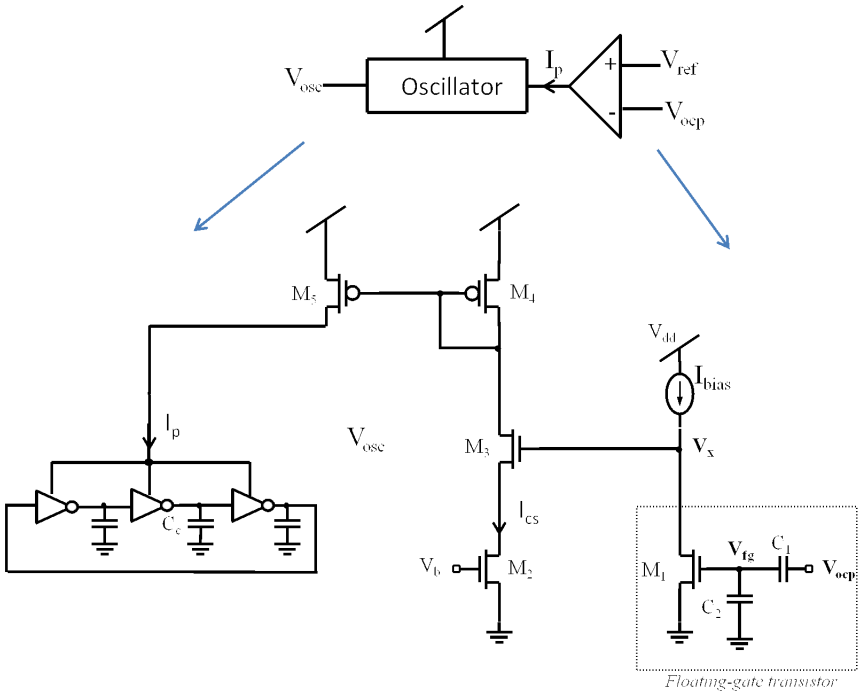


Figure 3.7 : Main oscillator feedback circuit

drop, consequently decreasing the current supplied by M_2. By limiting the current I_p of the inverters the frequency of oscillation can be controlled. This approach is used to make the charge pump more efficient and fast during the charging stage. Once the desired output voltage is reached, the oscillator drastically decreases its frequency consuming less power.

Figure**??** show the output of the oscillator and the voltage at V_{ocp}. It demonstrates how the frequency of the oscillator is decreased as V_{ocp} rises. The oscillation stars at a frequency of 140 kHz and finishes with a period of approximately 1.5 ms. Due to its frequency of operation the oscillator is the circuit that consumes most of the power in the scavenging system. Using this scheme power can be saved once the oscillator is not needed to operate at its maximum frequency.

3.2.2 Main Charge-Pump

In this work FGMOS are used as a the means to lowering the transistors threshold voltage. Figure 3.9 shows the schematic for a 3-stage charge pump where the

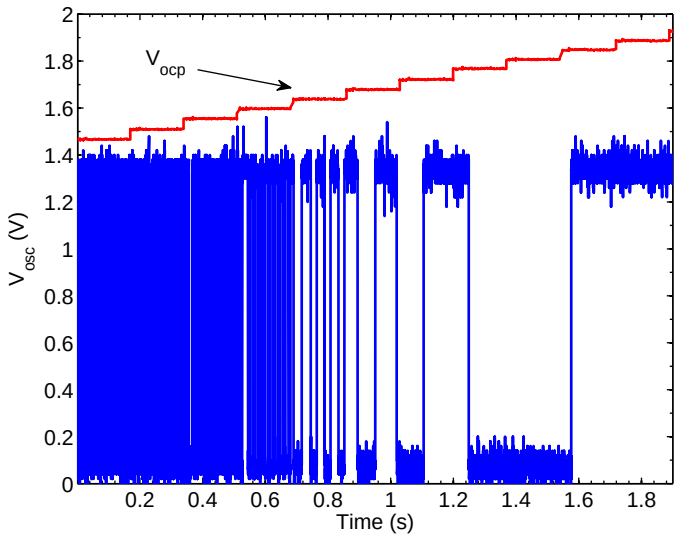


Figure 3.8 : Frequency variation change with a sweep of V_{ocp} in the feedback circuit.

diodes in a charge pump are replaced by floating-gate PMOS transistors. This type of connection was used before in [41] but the circuit was reported to work with a minimum voltage of 0.7V. Our use of the FGMOS along with the bulk connection at the higher voltage side of each stage helps in lowering the minimum input operational voltage of the charge pump.

Operation of the circuit its easily explained using Figure 3.9 . If clk=1, node X will be zero and the final voltage across the capacitor C_1 will be $V_{DD} - V_D$, where V_{DD} is the input voltage provided by the MPPT circuitry and V_D is a diode voltage drop due to D_1. At the same time, node Z will be equal to V_{DD} forcing node Y to V_{DD} and consequently diode D_2 will be reverse biased. When clk=0 node X will be V_{DD} increasing the initial charge of the first state to $2V_{DD} - V_D$, then D_1 will be reverse biased and D_2 forward biased. Now node Z will be equal to zero and the final voltage across the capacitor C_2 will be $3V_{DD} - 2V_D$. An additional diode voltage drop can be seen due to D_2, indicating an increase of diode voltage drops with the number of stages and degrading the charge pump efficiency. Observe that half period of the clock is used to step up the voltage in each stage. Therefore, an additional charge

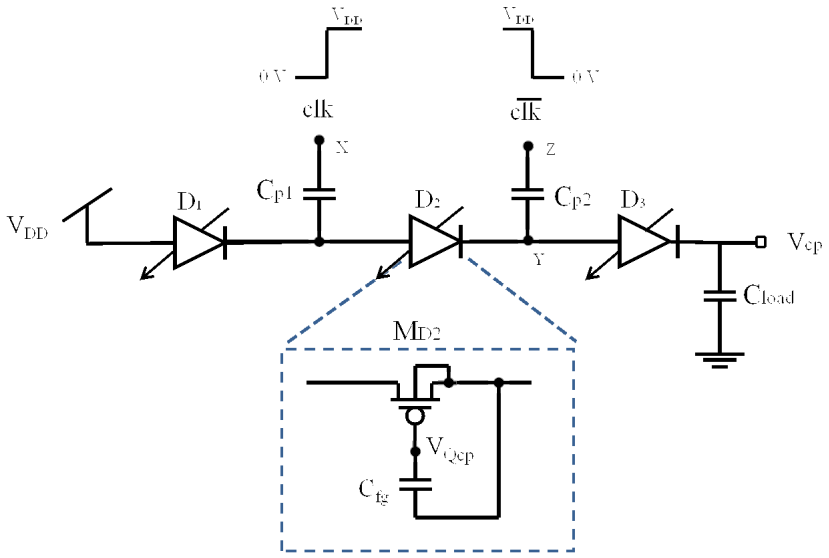


Figure 3.9 : Three stage charge pump with floating-gate diode-connected transistors.

pump with the clk signals inverted and connected to the same load was implemented. This implementation allows an increase in voltage for both charge pumps in each half period respectively, thus taking the advantage of the full period of the clock. In addition, more current can be provided than a single charge pump stage.

From the previous analysis the output voltage equation for the charge pump seems pretty straight forward but additional to charge modification in the floating-gate, on this design, the bulk is connected to the drain to achieve a lower threshold voltage when the transistor is on. The effect of the bulk-source voltage on the threshold is described by

$$V_{th} = V_{tho} + \gamma \cdot \left[\sqrt{2\Phi_s - V_{sb}} - \sqrt{2\Phi_s}\right] \tag{3.4}$$

where V_{tho} is the threshold voltage at $V_{sb} = 0$, γ is the body bias coefficient and $2\Phi_s$ is the surface potential.

Assuming sub-threshold operation, linearizing (3.4) around $V_{sb} = 0$ and taking V_{Qcp} into consideration gives

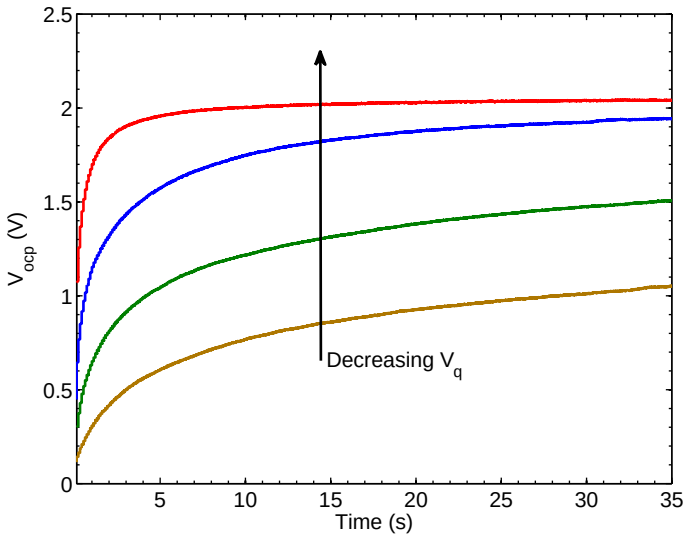


Figure 3.10 : Output voltage of the charge pump for different values of V_q with an input voltage of 0.4V.

$$V_{cp} \approx (V_{DD} \cdot N) - \frac{(V_{tho} + V_Q)}{\left[1 + \frac{\gamma}{2\sqrt{2\Phi_s}}\right]} \cdot N \tag{3.5}$$

It can be clearly seen from this formula that the more negative charge V_{Qcp} programmed at the floating node, less losses occur at the output. The ideal value to achieve zero losses would be when $V_{Qcp} = V_{th}$. However, this value cannot be achieved because when V_{Qcp} is near the threshold voltage the transistors starts to operate in the linear region, degrading the efficiency of the charge pump.

A 6-stage charge pump was designed for the solar scavenging system. The number of stages was chosen so the output voltage could reach 2V when the input voltage is at 0.4V. The response of the charge pump for three different programmed values at V_{Qcp} with the afore mentioned input voltage and a load of 47fF can be seen in Figure 3.10 . It is observed that as the injected negative charge increases, the output voltages approximates the ideal value as given by Equation 3.5 without the threshold voltage losses. By connecting the bulk of the transistor to the drain the threshold voltage is in fact reduced. This is because at the moment the diode starts conducting the

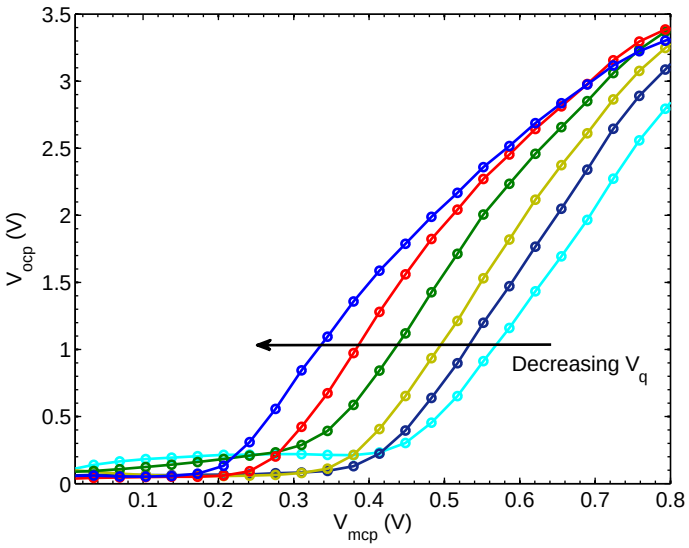


Figure 3.11 : V_{ocp} for an input voltage sweep for different V_q values.

instant value of the bulk voltage is lower than the source voltage. As the threshold is decreased a lower programmed voltage is needed.

Since the charge transfer between each stage depends proportionally of the capacitors C_p, 20pF capacitors were used to obtain more current from each stage. However, it can be noted in Figure 3.10 that the charge pump reaches its maximum output voltage at around ten seconds. This is a long time, taking into consideration the small capacitive load at the output. This behavior can be caused by a combination of various factors. The first can be the low frequency at which the oscillator described in the previous section is working. This causes the efficiency and response time of the charge pump to slow down. The programmed charge in the diode-connected transistors might also be affecting the efficiency of the charge pump. The charge at the floating may be causing a subthreshold current when the FG diodes are supposed to be off. This can also be causing the disparity between the calculated value and the actual value of the output voltage. Other factor is the capacitive load as the metal interconnect line, bare pad and buffer input capacitance must be added to the 470pF load . However, the circuit is designed to store charge in a big external capacitor to

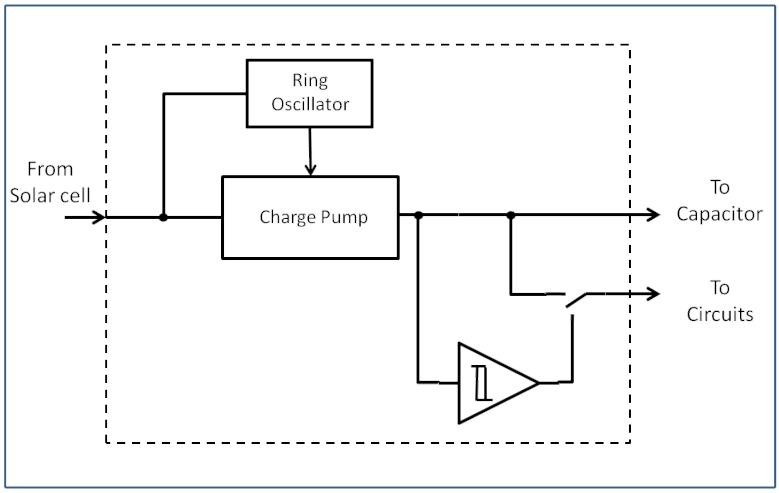


Figure 3.12 : Block diagram of the start-up circuit.

supply power to other loads for certain amounts of time. More than supplying the load with a large current, the charge pump has the benefit of operating with voltages as low as 400mV.

Figure 3.11 presents the output voltage of the charge pump for an input sweep. The sweep was done for six different programmed voltages at each FG transistor in 0.1V steps. The more negative the programmed voltage the lower the input voltage can be. As mentioned before, when the programmed voltage is too high the charge pump starts having considerable losses. This can be clearly seen in the leftmost graph where the output voltage starts degrading sooner than the others. The output voltage reaches a limit around 3.3V which is the voltage supply of the FG switches.

3.3 Start-up Circuit

Figure 3.12 shows the components of the start-up circuit. The start up circuit increases the photodiode voltage to a usable supply voltage for the MPPT and DC converter circuits. The circuit consists of a ring oscillator and the FGMOS charge pump presented in the previous section. The circuit is completed with a hysteresis comparator used to connect the output of the charge pump to the load; the hysteresis values can be programmed through the use of floating-gate transistors.

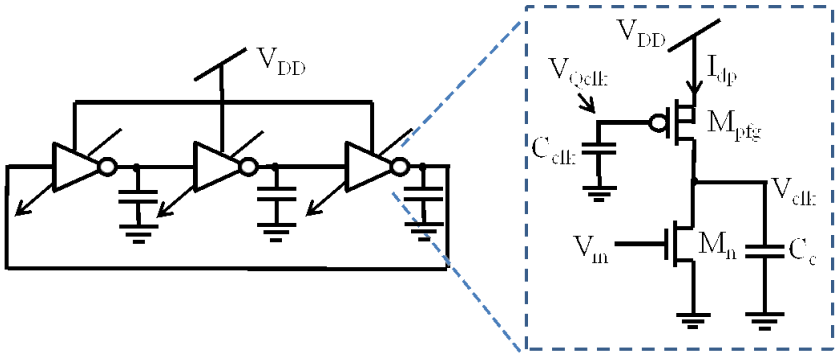


Figure 3.13 : Schematic of a 3-stage ring oscillator with floating-gate PMOS transistor.

3.3.1 Oscillator

Figure 3.13 shows the schematic diagram of the proposed approach towards a low voltage oscillator. It consist of a 3-stage ring oscillator built with current limited floating-gate transistor M_{pfg} that works as a programmable current source. By modifying the charge Q_{clk} on the floating node of M_{pfg}, an arbitrary current can be established though the inverter. From a different point of view, negative values of V_{Qclk} will allow the circuit to work with supply voltages below the threshold voltage of the PMOS transistor, typically around $0.9V$ for a $0.5\mu m$ process. It can be shown that the oscillator frequency will be dictated by the time it takes M_{pfg} to charge the load capacitance of each stage multiplied by the number of stages of the oscillator.

$$f_{osc} = \frac{I_{dp}}{V_{DD} \cdot C_c \cdot N} \tag{3.6}$$

Assuming weak inversion operation, the current passing through M_{pfg} is given by

$$I_{dp} = I_o \cdot e^{\left[\frac{V_{DD} - V_{th} - V_{Qclk}}{n \cdot U_T}\right]} \tag{3.7}$$

Finally substituting equation (3.7) into (3.6) gives the frequency with respect to V_{DD} and V_{Qclk}

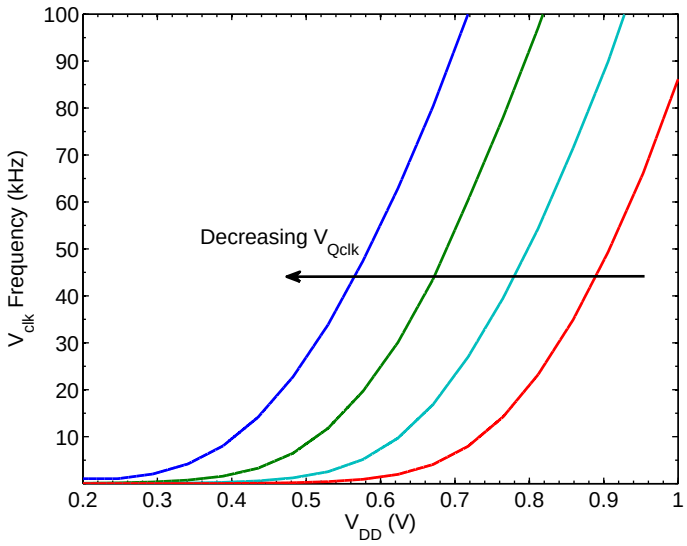


Figure 3.14 : Simulated results demonstrating the frequency of the oscillator with respect to V_{DD} for different V_{Qclk} values.

$$f_{osc} = \frac{I_o \cdot e^{\left[\frac{V_{DD}-V_{th}-V_{Qclk}}{n \cdot U_T}\right]}}{V_{DD} \cdot C_c \cdot N} \tag{3.8}$$

where I_o is the current at V_{gs}=V_{th}, n is the slope parameter, U_T is the thermal voltage, N represents the number of stages and $V_{Qclk} \approx \frac{Q_{clk}}{C_{clk}}$.

A 7-stage ring oscillator was simulated to validate the proposed approach towards a low voltage oscillator. Figure 3.14 shows the frequency behavior of the oscillator as a function of the supply voltage for several V_{Qclk} values. As expected from Equation 3.8, the exponential behavior of the current dominates f_{osc} and changes of V_{Qclk} can be viewed as changes in the effective threshold voltage of the floating-gate transistor. It can be seen clearly that operation of the circuit is possible for supply voltages values lower than 0.5V.

The seven stage oscillator was fabricated as part of the start-up circuit, meaning it is hard-wired to the charge pump described in the next section. Figure 3.15 shows the oscillator response with a supply voltage of 1.5V and a charge of approximately -0.6V at the floating node. Due to a design mistake the output of the oscillator is tied

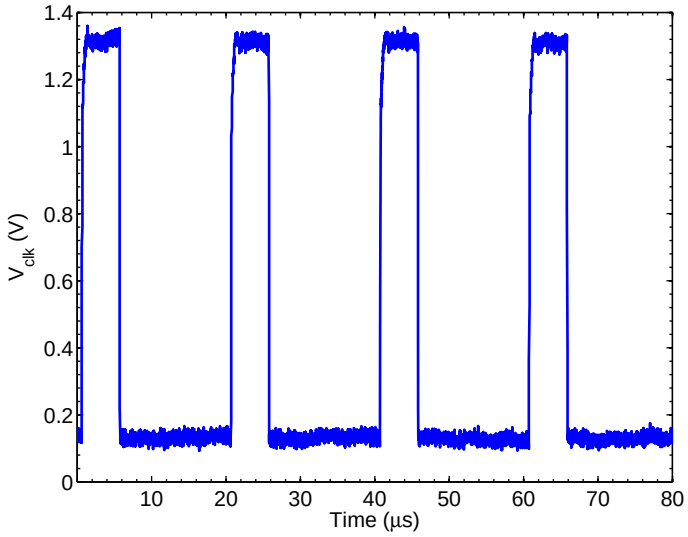


Figure 3.15 : Measured signal of the ring oscillator with respect a V_{DD} voltage of 1.5V and V_{Qclk} value of approximately -0.6V.

directly to a digital buffer. Since the buffer is designed to work under 5V a minimum supply of 1.5V is needed for it to work. Under these conditions the circuit has an output frequency of 50kHz an the output of the buffer. A level shifter would had to be designed to obtain the output wave under its normal working conditions at 0.5V. However, the design is known to work for voltages as low as 0.35V due to the fact that the complete startup circuit was tested at these voltages. This result is proved in the next section. A complete characterization of the circuit can be obtained in a future work by designing only the oscillator with the lever shifter mentioned before.

3.3.2 Complete Start-up circuit

Figure 3.16 presents a three stage representation of the complete proposed start-up circuit. The charge pump used in the start-up circuit was designed with the same characteristics as the one presented in Section 3.2.2. The only difference is that the aforementioned ring oscillator is connected directly to the charge pump, no switches are used to change each stage phase. This approach was used because the voltage under normal operating conditions of the oscillator is too low to activate the switches.

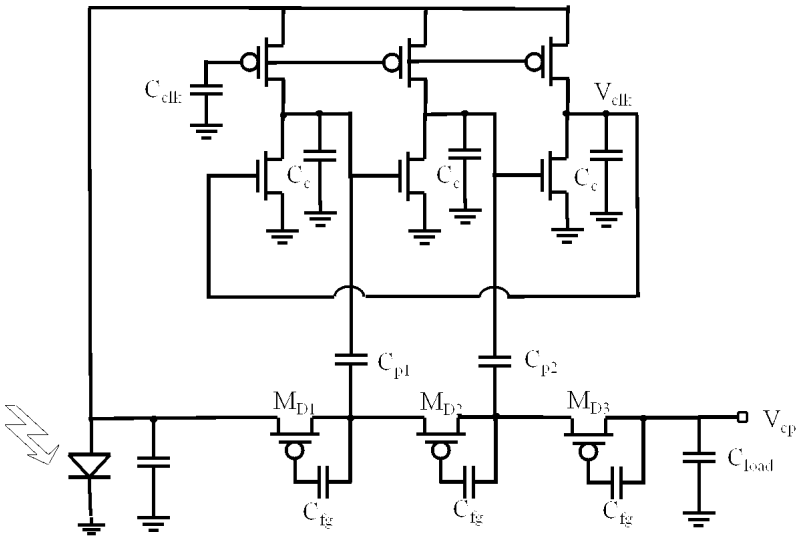


Figure 3.16 : Schematic of a 3-stage representation the proposed start-up circuit.

Additionally, the fabricated charge pump for this circuit consists of eight stages. The number of stages was chosen to ensure the output voltage was sufficient for a low input voltage of approximately 0.5V.

The fabricated start-up circuit input is hard-wired directly to the p-diff terminal of the photodiode, a connection to a bare pad is also connected at this node so an input voltage can be supplied to the circuit. At the same time, the pad serves as a way to measure the generated voltage from the photodiode. The output of the charge pump circuit is also connected to a bare pad since an external capacitor is to be connected at this site.

Characterization of the circuit was done by connecting a voltage supply at the input of the circuit and measuring the output. The output current is even smaller than in the main charge pump presented in Section 3.2.2. This is due to the fact that only one stage is used, capacitors C_p are 3pF and the input voltage is very low which means the charge transfer between stages is very small. As a consequence of these factors the output of the charge pump had to be connected to an external buffer and measurements taken at the output of it.

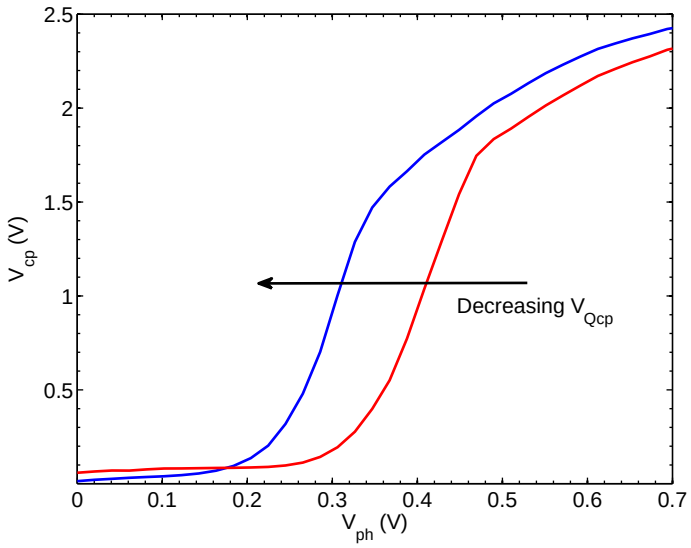


Figure 3.17 : Output voltage of the start-up circuit for two different programmed voltages.

Figure 3.17 presents the output voltage of the start-up circuit with respect to the input voltage. The graphs represent the the change in threshold voltage by the charge injected in the diode-connected FGMOS of the charge pump. The graphs were taken for two different programmed voltage while maintaining the charge at V_{fgp} of the oscillator constant. It is clearly seen how the start-up circuit is capable of working under very low input voltages. When the FGMOS of the charge pump are programmed at their optimum point a 1V output voltage can me obtained from an 0.3V input.

3.3.3 Hysteresis Comparator

The start-up circuit is completed by a hysteresis comparator that is in charge of connecting and disconnecting a load to the output voltage of the charge pump. The design of the comparator is simplistic in nature consisting only of two inverters, two NMOS FGs, a capacitor and three switches. The comparator's hysteresis is programmable which means that its tripping points can be changed to a desired value by adjusting the charge of the FGs. Figure 3.18 shows the schematic of the hysteresis

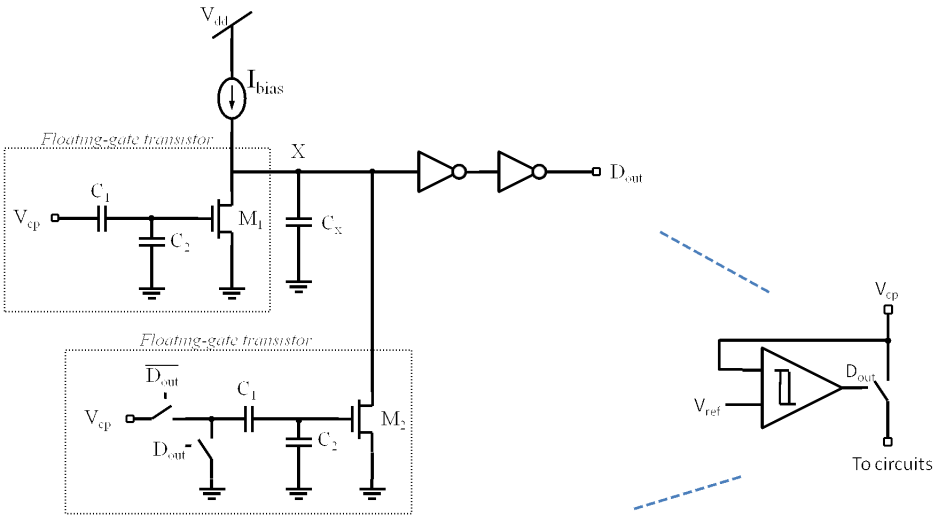


Figure 3.18 : Schematic of the hysteresis comparator.

comparator, both FG transistor have a capacitor coupling of 0.5 by connecting one of the V_Q terminals to ground an the other one to the output of the start-up charge pump. The behavior of the circuit can be explained by knowing the voltage change in capacitor C_X with respect to the input voltage V_{cp} and the programmed voltage at the floating node of each FG. The voltage at X will depend of the currents charging or discharging the node. At node X the current relation is

$$I_C = I_{bias} - I_d \tag{3.9}$$

I_d is the current of transistors dependent of its gate-source voltage,

$$V_{gs} = V_{cp} \cdot \frac{C_1}{C_1 + C_2} + V_Q \tag{3.10}$$

where V_{cp} its the charge pump output voltage and V_Q is the charge stored at the floating node. Inserting the previous equation in the saturation equation of the transistor gives current I_d. Substituting I_d and the current equation I_C with respect to voltage in a capacitor into Equation 3.9 the change in the capacitor voltage V_C with respect to time is obtained.

$$\frac{dV_{C_X}}{dt} = \frac{I_{bias}}{C_X} - \frac{K}{2C_X} \cdot \left(V_{cp} \cdot \frac{C_1}{C_1 + C_2} + V_Q - V_{th} \right)^2 \tag{3.11}$$

where K represents the charge mobility and oxide capacitance of the transistor.

Separating variables and integrating at both sides of the equation gives the final equation

$$V_{C_X} = \frac{1}{C_X} \int I_{bias}\, dt - \frac{K}{2C_X} \int \left(V_{cp} \cdot \frac{C_1}{C_1 + C_2} + V_Q - V_{th} \right)^2 dt \tag{3.12}$$

In this work, the comparator is used to close a PMOS switch when the charge pump reaches a voltage high enough to power the system and open it when it surpasses the low supply voltage limit so that the charge pump can recharge its output capacitor again. Following the equation, when $V_{cp} \cdot \frac{C_1}{C_1+C_2} \leq (V_Q - V_{th})$ both transistor are off and Capacitor C_X gets charged to the diode voltage by the current I_{bias}. When V_{cp} is sufficiently large to turn on the inverters the output D_{out} goes high. It is important to note that this output will remain low until the inverters can turn on. Once D_{out} is high M_2 is disconnected leaving M_1 in charge of monitoring the charge pump voltage. V_{cp} can increase until $V_{cp} \cdot \frac{C_1}{C_1+C_2} \geq (V_Q - V_{th})$, at this time M_1 is turned on and discharges the capacitor causing the digital output to go low, connecting V_{cp} to the load and turning on M_2. When V_{cp} reaches the voltage described by Equation 3.10 for M_2, this transistor is turned off letting the capacitor charge again and starting the process again. The behavior of the circuit its demonstrated in Figure 3.19 , where M_1 and M_2 were programmed to change at 1.5V and 1V respectively. The start-up circuit output V_{cp} is connected to a $1\mu F$ capacitor load and the load is the scavenging circuit.

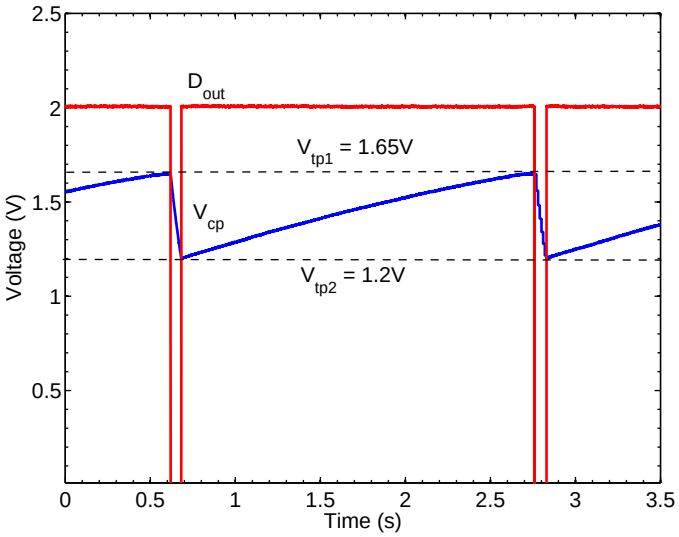


Figure 3.19 : Output voltage of the start-up (V_{cp}) circuit and D_{out}.

CHAPTER 4
Results

Three different versions of the solar system were for fabrication at MOSIS. All of them were fabricated in a $0.6\mu m$, single well, 3-metal, CMOS bulk technology and packaged in a 40 DIP package with a ceramic removable lid. In the first iteration the programming circuit presented in [34] was used since the circuit was already available and proved to work within the requirements of our system. The programming circuit was replaced in the second iteration by the charge modification system presented in Section 2.3.3 so that the floating gates could be in functional mode with no external supply voltage available. The only change between the second and third iteration was made in the start-up circuit; capacitors were added to each node of the ring oscillator. Although the capacitor size are very small the frequency of the oscillator can be greatly reduced by the increase of capacitive load at each node. Thus, decreasing the switching activity and speed of the start-up charge pump. Figure 4.1 shows the layout of the system, it can be seen that all the circuitry except the photodiodes were covered with metal-3 which is the top metal layer of the MOSIS $0.6\mu m$ CMOS technology. This was done as a protection mechanism to the circuits used to prevent the p-n junctions of the circuits to become active with sunlight.

Bare pads were used for the outputs and inputs of most of the circuits including the photodiodes, the charge pump outputs and the output of the MPPT circuit. These pads represent only a capacitive load to the internal pins as they do not include any type of circuitry to buffer the signals from the chip to the external world. Since the system works with such small currents when the chip was placed on the forty pin

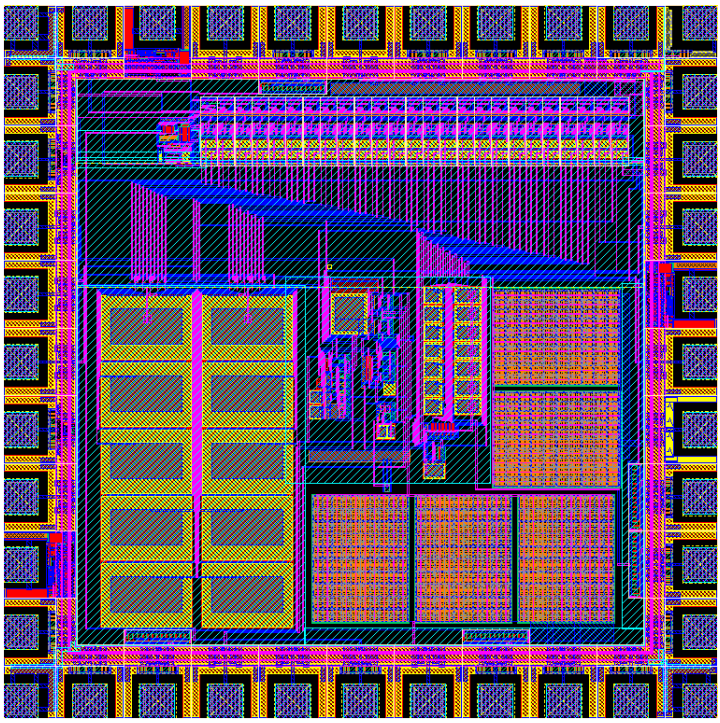


Figure 4.1 : Layout of the solar scavenging system sent to fabrication.

socket of the test bench, the bare pad outputs did not respond to the initial tests. It was determined that the metal of the sockets represented a big load for the circuits to handle. The solution was to pry out the pins of the chip from the testbench socket and wire-wrap them to the corresponding capacitors. Then, an external analog buffer consisting of an LMC660CN IC was used to measure the voltages at these pins.

Each block presented in the previous sections of this work were tested individually within the same chip while connected to each other. After having tested and characterized the individual parts of the solar energy scavenging system, a test of the whole system working together was conducted. The twenty four FGMOS of the system were programmed at their optimum points so that the whole system could be tested. Initially the system was taken out to the Sun in a wire wrapped board after it was programmed and the start-up circuit was reset. As soon as it was opened the voltage at the output of the start-up circuit was measured to be approximately the voltage of a photodiode but negative. This was the effect of the n-well/substrate

parasitic diode, since there are parts of the die that are still exposed to the light, the p-n junction between the substrate and the n-well of the last PMOS transistor of the charge pump was activated. As mentioned in Section 2.1 a parasitic diode forms between the n-well and the substrate, if sunlight reaches the substrate the current of this diode will surpass the current of the floating diode and draws it to ground. This behavior was observed because the bulk of the charge pumps PMOS transistor is connected to its drain, which its the output of the charge pump. Since there was not a strong ground the voltage measured between ground and the output of the charge pump was the negative of a diode voltage, the parasitic diode was conducting current to the substrate and the diode was forward biased from substrate to n-well. This behavior can also be attributed to the triode formed at each transistor. Any charge that is transmitted trough the substrate can cause the triode to latch-up and become a feed-forward circuit drawing current from the n-well. It is known that latch-up can occur in CMOS circuits under radiation or optical illumination environments.

Due to the problems mentioned above the system was tested with voltage supplies as inputs, one for the start-up circuit and one for the MPPT input diode voltage. A voltage of 0.8V was used as the input for the start-up circuit to make sure V_{cp} surpassed 1.5V. The start-up circuit was programmed so that it could reach its maximum output voltage with an input of 0.5V. As discussed in Section 3.2.2 the programming of the charge pump transistors can not surpass a certain limit before it starts to loose efficiency. The FGMOS of the ring oscillator, on the other hand, was programmed at a lower voltage so that it could worked better for lower voltages. The loss in efficiency of the charge pump can be contributed in part to the use of the type of inverter normally called a pseudo-NMOS inverter [42] used in the ring oscillator. It has the advantage of working under low voltages but the voltage transmitted to the output will not be the full rail voltage. The input to the MPPT circuit is set to 0.5V also, the charge pump was programmed at the same values as the start-up circuit

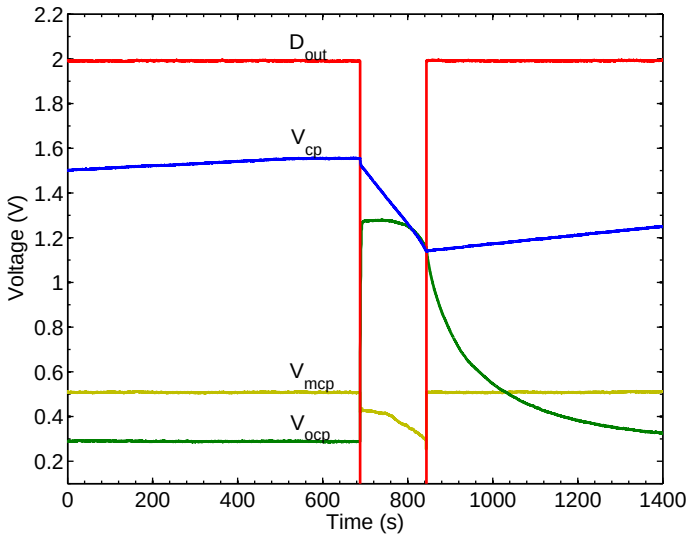


Figure 4.2 : Result of the complete energy scavenging system

and the oscillator FGMOS was programmed so that its frequency gets slower after V_{cp} reaches 1.5V.

Figure 4.2 shows the results of the complete system. The start-up circuit has a load of $47\mu F$ and an input voltage of 0.8V. The capacitor size was chosen so that the power management circuit could work for a couple of seconds. The complete charging of the load capacitor can not be presented due to the long time it takes to charge, this is due with the low output current of the start-up circuit which is approximately 36.6nA. Once V_{cp} reaches 1.55V D_{out} goes low and connects the $47\mu F$ capacitor to the power management system. A NMOS transistor is connected as a switch between the MPPT input and V_{mcp}, its gate connected to D_{out}. This switch has the purpose of charging the capacitor at V_{mcp} to the input voltage value when the rest of the circuit is turned off, once the power management system is connected the switch stops supplying the capacitor. This is the reason why the voltage at this node is initially 0.5V and once the MPPT and charge pump start to work it reduces to approximately 0.4V. A 470pF capacitor was connected at V_{mcp}, this capacitor maintains the optimal voltage when the charge pump starts to work. The main

charge pump also starts to work as soon as D_{out} goes low. Its output voltage can be seen in Figure 4.2 , where it reaches 1.3V for an input of 0.4V. It doesn't reach the desired value when compared to the results is Section 3.2.2 for various reasons. The first is that the load is much greater than the one used to characterize it so the time to charge it to the actual output value will increase. In this case the load is $1\mu F$ compared to the 470pF of the characterization, almost double the size. Other reason might be issued to process variation in the chip. As the threshold voltage changes from batch to batch the programmed voltage value at the FGMOS might not be the same for different chips. Another cause can be attributed to the lack of ability of the circuits to work under 1.5V of supply voltage. The current reference as well as the integrate and fire oscillator have been proven to work with 1.2V supply voltage but the main oscillator and the MPPT don't work well under this voltages. The MPPT is capable of working under 1.5V but the optimal voltage values starts suffering from an offset. Both V_{mcp} and V_{ocp} can be seen to decrease at some point while they are working. In the figure, voltage V_{ocp} starts to decay after D_{out} is set high. At this point the power management is disconnected from V_{cp}, since there is no switch between the output capacitor and the output of the charge pump all the charge stored at the capacitor discharges through the charge pump output transistor. This is a problem that can be solved by disconnecting the output capacitor from the charge pump using D_{out} as a control signal.

All test of the system were conducted in the Electronics Testing and Characterization Lab (ETC) using a custom board shown in Figure 4.3 . The board consists mainly of a Xilinx Spartan XEM-3001 FPGA with OpalKelly software. OpalKelly permits an easy way to communicate between the FPGA and Matlab. The rest of the board consists of an ADC, DAC and voltage amplifiers. The board was used to provide supply voltages and reset signals as well as the injection and tunneling voltages

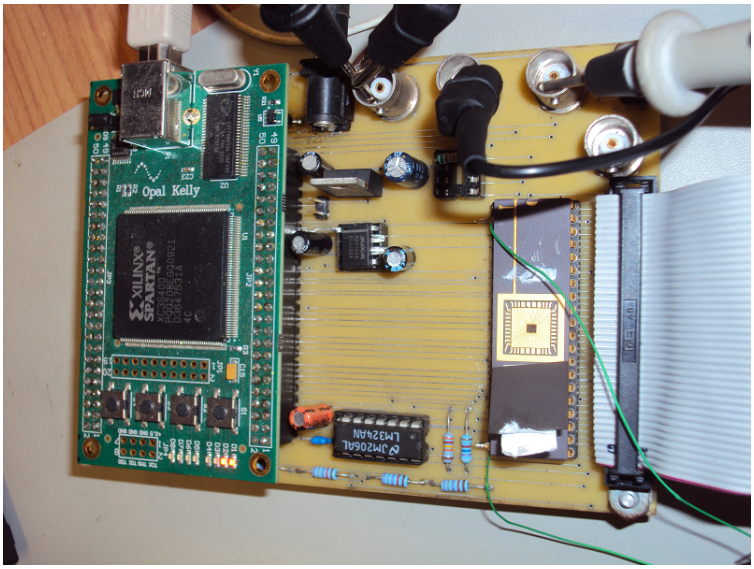


Figure 4.3 : Test board including the Spartan FPGA and the fabricated ASIC.

to the ASIC. DC measurements were made with a Tektronix DMM4040 voltmeter and signals with respect to time were captured with Tektronix DPO3014 oscilloscope.

CHAPTER 5
Conclusion & Future Work

This work presented the the requires elements to achieve an integrated Solar energy scavenging system. The proposed system was achieved through the use of low power design techniques and floating-gate transistors. Different areas were discussed toward its implementation as the use of integrated photodiodes, DC-DC conversion and maximum power point tracking techniques.

Different versions of the ASIC were fabricated in a $0.6\mu m$ single-well CMOS technology and tested. This technology offers a minimum threshold voltage of 0.7V for NMOS transistors, the critical parts of the design were proven to work well below that limit. A start-up circuit capable of working with voltages as low as 0.3V was presented along with ultra low voltage charge pumps. Floating-gate charge pumps where employed as the main DC conversion mechanism due to its low voltage operation capability and ease of implementation. The charge pumps have been demonstrated to work with voltages lower than the threshold voltages of the transistors of the used technology. A FGMOS programming circuit suitable for energy harvesting systems was design and implemented, the circuit doesn't need a supply voltage when it is in functional mode. A MPPT scheme achieved through the use of a low power oscillator and a switching capacitor sample and hold amplifier. Use the afore mentioned MPPT scheme provides a simple and integrable way of obtaining the maximum power of the solar cells without the need of external components. Characterization of the integrated photodiodes was presented, where a maximum power of $.22\mu W$ was obtained for a photodiode array. All parts were characterized individually and as part of the

complete system, proving the design to achieve its purpose. All this with voltage supplies lower than 1.5V. Results, although different in precision when compared to the results from simulations, demonstrate the usefulness and capabilities of the solar energy scavenging system.

There are some issues that can be explored in the future related to this work. A comparison between a regular charge pump and the FGMOS charge pump presented in this work can be used to compare how much more efficient the FGMOS charge pump is. Maximization of the output current the charge pump can supply is one of the main concerns to obtain a better scavenging system, several methods discussed in recent papers can be studied to achieve this. Also, for the charge pump, retention of the FGMOS charge with switching activity can be studied for future designs and different applications. For this work, the LRCM method was used to to simulate the photodiodes and calculate its maximum power point. Application of the LRCM method is used for big solar panels, but there is a possibility it could be used in the micro scale. Furthermore, an automatic digital implementation of the LRCM algorithm can be implemented and manufactured in a single chip. Other types of low power MPPT schemes can be studied and compared based on area and effectiveness. As mentioned before, a top layer of metal-3 was used in this work to protect the circuits from the light, it would be interesting to know the effect of capacitance on the circuits due to this protective layer.

It is made clear in this work that achieving a monolithic solar energy scavenging system is challenging in bulk technology. However, through the use of Silicon on Insulator (SOI) a complete monolithic implementation of the scavenging circuit could be possible. Also, on this technology series diodes could be connected, maybe arrays of these would supplant the need for a start-up circuit. Besides the use of a SOI technology, smaller scale technologies could be used for the the design of energy scavenging circuits in general. The smaller scale technologies can take advantage of

its low threshold voltages and low supply voltage operation to achieve more power efficient systems.

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