BUILT-IN SELF TEST IDD SUPPLY CURRENT SENSOR

By

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A dynamic current (iDD) sensor supply is presented. The sensor uses the pad inherent resistance (the available between the positive power supply, Vdd, and the mission circuit), which allows current measurements without placing a device between the power supply and the circuit under test (CUT). Characterization of the pad frame, potential integrated measuring solutions by a current to voltage conversion and a preview of its use as a flag for faulty circuits are presented. The proposed circuit is a Built-In Self Test (BIST) capable of using already available integrated structures for measuring current waveforms. Vdd ring characterization yields an equivalent resistance of 225.948 mΩ. Some of the challenges involved in the design of such a sensor are: high-gain, high-bandwidth, low-power, low-noise, linearity and high slew rate. Circuit design and simulations were implemented using Cadence 0.6um CMOS technology and AMI 0.6um fabrication process.

Resumen de Disertación Presentado a Escuela Graduada
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CIRCUITO SENSOR DE LA CORRIENTE DE SUPPLY IDD

Por

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2009

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Un sensor de corriente dinámico es presentado. Este utiliza la resistencia inherente (estructura entre el contacto de fuente de potencia positiva, Vdd, y el circuito de misión), para realizar medidas de corriente sin la necesidad de colocar un dispositivo entre Vdd y el circuito bajo prueba. Caracterización del marco de contactos, potentes soluciones integradas para medir a través de una conversión de corriente a voltaje y sus usos como una bandera para circuitos con fallas es presentado. El circuito propuesto es un Built-In Self Test (BIST) capaz de usar la estructura disponible para medir las formas de corriente. Caracterización del anillo de Vdd resultó en una resistencia equivalente de 225.948 mΩ. Retos envueltos en el diseño son: alta-ganancia, alto-ancho de banda, baja-potencia, bajo-ruido, linealidad, y alto-slew rate. El diseño del circuito y simulaciones fueron implementados usando Cadence tecnología CMOS 0.6 um y AMI 0.6 um para la fabricación.

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by

Melissa Rivera Rivera

I dedicate this work to all those who did not have the opportunity to study and to those who will not even have the opportunity to live because they are too small to speak for themselves. I dedicate this work to all poor and disable people. Because despite their circumstances in fact they have the strength, disposition and courage to work hard, inspire and serve others.

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This work would not have been possible without the support of many people. At first I wish to express my gratitude to God and to my family. Deepest gratitude is also to my friend Mr. William Rivera who was abundantly helpful I also want to thanks my advisor, Dr. Ducoudray for her invaluable assistance. I thank gratefully Texas Instrument Inc. and The GEM Scholarship for its economic support and also to my best friends who always have been there.

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LIST OF ABBREVIATIONS

DUT	Device under Test.
ICs	Integrated Circuits.
BIST	Built-In Self Test.
BICS	Built-In Current Sensors.
Op Amp	Operational Amplifiers.
SCM	Simple Current Mirror.
CCM	Cascoded Current Mirror.
FCCM	Fully Cascoded Current Mirror.
WCM	Wilson Current Mirror.
LVCM	Low Voltage Cascoded Current Mirror.
FVFCM	Flipped Voltage Follower Current Mirror.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
JFET	Junction Field Effect Transistor.
BJT	Bipolar Junction Transistor.
VCDA	Very large Common mode Differential Amplifier.
VLCT	Very Low Cost Tester.
SA_1	Stuck at Vdd fail.
SA_0	Stuck at Vss fail.

LIST OF SYMBOLS

t	Time (seconds)
μm	Micrometers.

CHAPTER 1
JUSTIFICATION

1.0.1 Motivation

Today, designing and developing test schemes for integrated circuits is challenging. As integrated circuits increase functionality, access to internal nodes becomes limited because of the quantity of components present in the design. This constraint adds complexity to the circuit's characterization. Historically, all nodes were 100% accesible, thus they were easily observed and controlled. As the world of integrated circuits developed, observability of internal nodes could only be addressed in an indirect manner [1].

Metrodology developed for testing internal nodes aided in retaining observability of the circuit. However, as the number of nodes increased, the time spent testing each node became and unbearable factor. It's severely increased the cost of testing without adding functionality and much benefit to the diagnostics. Test engineers developed novel and efficient methodologies that decreased test times while accurately detecting failing circuits. For example; testing highly complex circuits in VLSI usually equates to a significant increase in test time. This creates a delay in the time-to-market, thus an increase in the cost of the analog or mixed signal device.

Some of the efforts in reducing the time-to-market have alluded to the possibility of finding defective circuits early on, by measuring the power supply current. These currents are usually referred to as IDDQ (static current) and iDD (dynamic

current). A myriad of circuits have been developed to sense such currents. These circuits are eventually added to the mission circuits[1] to aid in the characterization and diagnostics. Nowadays, tests are organized to make an early detection of catastrophic faults or failing circuits. One of the methods proposed for such an endeavor is a supply current footprint measurement. The supply current footprint is a current waveform taken from the supply of a defect-free circuit. This becomes the signature or footprint of a defect-free device. Theory states that a defect-free circuit will have a specific current footprint. Defects in the architecture will create a current waveform that diverges from the defect-free one, known as a faulty supply current waveform.

A suggested method to sense the current signature is known as Vdd pulsing. This method consists of setting all the voltages in the Circuit Under Test (CUT) to a specific level and then pulsing the positive rail from Vdd to Vss and back to Vdd, recording the supply current waveform. This current waveform of a defect free circuit becomes the footprint that the remaining circuits will be compared to. To sense this current, a sensor must be designed and connected to the circuit. This creates an architecture capable of testing itself, known as Built-In Self-Test (BIST) circuits. BISTs are capable of sensing internal parameters within the chip without compromising its functionality.

The circuit proposed is a BIST capable of sensing the current waveform from the Vdd supply without diminishing the voltage supplied to the mission circuit. The BIST uses the bonding pad architecture to extract the current waveform.

[1] mission circuit = Circuit Under Test (CUT), circuit designed to perform a function, not specifically for testing.

1.0.2 Organization

The chapters in this thesis are organize as follow:

- Chapter 2 explores theoretical background on current mirrors and operational amplifiers.
- Chapter 3 presents more specific techniques for high gain, large bandwidth operational amplifiers.
- Chapter 4 presents the objectives of this work.
- Chapter 5 shows the method of analysis and the design general approach.
- Chapter 6 presents the desired parameter to be sensed in this work.
- Chapter 7 introduces the system designed in this work.
- Chapter 8 presents test results of the design.
- Chapter 9 summarizes conclusions and proposes future work to adopt the proposed scheme to other technologies.

CHAPTER 2
LITERATURE REVIEW

2.1 Current Mirrors

Current mirrors or current sensors are circuits capable of replicating a given current. Once it is mirrored, it can be amplified or used to source or sink current to any other circuit. Current mirrors range from the simplest to highly accurate and complex current replica circuits. A comparison among the most commonly used mirrors is provided.

The simplest current mirror configuration is known as a Simple Current Mirror (SCM). It consists of two transistors, a current sensing self-bias transistor and a mirroring active transistor. Figure 2–1, shows a simple current mirror configuration using NMOS transistors.

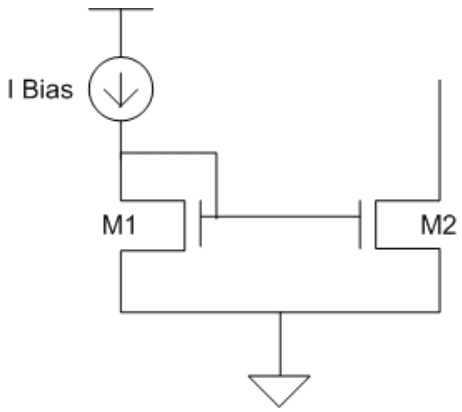

Figure 2–1: Simple Current Mirror

To have an accurate current replica both transistors must operate in the saturation region. The current in these transistors is given by:

$$Ids = \frac{\mu_n Cox}{2}\frac{W}{L}[V_{GS} - V_t]^2[1 + \lambda V_{DS}] \tag{2.1}$$

In figure 2–1 transistor M1 senses the biasing current and generates the biasing voltage for the gates of the transistors M1 and M2 (V_{GS1}, V_{GS2}). If both transistors are equally sized, and have the same threshold voltage, their currents will be similar. The circuit suffers from an output current offset if the drain to source voltages (V_{DS1}, V_{DS2}) of these transistors are not equal. The voltage V_{DS1} is set by the biasing current, I_{Bias}, while V_{DS2} depends on I_{Bias} and the load connected to transistor M2. Small signal analysis of this circuit shows that it has a low input impedance Rin = $(1/g_m)$ and a considerable output impedance of Rout= r_0. The analysis is shown in appendix A.

An ideal current source has an infinite resistance in parallel with the source. Mimicking an ideal current source entails increasing the output impedance. To accomplish this, the transistors of the simple current mirror will be cascoded. The Cascoded Current Mirror (CCM) (see figure 2–2) greatly increments the output impedance of the circuit. This increases the accuracy in the current replica by reducing the output current offset caused by difference in V_{DS}. See figures A–9 and A–10.

Transistors M1 and M2 in figure 2–2 sense the biasing current and generate the biasing voltages for the gates of M3 and M4 respectively. In this configuration, the gate to source voltage, V_{GS1}, in M1 equals the gate to source voltage in M3, V_{GS3}. V_{GS2} is equal to the gate to source voltage in M4, V_{GS4}.

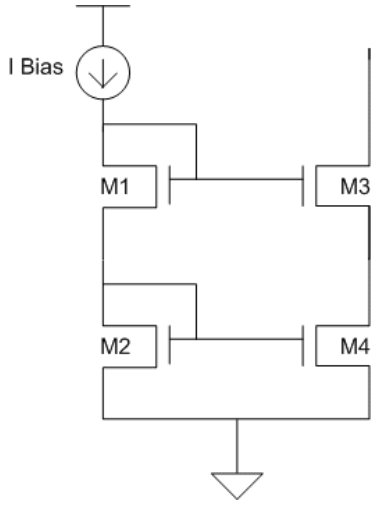

Figure 2–2: Cascoded Current Mirror

Analysis of this circuit shows a mild increase input impedance Rin = $(2/g_m)$, and a significant increase in output impedance Rout= $(g_m {r_0}^2)$. Although the output impedance in this circuit is a better approximation of an ideal current source, the circuit suffers from higher input voltage limitation and a decrease in the operational output voltage range (see Appendix A).

In order to maintain a low voltage supply and keep reasonable high output impedance another current mirror known as Low Voltage Cascoded Mirror (LVCM) is introduced. The input impedance is close to Rin = $(1/g_m)$ and maintains a high output impedance of Rout= $(g_m {r_0}^2)$. The LVCM works with a lower voltage supply at the cost of loosing the self biasing advantage.

Figure 2–3 shows the configuration for this circuit and the analysis is shown in appendix A.

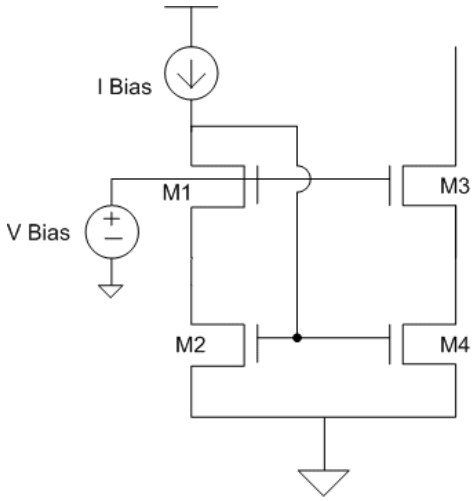

Figure 2–3: Low Voltage Cascoded Current Mirror

A very low input impedance can be achieved by the Flipped Voltage Follower Current Mirror (FVFCM), [2] [3], is one of the best options because it's Rin = $1/(g_m{}^2\ r_0)$. The FVFCM has a high Rout = $g_m\ r_0{}^2$ but it present a higher power consumption profile. The previous information is explained in detail in [4],[5],[6] and summarized in the table: 2–1

All these current sensors can be used for dynamic or static current sensing schemes. One of the oldest and most commonly used, test schemes was the measurement of the static current from the positive power supply known as IDDQ. IDDQ testing is widely used in industry because historically, in digital circuits, it detected several faults with ease. The use of Built-In Current Sensors (BICS) has the advantages of minimizing the need for external instrumentation. Its disadvantages are adding Si area and usually the consumption of small portion of the voltage supplied. The most common concern about BICS and BIST circuits is their impact

in the CUT performance.

Current Mirrors	Advantages	Disadvantages
Simple Current Mirror (SCM)	•Low input impedance (1/gm) •High output impedance (ro)	•Low accuracy in current replica
Fully Cascoded Current Mirror (CCM)	•Self biased (Dynamic; it changes with current) •Low input impedance (2/gm) •High output impedance ($gm*ro^2$)	•Greater voltage needed to polarize •Operational output voltage decreases
Wilson Current Mirror (WCM)	•Output impedance $r_{o3}\ (1+\frac{gm3}{gm2}(gm1r01+1)+\frac{1}{gm2r02})$	•It will always have a design error because by inspection it can be seen that always VDS1 = VGS1 + VDS2 conducting to the understanding that IDS1 ≠ IDS2 because VDS1> VDS2
Low Voltage Cascoded Current Mirror (LVSCM)	•Low input voltage requirements •Low input impedance (1/gm) •High output impedance ($gm*ro^2$)	•Needs external biasing
Flipped Voltage Follower Current Mirror (FVFCM)	•Low input impedance ($1/gm^2*ro1$) (Avoiding the problem of turning off the transistors) •Output impedance ($gm*ro^2$)	•Consumes more power

Table 2–1: Advantages and Disadvantages of Commonly used Current Mirrors

Lee and Tang [7], proposed a circuit that has a minimal impact on the CUT performance without using dual power. The circuit provides a scalable solution with a high sensitivity even for mild IDDQ differences. In [7] quasi linearly programmable current reference is used. This allows test engineers to select current references with accuracy. This design also shows a low sensitivity to parameter deviations caused by process or temperature variations. The performance impact of this circuit in the CUT is not minimal because of not using the dual power technique. The dual power technique [8], has proved to be a good solution to reduce the power dissipation in the circuits. This technique consists of using a higher voltage supply for circuits requiring higher a speed while part of the circuit working at lower frequencies a lower power supply is used. Disadvantages of the work proposed in [7] are a higher power consumption and a drop in the operating frequency of the circuit.

At the beginning, digital circuit design researchers used IDDQ measurements to determine possible defects in a circuit. As mentioned before IDDQ is the measurement of the static current from the positive power supply. Defects in small digital circuits affect greatly this current and faulty circuits were easily detected by using this method. Nowadays, there is an enormous increase in the complexity of circuit design. This causes that the parametric and catastrophic defects are not easily detected by this method. In modern current circuits the iDD pulse metrology has been implemented to sense these faults.

Palumbo and Pennisi, [9], proposed a current sensor which minimized the supply voltage requirements for a class AB current mirrors. A class AB current mirror configuration uses both n-type and p-type current mirrors. This allows an increase in signal amplitude to quiescent current ratio and reduces power dissipation and offset. The main drawback of class AB current mirrors is the high supply voltage required. They presented a topology with low-voltage requirements, able to operate with 2V, implemented in a standard 0.8μm CMOS technology. Their solution exhibits high accuracy, linearity and an extremely high output impedance, without compromising the frequency response. Their circuit DC power dissipation is 57 μW. The circuit output resistance is about 22 GΩ. The low-frequency current transfer gain is -1.6 10^{-3}dB and the cut-off frequency is about 35 MHz.

Ducoudray, Carvajal and Angulo, [3], developed a dynamic current sensor testing scheme (iDD). This method measures the current waveform from the supply when the voltage from the supply has a pulse or ramp signal. The features needed for this type of measurement are a high gain and high bandwidth to measure the transient iDD waveform. They designed a Flipped Voltage Current Sensor (FVFCS) based on the Flipped Voltage Follower (FVF). This circuit provides a good solution

to measure iDD because of the followings:

- low supply
- low input voltage requirements
- very low input impedance
- capacity to sink large current
- approximately constant input voltage

The FVFCS has several stages. The first stage is a FVF, followed by a wide swing low-voltage cascode mirror which feed a load resistor. The load resistor transforms the iDD supply current into an observable voltage V_{RL}. A high frequency buffer is also included to drive the voltage signal across R_L out of CHIP and isolate it from the large output load capacitance C_L. This FVFCS was designed in a 0.18 μm technology, the NMOS transistor sizes were 5 μm/0.2 μm and the PMOS were 35 μm/0.2 μm, C_{in}=5 pF and C_L=5 pF. SPICE simulations with a bias current I_B=130 μA and a single supply voltage Vdd=1.8 V were performed. From the simulations a bandwidth (BW) of 613 MHz was determined for the FVFCS. Analog and digital circuits were used as CUTs and their supply current was used as stimulus I_{IN} for the FVFCS. Simulation and experimental results verify that high speed and low voltage requirements were obtained.

Other researchers have also used current mirrors not only to measure IDDQ but to fix variations induced by circuit faults. For example, Miura's [10] designed a sensor circuit that could potentially detect IDDQ sinking faults. The sensor designed, is also capable of reestablishing the Vdd definition in case a fault is present. The circuit introduced by Miura, [10] has a diode connected between Vdd and the CUT. This diode prevents reverse current to flow into the positive power supply

(Vdd) for a fault-free circuit. When a fault is present and causes a large current there is a voltage drop in the sensor. The current increase is detected and copied by a current mirror. It is converted into voltage by using a load resistor. This forms a loop that compensates for the VDD drop caused by the fault. The main drawbacks of this design are that if the load resistor is large the CUT performance degrades and accurate measurement of the current is difficult. Also having two different power supplies assumes that the diode voltage drop for the second power supply is going to be exactly the same after fabrication ($V_{D1} = V_{D2}$). This design has a device between the Vdd power supply and the CUT, this concept affects the voltage delivered to the CUT. Simulation results also show that the fault detection time of the sensor becomes slower as the fault current decreases.

2.2 Operational Amplifiers

Operational Amplifiers (Op Amps) are one of the most commonly used analog circuits. Their characteristics make them attractive for many uses, such as the measurement of IDDQ through a voltage drop. Figure 2–4; shows the basic structure of the Op Amp. This single ended differential amplifier is composed of two terminals, an inverting and a non-inverting input and a single output terminal.

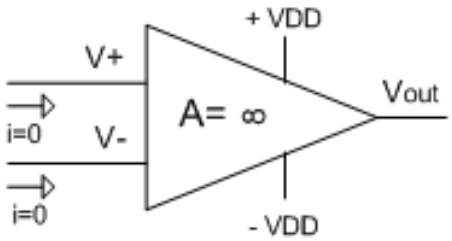

Figure 2–4: Basic Configuration of the Op Amp

The Op Amp's response depends on the difference between the differential inputs and the circuit's gain. Vout= $A(V_+ - V_-)$, where A is the circuit's gain. The ideal characteristics are: infinite open loop gain, infinite input impedance, zero output impedance, infinite bandwidth, zero offset voltage, infinite slew rate, and zero noise. The differential pair in figure 2–5, show the ideal characteristics. In the design of differential amplifier MOSFETs and JFETs are preferred over the BJTs because these provide a higher input impedance, [11], [12].

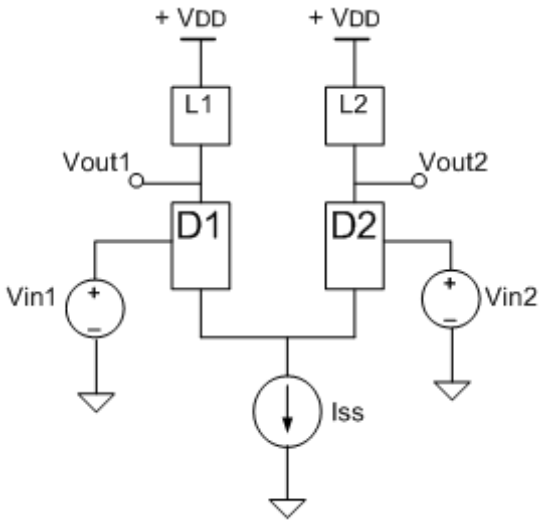

Figure 2–5: Internal Op Amp Circuit. *D1* and *D2* represent any active device. *L1* an *L2* represent any load applied to the Op Amp.

Operational amplifiers main configurations are:

a) Voltage Follower

b) Inverting Amplifier

c) Non-inverting Amplifier

The Differential Amplifier configuration circuit shown in figure:2–6 measures the difference between two voltages, V_1 and V_2. To calculate this difference, it is important to recall that the current through *R1*, $I_{R1}= I_{Rf}$ and $I_{R2}= I_{Rg}$. Using KCL

the current in the negative input terminal of the Op Amp is:

$$I_1=\frac{V1-V-}{R1}=\frac{(V-)-Vout}{Rf}.$$

Solving for Vout =

$$\text{Vout}= V_-(1+\frac{Rf}{R1})\text{-}V1\frac{Rf}{R1}$$

Note that the bottom branch formed of R_2 and Rg is a voltage divider where $V_-=V_+=\frac{Rg}{R2+Rg}$. Now substituting this V_- into Vout,

$$\text{Vout}= \frac{Rg}{R2+Rg}(1+\frac{Rf}{R1})\text{-}V_1(\frac{Rf}{R1})$$

Notice that if $R_1= R_2$ and $Rf= Rg$ this equation will be simplified to:

$$\text{Vout}=\frac{Rf}{R1}(V_2\text{-}V_1)$$

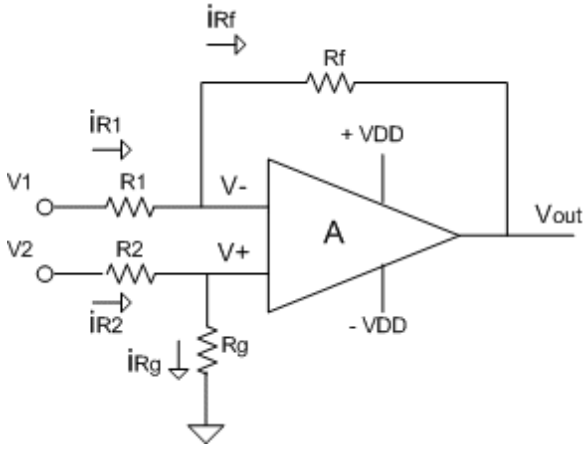

Figure 2–6: Differential Op Amp Configuration (combination of an inverting and a non-inverting amplifier)

2.3 Summary of Five Different OpAmps Configurations:

2.3.1 Single Stage

The following figure shows the circuit topology for the single stage differential amplifier. The topology advantages and disadvantages are presented below.

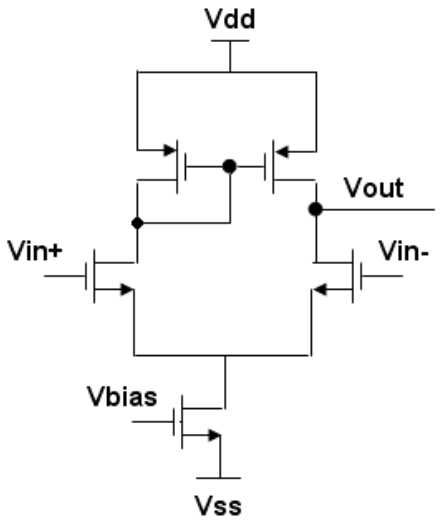

Figure 2–7: Single Stage Circuit Topology

Advantages: Its low output impedance leads to high unity gain bandwidths thus high speeds.

Disadvantages: In the other hand this same low output impedance causes the gain to be low.

2.3.2 Double Stage Amplifier

The following figure shows the circuit topology for the double stage circuit. The topology advantages and disadvantages are presented below.

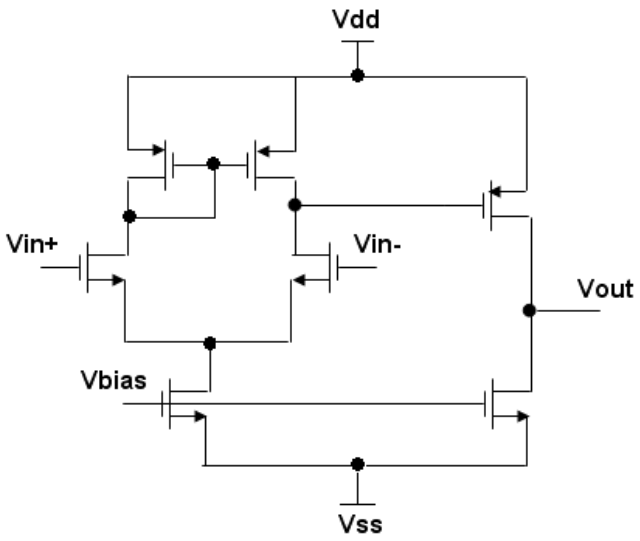

Figure 2–8: Double Stage Circuit Topology

Advantages: Adding another stage increases the output impedance making the gain higher compared to single stage.

Disadvantages: Increasing the output impedance, reduces the speed compared also with the single stage OpAmp, by adding a low frequency pole. This configuration need compensation to stabilize the OpAmp.

2.3.3 Telescopic Cascoded

The following figure shows the circuit topology for the telescopic cascoded circuit. The topology advantages and disadvantages are presented below.

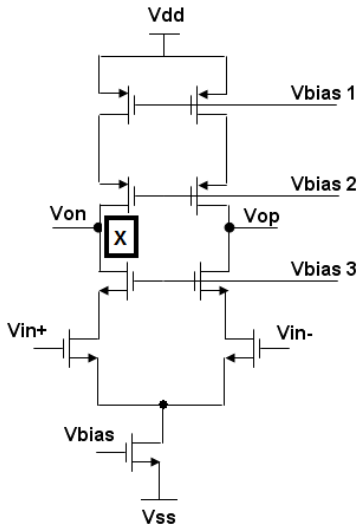

Figure 2–9: Telescopic Cascoded Circuit Topology (showing node X)

Advantages: Single stage OpAmp that exhibits one dominant pole at the output node *(node X)*, which has the highest impedance and in most cases the highest capacitance. For a better understanding it can be recall that $\lambda = \frac{1}{w} = \text{RC}$. If, RC increases $\rightarrow$ λ increases thus w decreases. Because of these reasons this structure typically has higher frequency capability and speed and consumes less power than other topologies. High gain is achieved by the cascoded transistors that contribute as an active load that increases the output resistance.

Disadvantages: Limited output swing due to cascoded transistors (w decreases with the RC increase), which is not desired in low supply voltages.

2.3.4 Regulated Cascoded or Gain Boosting

The following figure shows the circuit topology for the regulated cascoded or gain boosting circuit. The topology advantages and disadvantages are presented below.

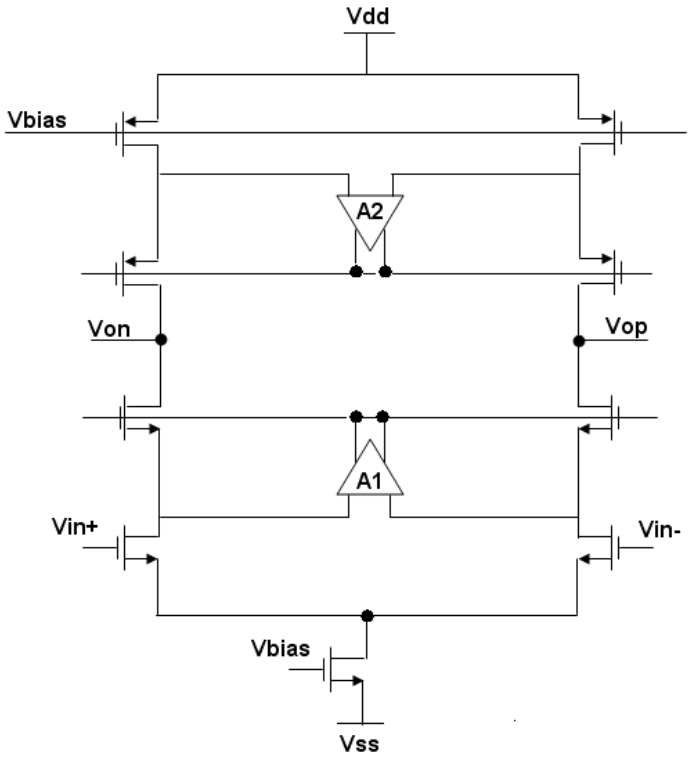

Figure 2–10: Regulated Cascoded Circuit Topology

Advantages: It achieves higher gain and speed without decreasing the output voltage swing. This is accomplished because the gain can be increased by approximately the gain of the gain boost amplifiers. Other advantage is the reduction in harmonic distortion. These are canceled in a fully differential topology when taking the difference in the positive and negative outputs. It is also typical that this topology rejects substrate and coupled noise. This is possible because output lines are typically laid out close to one another and this noise signals appears as a common mode signal on the outputs of the OpAmp and is eliminated when taking the

difference of the two signals at the output. Fully differential circuit topologies also offers a stable *CM* voltage definition $\mathbf{V}_{CM}$. Controlling easier the *CMR* requirement when designing.

Disadvantages: The additional amplifiers that contribute in increasing the gain have to be carefully designed so these does not affect the overall amplifier speed. These must have a very large bandwidth for not affecting the entire configurations speed. This topology requires adding a common-mode feedback *(CMFB)* circuit to ensure that the common-mode output unaffected by process or temperature variations.

2.3.5 Folded Cascoded

The following figure shows the circuit topology for the folded cascoded circuit. The topology advantages and disadvantages are presented below.

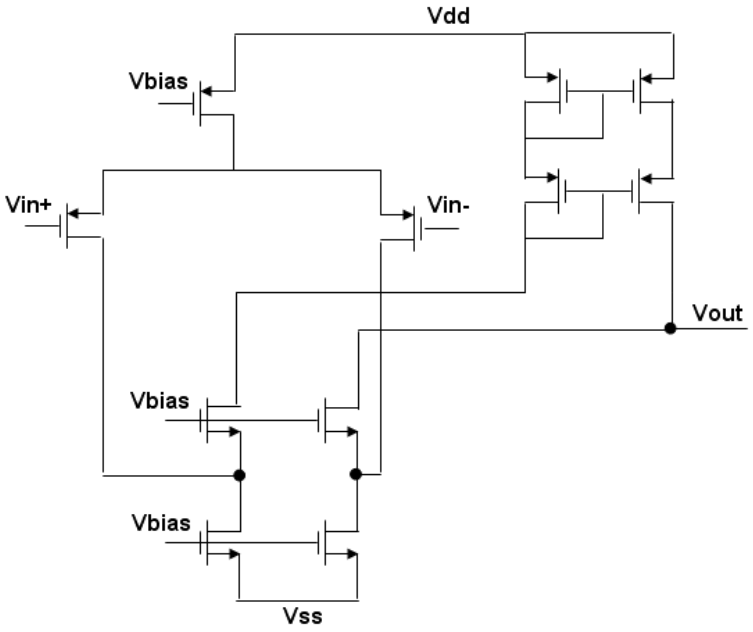

Figure 2–11: Folded Cascoded Circuit Topology

Advantages: This circuit combines the advantages provided by the two-stage amplifier and the telescopic cascode amplifier. Low supply voltage, high output voltage swing.

Disadvantages: Compared with the two stage amplifier this one has less gain and compared with the telescopic cascoded it is slower.

2.4 Summary of Gain vs. BW depending on the circuit topology

The following table presents a summary of the gain and bandwidth capabilities of the different structures presented above.

Gain vs BW Circuit Comparisons		
Structure	**Gain**	**BW**
Single Stage	Medium	Medium
Double Stage	High	Low
Telescopic Cascoded	Medium	Highest
Folded Cascoded	Medium	High
Regulated Cascoded or Gain Boosting	High	Medium

Table 2–2: Summary of Gain vs. BW depending on the circuit topology.

2.5 Bootstrapping Technique

This technique is used when the output voltage must swing up to V_{DD}. This technique is based on increasing the effective output resistance. To illustrate this concept figure 2–12 will be used.

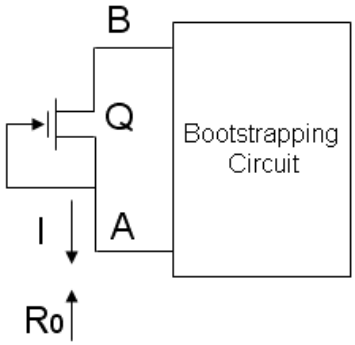

Figure 2–12: Bootstrapping circuit used to explain the bootstrapping technique, [Sedra/Smith97].

The circuit inside the box "Bootstrapping Circuit" senses the voltage at the bottom node of the current source A and causes a voltage B to appear at the top

node. The relationship between these nodes is given by:

$$V_B = V_S + \gamma\, V_A$$

V_S is the dc voltage required to operate the current-source transistor in saturation and γ is a constant less than 1. The incremental output resistance of the bootstrapped current source can be found by causing the voltage V_A to increase by an increment v_a. To find the output resistance: the following steps are done:

1) Note that an increment in V_B can be represented as $v_b = \gamma v_a$.

2) An incremental current through the current source is therefore $(v_a\text{-}v_b)/r_0$ or $(1\text{-}\gamma)v_a/r_0$.

3) The output resistance R_0 is: $R_0 = (V_a r_0)/[(1\text{-}\gamma)v_a] = r_0/(1\text{-}\gamma)$.

In other words, the output impedance is increased by the factor of $1/(1-\gamma)$ which increases as γ approaches unity. Bootstrapping circuit senses any change in voltage that occurs at one terminal of the current source and causes an almost equal change to occur at the other terminal. By following this logic, it is possible to maintain almost constant the voltage across the current source causing minimal change in the current through the current source transistor.

Using several OpAmp configurations, researchers have designed several sensors. Zohdy and Purcell, [11], proposed a general procedure for designing high performance OpAmps. They suggested using standard cells which fit certain criteria. The component chosen for implementation of the OpAmp is the Very large gain,

Common mode Differential Amplifier *(VDCA)*. The simulated[1] results from this design are: 140 dB open-loop gain and 43 MHz unity gain frequency *(GBW)*. The circuit is implemented using a 2.0 μm nwell CMOS technology through MOSIS. The self-biased Op Amp requires only power supplies of 2.5 V in the positive rail. It occupies an area of 113 μm x 474 μm.

The advantages of using a *VDCA* are: self-biasing, fully complementary, very large input common mode range. The disadvantages of using a *VDCA* are: that PMOS and NMOS transconductance matching is required and high output impedance (6 MΩ). Such matches are often required, though difficult to obtain in analog circuits. For the designed op amp, comparator transistors were mismatched; leading in this way to an output offset value of 150 mV for 0 V input offset.

Another design for high gain, high bandwidth applications was proposed by Parihar and Gupta, [13]. The design consisted of a two stage fully differential RC Miller compensated CMOS operational amplifier. It was implemented in 0.18 μm technology. Results show a DC differential gain $\succ$ 95 dB, unity gain bandwidth of $\approx$ 135 MHz, phase margin of $\approx 53^o$, and a slew rate of $\approx$ 132 V/μS for typical 1 pF differential capacitive load. Here, the improvement in unity gain bandwidth was achieved by increasing the bias current. This decreases the DC gain and increases power dissipation. The advantages of this circuit are a better balance between the gain and bandwidth. It accomplishes a higher gain and bandwidth values. Some disadvantages of this circuit are area consumption, power dissipation and the introduction of an additional pole per stage into the system. This potentially suffers

[1] the simulations were done in Berkeley Spice3f Level-2 simulation

from stability problems thus a proper compensation technique must be employed.

CHAPTER 3
HIGH GAIN, LARGE BANDWITH DESIGNS AND TECHNIQUES

3.1 Gain and bandwidth increasing techniques

This section presents several improvement techniques for gain and bandwidth used in different recent designs.

Meaamar, [14], presents one of the most commonly used methods for gain enhancement, it is called a regulated cascode or gain boosting amplifier. It improves the DC gain and output impedance by inserting an active feedback path from the output of the gain stage to set the voltage of *MA*. The negative feedback drives the gate of *MB* until V_y has the same value as V_{ref}. In this way *Vout* it is less sensitive to variations in V_y. *MA* operates as a degeneration resistor, sensing the output current and converting it into voltage (V_y). The Voltage at V_y can now be subtracted from *Vref*, placing the transistor *MB* in a current-voltage feedback loop. The drain voltage at transistor *MB* is less sensitive to V_y variations because the OpAmp's gain *(A)* regulates this voltage, in other words, it is like having a virtual ground at V_y.

With smaller variations at V_y due to changes in *Vout*, the output current remains constant, yielding a higher output impedance of *Rout* = A (g_{mB} r_{0B} r_{0A}). Note that the *Rout* obtained is the same as in the double cascoded configuration.

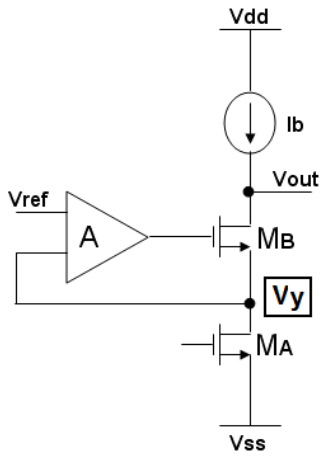

Figure 3–1: Regulated Cascoded or Gain Boosting Amplifier structure.

Another method that Meaamar uses as a gain enhancement technique is a fully double differential folded-cascode amplifier. In this case the bias current is increased by increasing the width of the transistors in the current source network and composite transistors, [14]. A single transistor connected to the source and parallel connected transistors to the drain constitute the composite transistors. This technique allows the cascoding transistors improve the gain of the OTA without deteriorating any of the bandwidth and linear output voltage range of the OTA. A composite transistor has two main advantages over its "dc equivalent" uniform width transistor:

- significant area saving
- higher cutoff frequency

The problem observed from the conventional way to obtain a low output conductance by means of a rectangular long channel transistor is that it reduces the electrical field along the whole transistor channel, giving rise to a long transit time [15]. Depending on the circuit application an OTA or an OpAmp architecture could be chosen. The difference between an OTA and an OpAmp is that an OTA can only drive capacitive loads while the OpAmp has an output buffer so that it is able to drive resistive loads also. The main difference is that the Rout of OTA's are high while the OpAmp Rout is low, the OTA is used to drive different current to the output, the OpAmp drives differential voltage.

It should also be mentioned that because of the g_m mismatch that exists in the doubled differential cascoded pairs, a good CMRR and large geometry should be provided for this topology. CMRR is the rejection range for a signal that is common two both inputs in a circuit. It should be very high in applications where the interest signal is represented through a small fluctuation in voltage that is superimposed in an offset voltage or when the information of interest is contained in the difference of the two signals. The CMRR is given by the following equation:

$$\text{CMRR} = 20 \log (\text{Ad} / |\text{As}|)$$

where: Ad= differential gain; As= common mode gain

In other words, the CMRR is the quantity of rejection of a common signal at the input reflected at its output, ideally it should be infinity.

A technique used in this design for improving the transient response was to increase the size of the CMFB transistors, [14]. This design also uses a technique for reducing the systematic offset. By increasing the width of the differential pair, the systematic errors associated with the fabrication process become less significant.

This is achieved at the cost of limiting the speed due to the increase in the inputs capacitance when increasing the transistor sizes. The size of the differential pair can be increased up to reaching the maximum current that the tail of the bias circuit can offer. Device mismatch has to be seriously considered because this also affects the common mode rejection ratio and the power supply rejection ratio.

When using a single pole model for the OpAmp, the settling time is determined by the gain-bandwidth product of the OpAmp and the feedback factor of the circuit [14]. However in most circuits there are more poles and zeros than one dominant pole. In case of using an OpAmp in a closed loop design, its frequency response has to be close to the single pole response. In other words there has to be a low frequency dominant pole while the other poles fall at much higher frequencies.

Shahrjerdi, [16], also presents other gain enhancement techniques. The first technique is a stacked structure such as telescopic or folded cascoded structure. It is appropriate for circuits that require high speed and moderate DC gain. These structures are capable of increasing the speed and output impedance to a specific power level when compared with a simple two-stage amplifier. On the other hand, it is also important to clarify that the DC gain of a stacked structure is too low for high accuracy applications.

Another technique for improving the DC gain that Shahrjerdi presents is to cascode the stacked OpAmp's in a multistage configuration. The disadvantages of this technique are higher power consumption and drastically reduced speed.

Shahrjerdi states that a better gain enhancement technique is to include an active feedback path from the output of the gain stage. This increases the output

impedance and hence the DC gain. In this structure, the DC gain and the output impedance of the main OpAmp are multiplied by a factor of about *(1+a_0)*, where a_0, is the gain of the additional feedback path. The main advantage of this structure is that if the Unity Gain Bandwidth (UGBW) of the additional OPAMP is chosen properly it has almost no degrading effect on the UGBW and thus in the speed of the main amplifier. (Same as regulated cascode or gain boosting amplifier presented above by Meaamar, [14].)

In this structure using a telescopic OTA with NMOS input transistors is a solution for fast settling OpAmp. This is, because NMOS input pair provides a higher $\frac{g_m}{I_D}$ ratio. However, the disadvantages of using NMOS pair are body effect, poor CMRR and higher input offset. In the other hand by using fully differential structures the degrading effects of clock feed-through and common mode distortions are significantly reduced. Main disadvantages of fully differential structures are that these require a common-mode feedback (CMFB) circuit. The CMFB circuit sets the common-mode output voltage to a specific level preventing the transistor to enter into triode operation.

Switched capacitor structures are typically preferred as CMFB structure because of the higher accuracy and linearity when compared with other continuous-time structures. The drawback of this structure is based on the size selection of the capacitors connected to the output pins. These capacitors should be large enough compared to the total parasitic capacitance of the output nodes for obtaining a reasonable common-mode gain. At the same time, these capacitors add load at the output reducing the operation speed of the OpAmp. Based on the previous explanations, an intermediate value should be chosen for the capacitor.

Mohammad, [17], design was based on a standard folded cascoded structure with around 50dB of gain and with two gain boosting stages where these should provide the other 50dB of gain for a total of 100dB gain.

This work also presents the advantages of using the gain boosting method for gain enhancement. The advantages are; the extra stage does not change the original gain frequency; the use of this structure provides simpler biasing by using low voltage cascode current mirrors. Increasing the output resistance generates and increase in DC gain. The impedance of transistors that are not in the signal path can be increased by increasing the channel length. Mohammad also used a technique to increase the voltage swing. It consisted of using the NMOS load folded cascode amplifier to boost the PMOS branch of the main folded cascode amplifier and the PMOS load folded cascoded amplifier to boost the NMOS branch of the main folded cascoded amplifier.

In this design a CMFB circuit was added because of the advantage of these structures of being less sensitive to device properties and mismatches, thus having a more stable output. The proposed CMFB circuit proposed is capable of sensing the output Common Mode level, comparing it with a preset reference and return the error to the amplifier's bias network. The main concern of this design is to assure that any pole or zero added is far away from the dominant pole to avoid stability problems. In other words, the CMFB allows the OpAmp to have a common mode output voltage that is less sensitive to process and temperature variations.

For fully differential folded cascoded OpAmp circuits the dominant pole is typically located at the output node which has the highest impedance in most cases. The unity gain frequency in Mohammad, [17], is determined by w_u=-g_m/C_L, where

in this case the sizes of the input transistors: are designed in order to satisfy the unity gain frequency specification. Where C_L is mainly the gate to source capacitor of the output transistor.

Aziz in his paper, [18], presents more preferred uses of OTAs. OTAs are preferred in driving fully capacitive loads such as switched-capacitor circuits. This is because they are very efficient in terms of speed and power especially for the case of a telescopic configuration. Achieving high gain with single stage OTAs is becoming increasingly more difficult due to the shorter channel lengths of new technologies.

Techniques that alleviate this problem are the following:

When using a 3V or more power supply: A solution could be using the cascoded current mirrors. The drawback of this solution is the lost of voltage swing.

When power supply is smaller than 3V and higher than 2V: Single stage OTAs are not very good alternative because of the difficulties in realizing high output-impedance active load without reducing the output voltage swing significantly. In this case the introduction of wide-swing current mirrors help mitigates this problem compared to traditional cascoded circuits for power supply voltages higher than 2V.

When lowering the power supply ever further: The afore mentioned technique is not longer appropriate. At this point, fully differential OpAmps are a better option for low-voltage applications, since these do not need cascoded output stages. In the other hand, a downside of this design compared to single-stage structures is the extra capacitors needed for frequency compensation causing a bandwidth reduction. In this case, additional power will also be needed to reclaim the lost bandwidth.

In case of using a fully-differential current-mirror OpAmp, as the current gain is increased the total capacitance at the gate of the load transistors increases,[18], causing a pole close to the associated second poles in lower frequencies, thus affecting circuit's stability. Another aspect discussed by Aziz, [18], is the OpAmps primary source of noise. The 1/f noise is the main source of noise in OpAmps. Since noise associated with temperature is proportionally to g_m, lowering the noise can be achieved by increasing the width of differential pair of the load transistors [**?**]. The load increase can be achieved by rising the channel length, L, of the load transistors. This advantage comes at the expense of increasing the parasitic capacitance at the gate of the load transistors making the design very difficult to create without consuming too much power and area.

A 2-stage Differential OpAmp, has the potential to achieve a high gain and output swing. The main issue with this structure is that it requires compensation and this process moves the dominant pole to a lower frequency making the OpAmp more stable but slower. In the design proposed by Aziz, [18], for moderate speed and power, the 2-stage topology resulted more suitable than the current mirror operational amplifier. In this case the transconductance of the differential pair and the compensation determines the unity gain frequency. There are two alternatives to increase the unity gain frequency: increase in the transconductance of the differential pair transistors (by larger bias current or larger W/L) or reduce the capacitance of the compensation capacitor.

There is a need of using a CMFB to control the common-mode voltage at differential nodes that cannot be stabilized by the negative differential feedback. Capable of suppressing common-mode component, that tends to saturate the differential stage. In Aziz's design, [18] the input stage of the amplifier was designed using

p-channel devices because this has the benefits of lower 1/f noise and high slew rate.

Two mayor limitations are addressed by Kundu, [19], regarding single stage regulated cascode structures:

- Due to short channel effect and due to the high current density in modern transistors, DC gain requirements are not accomplished.
- UGB is limited by the parasitic poles for multi-stage implementations and settling response depends on relative pole positions.

Using two stage implementations helps to get higher DC gain, UGB, linearity and faster settling response. Two stage implementations also help to overcome output swing limitation in low voltage applications.

The work presented in this paper, [19], consists of three amplifiers:

- Telescopic cascode input stage.
- Folded cascoded gain boosting amplifier: offers compensation (DC gain) for the reduction in output resistance.
- Class A-B output stage: more DC gain and rail to rail output swing.

This paper presents a hybrid optimization algorithm called Differential Evolution (DE). The importance to optimize is based on the interest to find out the global optimum solution in a circuit performance in terms of different parameters such as DC gain, UGB, settling time and current consumption. The DE idea is to add the weighted difference vector between two population members to a third member of the population. An important part in the optimization process is the

cost or objective function. In this application the circuit parameters such as: transistors widths, resistor values, among others are chosen as the optimization variables.

The settling time is given by the ratio among the two dominant poles as well as the nulling zero and the pole zero doublet arising from the gain boosting stage. Real OpAmps generally have a pole-zero doublet in addition to two significant poles. Doublets arise from mismatches in pole-zero compensation due to process tolerances or because of frequency limitation of current mirrors when used for a differential to single conversion from the feed-forward capacitor in a voltage follower. A pole-zero doublet does not affect significantly the frequency response in a closed-loop amplifier but it can greatly affect the time response, [20].

Because of the two stage implementation two dominant poles are added to the systems transfer function. Miller compensation technique was employed in this design to separate these two poles to assure close loop stability. The first dominant pole appears at the output of the input stage and the second dominant pole at the output of the overall OpAmp.

In his work, Palmisano, [20], presents the other advantage of having negative feedback. It helps to reduce the Total Harmonic Distortion (THD). Where the THD is a measure of the quality of the design of the output stage. This term is the rms of the value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms of the fundamental.

In this paper Palmisano specifies what are the design cycles that he uses when designing:

1. Based on bias voltages calculations, make the proper selection of circuit topology.
2. Based on first order circuit analysis and calculations, identify design variables and determine their range of variation.
3. Through the optimization process, find the best appropriate results for DC gain, UGB, current consumption. Explore if the design is realistic within the available design space and limits.

Wang in his work, [21], presents the Telescopic Amplifier advantages and disadvantages. The advantages are: typically consumes less power and has higher frequency capability compared to other topologies. This is because it is a single stage amplifier that exhibits one dominant pole. It's speed is higher than most other types of amplifiers. The disadvantages are: output swing limited due to cascoded transistors.

A gain boosting technique was required for improving the gain in this design. The gain boosting technique used in this case was a cascoded gain stage with gain enhancement (the same discussed and presented in the design by [14]).

In case of high gain desired the two-stage configuration designs are typical. Although it is important to note that telescopic configuration gives both high gain and high bandwidth without the need of any compensation. Using these concepts, a fully differential telescopic cascode op-amp that has two fully differential folded cascoded boosting amplifiers was designed. The input differential pair in this design was implemented with NMOS to achieve higher gain and speed. Other advantages

of fully differential OpAmp are greater output swing, avoid mirror poles, eliminating even-order distortion and reject noise from the substrate. The drawback of this topology is the need to add a common-mode feedback (CMFB) circuit.

3.2 Specifications Table Comparing the Five Papers

The table below presents a comparison among different OpAmp designs. The aspects of most importance were Gain and BW.

Author	Title	Technology	Gain	Vdd	BW
[Meaamar 06]	A 0.18um, 1.8 V CMOS High Gain Fully Differential Opamp Uitilized in Pipelined ADC	0.18um CMOS	>95dB	1.8 V	3.28 MHz
[Shahrjerdi 03]	A Fast Settling, High DC Gain, Low Power OPAMP Design for High Resolution, High Speed A/D Converters	0.35um CMOS	96dB	3 V	1 KHz
[Mohammad 07]	Very High-Gain and Fast-Settling Opamp for Switched-Capacitor Applications	0.35um CMOS	100dB	3.3 V	4 MHz
[Aziz 04]	A 1.8-V Fully Differential 2-Stage OPAMP Switched-Capacitor Delta-Sigma Modulator for Bluetooth Application	0.18um CMOS	76.6 dB	1.8 V	3.71 MHz
[Kundu 08]	A Fast settling 100dB OPAMP in 180nm CMOS process with compensation based optimization.	0.18um CMOS	100 dB	1.8 V	8.07 MHz
[Wang 04]	Analysis and Design of Fully Differential Gain-Boosted Telescopic Cascode Opamp	0.35um CMOS	129 dB	3.3 V	1.25 MHz

Table 3–1: Comparison among different High Gain and High BW OpAmp Designs

The Vdd used is not a true comparison due to the differences between the threshold voltages on smaller technologies. This is because the most transistors involved in a design, the most Vdd required.

CHAPTER 4
OBJECTIVES AND METHOD OF ANALYSIS

4.1 Objectives

4.1.1 General Objective

Although several circuits exist to measure current and different schemes have been proposed for measuring iDD, most of them can be classified in two parts. First, there are sensors introduced between Vdd and the CUT, and the ones that are introduced in parallel but only sample a part of the current, see figure 4–1. The implementation of sensors to test currents in an integrated circuit, introduces switches parasitic capacitance and resistances that often limit the capability of the mission circuit and sensor.

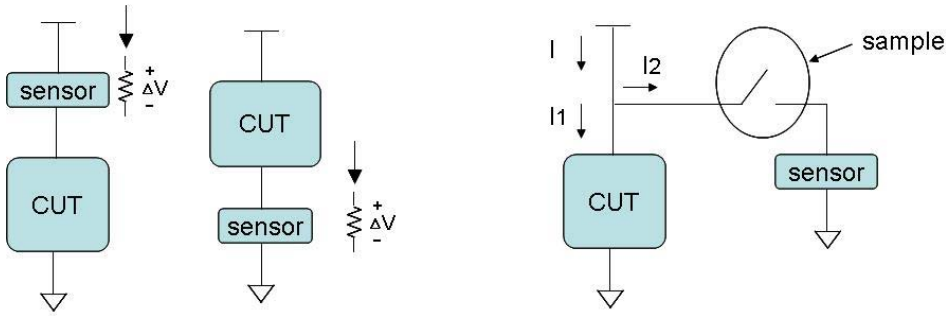

Figure 4–1: Current iDD test schemes

The proposed circuit uses already available integrated structures for measuring current waveforms without introducing a device in series with the CUT. Some of the challenges involved in the design of such sensor are: high gain, large bandwidth, low power, low noise and high slew rate. Placement of the proposed sensor is shown in figure 4–2.

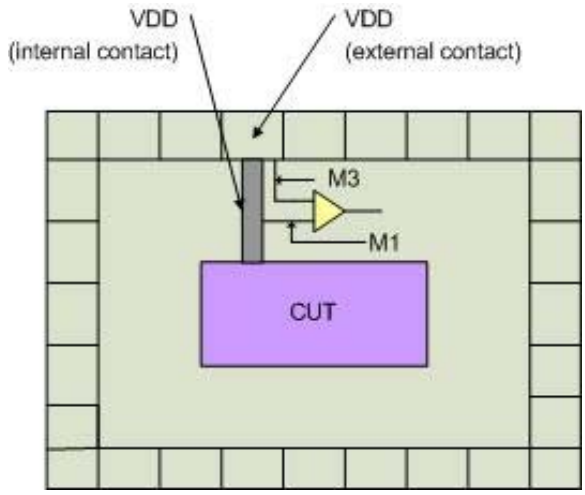

Figure 4–2: Proposed solution sensor placement

4.1.2 Specific Objectives

Obtain a sensor that is that can potentially be used for sensing, quiescent and dynamic currents from the positive or negative power supplies and for analog, digital and mixed signal circuits.

4.2 Method of Analysis

4.2.1 Design Needs

Primary needs

High Gain. Because the target input difference is generally very small (uV).

Large Bandwidth (BW). The signal to be detected is any circuit under test (CUT) might have very fast transition responses, therefore the need of a large BW response sensor.

Capable of sensing continuous input signals. The transient response will have a characteristic form, depending on the CUT on - off transitions and the sensor has to be capable of reproducing this shape.

Secondary needs

Low input swing. The signal to be captured varies within (uV to mV from Vdd) not requiring a large swing input to sense it. This is not an issue as long as Vdd is within the operational input voltage range.

Low noise. A low noise design provides a more accurate replica, being able of have a more exact representation at the output of the input signal.

4.2.2 Circuit General Approach

The proposed circuit (figure 4–3) will be capable of sensing the voltage difference that exists among the layers between the Vdd supply and the CUT.

Solution proposed:

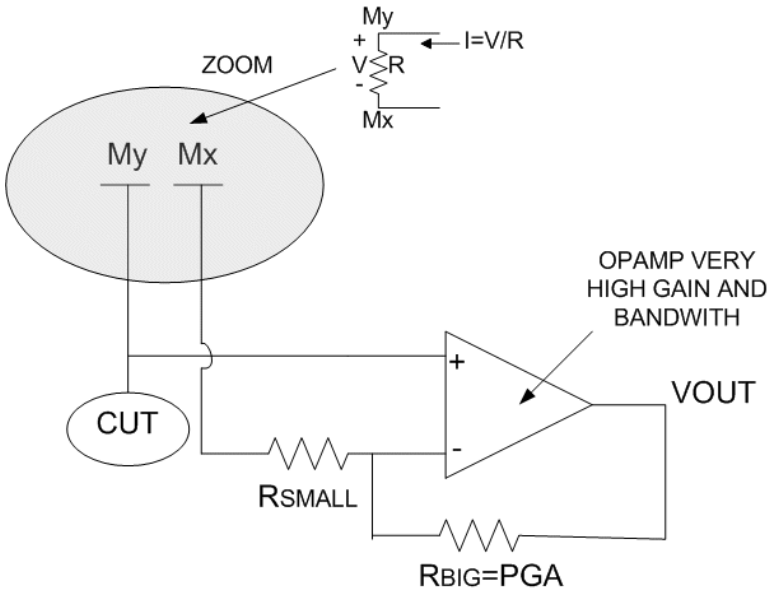

Figure 4–3: Proposed buit-in iDD and IDDQ test scheme.

The proposed circuit is composed of a high gain and high bandwidth differential amplifier. Where R is the resistance seen from My to Mx where My and Mx represent the several metal layers that are contained in the ring pad from the Vdd supply to the CUT. Where some of these layers are connected to the power supply (the superior layers, in figure 4–3 is represented by My) and the rest are connected to a base of metal connections through vias (in figure 4–3 this point is represented by Mx). For more details see figure 4–4.

Due to the small voltage drop in the resistance value (R) that exists between two metal layers, Mx and My in the figure 4–3, the Op Amp will need to have a high

gain, and a large bandwidth to detect small signals at different frequency ranges. This circuit does not require a large input voltage range due to the small voltage drop to be sensed by the terminals.

Figure:4–4 shows a more detailed view of the desired parameter to be sensed. The diagram shows the contact between the metal layers that causes a minute drop from the Vdd supply to the DUT.

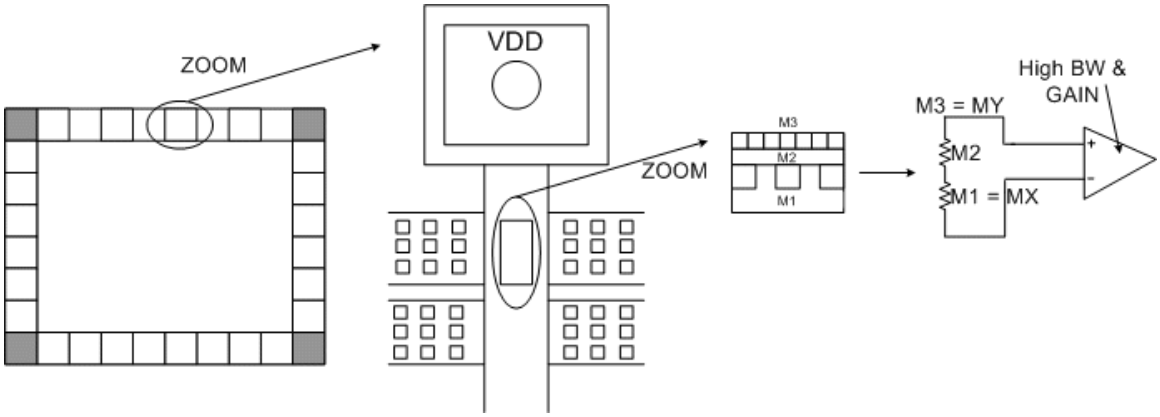

Figure 4–4: View of the Vdd ring voltage drop area from My to Mx (M3 - M1).

Where M1, M2 and M3 in figure 4–4 represent three metal layers.

A constraint for the implementation of this test scheme is that the Vdd connection to the CUT must be made with M1 and so the connection of the sensor with the outer top metal layer. The design of this circuit will be develop with a technology of 600n in Cadence.

4.2.3 Design Ideas

After reviewing several structures, the initial design ideas of a differential input/output OpAmps were:

- Design the main stage with a folded cascoded structure to take care of large BW and then control the gain with a cascoded gain boosting structure.
- Design the main stage using a double stage structure to take care of large gain followed by a cascoded output to improve the bandwidth.

4.2.4 Design Steps

In order to design the proposed solution, previous circuits were carefully studied. These were analyzed and compared according to their respective advantages / disadvantages such as; noise immunity, power consumption, gain, bandwidth and area, among others. Different current mirrors and differential amplifiers were tested, see Appendix B. The Vdd ring structure is another parameter that was also analyzed and characterized in this design.

The design was tested via simulation until an optimal solution was achieved. Analysis such as: DC sweep for obtaining the DC bias or operating point, AC for gain and stability, linearity and transient analysis to study the current waveform verified the circuit's behavior. Aspects as observability and controllability were also taken into account in order to have a good design for test (DFT [22]).

During the layout generation techniques to minimize fabrication mismatch were implemented such as Common Centroid and Interdigitation, [23].

CHAPTER 5
CUT PAD AND VDD RING

5.1 Pad Equivalent Resistance

For calculating the pad equivalent resistance small signal characterization of the pad was needed. In figure 5–1 a view of the pad under characterization is shown.

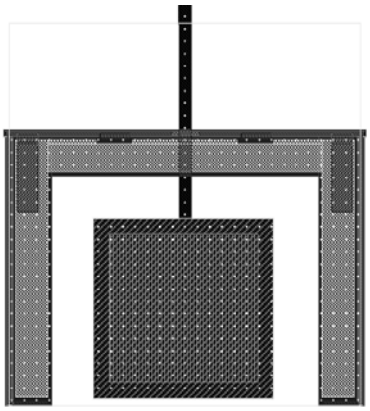

Figure 5–1: Pad Under Characterization

The first step for the characterization was to look into the Mosis website for recent test results using the same technology to get the metal sheet resistances and contact resistances present in the pads.

Tables 5–1, 5–2, 5–3, and 5–4 show random data collected from the Mosis website from different fabrication processes. The tables show different metals sheets resistances (M1, M2, M3 with Ω / sq units) and contact resistances M2 contact (via 1) and M3 contact (via 2) with Ω units. Note that 5–1 shows the data used in this

pad characterization.

Figure 5–1 show test data results for SPICE Model Parameters on Semi C5 (0.50 micron). The data used in this design during pad characterization.

Test Data - On Semi C5 (0.50 micron)					
RUN	M1 (Ω/□)	M2 (Ω/□)	M3 (Ω/□)	M2 contact (Ω)	M3 contact (Ω)
T5AV (#2_C5N)	0.09	0.09	0.05	0.86	0.78
T8CG	0.09	0.09	0.05	0.86	0.80
T8BY	0.09	0.09	0.05	0.94	0.89
T89Y	0.09	0.09	0.05	0.90	0.83
T85R	0.09	0.09	0.05	0.88	0.85
T85Z	0.09	0.09	0.05	0.84	0.82
T84F (C5T)	0.09	0.09	0.05	0.88	0.79
T84F (C5N)	0.09	0.09	0.05	0.91	0.79
T82Q	0.09	0.09	0.05	0.90	0.86
T7AC	0.09	0.09	0.05	0.91	0.84
T81A	0.09	0.09	0.05	0.89	0.81
T77X	0.09	0.09	0.05	0.92	0.82
T7CU	0.09	0.09	0.05	0.88	0.84
T78M	0.09	0.09	0.05	0.84	0.74
T73G	0.09	0.09	0.05	0.94	0.91
T72U	0.09	0.09	0.05	0.87	0.86
T6AU	0.09	0.10	0.05	0.97	0.79
T66H	0.09	0.09	0.05	0.89	0.84
T62R	0.09	0.09	0.05	0.92	0.96
T5BK	0.09	0.09	0.05	0.91	0.86
Average	0.09	0.09	0.05	0.90	0.83
Stand Deviation	2.8E-17	0.00224	7.1E-18	0.033635038	0.049672612

Table 5–1: Wafer Electrical Test Data and SPICE Model Parameters on Semi C5 (0.50 micron)

Figure 5–2 show test data results for SPICE Model Parameters IBM 5HP, 5AM, 5DM, 5PA (0.50 micron)

Test Data - IBM 5HP, 5AM, 5DM, 5PA (0.50 micron)					
RUN	M1 (Ω/□)	M2 (Ω/□)	M3 (Ω/□)	M2 contact (Ω)	M3 contact (Ω)
T8BX (5AM_NI)	0.08	0.05	0.04	0.30	0.63
T86D (5AM_NI)	0.08	0.05	0.04	0.31	0.69
T82G (5AM_NI_CM)	0.08	0.05	0.05	0.31	0.68
T82G (5AM_NI)	0.08	0.05	0.05	0.31	0.67
T79U (5AM_NI_CM)	0.09	0.05	0.05	0.31	0.66
T79U (5AM_NI)	0.09	0.05	0.05	0.31	0.66
T75V (5AM_NI_2)	0.08	0.05	0.04	0.33	0.67
T71G (5AM_NI)	0.08	0.05	0.05	0.33	0.67
T6BH (5DM)	0.08	0.05	0.04	0.34	0.61
T67P (5HP)	0.08	0.05	0.05	0.30	0.62
T69D (5HP)	0.08	0.05	0.02	0.33	0.70
T65P (5HP)	0.07	0.05	0.01	0.35	0.75
T65P (5AM_NI)	0.08	0.05	0.05	0.39	0.73
T4AB (5AM_NI_3)	0.08	0.05	0.05	0.33	0.72
T5CS (5AM_NI)	0.08	0.05	0.05	0.32	0.68
T57W (5AM_NI_2)	0.08	0.05	0.04	0.37	0.72
T54F (5AM_NI)	0.08	0.05	0.05	0.39	0.78
T54F (5HP)	0.08	0.05	0.02	0.36	0.75
T51F (5HP)	0.08	0.05	0.02	0.38	0.74
T46D (5AM_NI_F)	0.08	0.05	0.04	0.35	0.65
Average	0.0805	0.05	0.0405	0.336	0.689
Stand Deviation	0.00394	7.1E-18	0.01276	0.029271865	0.046441814

Table 5–2: Wafer Electrical Test Data and SPICE Model Parameters IBM 5HP, 5AM, 5DM, 5PA (0.50 micron)

Figure 5–3 show test data results for SPICE Model Parameters IBM 7RF, 7WL, 7SF, 7HP (0.18 micron)

Test Data - IBM 7RF, 7WL, 7SF, 7HP (0.18 micron)					
RUN	M1 (Ω/▭)	M2 (Ω/▭)	M3 (Ω/▭)	M2 contact (Ω)	M3 contact (Ω)
T8CJ (7RF_4LM_AM)	0.06	0.09	0.09	2.52	5.03
T8BU (7WL_7LM_MA)	0.07	0.09	0.09	2.13	3.94
T81D (#1_7HP_6LM_AM_C4)	0.06	0.06	0.06	0.59	1.14
T89S (7WL_7LM_MA)	0.07	0.09	0.09	2.40	4.54
T86L (7RF_6LM_MA_5V)	0.06	0.09	0.09	2.43	4.46
T87Z (7WL_7LM_MA)	0.07	0.09	0.09	2.26	4.13
T6BB (#1_7WL_7LM_MA)	0.06	0.09	0.09	2.10	4.05
T71P (7HP_5LM_AM_4)	0.06	0.06	0.07	0.72	1.33
T82M (7RF_6LM_ML_QT	0.08	0.10	0.10	2.27	4.16
T48T (7WL_4LM_AM_2)	0.07	0.09	0.09	2.18	4.15
T85S (7WL_5LM_MA)	0.07	0.09	0.09	2.29	4.46
T84E (7RF_6LM_MA	0.08	0.09	0.09	2.08	4.49
T83S (7WL_7LM_MA)	0.06	0.09	0.09	2.14	3.99
T81Z (7WL_7LM_MA)	0.07	0.10	0.09	2.17	3.99
T7CA (7RF_6LM_ML)	0.07	0.10	0.10	2.50	4.54
T7CW (7RF_6LM_ML)	0.07	0.09	0.09	2.10	4.03
T7BM (7WL_7LM_MA)	0.08	0.09	0.09	2.18	4.01
T7AD (7RF_6LM_ML)	0.07	0.09	0.10	2.49	4.74
T6BZ (7HP_5LM_AM	0.07	0.06	0.06	0.71	1.40
T77V (7HP_7LM)	0.07	0.05	0.05	0.76	1.53
Average	0.0685	0.085	0.0855	1.951	3.7055
Stand Deviation	0.00671	0.01469	0.01395	0.659616316	1.243130492

Table 5–3: Wafer Electrical Test Data and SPICE Model Parameters IBM 7RF, 7WL, 7SF, 7HP (0.18 micron)

Figure 5–4 show test data results for SPICE Model Parameters TSMC CL018/CR018/CM018 (0.18 micron)

Test Data - TSMC CL018/CR018/CM018 (0.18 µm)					
RUN	M1 (Ω/▭)	M2 (Ω/▭)	M3 (Ω/▭)	M2 contact (Ω)	M3 contact (Ω)
T92Y (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.83	9.74
T77A (MM_NON-EPI_THK-MTL_HR8)	0.08	0.08	0.08	4.57	9.58
T73D (MM_NON-EPI)	0.08	0.08	0.08	4.40	8.58
T6CA (MM_NON-EPI_THK-MTL_HR8)	0.08	0.08	0.08	4.69	10.47
T68B (MM_NON-EPI)	0.08	0.08	0.08	4.79	9.24
T66D (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.19	8.71
T64H (MM_NON-EPI_THK-M)	0.08	0.08	0.08	4.61	9.11
T58F (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.08	8.43
T57Q (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	6.91	13.63
T55U (MM_NON-EPI)	0.08	0.08	0.08	5.26	10.95
T53R (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.88	9.87
T4BK (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.18	8.97
T49P (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.63	9.09
T47R (MM_NON-EPI_THK-MTL	0.08	0.08	0.08	5.27	9.70
T46U (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.35	8.81
T44E (MM_NON-EPI)	0.08	0.07	0.07	4.29	8.58
T42P (MM_NON-EPI_THK-MTL)	0.08	0.08	0.07	4.25	8.74
T3CV (MM_NON-EPI)	0.08	0.08	0.08	4.20	9.08
T3AZ (MM_NON-EPI_THK-MTL)	0.08	0.08	0.08	4.37	9.20
T38N (MM_NON-EPI)	0.08	0.08	0.08	5.01	9.40
Average	0.08	0.0795	0.079	4.688	9.494
Stand Deviation	1.42E-17	0.00224	0.00308	0.630793986	1.165311795

Table 5–4: Wafer Electrical Test Data and SPICE Model Parameters TSMC CL018/CR018/CM018 (0.18 micron)

From these data results it can be observed that the smaller the fabrication technology the bigger the contact resistance. The standard deviation increases as the fabrication technology decreases. This indicates that the padframe contacts resistances are less controllable thus inducing different leakage currents associated with it. Having a BIST sensor capable of detecting this specific drop helps in the characterization of the leakage current directly associated with this factor. These factors make very necessary the implementation of a monitoring sensor. A sensor that is capable of without adding any signal disturbance or device between the Vdd and CUT can detect and magnify the voltage drop associated with the pad frame connections.

Summary of the values obtained from Mosis and used in the characterization:

Via 1: M2-M1: 0.90 Ω

Via 2: M3-M2: 0.83 Ω

Metal 1: 0.09 Ω/sq

Metal 2: 0.09 Ω/sq

Metal 3: 0.05 Ω/sq

The formula to calculate the sheet resistance is given by:

R= # sq (resistance/sq)

Figure 5–2 shows a zoom of the vias array in the pad.

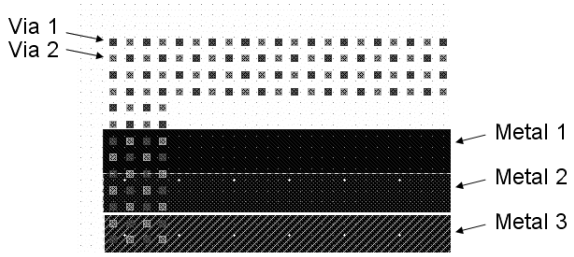

Figure 5–2: Zoom of the Via Contacts in the Pad and Other Metal Layers Used.

The small signal circuit for the vias part in the pad circuit is shown below in figure 5–3:

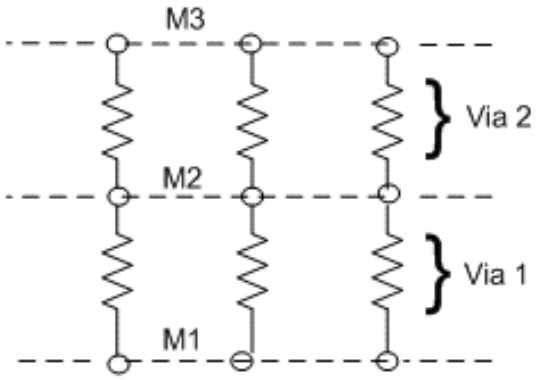

Figure 5–3: Small Signal Equivalent Circuit for the Vias

In terms of the complete characterization process a pad to pad connection was utilized, see figure 5–4:

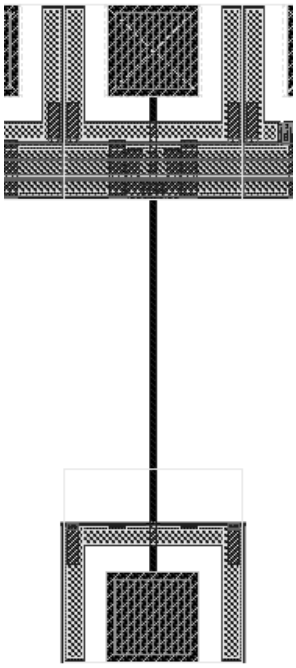

Figure 5–4: Pad to Pad Connection Used for the Pad Characterization

The equivalent circuit for this pad to pad connection is presented in figure,5–5:

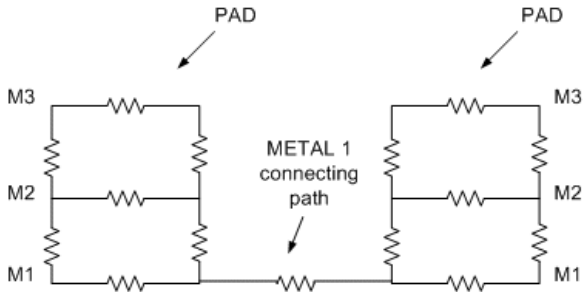

Figure 5–5: Small Signal Equivalent Circuit for the Pad Characterization

Computing the pad equivalent resistance

In each pad there are 2 sets of 176 Via 1 and 176 Via 2 parallel connected vias. These are separated by the resistance of the metal layers used to contact. Once these resulting via 1 and via 2 parallel equivalent resistances were computed separately these were added in series for each set, see calculations below:

Via 1: $1/\text{Re} = 176/0.9$ ... $\text{Re} = 0.005114\ \Omega$

Via 2: $1/\text{Re} = 176/0.83$ ... $\text{Re} = 0.004716\ \Omega$

Via 1 + Via 2: $0.005114\ \Omega + 0.004716\ \Omega = 0.009830\ \Omega = 9.83\text{m}\Omega$

The total equivalent resistance obtained by each single pad was: $4.915\text{m}\Omega$.

The metal layers resistance were obtained as shown below:

Metal 1= 1sq (0.09 Ω/sq) = 0.09 Ω

Metal 2= 1sq (0.09 Ω/sq) = 0.09 Ω

Metal 3= 1sq (0.05 Ω/sq) = 0.05 Ω

Note that the interconnection of the pads was done by using Metal 1. In this case Metal 1 has the largest resistance. This is because the metal path that interconnects the two pads is very thin and long. The total number of squares (sq) encountered in this path is 18. The resistance was calculated according to the following formula:

Metal 1= 18sq (0.09 Ω/sq) = 1.62 Ω

Note that when comparing this small trace with the large contact layer it has more resistance because it contains more squares within it versus having a larger area but making only one square. Adding these equivalent impedances to the Metal

1 path resistance yields an equivalent pad to pad resistance of 1.854915 Ω.

5.2 VDD Ring Equivalent Resistance:

For calculating the Vdd Ring equivalent resistance, a similar procedure was followed. In this case the first step was to determine which metal layers were part of the Vdd ring. Mosis website was used to determined recent test data results using the same technology. With these values then proceeded calculate the equivalent resistance of the internal Vdd ring. The ring is composed of many parallel and series resistances interconnected. After the calculations were done it was found that the equivalent resistance of the internal Vdd ring was: 0.006278Ω. This value does not include the metal layers needed to connect this ring with the corresponding external pad. The impedance associated with this connection was: 0.21967 Ω. In summary the total equivalent resistance that exists from the external Vdd pad to the internal Vdd ring is about: 0.225948 Ω. = 225.948 mΩ

Figure 5–6 presents the Vdd ring characterized above. As seeing in the figure the Vdd ring includes and internal ring and the external pad.

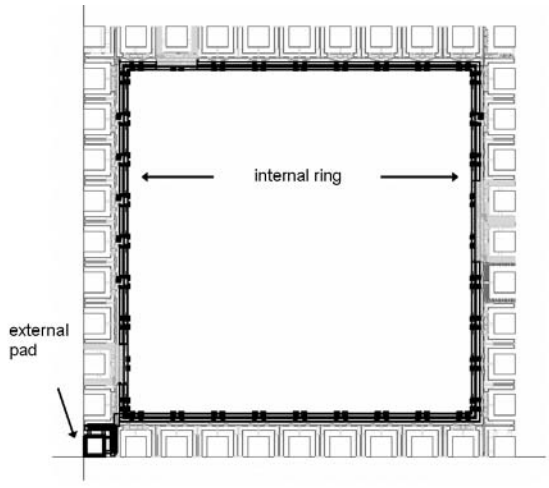

Figure 5–6: Characterized Vdd ring from the external pad to the internal ring.

Figure 5–7 presents a zoom of the characterized Vdd external pad area.

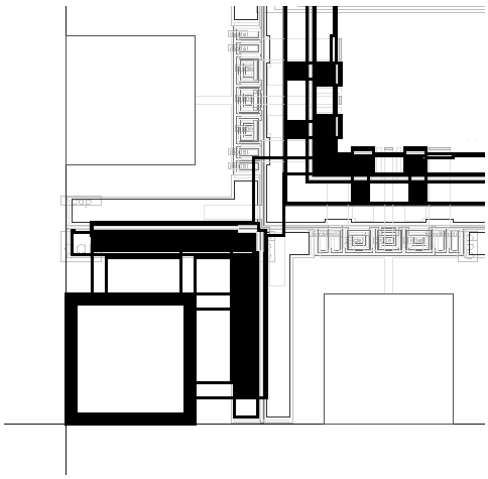

Figure 5–7: Vdd external pad.

CHAPTER 6
CIRCUIT DESIGN

6.1 Differential Amplifier Circuit Design and Simulation Responses

Different structures were implemented in order to be used as the desired sensor. Appendix B shows the schematics, DC and AC simulation results for some of these designs, see figures: B–10 to B–18. These were not taken as good solutions to the desired application because, despite of the good gain and stability of these structures, none of these could operate close to Vdd.

The first OpAmps considered were the Telescopic OpAmp and the Folded Cascoded OpAmps, these resulted to be very attractive solutions because of their high gain and large BW properties. The main constraints imposed by these structures bring are their limitation to operate near the Vdd region. Their input voltage is limited by the V_{DS} voltage drop produced by the transistors used as load.

Due to this limitation OpAmp structures with less voltage load V_{DS} drop were studied. Two designs providing an AC gain of more that 60 dB were designed and tested. These structures are the **differential amplifier with two gain stages** and the **differential amplifier with three gain stages**.

6.1.1 Differential Amplifiers with two gain stages

The schematic for the differential amplifier with two gain stages is shown in figure 6–1. In this design Vdd = 3 V, I_{bias} = 35 $_{\mu}$A, l=1.2 $_{\mu}$m and the transistor sizes are given below:

- M1: w = 80 $_{\mu}$m
- M2: w = 80 $_{\mu}$m
- M3: w = 25 $_{\mu}$m
- M4: w = 25 $_{\mu}$m
- M5: w = 75 $_{\mu}$m
- M6: w = 5 $_{\mu}$m
- M7: w = 15 $_{\mu}$m
- M8: w = 25 $_{\mu}$m

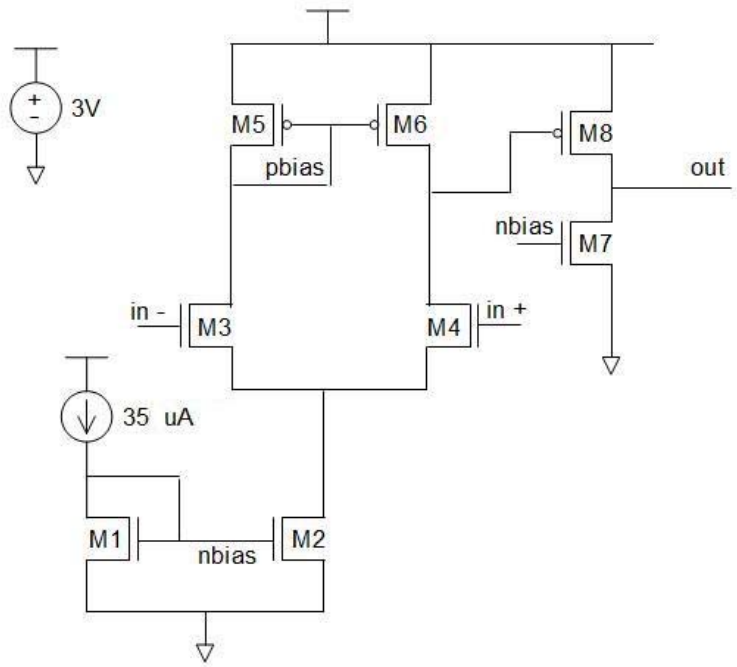

Figure 6–1: Differential amplifier with two gain stages schematic

Results for the differential amplifier with two gain stages are shown below. Simulations such as AC analysis, transient response and DC sweep are shown. The AC result when the DC input signal is the same for both inputs is shown in figure 6–2. In this case, both inputs where 3V (Vdd) each. The gain obtained with this set-up was 60.25 dB and a 3dB frequency of 135 Mhz.

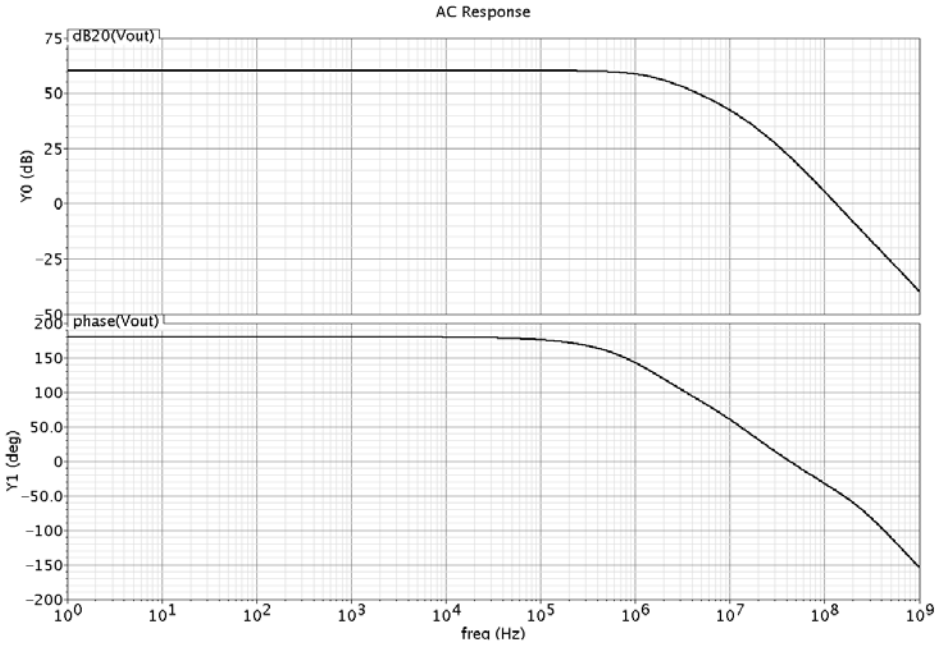

Figure 6–2: Differential amplifier with two gain stages AC Response with same DC voltage at both inputs

The AC result was also simulated when DC the input signal in both inputs had a difference of 1 mV. The result is shown in figure 6–9. In this case the non-inverting input was 3 V (Vdd) and the other was 2.999 V. The gain obtained with this new set-up was 57.32 dB and a 3dB frequency of 132 MHz.

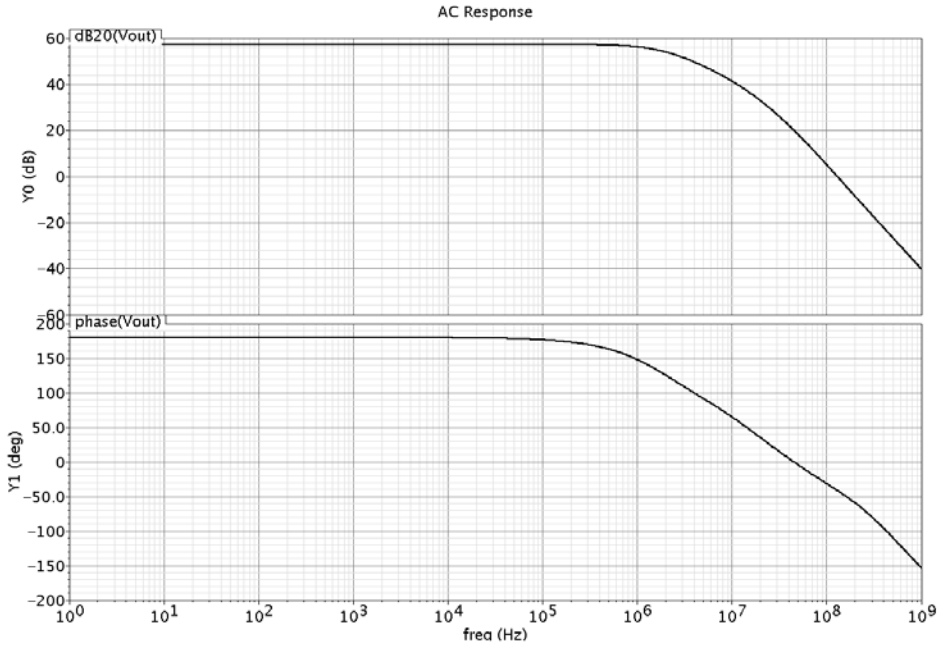

Figure 6–3: Differential amplifier with two gain stages AC Response with 1 mV difference at both inputs

In case of a close loop system desired, the needed compensation scheme between the first and the second stage is an RC combination of:

In this case $f = 10^4 \Rightarrow 2\pi f = \omega = 62{,}831.9 = 1/\tau \Rightarrow \tau = 1.59155\times10^{-5} = RC$

Assuming C = 30pF, R = 530516 Ω

Transient response of the circuit is shown in figure 6–4.

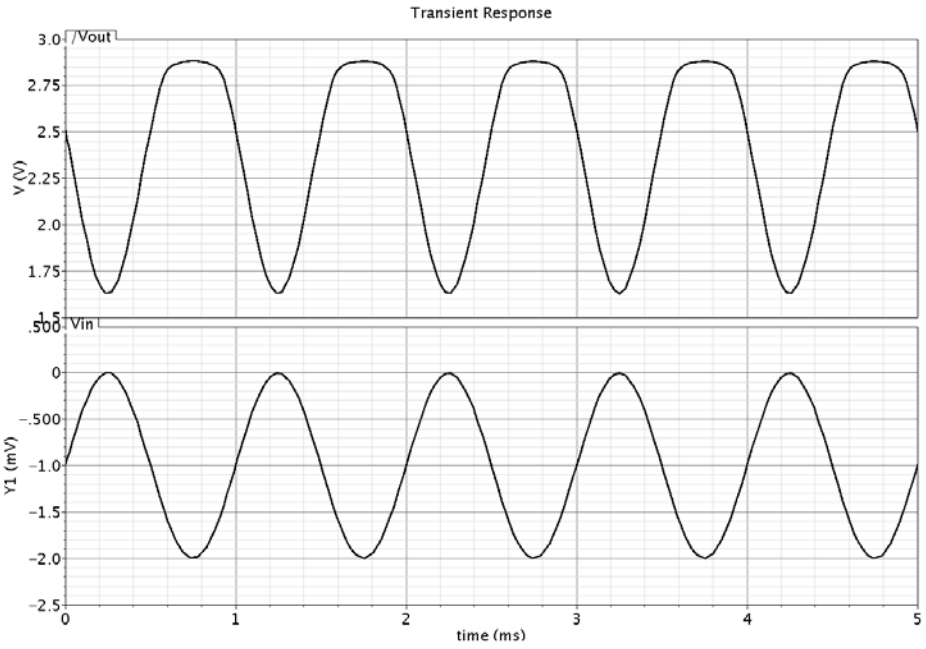

Figure 6–4: Differential amplifier with two gain stages Transient Response with 1 mV difference at both inputs

This transient response shows the result of 1 mV input difference. The input signal shown is negative because it was calculated as the difference between the lower input voltage (2.999 V) minus the higher input voltage (3 V). This condition saturated the output thus a way to avoid saturation is to decrease the gain by adding feedback.

The DC Sweep response with 1 mV difference at both inputs is shown in figure 6–5.

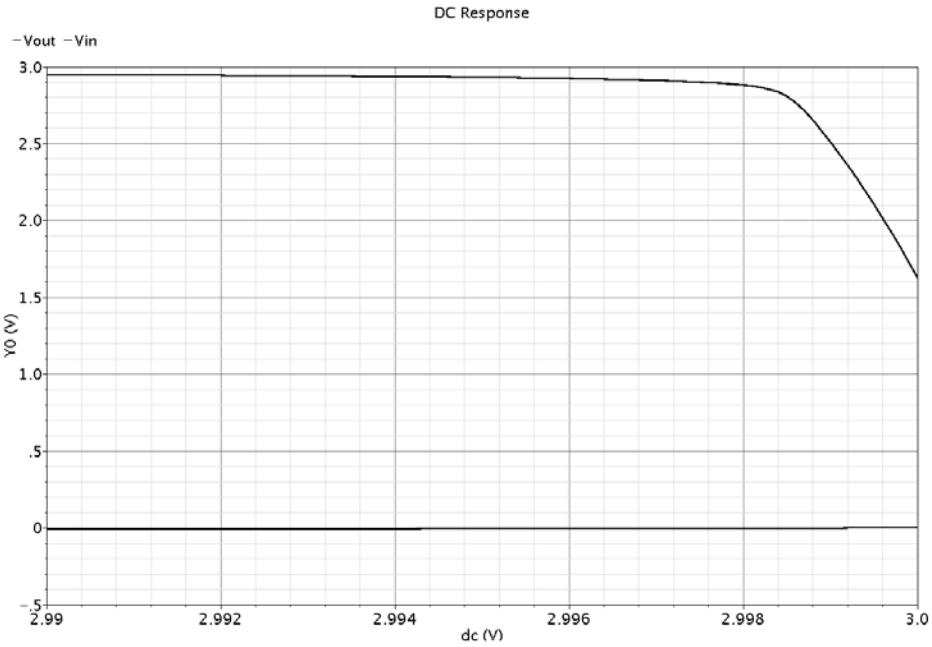

Figure 6–5: Differential amplifier with two gain stages DC Sweep Response with 1 mV difference at both inputs

Figure 6–6 shows a zoom of DC response close to Vdd. The resulting slope from this DC sweep analysis was 626.45 V/V. Vin range varies from 2.998 V to 3 V and Vout from 1.629 V to 2.8819 V.

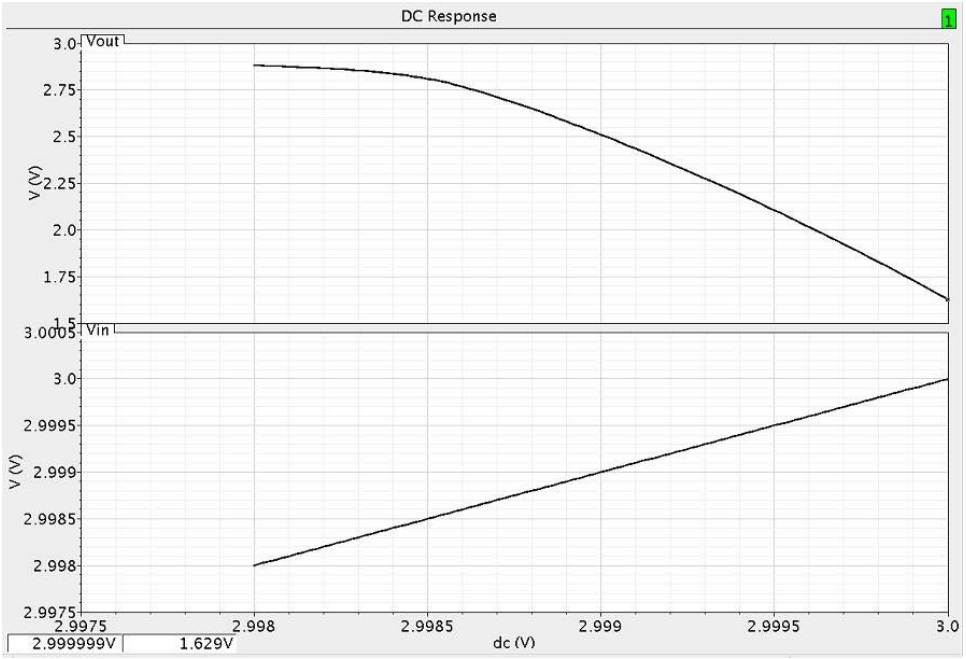

Figure 6–6: Zoom of the DC Sweep Response close to Vdd

6.1.2 Differential amplifier with three gain stages

The Schematic for the differential amplifier with three gain stages is shown in figure 6–7. In this design Vdd = 3 V, I bias = 50 uA, l=1.2 um, C_L=20 pF and the transistor sizes are given below:

- M1: w = 22.65 $_\mu$m
- M2: w = 22.65 $_\mu$m
- M3: w = 10 $_\mu$m
- M4: w = 10 $_\mu$m
- M5: w = 34 $_\mu$m
- M6: w = 34 $_\mu$m
- M7: w = 50 $_\mu$m
- M8: w = 150 $_\mu$m
- M9: w = 5 $_\mu$m
- M10: w = 150 $_\mu$m

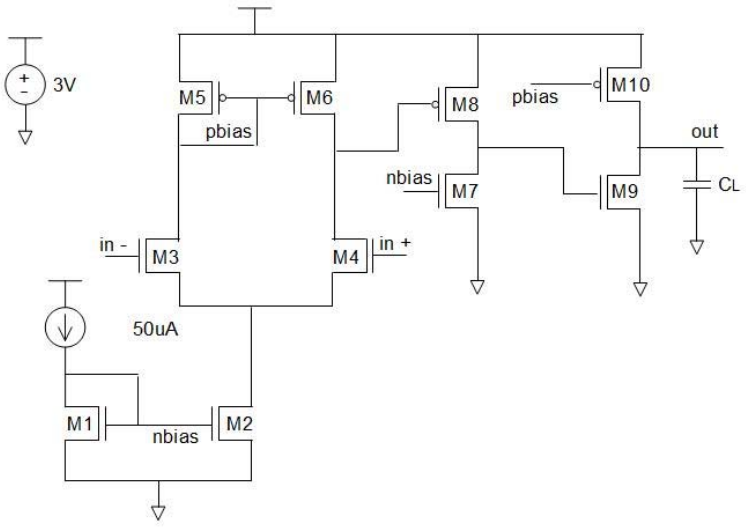

Figure 6–7: Differential amplifier with three gain stages schematic

Results for the differential amplifier with three gain stages are also shown. Simulations such as AC analysis, transient response and DC sweep are shown. The AC result when DC the input signal in both inputs is the same is shown in figure 6–8. In this case both inputs where 3V (Vdd) each. The gain obtained with this set-up was 40.47 dB and a 3dB frequency of 77.5 MHz.

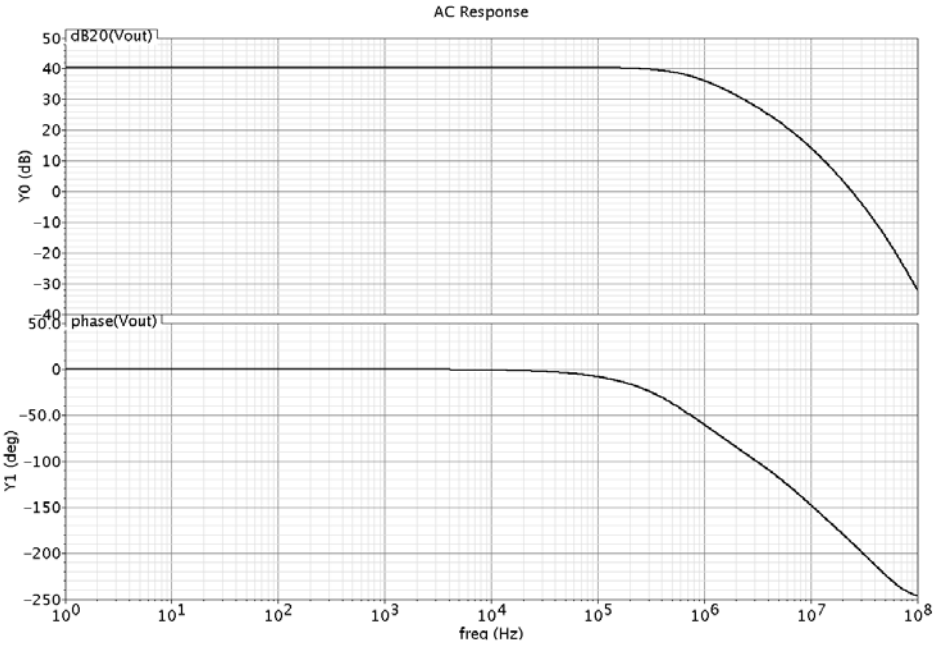

Figure 6–8: Differential amplifier with three gain stages AC Response with same DC voltage at both inputs

An AC simulation when the DC input signal of both inputs was different by 1 mV was done. The result is shown in figure 6–9. In this case one input was 3 V (Vdd) and the other was 2.999 V. The gain obtained with this new set-up was 71.54 dB and a 3dB frequency of 28.85 MHz. This second OpAmp needed a load capacitance of 20 pF for a stable response.

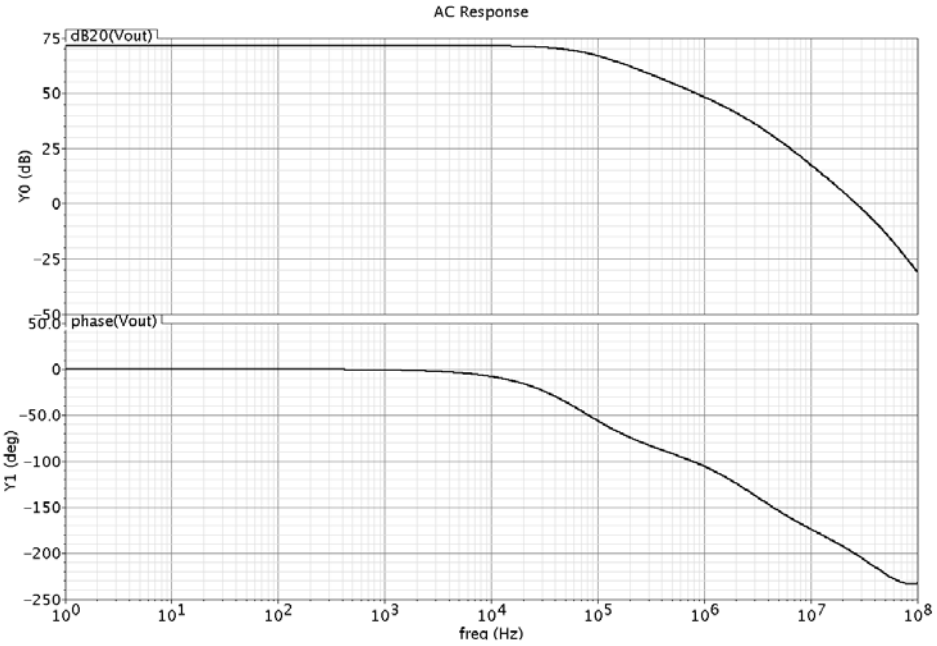

Figure 6–9: Differential amplifier with three gain stages AC Response with 1 mV difference at both inputs

In case of a close loop system desired, the needed compensation scheme between the second and third stage is an RC combination of:

In this case f = $10^5 \Rightarrow 2\pi f = \omega = 628{,}319 = 1/\tau \Rightarrow \tau = 1.59155\times10^{-6} = RC$

Assuming C = 30pF, R = 53051.6 Ω

Transient response of the circuit is shown in figure 6–10.

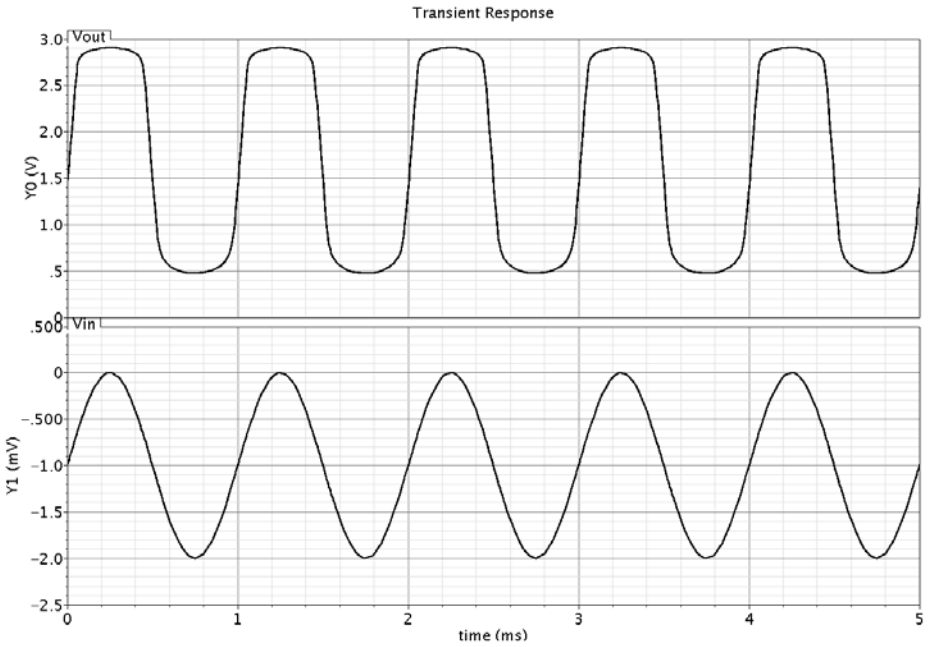

Figure 6–10: Differential amplifier with three gain stages Transient Response with 1 mV difference at both inputs

This transient response shows the result of 1 mV input difference. The input signal shown is negative because it was calculated as the difference between the lower input voltage (2.999 V) minus the higher input voltage (3 V). Again the open loop gain is big enough as to saturate the output, thus feedback is needed.

DC Sweep response with 1 mV difference at both inputs is shown in figure **??**. The resulting slope from this DC sweep analysis was higher than in the simple differential amplifier with the additional gain stage, previously presented.

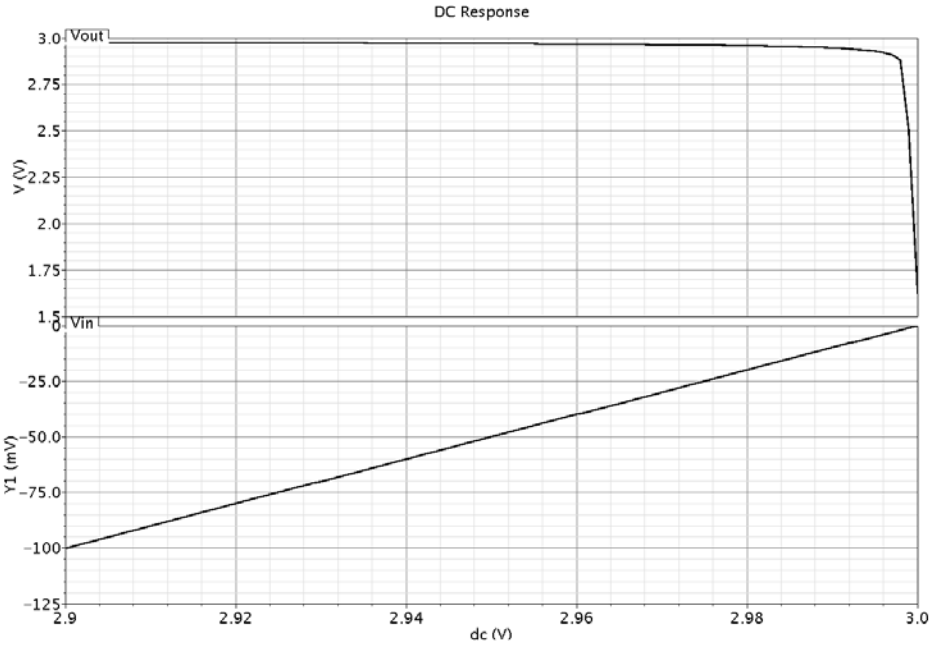

Figure 6–11: Differential amplifier with three gain stages DC sweep Response with 1 mV difference at both inputs

Figure 6–12 shows a zoom close to Vdd. The resulting slope from this DC sweep analysis was 3,477 V/V. Vin range varies from 2.9988 V to 2.9993 V and Vout from 0.81758 V to 2.5561 V.

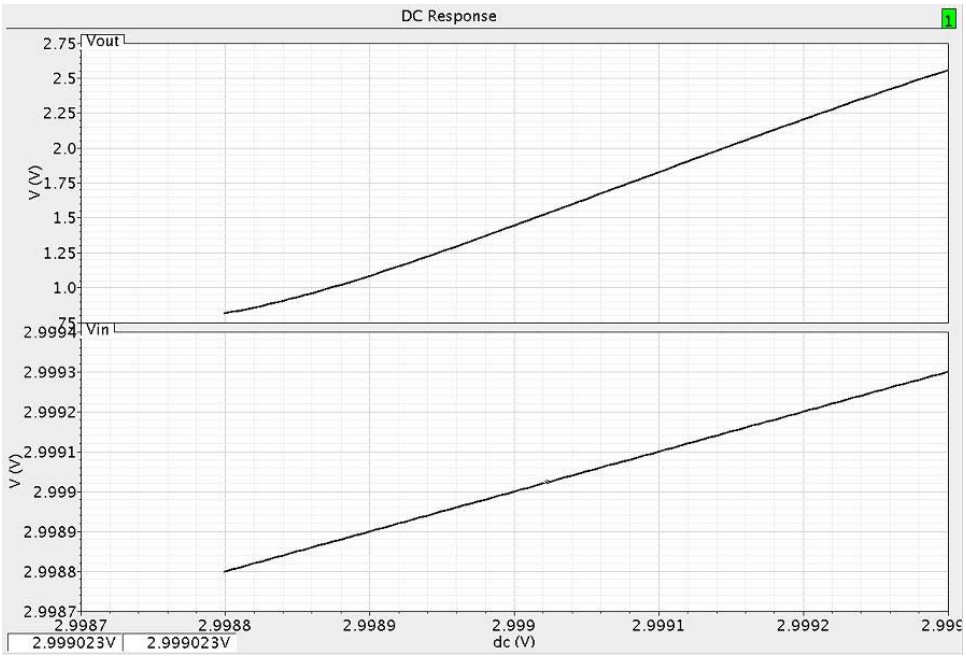

Figure 6–12: Differential amplifier with three gain stages DC sweep Response with 1 mV difference at both inputs

After these results the differential amplifier with three gain stages was selected as a better alternative because of the higher gain solution and higher DC sweep slope (representing a more drastic change at the output in relationship with a small change in the input voltage) that it represents compared with the simple OpAmp with the output cascoded one time.

6.1.3 Differential amplifier CMMR

The differential amplifier differential input gain A_d = 71.54 dB was obtained when the inputs are 3 V and 2.999 V. For the common mode voltage of 2.9995 V the *CM* gain (As gain) was = - 21.68 dB. Figure 6–13 shows the As gain response. In this case the CMRR = 20log $\frac{71.54}{|-21.68|}$ = 10.37 dB.

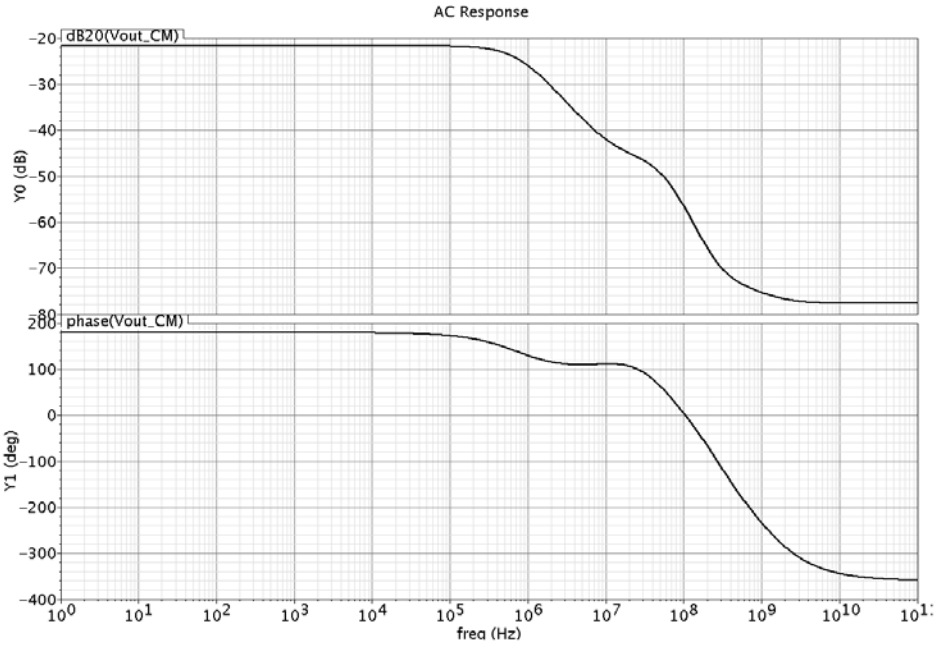

Figure 6–13: Common Mode OpAmp Response

6.1.4 Differential amplifier Slew Rate

The following figure 6–14 shows the sensor response to a positive pulse for slew rate calculation purposes. The input voltage source used was a pulse of 20ns as rising and falling time. The pulse width was 1 us and the period was 2 μs. The pulse also had a delay of 250 ns. Because the OpAmp has three amplification stages the output response signal has a negative slope. Note that in figure 6–14 the negative of the output signal was plotted in order to have positive voltage readings. An output voltage change from 3 V to 3.294 mV took from 455.8 ns to 831.4 ns. In other words a Δv of 2.99671 V took a Δt of 375.6 ns. The positive slew rate response was: 7.97849 V/μs.

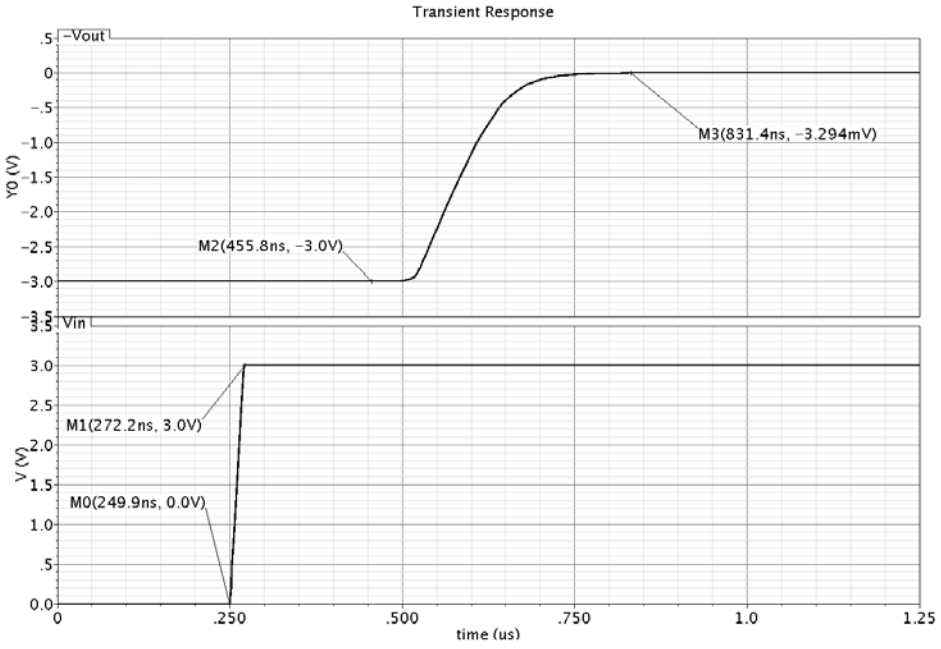

Figure 6–14: Positive Slew Rate OpAmp Response

6.1.5 Differential amplifier Input Referred Noise

The following figure 6–15 shows the equivalent input noise response when simulated via Cadence.

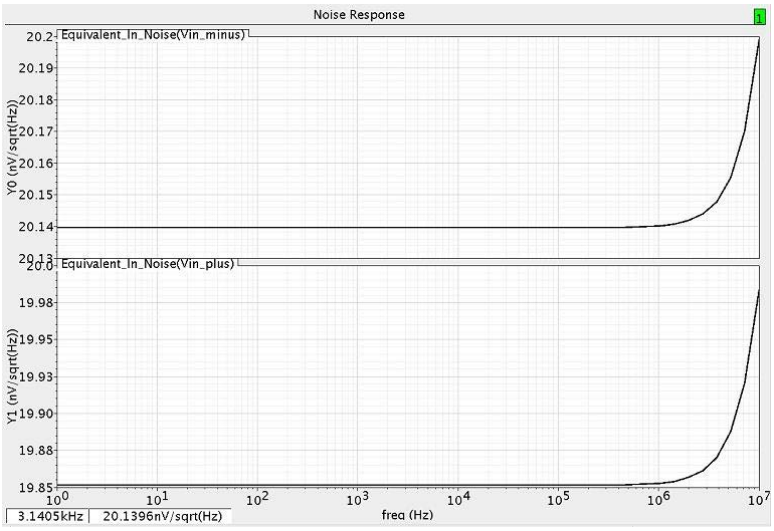

Figure 6–15: Input Referred Noise Response

The following figure 6–16 shows the equivalent input noise response.

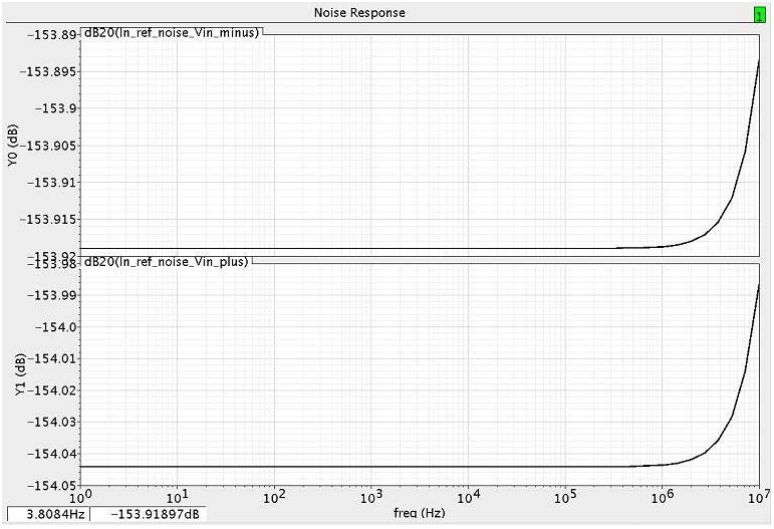

Figure 6–16: Input Referred Noise Response in dB

The following figure 6–17 shows the squared equivalent input noise response.

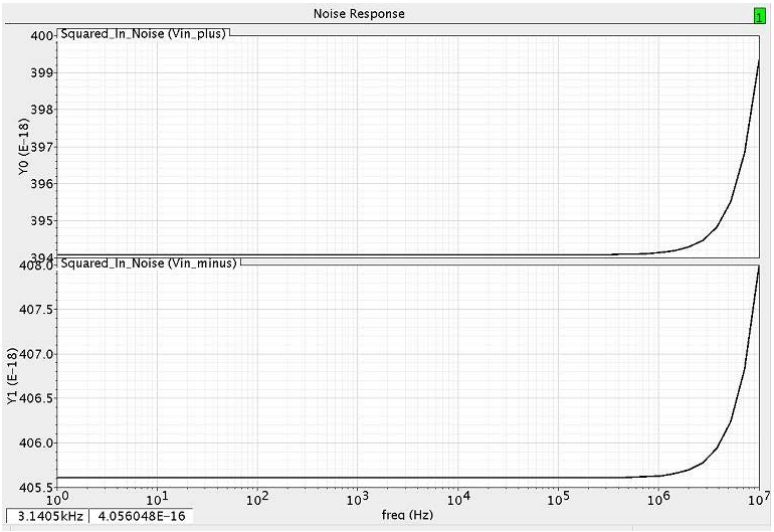

Figure 6–17: Squared Input Referred Noise Response

In this design an open loop gain circuit is presented. Ideally the system should include feedback because this will avoid complications associated with output saturation specially in case the circuit has noise in the power rail. This feedback could be programmable, in this way having the GBW product frequency, the circuit's 3dB frequency can be obtained. One this frequency is obtained the appropriate compensation RC values can be calculated according to the following relationships:

$2\pi f = \omega = 1/\tau \ \tau = RC$

6.1.6 Sensor Output Resistance, Gain and Power Consumption calculations

Rout:

Calculations for Rout yield: Rout = $r_{09} \parallel r_{010} \approx r_0/2 \approx 39.370$ KΩ.

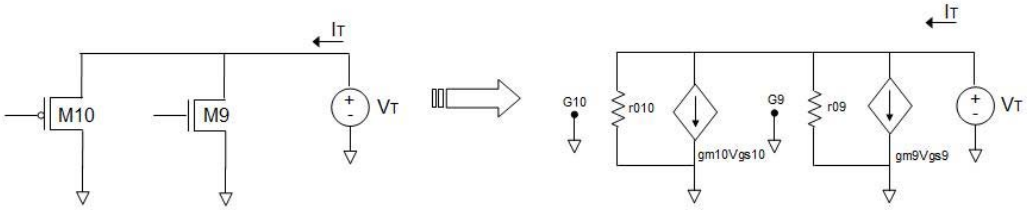

Figure 6–18: Sensor Output Resistance

Gain:

$Av_{total} = Av_{stage3}$

$Av_{stage1} = - g_{m4} (r_{04} \parallel r_{06})$

$Av_{stage2} = Av_{stage1} [- g_{m8} (r_{08} \parallel r_{07})]$

$Av_{stage3} = Av_{stage2} [- g_{m9} (r_{09} \parallel r_{010})]$

I_D and gm values were obtained from the simulation results. The λ was assumed to be = 0.01 V^{-1}, g_{m4} = 167.7 uΩ^{-1}, g_{m8} = 1.087 mΩ^{-1}, g_{m9} = 240.3 $\mu\Omega^{-1}$, I_D = 127 μA, $r_0 = 1/(\lambda\ I_D) \approx 78.740$ KΩ

$Av_{total} = \frac{-(gm4*gm8*gm9)r0^3}{8} = \frac{-4.38043*10^{-11}*78740^3}{8}$ = -2673.1 V/V = 68.54 dB

Error between calculated gain and simulation results:

Av_{total} simulation = 71.54 dB

Av_{total} calculated = 68.54 dB

Error % = $\frac{experimental\ value - accepted\ value}{accepted\ value} \times 100 =$

$\frac{71.54dB - 68.54dB}{68.54dB} \times 100 = 4.377$ %

Power:

Power consumption was calculated as the sum of all the DC currents circulating through the circuit at the DC operation point.

I total = 50 μA + 52.03 μA + 129.3 μA +127 μA =

P = V*I = 3*(358.33 μA)= 1.075 mW

6.1.7 Comparative Analysis for i_{DD} sensors

Next table 6–19 shows a summary of different designed BISTs that are useful for i_{DD} sensing. None of these available structures compares directly to the approach used in this work. This work utilizes the available structure to perform the current to voltage conversion. The rest of the presented alternatives introduces a device between Vdd and the CUT or only samples part of the current.

Reference	Gain	BW	Area	Tech	VDD
[Antonioli00]	Not provided	50 MHz	5,600 um²	0.35 um CMOS	Not provided
[Ducoudray03]	52 dB	60 MHz	0.06 mm²	0.5 um CMOS	1.8 V
[Kilic01]	92 dB	1 KHz	0.019 mm²	0.8 um CMOS	5 V
[Kim01]	Not provided	tested at a maximum of 50 MHz	0.1225 mm²	180 nm CMOS	Not provided
Thesis Design	71.54 dB	28.85 MHz	4,185 um²	0.6 um CMOS	3 V

Figure 6–19: Table shows a summary of different designed BISTs used as i_{DD} sensors

CHAPTER 7
SIMULATIONS AND RESULTS

7.0.8 iDD Characterization

iDD is the current that flows from the positive power supply at any moment through the circuit. $i_{DD} = I_{DD} + i_{dd}$, where I_{DD} stands for the DC current and i_{dd} stands for the AC current. i_{DD} can be characterized and defined as the footprint waveform for defect free circuits during Vdd pulsing and/or during normal operation. Current footprint waveform is the i_{DD} response for a defect free circuit. This curve typically shows small spikes associated with the turn off-on of internal capacitances, [2]. The generation of this waveform allows test engineers to use it as a footprint (reference). They can compare other CUT responses with this one and depending on the resulting waveform, determine if the new CUT is a defect free one or not. Vdd pulsing consists in pulsing the CUT's Vdd supply maintaining the sensors Vdd in a defined dc voltage level.

The steps followed for generating and iDD footprint and testing a CUT for different failures were:

1. Current Waveform: Use a small resistor to develop a voltage drop across the sensor input terminals.
2. CUT: Run a transient simulation of the CUT with and with-out the sensor (ensure there is no added error from the sensor).
3. iDD footprint: Pulse Vdd and capture the iDD current response for a defect-free circuit.

4. iDD response: Induce some parametric and catastrophic failures in the CUT and pulse Vdd. Capture these waveforms and compare them with the iDD footprint.

Figure 7–1 shows a block diagram of the Vdd pulse set-up.

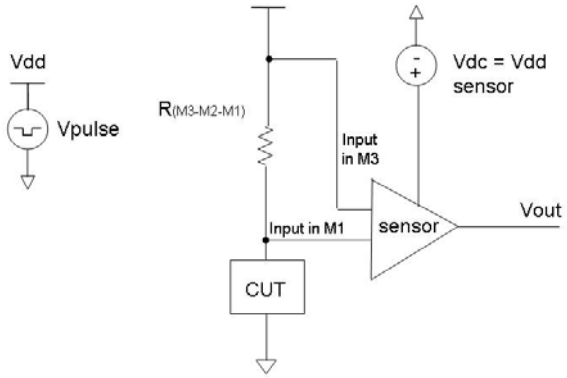

Figure 7–1: Diagram showing CUT and sensor circuit connections when performing Vdd pulsing.

Figure 7–2 shows a block diagram of the CUT and sensor during normal operation.

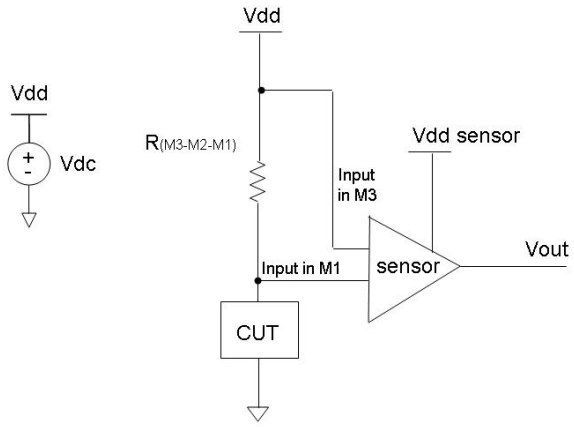

Figure 7–2: Diagram showing CUT and sensor circuit connections during normal operation.

7.0.9 Vdd pulsing

The result of the iDD response when pulsing Vdd is shown for a defect-free CUT and for different failures in the CUT. Then the same failures are presented for the CUT and sensor were under normal operation (Vdd = Vdc) conditions.

CUT #1

The first CUT is an inverter with PMOS dimensions of w= 4.5 μm, l= 600 nm and NMOS dimensions of w= 1.5 μm, l= 600 nm. A small resistor (300 mΩ) was placed between the Vdd terminal and the PMOS source to simulate the impedance associated with the pad frame.

Vdd pulse set-up was: V_1= 3 V, V_2= 0 V, delay= 500 ns, rise time= 20 ns, fall time= 20 ns, pulse width= 10 μs, period= 20 μs, Vdc= 3 V.

First, a transient response was used to verify that the CUT with and without the sensor will have the same response.

Figure 7–3 shows that the transient response is the same with no deviations or offset present.

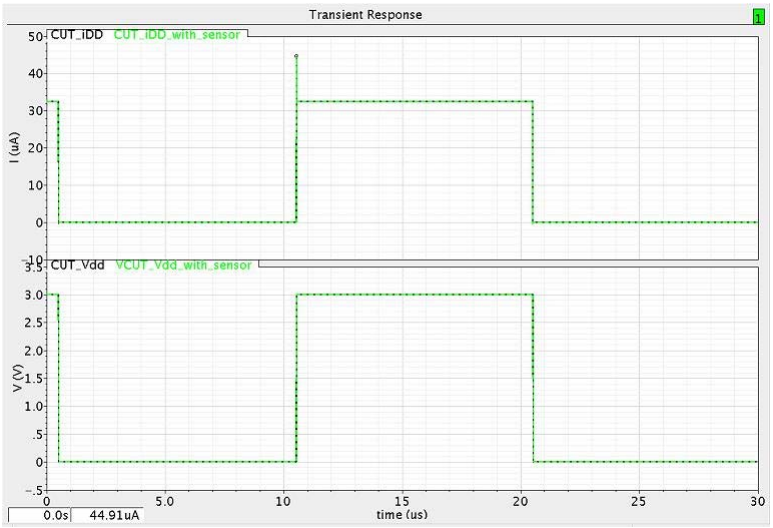

Figure 7–3: Transient response of the CUT with and without the sensor.

The results obtained from pulsing Vdd for an iDD footprint when no failure is present compared with when failures are present is shown in figure 7–4.

The faults are identified as:

Fault # 1: Larger PMOS size (from w= 4.5 μm to w= 4.65 μm).

Fault # 2: short from CUT's input to output.

Fault # 3: SA 1.

Fault # 4: SA 0.

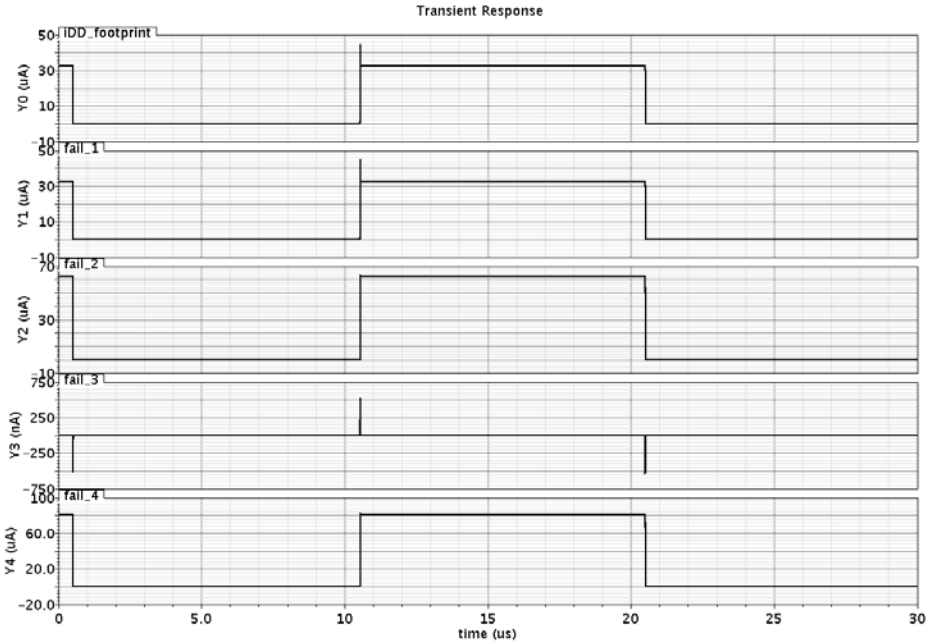

Figure 7–4: iDD curves when pulsing Vdd.

From this plot it can be seen that all curves show some deviation from the iDD footprint waveform. Next figures zoom on these plots for better visibility of the changes. The plots show the iDD current curve versus the sensor response.

Figure 7–5 shows the iDD curve and sensor output response for fault #1, when pulsing Vdd. This is a parametric fault. There is a slight difference in the dc current value ($\approx 0.0321\ \mu$A) of the i_{DD}. This difference is negligible but still to be captured by the sensor. The small difference detected is shown 7–6 ($\approx 1.1\ \mu$V).

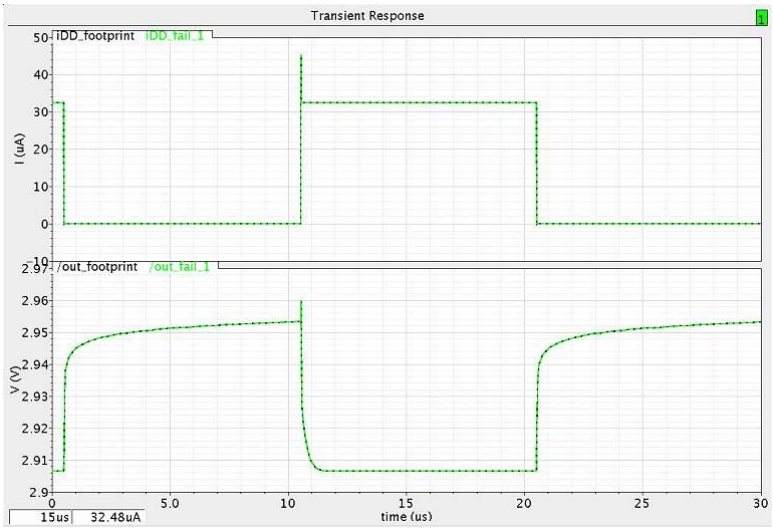

Figure 7–5: iDD curve and sensor output response for fault #1, when pulsing Vdd.

Zoom of the sensor's response fault #1 shown previously in figure 7–5. In this plot it is easier to appreciate the iDD current dc magnitude increase from the defect free CUT to the faulty CUT.

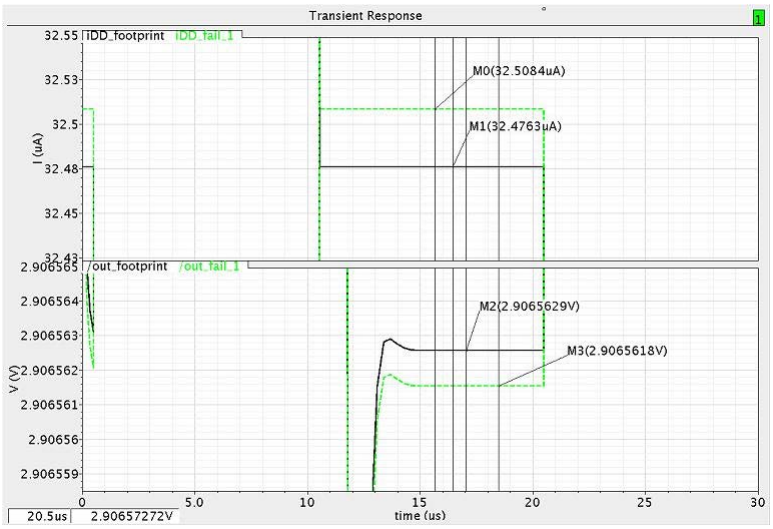

Figure 7–6: Zoom view of the iDD curves and sensor output response for fault #1, when pulsing Vdd.

Figure 7–7 shows the iDD curve and sensor output response for fault #2, when pulsing Vdd. In this cases the plots show the response to a catastrophic fault. In both cases (current and voltage) the curve variations are very noticeable.

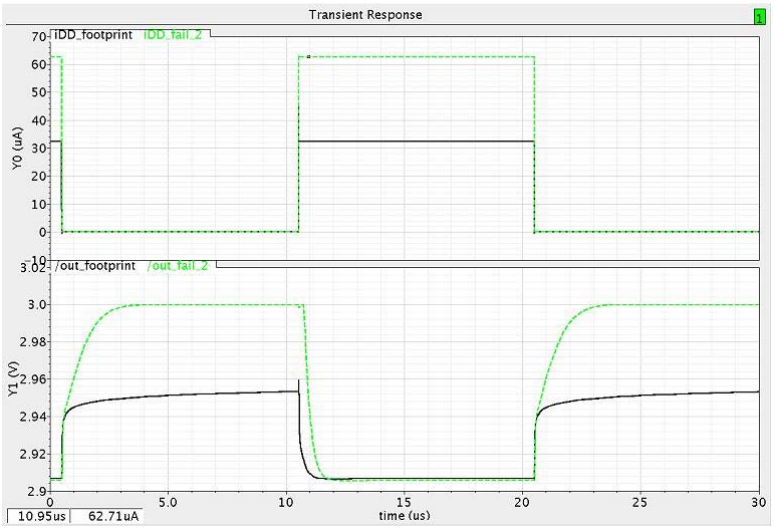

Figure 7–7: iDD curves and sensor output response for fault #2, when pulsing Vdd.

Zoom of the sensor's response to fault #2 shown previously in figure 7–7. In this plot it is easier to appreciate the rise time delay present in the iDD curve that is reflected in the sensor's output of figure 7–7 from the defect free CUT to the failing CUT.

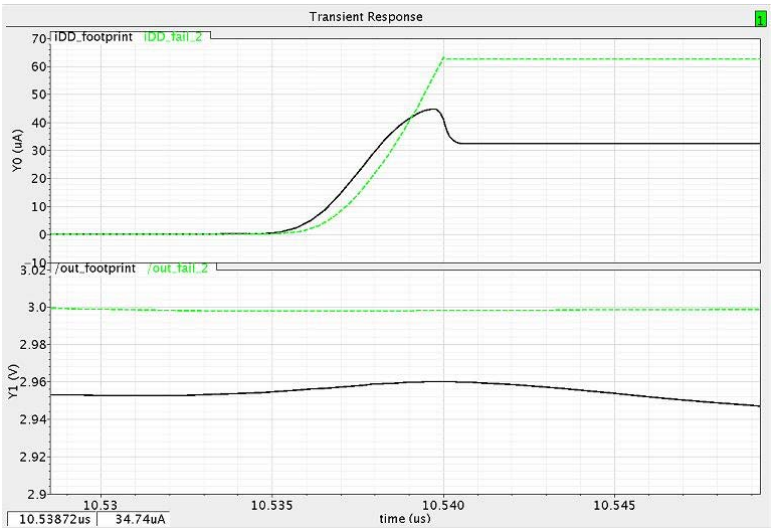

Figure 7–8: Zoom view of the iDD curves and sensor output response for fault #2, when pulsing Vdd.

Figure 7–9 shows the iDD curve and sensor output response for fault #3, when pulsing Vdd. A second catastrophic fault is shown, a stuck at one (Vdd). This fault shows a different current response waveform and a slightly smaller current spike. The spike at the output may be smaller due to the fact that the output is close to Vdd. It is not greatly magnified but a zoomed view is shown in figure 7–10 for better appreciation.

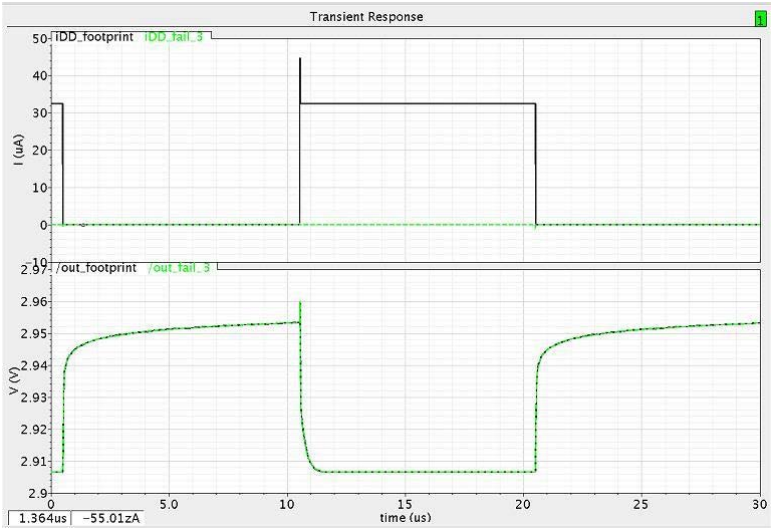

Figure 7–9: iDD curves and sensor output response for fault #3, when pulsing Vdd.

Zoom of the sensor's response to fault #3 shown previously in figure 7–9. Here is easier to appreciate the output sensor's variation from the defect free CUT to the failing CUT ≈20.5 μV.

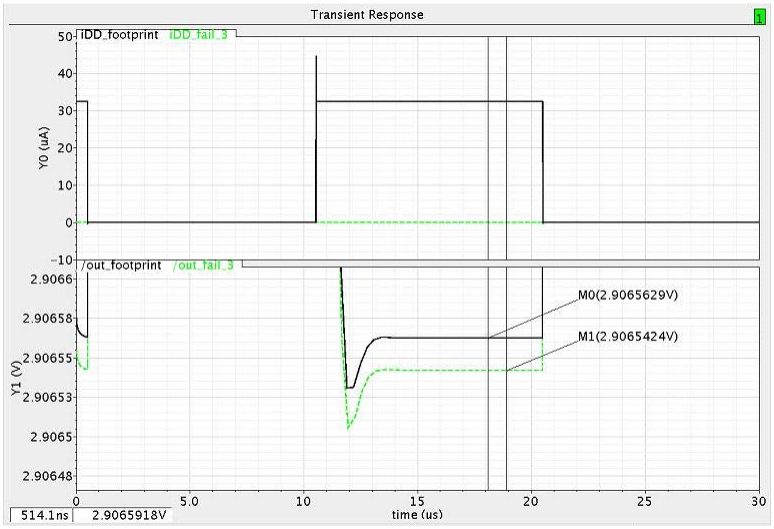

Figure 7–10: Zoom view of the iDD curves and sensor output response for fault #3, when pulsing Vdd.

Figure 7–11 shows the iDD curve and sensor output response for fault #4, when pulsing Vdd. This figure shows the third catastrophic CUT response. This is a stuck at zero fault and the iDD and sensor response captured very well this fault.

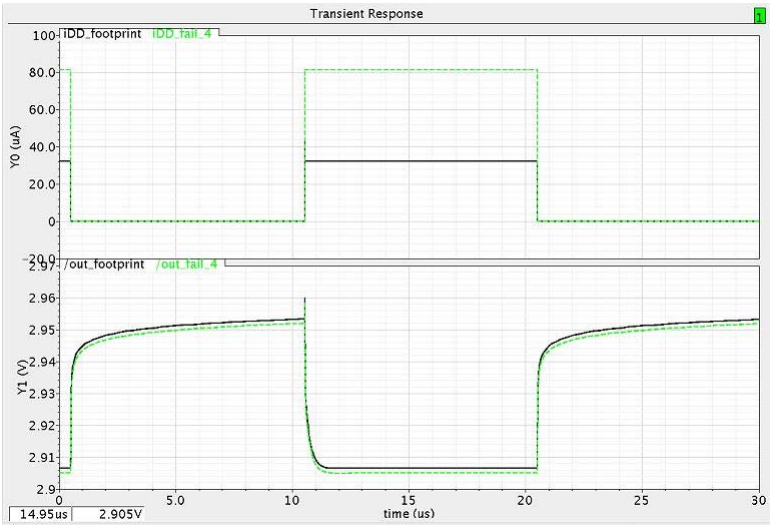

Figure 7–11: iDD curves and sensor output response for fault #4, when pulsing Vdd.

Zoom of the sensor's response with fault #4 is shown previously in figure 7–11. Here it is easier to appreciate the difference between the sensor's output response waveform for the defect-free CUT and the faulty CUT.

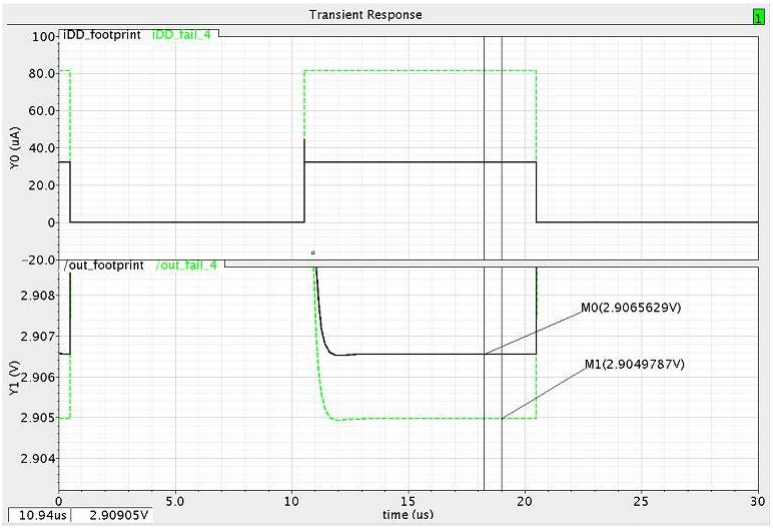

Figure 7–12: Zoom view of the iDD curves and sensor output response for fault #4, when pulsing Vdd.

7.0.10 Sensor response during normal operation

The following results where obtained when used simulating the real application during normal operation. The faults used when pulsing Vdd are now repeated but when Vdd is not pulsed but a DC source. In this new set-up, Vdd the CUT is operating. The input pulse set-up is defined as:

Vin pulse set-up was: V1= 3 V, V2= 0 V, delay= 500 ns, rise time= 20 ns, fall time= 20 ns, pulse width= 10 μs, period= 20 μs, Vdc= 3 V.

The first figure 7–13 presents the sensor's response in case of a parametric fault is encountered in the PMOS transistor size of the CUT, fault #1.

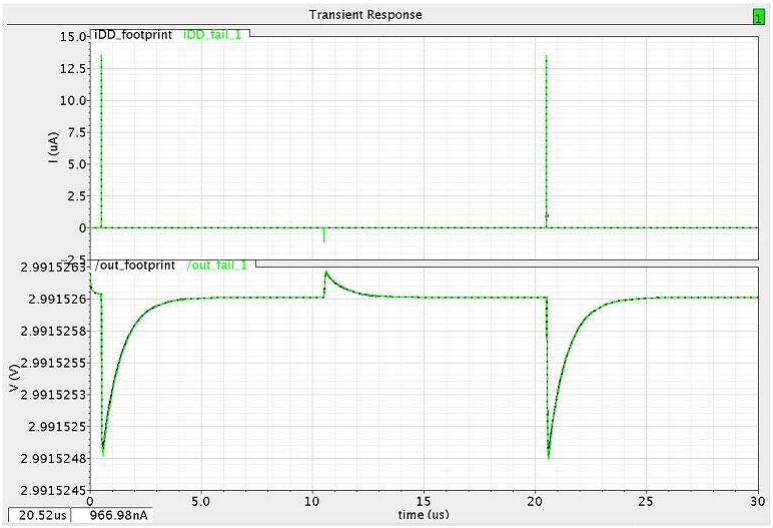

Figure 7–13: Sensor response when a parametric fault is found in the PMOS transistor size of the CUT.

From this figure the differences between the defect-free CUT and the faulty CUT are not very clear. Figure 7–14 shows a zoom in a small section during the signal transition where some differences can be appreciated.

Figure 7–14 shows a zoom in a small section during the signal transition.

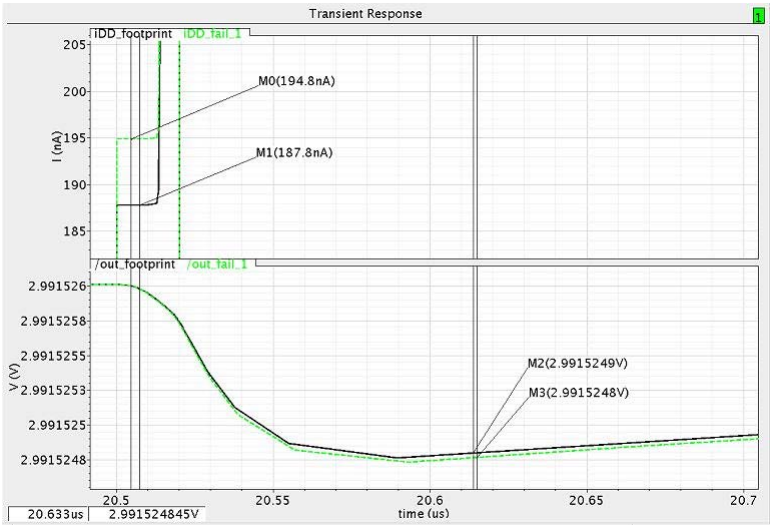

Figure 7–14: Zoom of a section of the figure 7–14.

The following figure 7–15 presents the sensor's response in case a catastrophic fault is encountered in the CUT. The fault problem simulated was a short between the input and the output of the CUT (an inverter). i_{DD} waveform obtained from the faulty circuit varies significantly from the footprint.

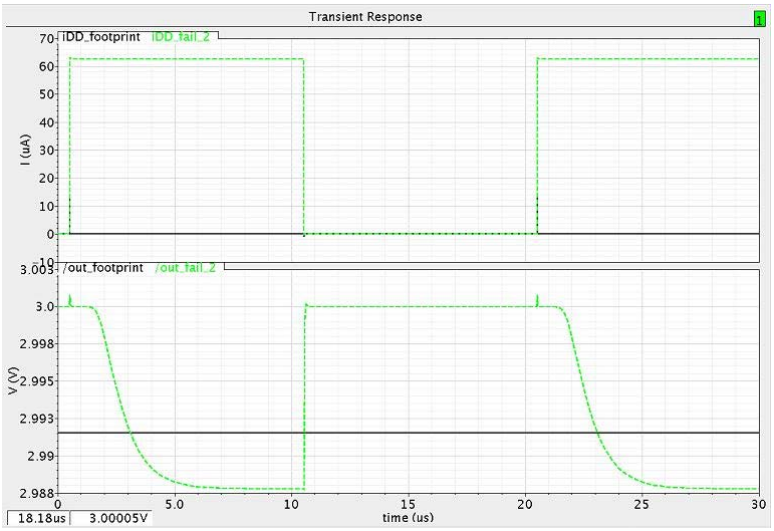

Figure 7–15: Sensor response to a catastrophic fault of a short between input and output.

Next is the case of another catastrophic fault, a SA_1 (Stuck at one fault). In this case the CUT's output is shorted to Vdd. Figure 7–16 presents the sensor's response in case a catastrophic fault is encountered in the CUT (an inverter). As in 7–15 the output signal shows a dramatic difference response with the fault.

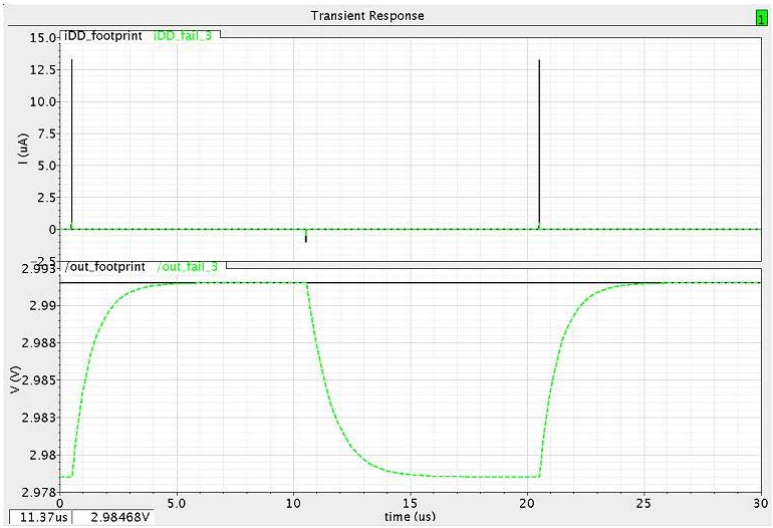

Figure 7–16: Sensor response to a catastrophic fault, a short between output and Vdd

The last fault simulated is another catastrophic fault, a SA_0 (Stuck at Vss fault). In this case the CUT's output is shorted to Vss. Figure 7–17 presents the sensor's response in case this catastrophic fault is encountered in the CUT (an inverter). Also in this case, as in 7–15 and 7–16, the output signal shows a dramatic response to this failure.

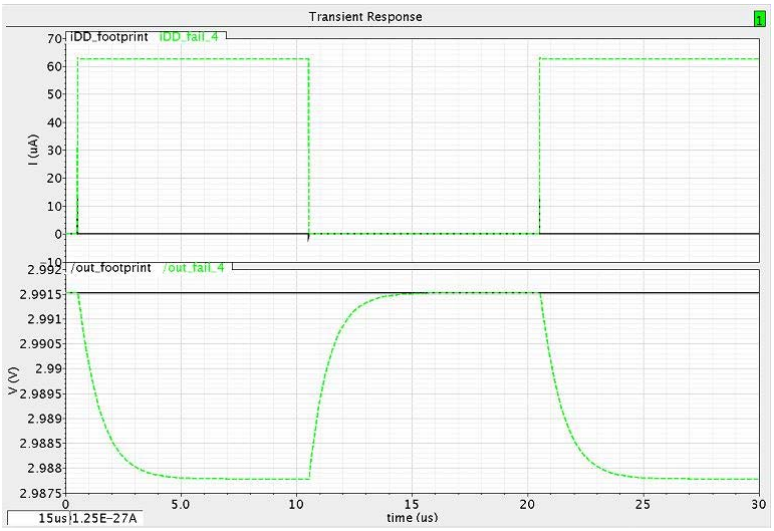

Figure 7–17: Sensor response to a catastrophic fault, a short between output and Vss

CUT #2

The second CUT is a differential amplifier with input NMOS dimensions of w=19.95 μm, l=1.2 μm, PMOS load of dimensions of w=60 μm, l=1.2 μm. The differential amplifier bias circuit is a simple current mirror of dimensions of w=40 μm, l=1.2 μm and I_{Bias} =50 μA. A small resistor (300 mΩ) was placed between the Vdd terminal and the PMOS source to simulate the impedance associated with the pad frame.

When testing using Vdd pulsing the Vdd pulse set-up was:
V_1= 3 V, V_2= 0 V, delay= 500 ns, rise time= 20 ns, fall time= 20 ns, pulse width= 1 μs, period= 2 μs, Vdc= 3 V.

First, a transient response was used to verify that the CUT with and without the sensor will have the same response.

Figure 7–18 shows that the transient response is the same with no deviations or offset present.

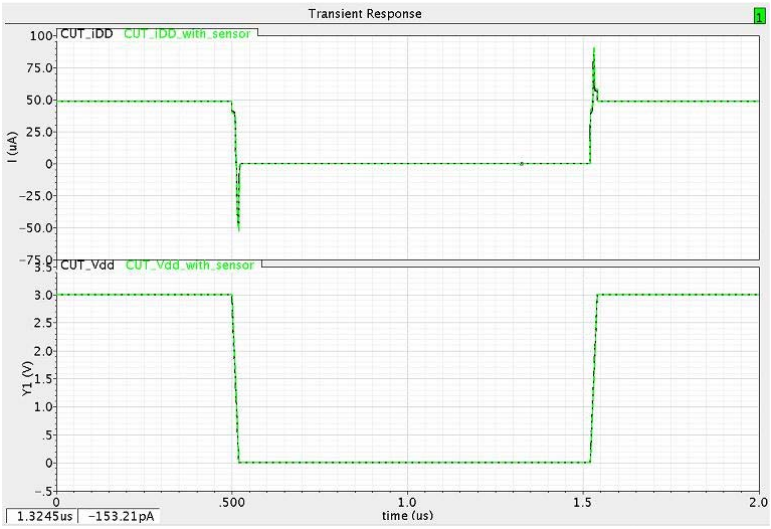

Figure 7–18: Transient response of the CUT with and without the sensor.

The results obtained from pulsing Vdd for a defect-free iDD footprint compared with the iDD waveform when faults are present is shown in figure 7–19.

The faults are identified as:

Fault # 1: Larger differential input NMOS size (positive input) (from w= 19.95 μm to w= 22.05 μm).

Fault # 2: short from CUT's input to output.

Fault # 3: SA 1.

Fault # 4: SA 0.

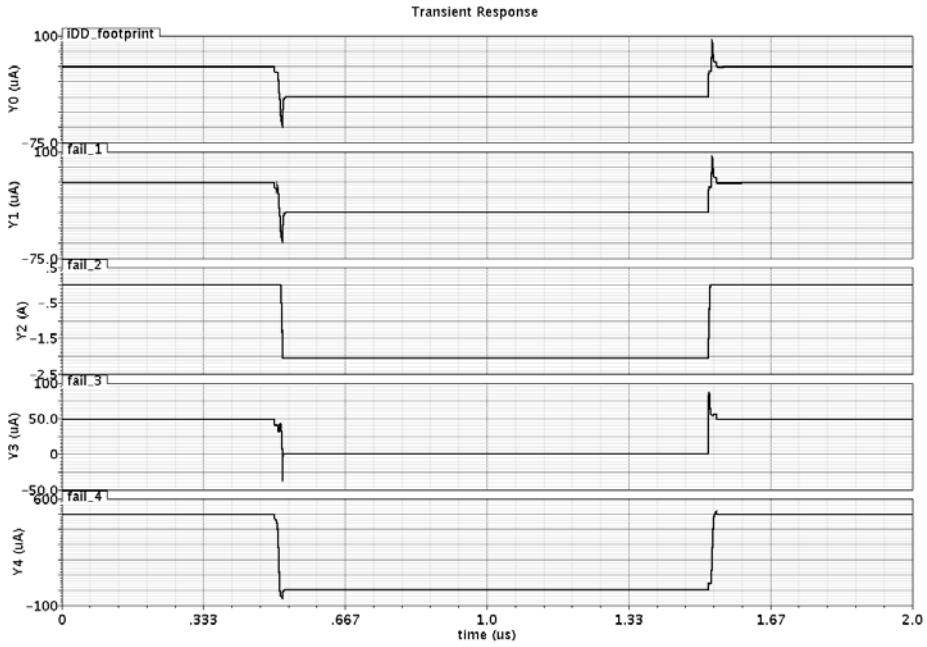

Figure 7–19: iDD curves when pulsing Vdd.

From this plot it can be observed that all waveforms show some deviation from the iDD footprint. Next figures show specific views of these plots to make more visible these changes. The plots show the iDD current waveform versus the sensor response.

Figure 7–20 shows the iDD curve and sensor output response for fault #1, when pulsing Vdd. This is a parametric fault. The iDD from the CUT and the sensor's response have no visible differences.

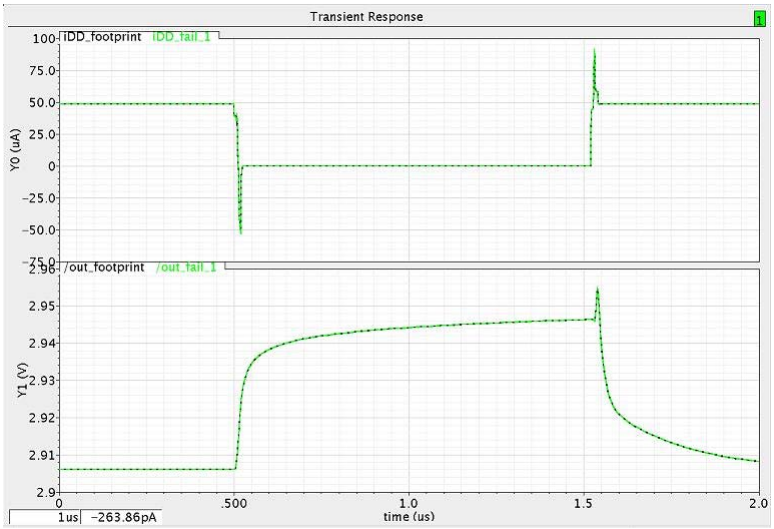

Figure 7–20: iDD waveform and sensor output response for fault #1, when pulsing Vdd.

Figure 7–21 shows the iDD curve and sensor's output response for fault #2, when pulsing Vdd. In this case the plot show the response to a catastrophic fault. In both cases (current and voltage) the curve variations are very noticeable.

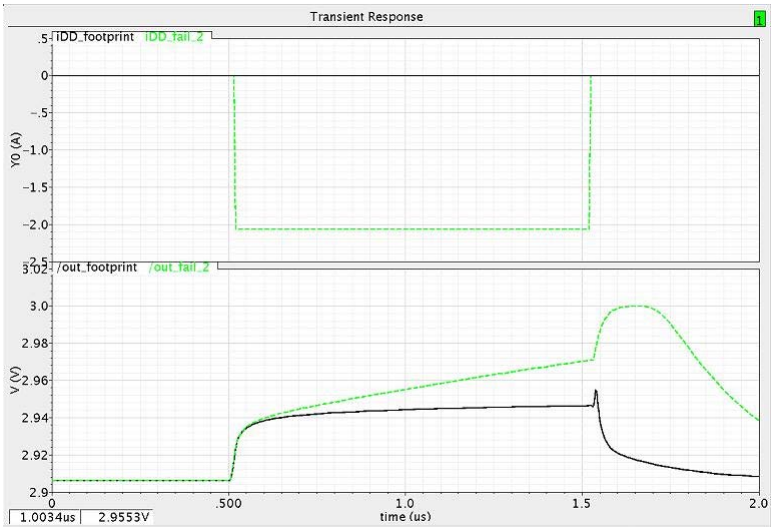

Figure 7–21: iDD curves and sensor output response for fault #2, when pulsing Vdd.

Figure 7–22 shows the iDD curve and sensor's output response for fault #3, when pulsing Vdd. A second catastrophic fault is shown. In this case a stuck at one (Vdd) fault is simulated. This fault shows a different current response and a slightly different shape in the current spike. The spike difference is too small to be captured by this sensor.

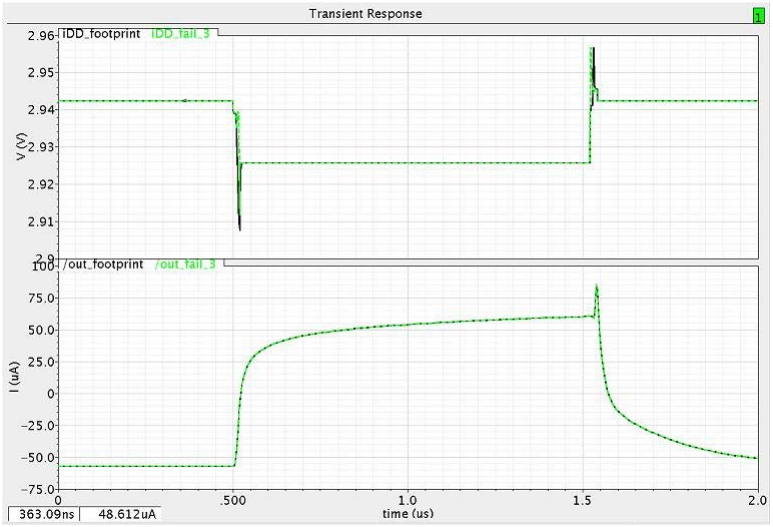

Figure 7–22: iDD curves and sensor output response for fault #3, when pulsing Vdd.

Figure 7–23 shows the iDD curve and sensor output response for fault #4, when pulsing Vdd. This figure shows the third catastrophic CUT response. This is a stuck at zero fault and the iDD and sensor response captures clearly this fault.

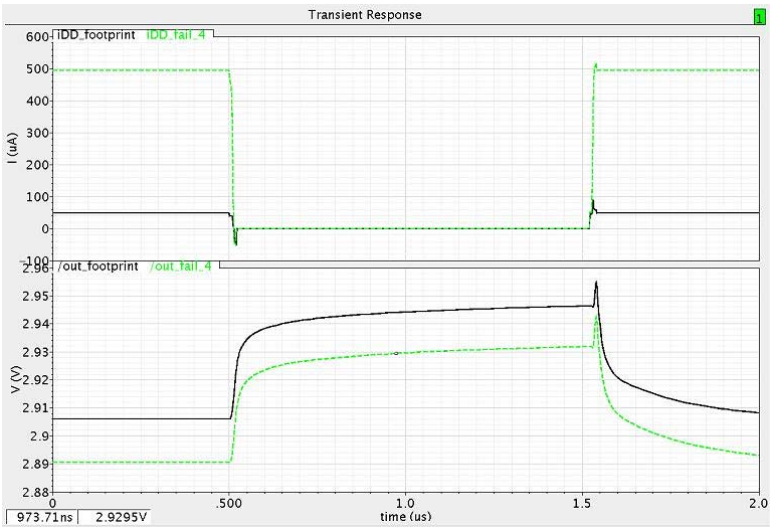

Figure 7–23: iDD waveforms and sensor output response for fault #4, when pulsing Vdd.

7.0.11 Sensor response during normal operation

The following results where obtained when simulating the circuit during normal operation. The same failures that were reviewed when pulsing Vdd are now repeated but Vdd is a Vdc source. The CUT that was previously being tested at a steady input voltage is now operating with an input sinusoidal source (Vin minus). The positive terminal of the differential amplifier is fixed at a DC voltage of 1.48 V. The Vin minus sinusoidal source set-up is defined as:

Vin sinusoidal set-up was: AC magnitude: 1 V Offset voltage V= 1.4799 V, Amplitude V= 10 mV, Frequency = 1M Hz, Vdc voltage= 1.4799 V.

The first graph in figure 7–24 presents the sensor's response in case a parametric fault is encountered in the PMOS transistor size of the CUT, fault #1. The original input maximum values for current and voltage are: 0.1663 μA and 3.2 μV respectively. The output values are: 0.1946 μA for the current and 3.7 μV for the voltage.

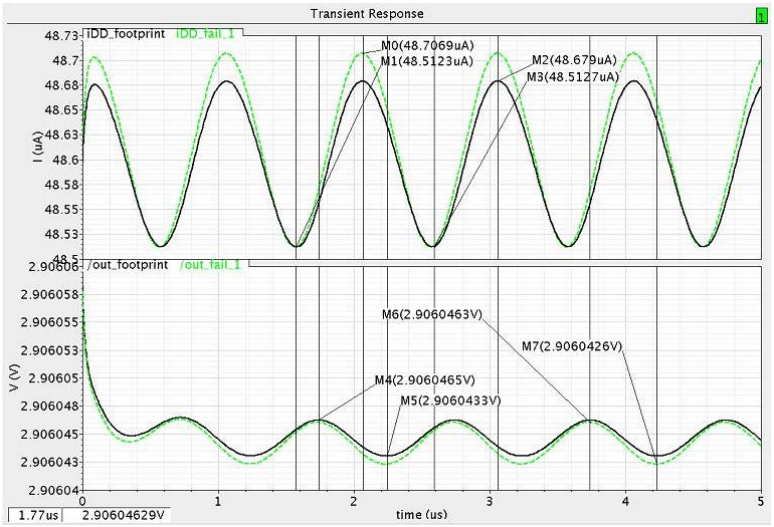

Figure 7–24: Sensor response when a parametric fault is found in the PMOS transistor size of the CUT.

The following figure 7–25 presents the sensor's response in case a catastrophic fault is encountered in the CUT. The simulated fault was a short between the input and the output of the CUT. In this case, the sensor's output response shows a significant variance to the input signal. The original input maximum values for current and voltage are: 0.1663 μA and 3.2 μV respectively. The output values are: 5.1058 μA for the current and 98.9 μV for the voltage.

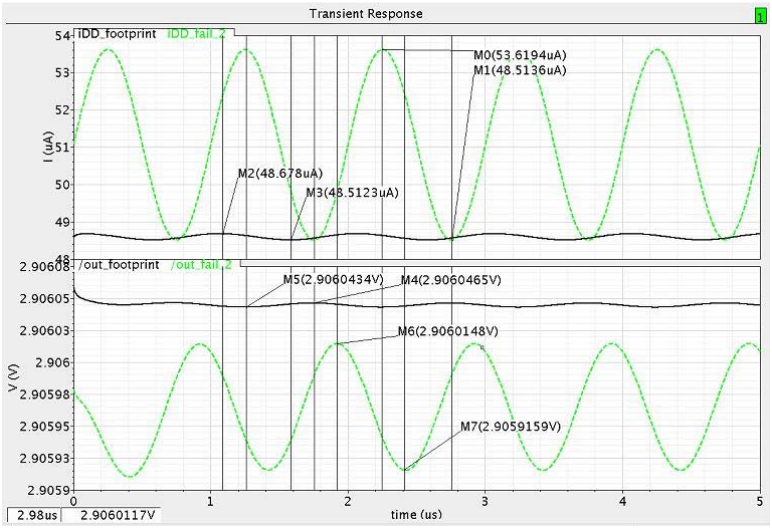

Figure 7–25: Sensor response to a catastrophic fault of a short between input and output.

Next is the case of another catastrophic fault, a SA_1 (Stuck at Vdd fault). In this case the CUT's output is shorted to Vdd. Figure 7–26 presents the sensor's response in case a catastrophic fault this encountered in the CUT. The original input maximum values for current and voltage are: 0.1663 μA and 3.2 μV respectively. The output values are: 0.0337 μA for the current and 0.7 μV for the voltage.

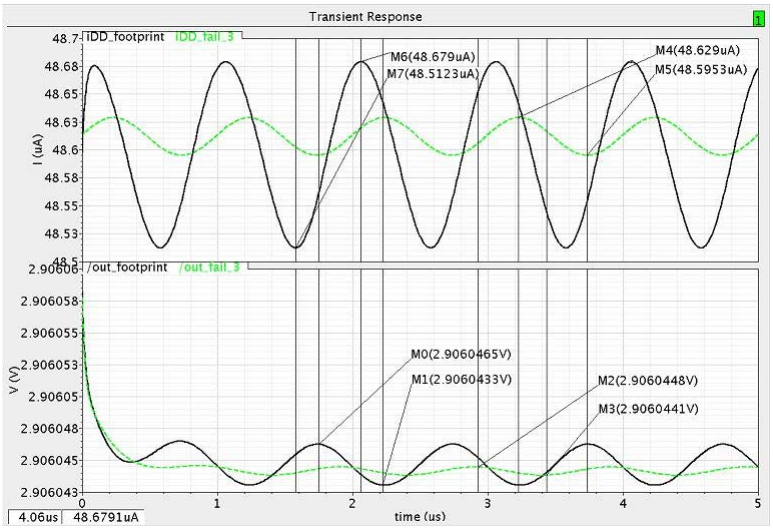

Figure 7–26: Sensor response to a catastrophic fault, a short between output and Vdd

The last fault simulated was a SA_0 (Stuck at zero fail). In this case the CUT's output is shorted to Vss. Figure 7–27 presents the sensor's response in case this catastrophic fault is present in the CUT. Also in this case, as in 7–25 and 7–26, the output signal shows a dramatical difference when the fault is present. The original input maximum values for current and voltage are: 0.1663 μA and 3.2 μV respectively. The output values are: 15.328 μA for the current and 344.4 μV for the voltage.

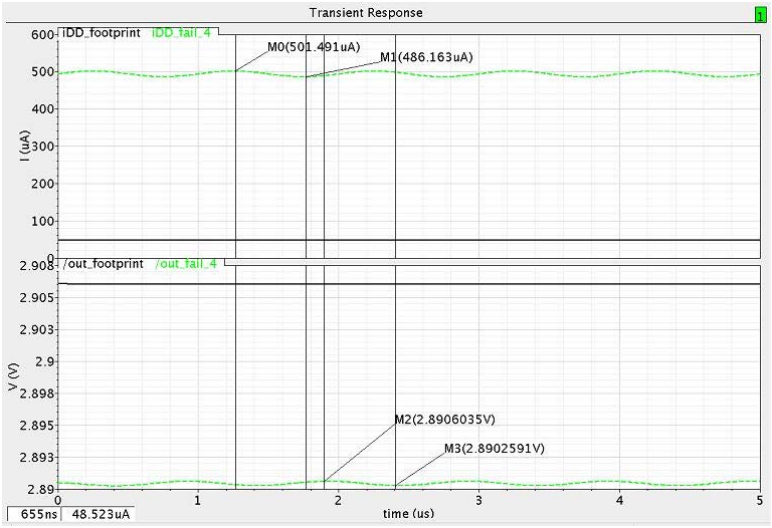

Figure 7–27: Sensor response to a catastrophic fault, a short between output and Vss

7.1 Characterization of Sensor Circuit

The following section discusses the proposed sensor and its responses. It shows some possible parametric or catastrophic failures identified in the sensor shown in figure 7–28. The limitation for performing the sensor characterization via this set-up, is the need of an additional voltage source for the Vin minus input voltage of the differential pair.

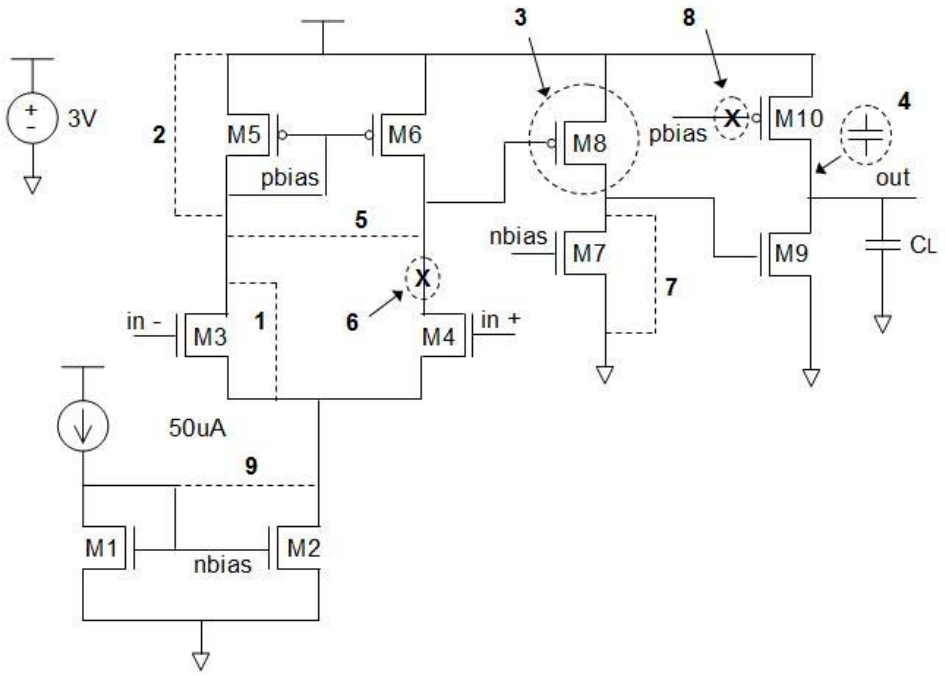

Figure 7–28: Circuit showing possible failures in the sensor circuit.

The defects shown are some of the possible failures that could be present in the sensor after the fabrication process. The defects were tested by pulsing Vdd and obtaining the CUT iDD waveform. This characterization contributes to ensure that the sensor circuit does not posses any failure before using it.

Fault # 1, shows a short from drain to source in M3.

Fault # 2, shows a short from drain to source in M5.

Fault # 3, PMOS M8 is missing.

Fault # 4, is a 5 pF capacitor between the drain of M10 and the output.

Fault # 5, is a short between the drain of M3 and the drain of M4.

Fault # 6, represents an open in the drain of M4.

Fault # 7, shows a short from drain to source of M7.

Fault # 8, shows an open in the gate of M10.

Fault # 9, is a short from drain to gate in M2.

In case of no failure found the iDD current will look like in figure 7–29. This no fault current is known as the iDD footprint.

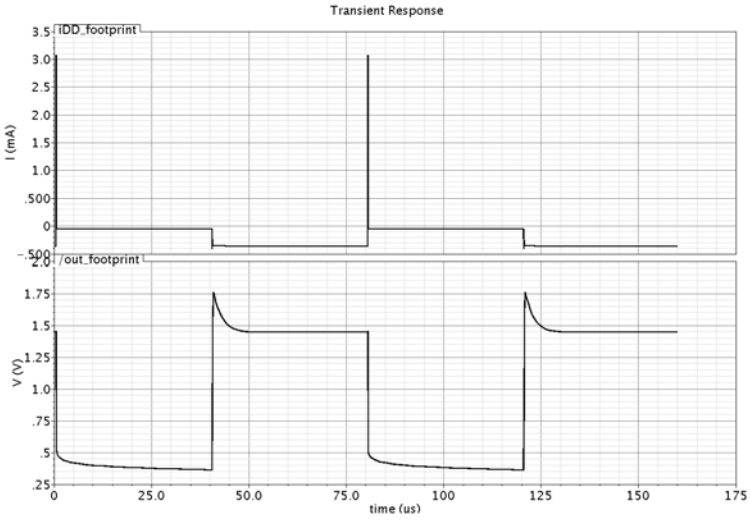

Figure 7–29: iDD footprint of the Sensor Circuit.

In case of fault #1 found the iDD current will look like figure 7–30.

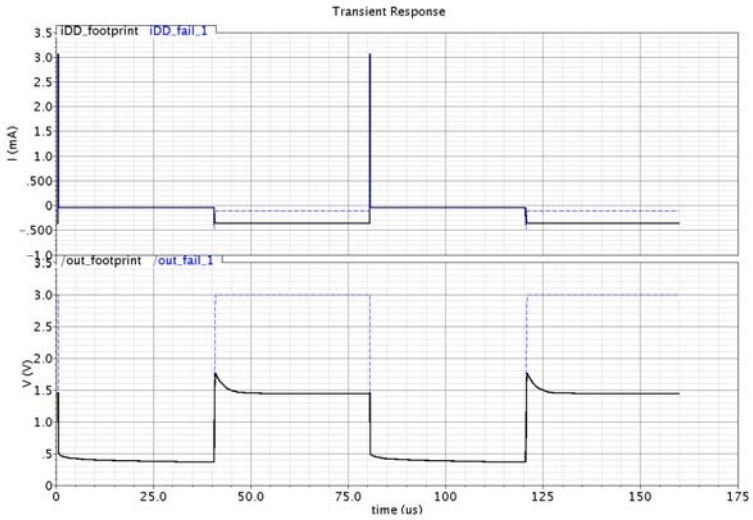

Figure 7–30: Possible fault #1 in the sensor circuit.

In case of fault #2 found the iDD current will look like figure 7–31.

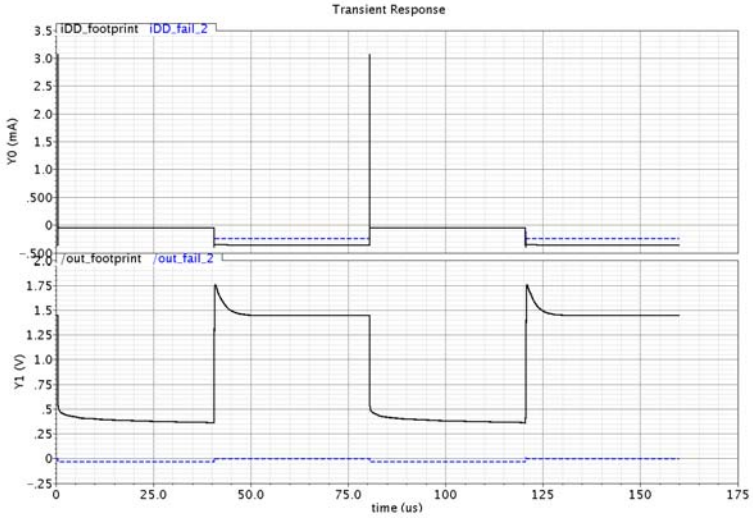

Figure 7–31: Possible fault #2 in the sensor circuit.

In case of fault #3 found the iDD current will look like figure 7–32.

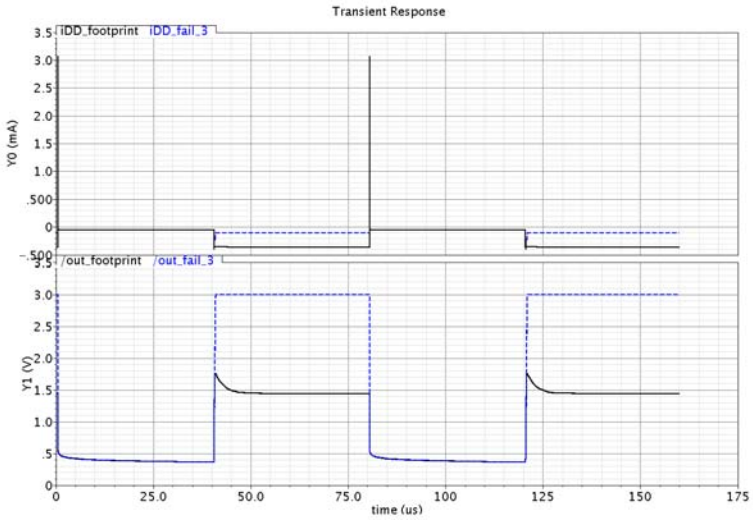

Figure 7–32: Possible fault #3 in the sensor circuit.

In case of fault #4 found the iDD current will look like figure 7–33.

Figure 7–33: Possible fault #4 in the sensor circuit.

In case of fault #5 found the iDD current will look like figure 7–34.

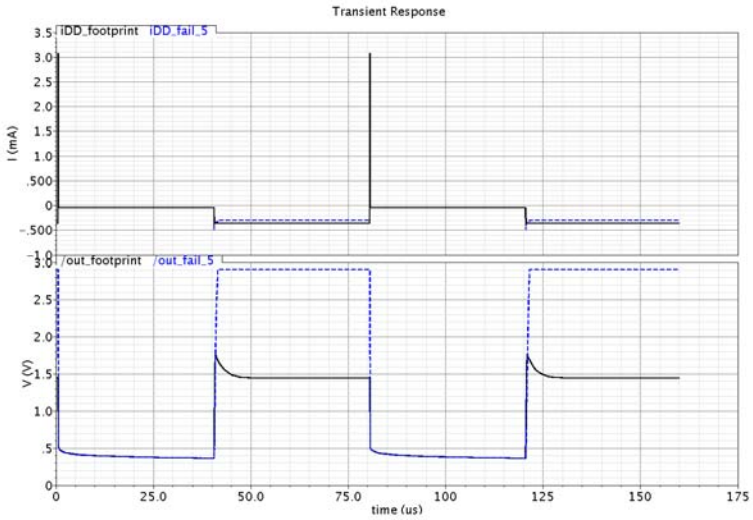

Figure 7–34: Possible fault #5 in the sensor circuit.

In case of fault #6 found the iDD current will look like figure 7–35.

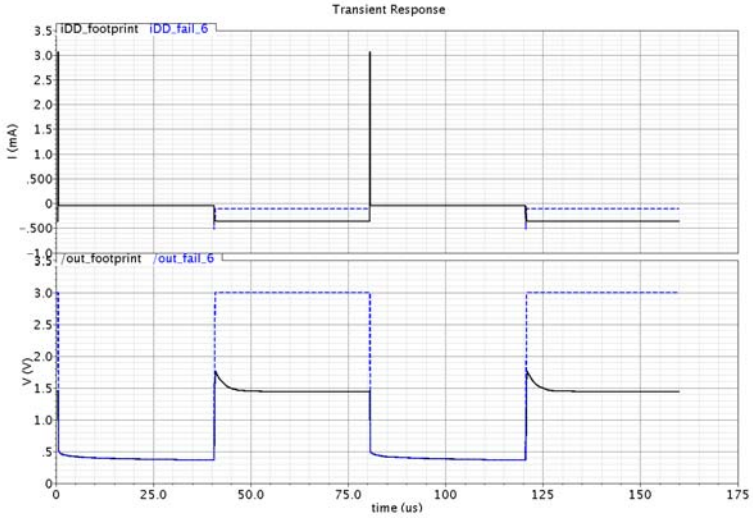

Figure 7–35: Possible fault #6 in the sensor circuit.

In case of fault #7 found the iDD current will look like figure 7–36.

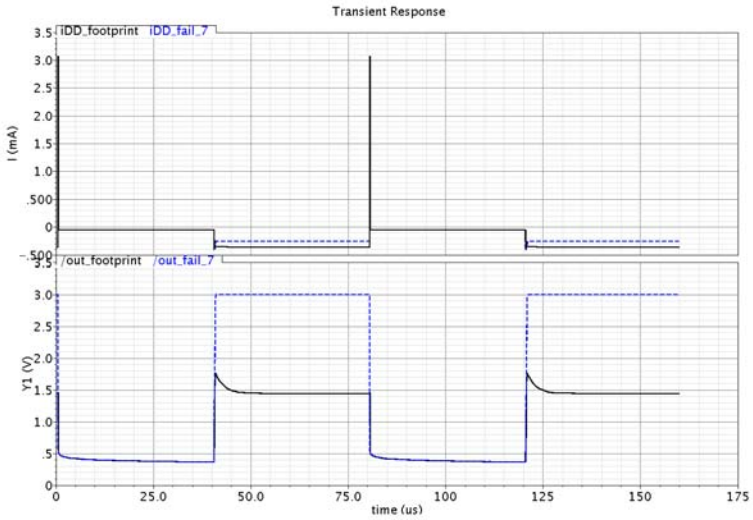

Figure 7–36: Possible fault #7 in the sensor circuit.

In case of fault #8 found the iDD current will look like figure 7–37.

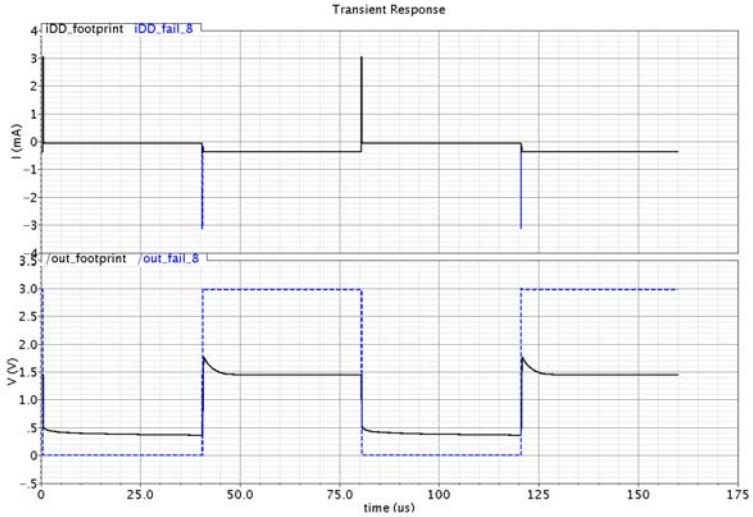

Figure 7–37: Possible fault #8 in the sensor circuit.

In case of fault #9 found the iDD current will look like figure 7–38.

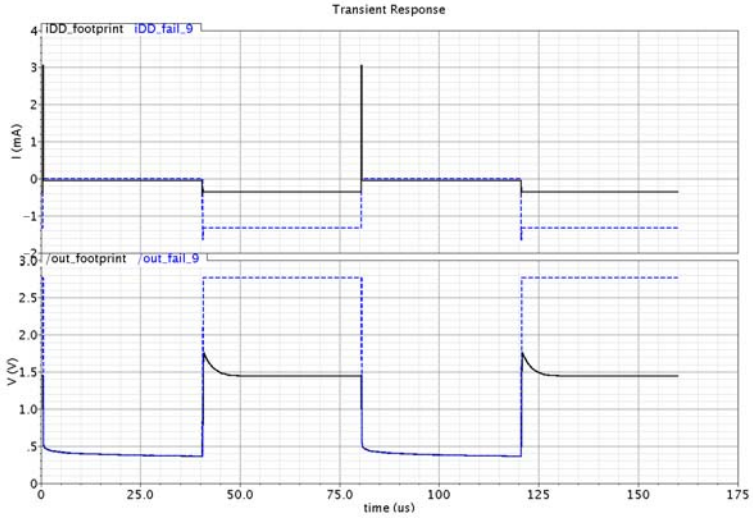

Figure 7–38: Possible fault #9 in the sensor circuit.

CHAPTER 8
CONCLUSION AND FUTURE WORK

8.1 Conclusion

Developed a methodology that through the use of available pad frame structures perform the iDD test. An iDD Built-in Current Sensor circuit was designed using Cadence 0.6 um. This new scheme helps in the early detection of catastrophic faults in CUTs thus, contributing in test time reduction because of advantage of removing such CUTs from the tester faster and allowing others CUTs to continue to be tested. This structure brings the advantages of being able to be used in the Vdd terminal or in the Vss terminal with-out introducing any devices between the terminals and the mission CUT.

8.2 Future Work

- Develop a test routine where the Vout pin can be shared with other pin, eliminating the need of this specific output pin. In other words to share this, Vout pad, with any other CUT pad that does not affect the iDD curve when being under tests.

- Create fault dictionaries for different failures encountered in circuits.

- Implement a programmable gain arrangement for controlling the gain according to the signal of interest.

APPENDICES

APPENDIX A
Current Mirror Circuits and Simulations

A.1 Input and Output Resistances Small Signal Analysis of Current Mirrors:

Simple Current Mirror

From the figure A–1 the Rin obtained using the absorption theorem [24] is Rin= $\frac{1}{gm}$.

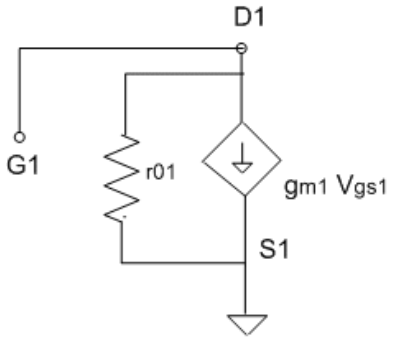

Figure A–1: Simple Current Mirror Small Signal Input Circuit

To calculate the output resistance Rout in figure A–2 a test voltage source (V_T) and test current (I_T) are used. Where the V_T/I_T relationship gives the output resistance as Rout= r_{02}.

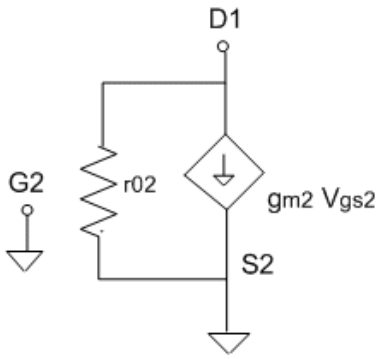

Figure A–2: Simple Current Mirror Small Signal Output Circuit

Fully Cascoded Current Mirror

To calculate the input resistance Rin a test voltage source (V_T) and test current (I_T) are also used . In this case the I_T equation is given by:

$$I_T = g_{m1}V_{gs1c} + \frac{Vtest-Vx}{r01c}$$

where: $V_{gs1c} = (V_T - V_x)$ and $V_x = \frac{Itest}{gm1+y}$; here y=$\frac{1}{r01}$.

By substituting these values in the I_T equation turns to be:

$$I_T = g_{m1c}V_T - \frac{Itestgm1c}{gm1+y} + \frac{Vtest}{r01c} - \frac{Itest}{(gm1+y)ro1c}; \text{ here } y=\frac{1}{r01}$$

Then solving this equation for $\frac{VT}{IT}$, Rin is obtained as = $\frac{2}{gm}$.

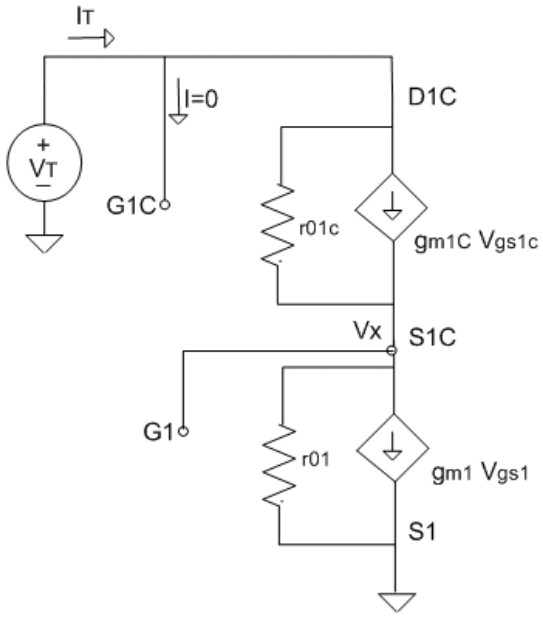

Figure A–3: Fully Cascoded Input Resistance

For obtaining the output resistance (Rout) a similar procedure is done. A (V_T) and (I_T) are also needed. Figure A–4 shows the small signal model.
In this case the I_T equation is given by:

$$I_T = g_{m2c}\ (-V_x) + \frac{Vtest - Vx}{r02c} \text{ and } I_T \text{ is also } = \frac{Vx}{r02}.$$

Solving for Vx; $Vx = I_T r_{02}$ and substituting this Vx in the previous I_T equation an expression for $\frac{Vtest}{Itest}$ is obtained as;

$$\text{Rout} = r_{02c} g_{m2c} r_{02} = g_m r0^2.$$

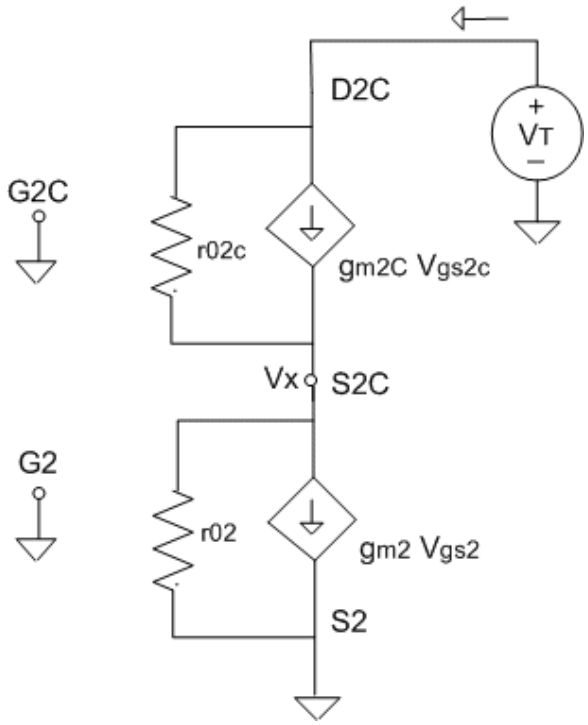

Figure A–4: Fully Cascoded Output Resistance

Low Voltage Cascoded Current Mirror

The small signal circuit for the calculation of the input resistance of a Fully Cascoded Current Mirror (FCCM) is presented in figure A–5. Here I_T is given by:

$$I_T = \frac{Vtest-Vx}{r01c} + g_{m1c}\ V_{gs1c}$$

and I_T is also:

$$I_T = \frac{Vx}{r01} + g_{m1}\ V_{gs1}$$

where: V_{gs1c} = 0-Vx and V_{gs1} = V_T-0. From the second I_T equation, solving for Vx you get = (- g_{m1} V_T + I_T)r_{01}. Now substituting this Vx in the first I_T equation and using algebraically manipulations and approximations the following $\frac{VT}{IT}$ relationship is found;

$$Rin = \frac{gm1cr01}{gm1cgm1r01} = \frac{1}{gm1}$$

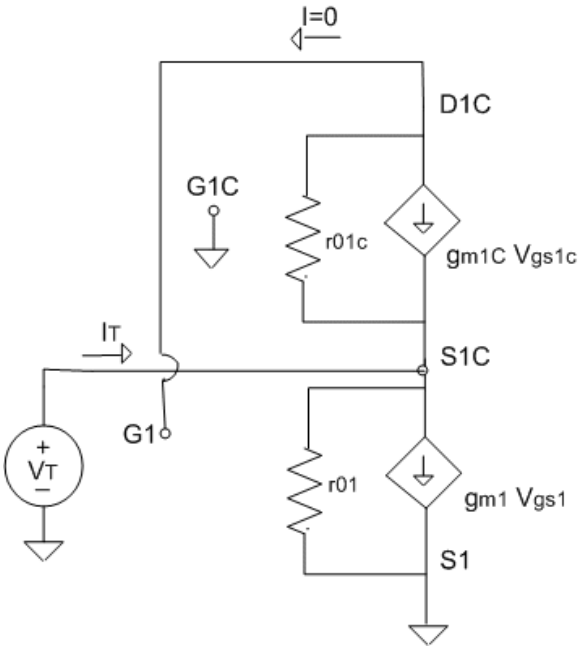

Figure A–5: Low Voltage Cascoded Input Resistance

The low voltage cascoded output resistance is calculated in the same manner as the fully cascoded output resistance.

A.2 Current Mirror Circuits: Schematic, DC and AC simulations and Layout

Circuits shown are: Simple Current Mirror, Cascoded Current Mirror, Low Voltage Cascoded Current Mirror

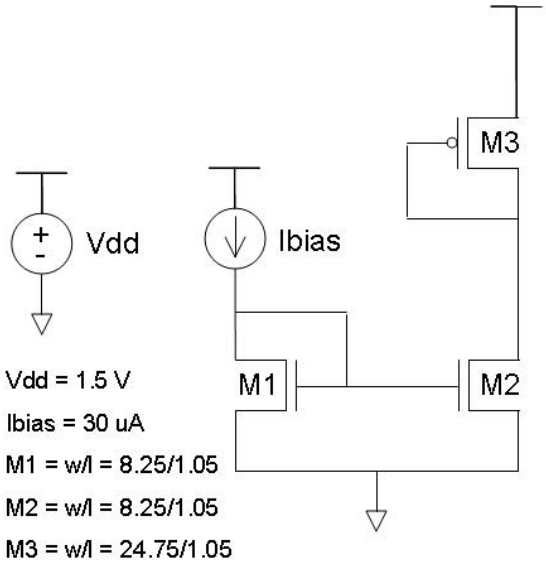

Figure A–6: Schematic of Simple Current Mirror

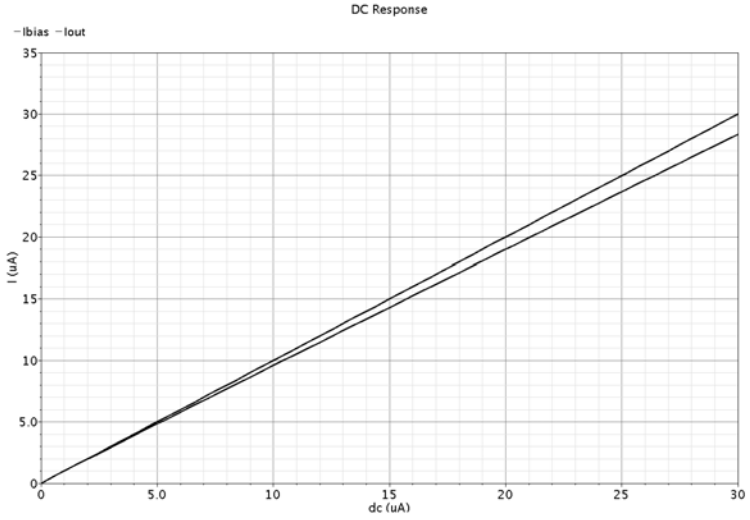

Figure A–7: DC Simulation of Simple Current Mirror

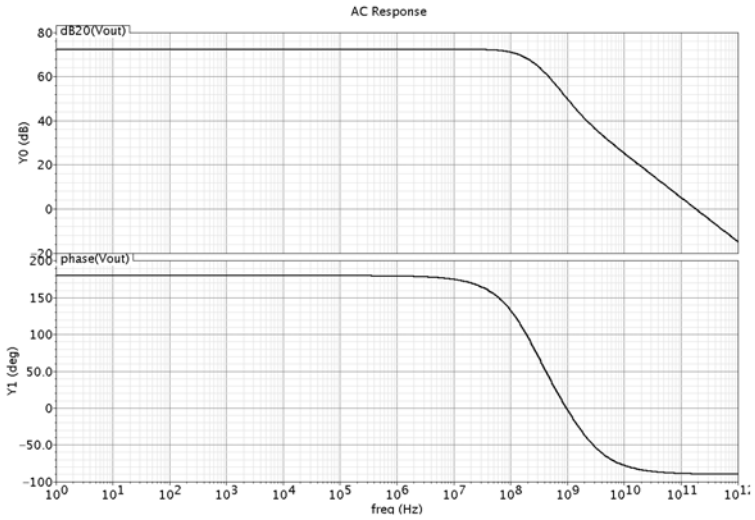

Figure A–8: AC Simulation of Simple Current Mirror

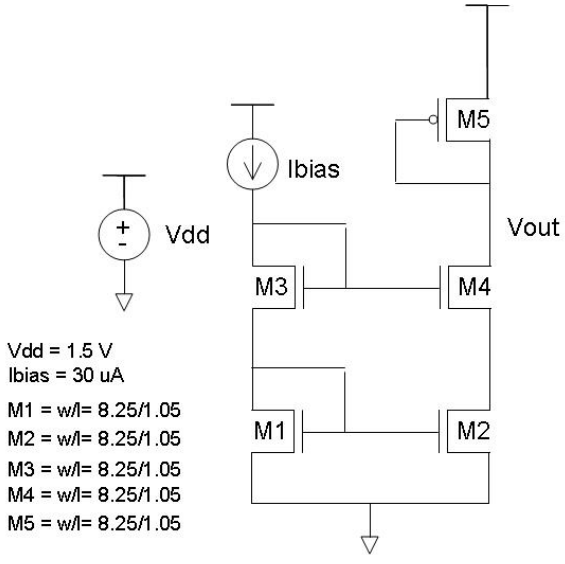

Figure A–9: Schematic of Cascoded Current Mirror

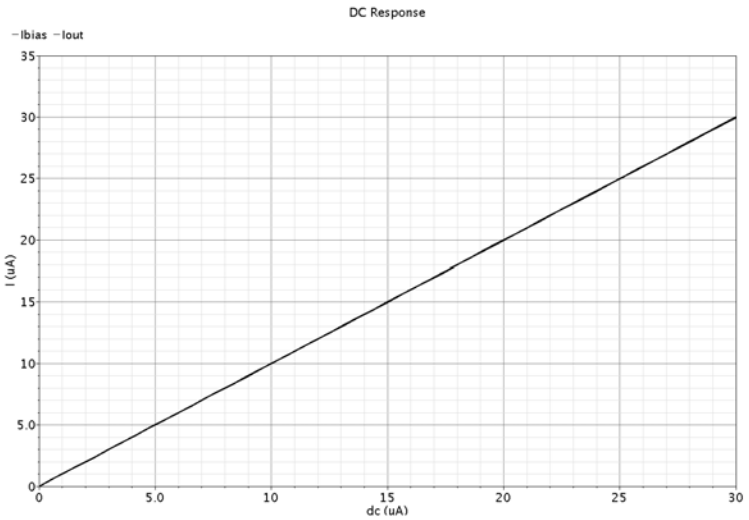

Figure A–10: DC Simulation of Cascoded Current Mirror

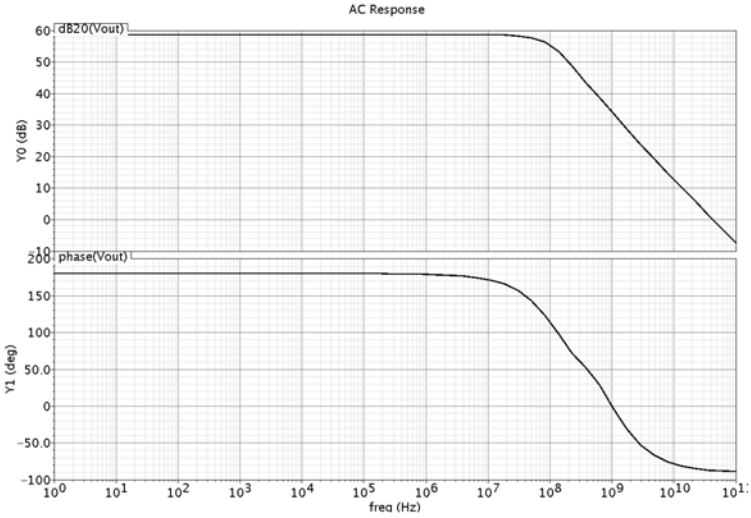

Figure A–11: AC Simulation of Cascoded Current Mirror

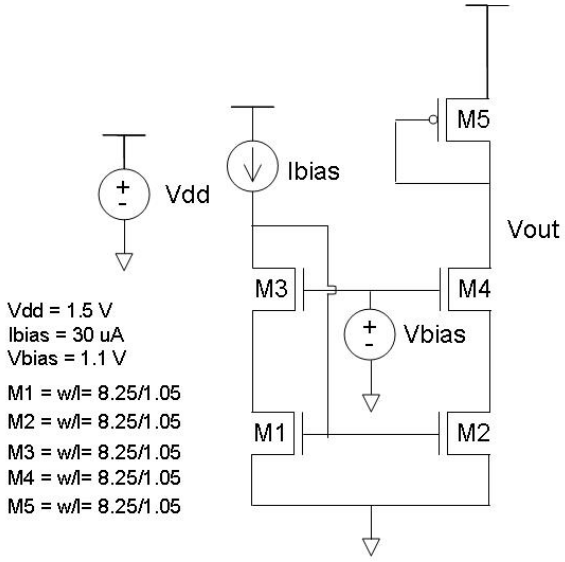

Figure A–12: Schematic of Low Voltage Cascoded Current Mirror

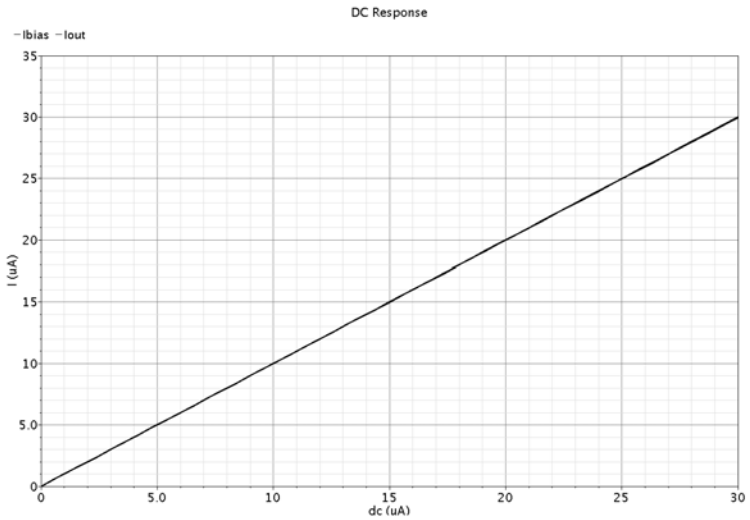

Figure A–13: DC Simulation of Low Voltage Cascoded Current Mirror

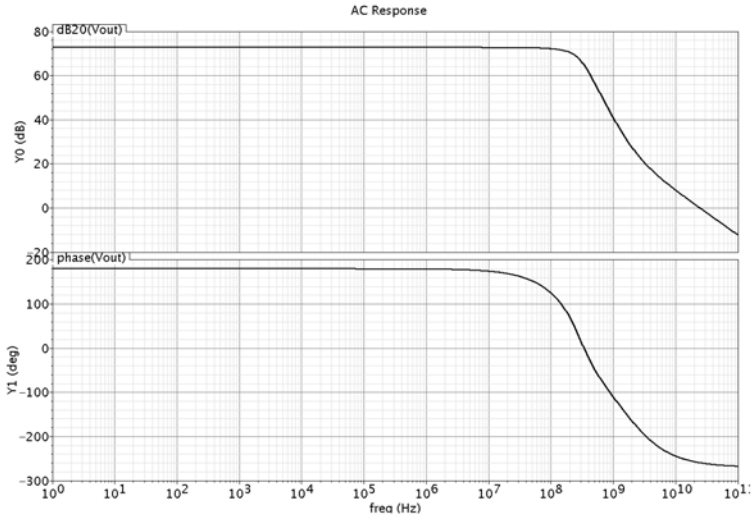

Figure A–14: AC Simulation of Low Voltage Cascoded Current Mirror

APPENDIX B
Differential Amplifiers Circuits and Simulations

B.1 Differential Amplifiers Circuits: Schematic, DC and AC simulations and Layout

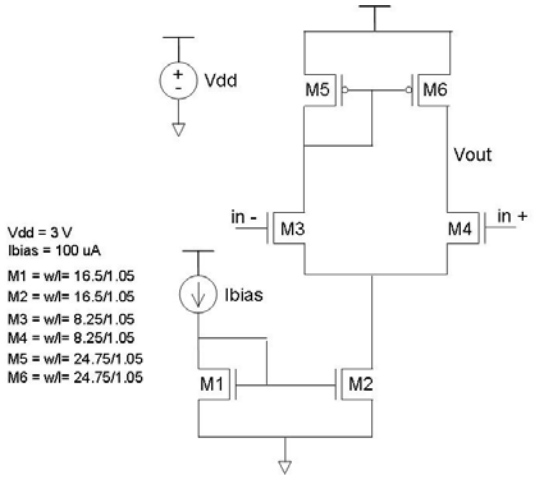

Figure B–1: Schematic of Differential Amplifier 1

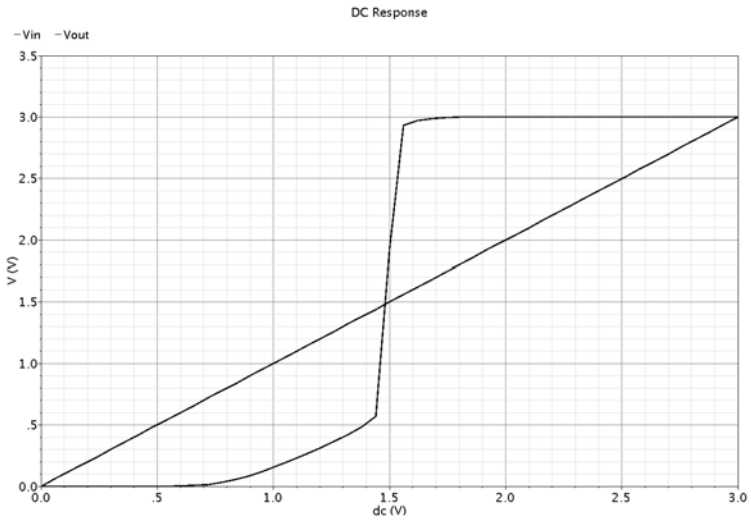

Figure B–2: DC Simulation of Differential Amplifier 1

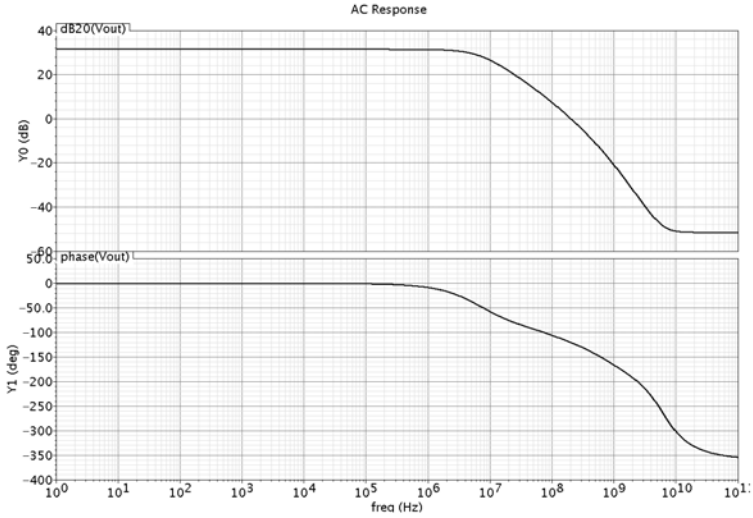

Figure B–3: AC Simulation of Differential Amplifier 1

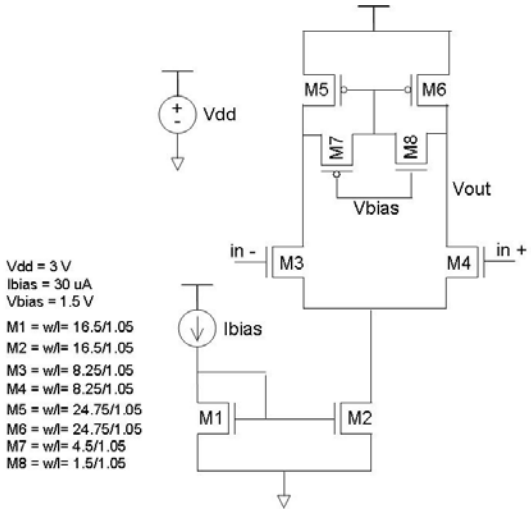

Figure B–4: Schematic of Differential Amplifier 2

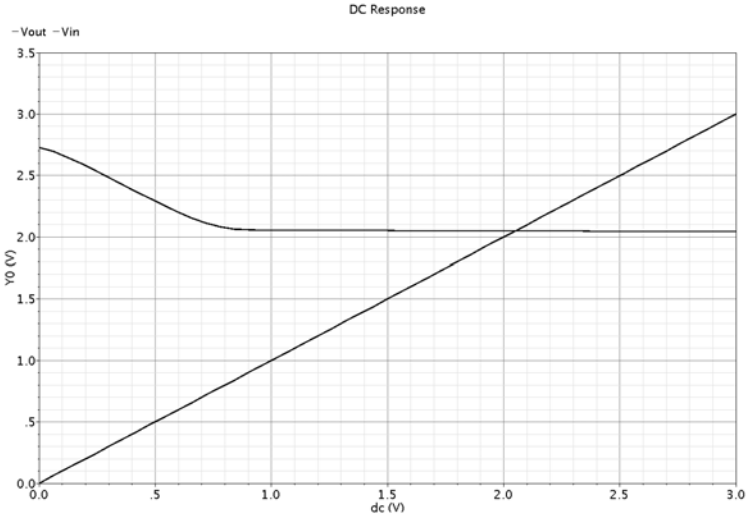

Figure B–5: DC Simulation of Differential Amplifier 2

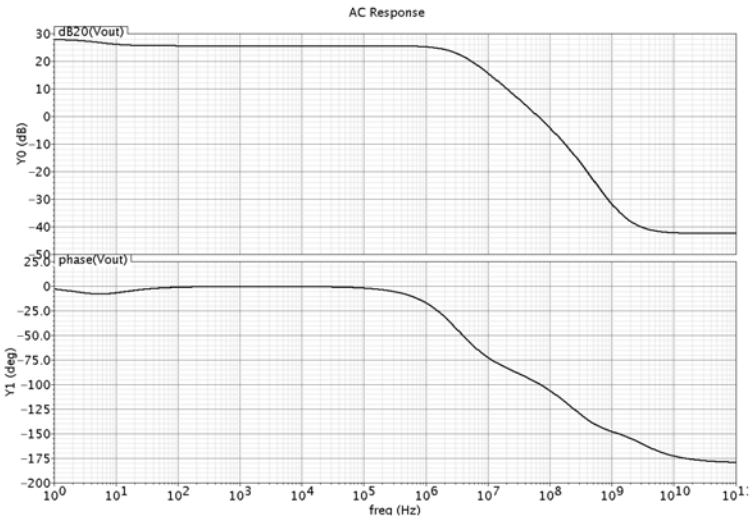

Figure B–6: AC Simulation of Differential Amplifier 2

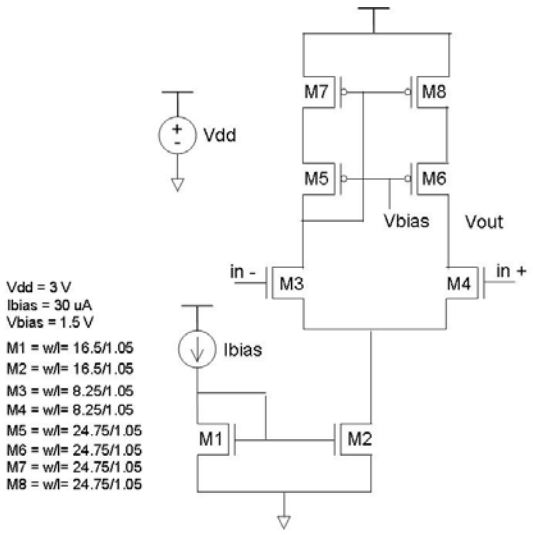

Figure B–7: Schematic of Differential Amplifier 3

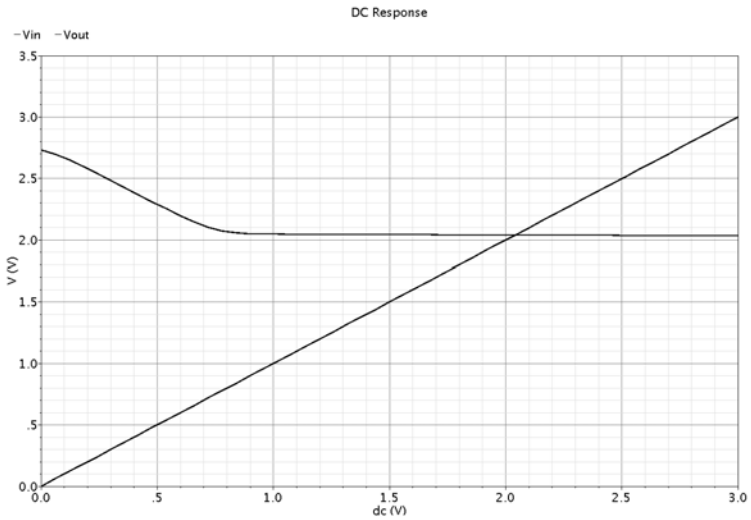

Figure B–8: DC Simulation of Differential Amplifier 3

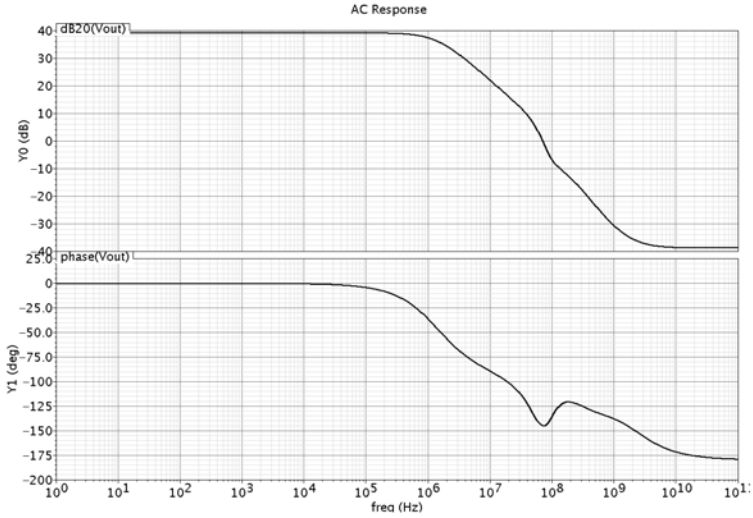

Figure B–9: AC Simulation of Differential Amplifier 3

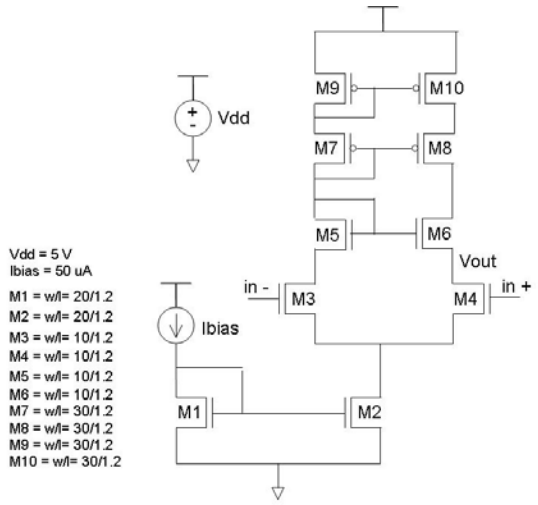

Figure B–10: Schematic of Differential Amplifier 4

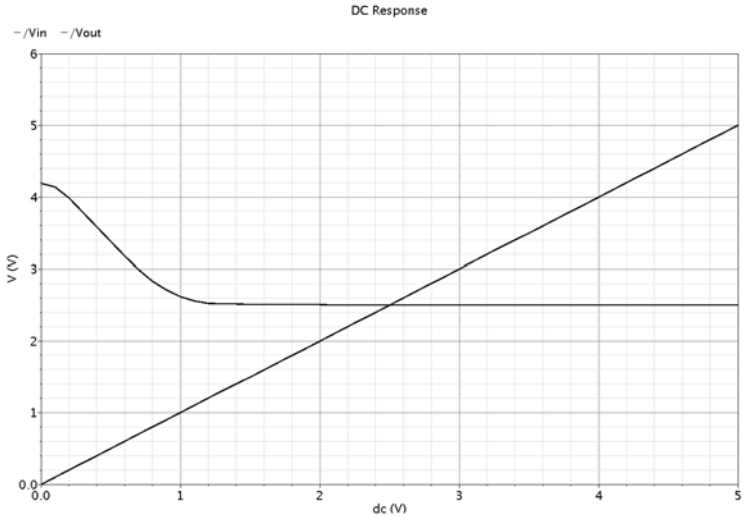

Figure B–11: DC Simulation of Differential Amplifier 4

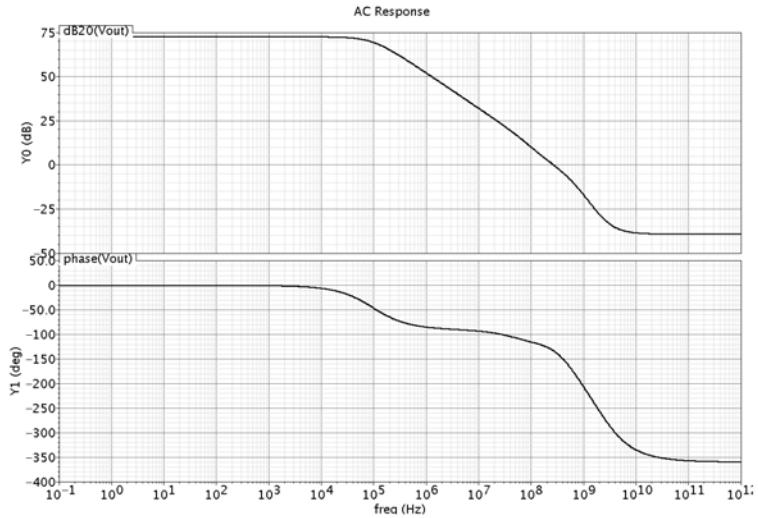

Figure B–12: AC Simulation of Differential Amplifier 4

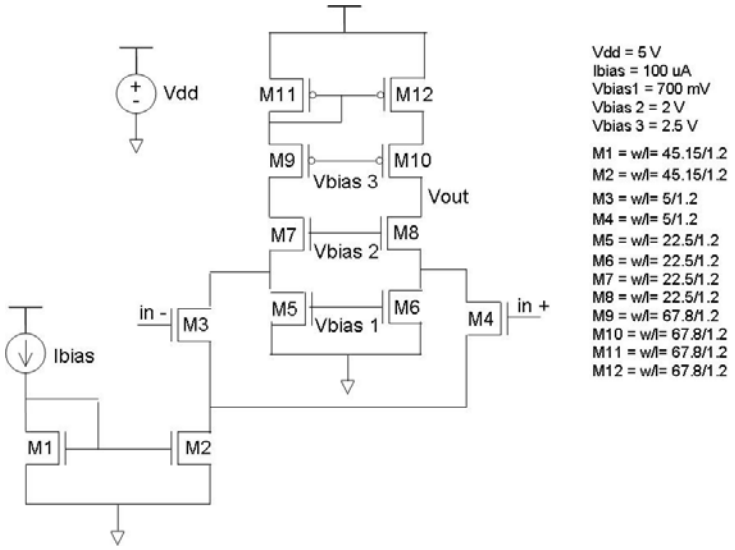

Figure B–13: Schematic of Differential Amplifier 5

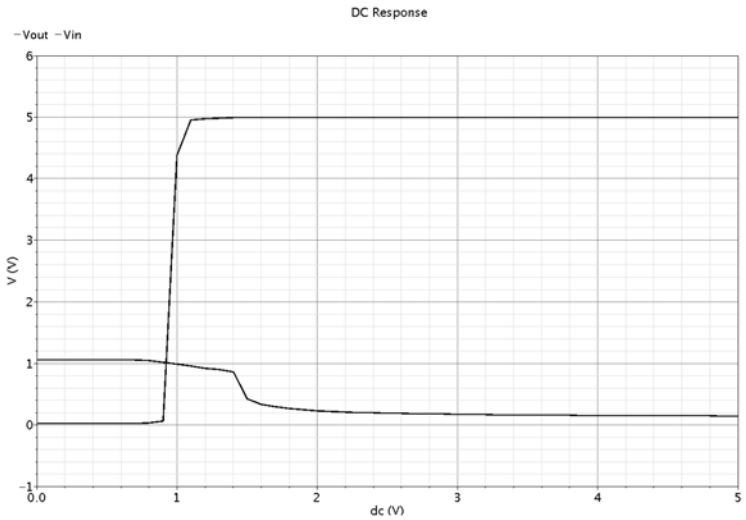

Figure B–14: DC Simulation of Differential Amplifier 5

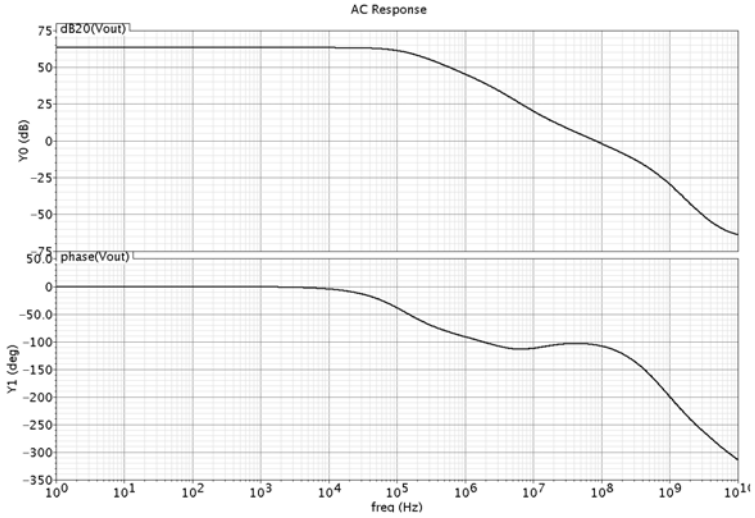

Figure B–15: AC Simulation of Differential Amplifier 5

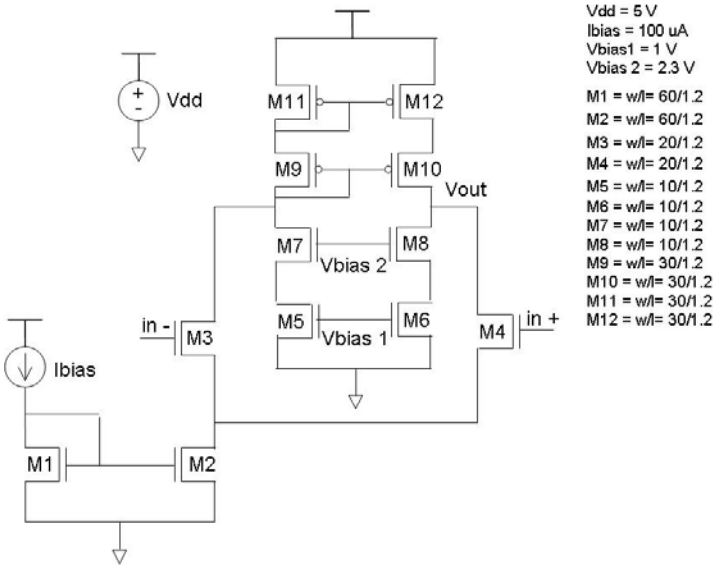

Figure B–16: Schematic of Differential Amplifier 6

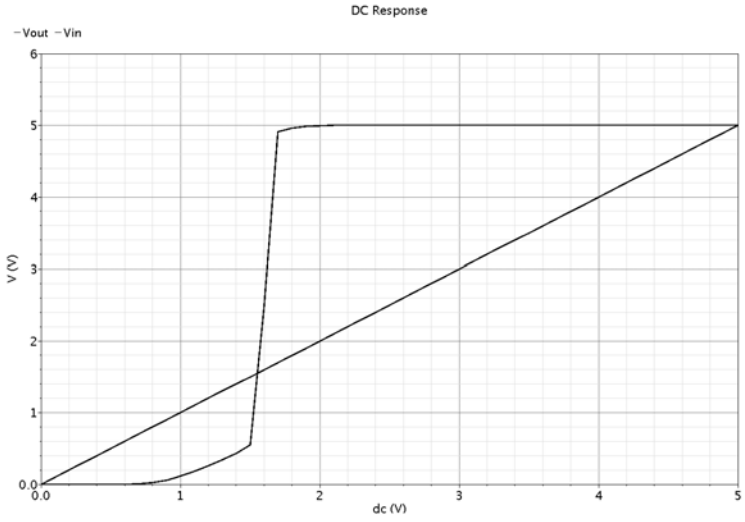

Figure B–17: DC Simulation of Differential Amplifier 6

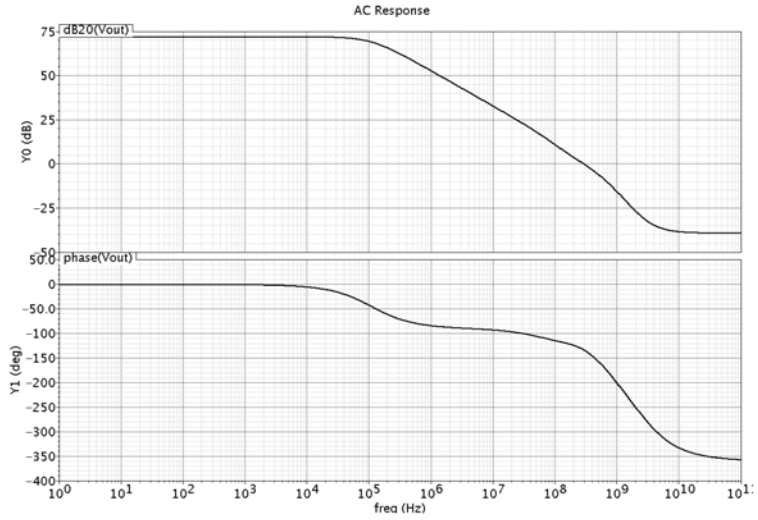

Figure B–18: AC Simulation of Differential Amplifier 6

APPENDIX C
LAYOUTS

Layout of different current mirrors previously discussed and presented in AppendixA.

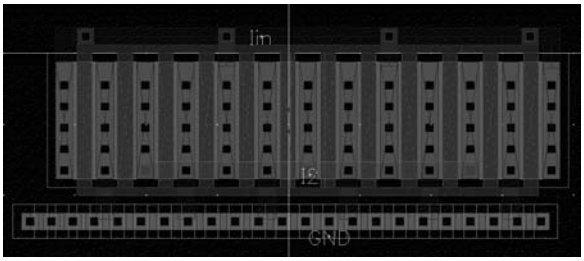

Figure C–1: Layout of Simple Current Mirror

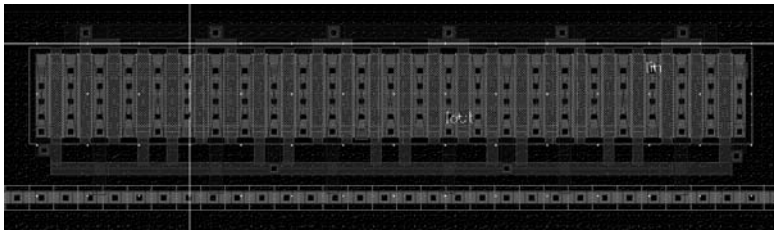

Figure C–2: Layout of Cascoded Current Mirror

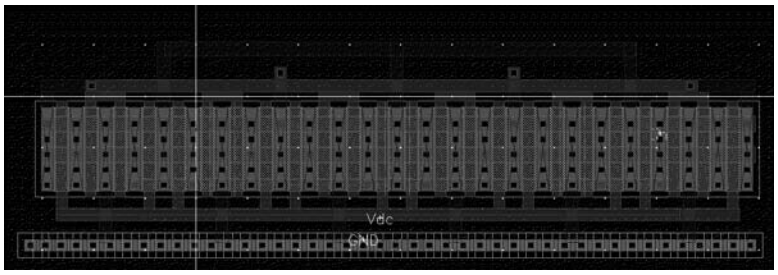

Figure C–3: Layout of Low Voltage Cascoded Current Mirror

Layout of different OpAmps previously discussed and presented in AppendixB.

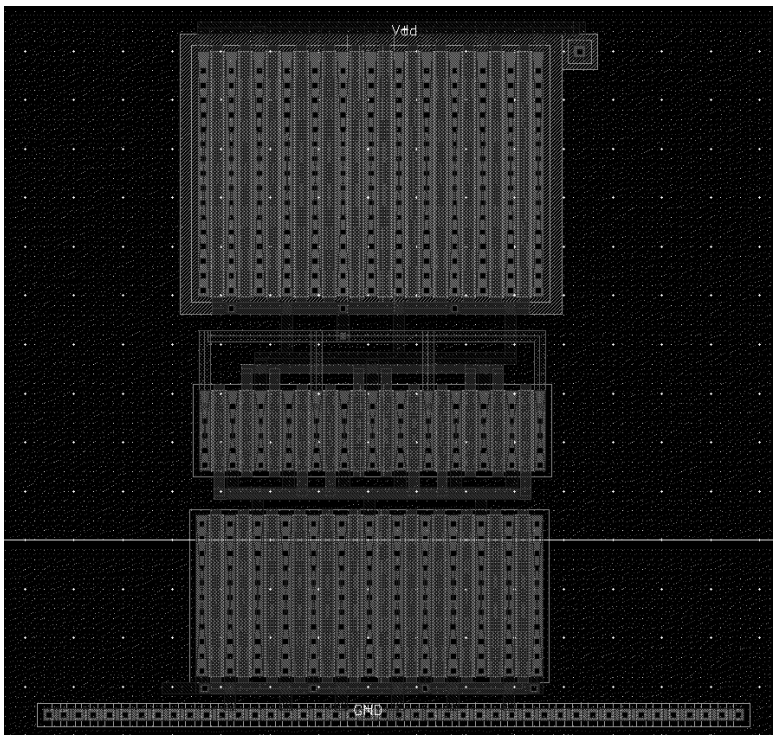

Figure C–4: Layout of Differential Amplifier 1

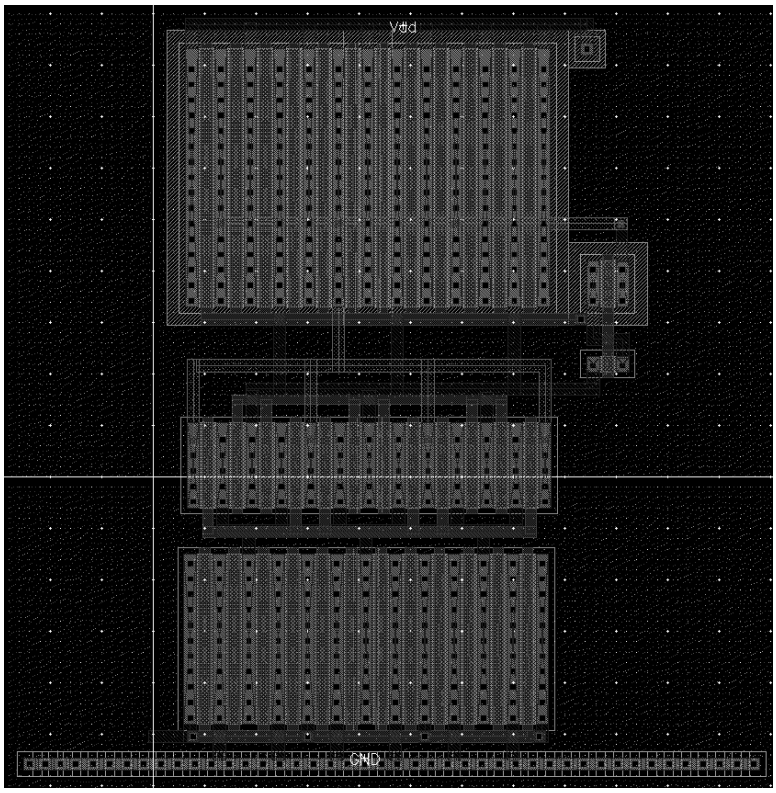

Figure C–5: Layout of Differential Amplifier 2

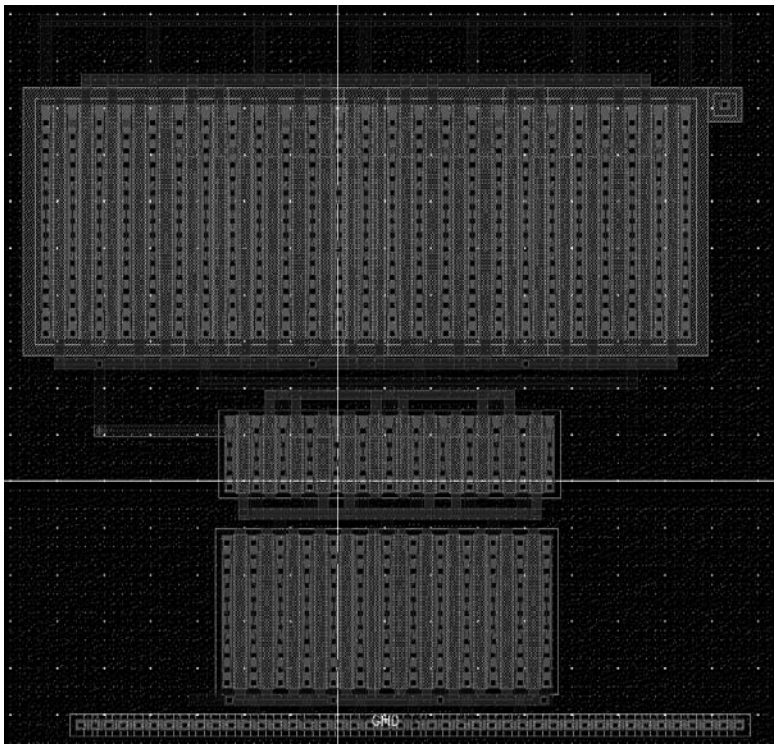

Figure C–6: Layout of Differential Amplifier 3

Layout of the designed Differential Amplifier (with-out the capacitor). Total area is 3,159.36 μm^2.

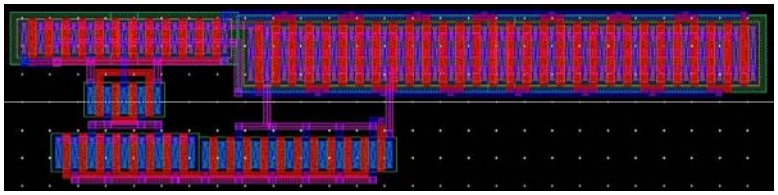

Figure C–7: Layout of the designed Differential Amplifier (without-the capacitor)

Layout of designed Differential Amplifier (with the capacitor).

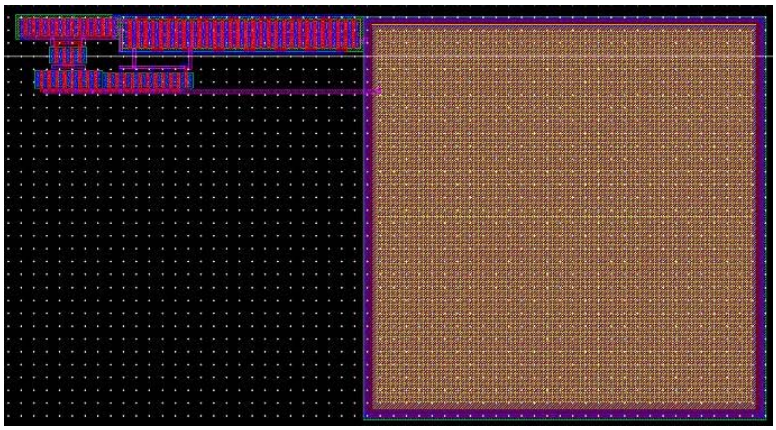

Figure C–8: Layout of the designed Differential Amplifier (with the capacitor)

Layout of a chip that was sent to be fabricated for characterization of metals, vias and poly layers.

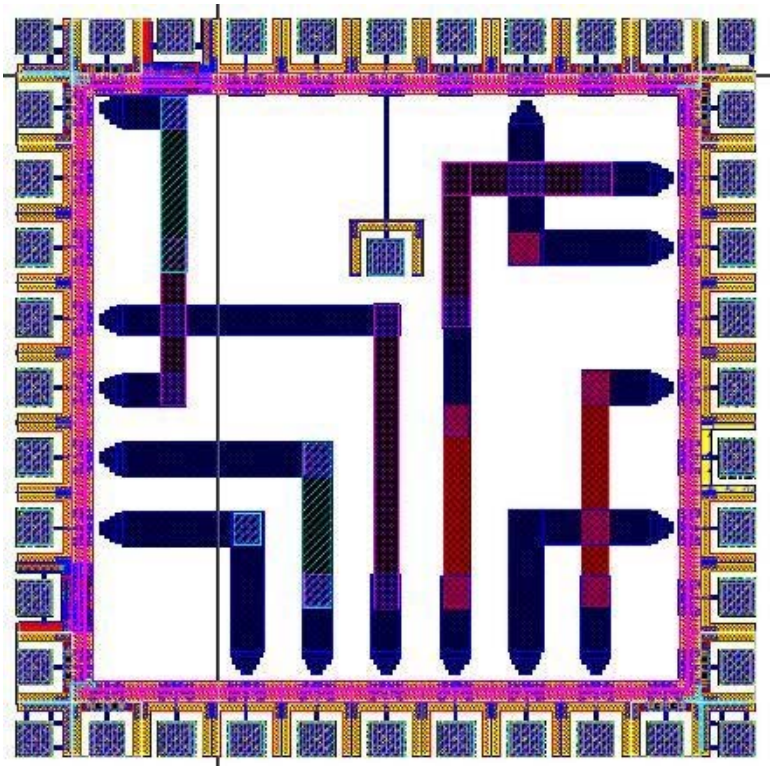

Figure C–9: Layout for characterization of metals, vias and poly

Layout of a chip that was sent to be fabricated for characterization of different transistors (NMOS and PMOS).

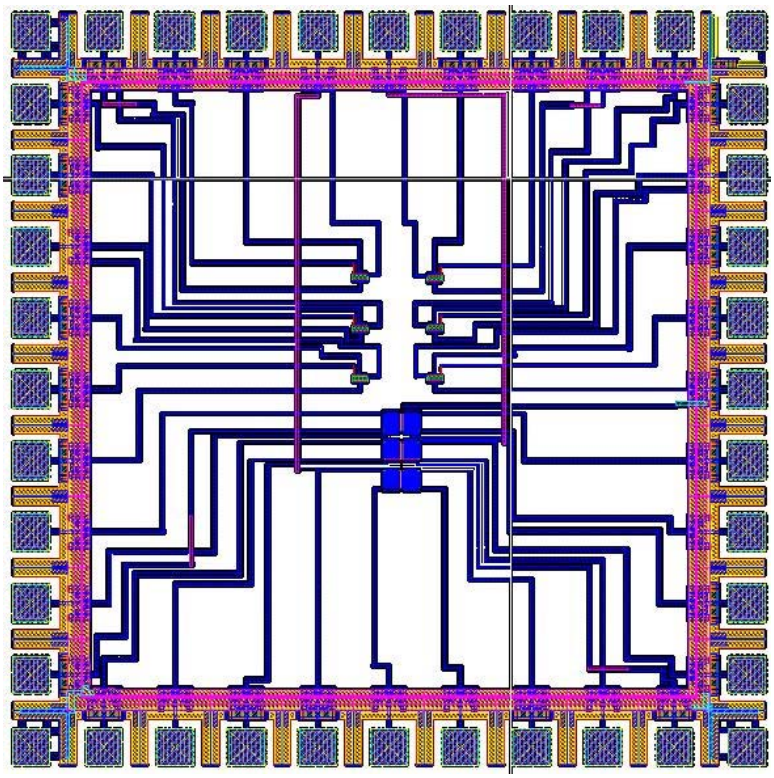

Figure C–10: Layout for characterization of different transistors

Sample of the fabricated chips that will be used to perform the characterization.

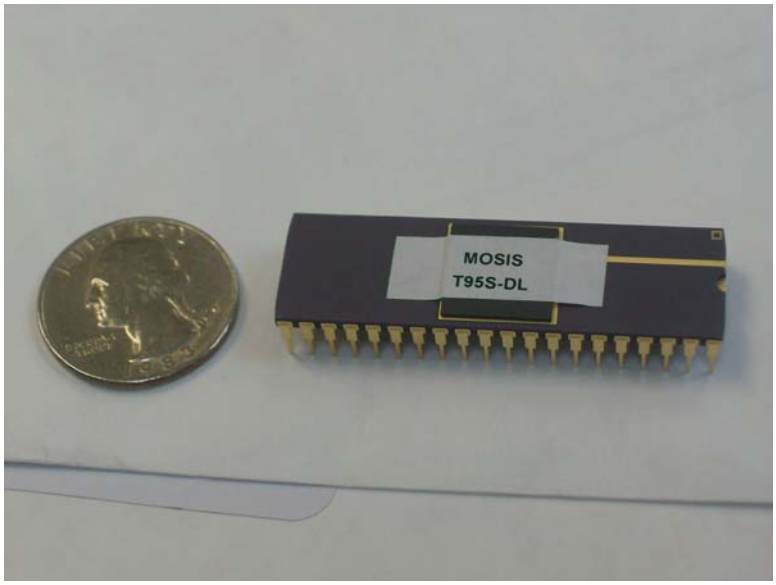

Figure C–11: Layout of the designed Differential Amplifier (with the capacitor)

APPENDIX D
LIST OF DEFINITIONS

1. **Input Offset Voltage:** This is the small voltage that exits in the output pin when both inputs are shorter together. This difference is corrected by applying a small voltage (input offset voltage) between the inputs until the Vout=0V.

2. **Total Power Dissipation:** It is the subtraction of the total DC power supplied to the OpAmp minus the power delivered by the OpAmp to the load.

3. **Power Supply Rejection Ratio (PSRR):** The PSRR is defined as the ratio of the change in supply voltage to the change in output voltage of the op amp caused by the change in the power supply. PSRR = $\frac{\delta VDD}{\delta VOUT}$. It represents a measure of the OpAmp ability to prevent that the output is affected by noise in the power supply. (units: dB)

4. **Common Mode Rejection (CMR):** This represents the ability of an OpAmp to amplify any differential input signal between both inputs rejecting any signal that is common between them.

5. **Input Bias Current:** This is the measure of the average of the currents into the two input terminals when the output is at zero volts.

6. **Open Loop Gain:** Ratio of output voltage vs. differential input voltage without any feedback.

7. **Slew Rate:** Represents the incapacity of an amplifier to follow fast input signal variations. Slew rate is defined as the maximum rate of change of the OpAmp output voltage for all possible input signals (maximum rate at which the load capacitance can be charged). In other words, the maximum operation frequency for a given output voltage. SR is given by: $|\delta\ V_{OUT}/\ \delta\ t|$max or I/C_L (units: V/μs.)

8. **Settling Time:** This is the time necessary for the output to reach a value within a certain tolerance.

9. **Input Offset Current:** It is the difference between the currents into the two input terminals when the output is held at zero.

10. **Output Offset Voltage:** It is the output voltage at the output terminal with respect to ground when both the input terminals are grounded.

11. **Output Swing:** To determine the output swing of an OpAmp a sinusoidal signal has to be applied to the inputs and by observing the output determine the maximum amplitude of the input sinusoidal that does not result in a distorted output signal.

12. **defect:** Physical error, a not desired change in a circuit's design or system due to fabrication process, eg. misaligments, a larger size capacitor, resistor or transistor.

13. **fault:** Manifestation of the presence of a defect. It is typically found when a part does not meet with the specifications. eg. something does not turn on. Failures could be global, parametrics or catastrophic.

14. **Global Failures:** These fails are seen through the entire wafer or lots of wafers. These fails are often because of different acid concentrations that lead to differences in the etching.

15. **Parametric Failures:** Failures that occurs inside the same die. A parametric failure does not necesarity causes a circuit to loss fuctionality but results have to be studied to analyze how these affect the specs limits.These fails are caused by defects associated with the fabrication process. eg, two different threshole voltages for two different transistors inside the same die.

16. **Catastrophic Failures:** Failures caused by defects usually associated with the fabrication process that completely affects the CUT functionality (typically short and open circuits). Usually captured by go/nogo tests or functional test. Open fails are typically caused by missing materials, misaligment and electromigration defects. Short fails are typically due extra material and not enought etching. These tests are typicaly run at the beginning of a test routine, discarding bad CUTs promptly thus saving test time.

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