ELECTRO-THERMAL MODELING
OF A POWER ELECTRONIC MODULE

By

José Miguel Ortiz-Rodríguez

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Approved by:

[redacted]
Manuel Jiménez, Ph.D.
Member, Graduate Committee
05/17/2004
Date

[redacted]
Krishnaswami Venkatesan, Ph.D.
Member, Graduate Committee
May 18, 04
Date

[redacted]
Miguel Vélez-Reyes, Ph.D.
President, Graduate Committee
May 14, 2004
Date

[redacted]
Héctor Méndez , Ph.D.
Representative of Graduate Studies
May 17, 04.
Date

[redacted]
Jorge L. Ortiz-Álvarez, Ph.D.
Chairperson of the Department
May 18, 2004
Date

ABSTRACT

An electrothermal model for a power electronic module is presented. The model is developed by representing the internal thermal behavior of the module as a RC network using an electrical circuit equivalent for the thermal heat conduction equation in one dimension. The physical characteristics of the module, like thermal properties of its constituents and all its dimensions, are used to subdivide its structure into a finite number of thermal components or nodes. To validate the model, two experiments were made: a train of high-power pulses was applied to obtain a fast-transient response of the innermost layers close to the semiconductor junctions, and a constant low-power level was applied to obtain a slow-transient response of different points located throughout the module plus its heat dissipation elements. Simulations performed with the module model showed an acceptable agreement with the acquired experimental measurements.

RESUMEN

Un modelo electrotermal para un módulo de electrónica de potencia es presentado. El modelo es desarrollado representando el comportamiento termal interno del módulo como una red RC usando un circuito eléctrico equivalente para la ecuación de conducción termal en una dimensión. Las características físicas del módulo, como las propiedades termales de sus constituyentes y todas sus dimensiones, son usadas para subdividir la estructura en un número finito de componentes termales o nodos. Para validar el modelo, dos experimentos fueron realizados: un tren de pulsos de alta potencia fue aplicado para obtener una respuesta de transiente rápida de las capas más internas cercanas a las juntas de los semiconductores, y un nivel constante de baja potencia fue aplicado para obtener una respuesta de transiente lenta para diferentes puntos localizados a través del módulo más sus elementos de disipación de calor. Simulaciones realizadas con el modelo del módulo mostraron una concordancia aceptable con las medidas experimentales adquiridas.

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LIST OF ACRONYMS

AHBC	**A**symmetrical **H**alf-**B**ridge **C**onverter
CAD	**C**omputer-**A**ided **D**esign
CPES	**C**enter for **P**ower **E**lectronics **S**ystems
DBC	**D**irect **B**ond **C**opper
DPS	**D**istributed **P**ower **S**ystem
EMI	**E**lectro-**M**agnetic **I**nterference
FDM	**F**inite **D**ifference **M**ethod
FEM	**F**inite **E**lement **M**ethod
GPIB	**G**eneral **P**urpose **I**nterface **B**us
IGBT	**I**nsulated-**G**ate **B**ipolar **T**ransistor
IPEM	**I**ntegrated **P**ower **E**lectronics **M**odule
MAST-AHDL	**M**odeling **A**nalog **S**ystems with **T**emplates – **A**nalog **H**ardware **D**escription **L**anguage
MCM	**M**ulti-**C**hip **M**odules
NIST	**N**ational **I**nstitute of **S**tandards and **T**echnology
PWM	**P**ulse-**W**idth **M**odulation
RCCM	**R**esistance/**C**apacitance **C**omponent **M**odel
RF	**R**adio **F**requency
SiC	**Si**licon **C**arbide
SMT	**S**urface **M**ount **T**echnology
UPRM	**U**niversity of **P**uerto **R**ico, **M**ayagüez Campus
VT	**V**irginia **P**oly**t**echnic Institute and State University

CHAPTER 1

INTRODUCTION AND RELATED LITERATURE

The vision of the Center for Power Electronics Systems (CPES) is to introduce the use of novel integrated systems as an approach to standardize power electronic components and packaging techniques in the form of Integrated Power Electronic Modules (IPEMs). Its goal as a research center is to achieve high levels of standardization by providing the basic building blocks necessary to develop more complex power systems. These building blocks are in turn customized for specific applications, by following a design starting from a predetermined set of specifications given according to present industrial and marketing needs. Once these IPEMs are developed, these industries quickly and effectively will provide their customers with a high level of customization and flexibility, giving them a competitive advantage.

A problem with model development process for power electronic systems is that the different analysis steps needed during this process usually require much time and need to exchange information to address different thermal, mechanical, electromagnetic, and electronic interactions present in the modules and components. CPES y seeking a solution for this time-consuming process by developing a virtual prototyping approach, where a main software tool controls the other different software tools dedicated to the analysis of the different physical interactions previously mentioned. This approach allows for parametric and other computed values exchange among the different simulation and analysis tools involved in the design process.

The purpose of this work is to present a method that can be applied to solve one of the most important analysis steps during the development of a new power electronic component: the development of its thermal model. Although there are tools that can find precise thermal profiles for a given component, they tend to be computationally expensive and do not provide for the appropriate thermal analysis under dynamic conditions needed for the fast model development needed by CPES. That is one flaw in the virtual prototyping approach that affects how the electronic and thermal models share

information during a dynamic simulation. Thermal models are a crucial part of every power design, because temperature-induced effects are deeply related to the electrical performance and overall reliability of such a high-power managing element. With a reduced order thermal model available for the IPEM, many systems that will use it as a building block can be quickly simulated an analyzed without the need to sacrifice valuable prototypes in experimental tests, and these models can show possible design flaws which can be corrected to improve the reliability and performance of the actual prototype.

The selected modeling method in this work was the use of an electrical RC network equivalent to represent the equivalent thermal behavior of the IPEM, based on the use of discrete thermal components. These components were determined from the geometric and material characteristics of the module, and coded as a device to be used in a circuit analysis environment, so it could be coupled with the electric circuit of the IPEM to allow for the simulation of a complete electro-thermal model. These reduced order models are also computationally faster than the 3D finite element modeling approaches of many thermal design and analysis tools, and are a better alternative for the virtual prototyping approach being followed by CPES.

1.1 PREVIOUS WORK ON THE IPEM PROTOTYPES DESIGN

Many tests have been performed to the CPES IPEM since its first prototypes were made, and it has been redesigned many times, always improving its characteristics and performance. Now that its physical design is almost complete, one of the final tasks still needed is to develop its electrothermal model in order to obtain more information about its physical limits and how it will react under simulation to extreme conditions.

To ensure the reliability and performance of the IPEM before being released as a final product to the power electronics community, it has been under constant analysis and redesign since its first prototypes were developed, using a variety of tools. A software system integration approach was proposed in [Chen et al., ‘01] combining (i) I-DEAS, (ii) Maxwell Q3D Parameter Extractor, (iii) SABER, and (iv) iSIGHT computer tools to

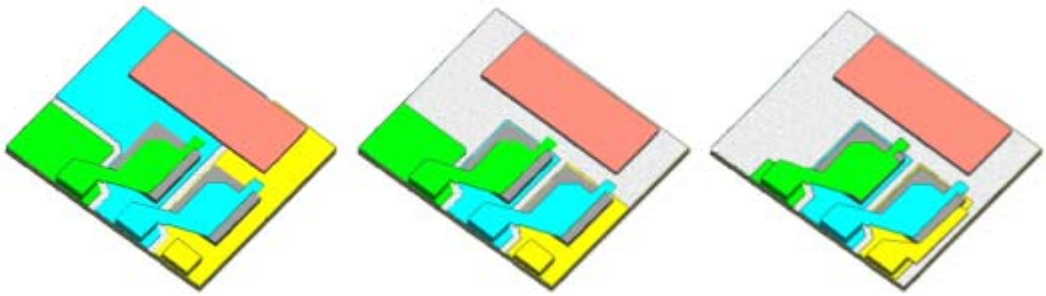
perform the necessary respective tasks of (i) mechanical modeling and analysis, (ii) electrical parameter extraction, (iii) electrical simulation, and (iv) program control and optimization. Figure 1.1 shows some of the prototypes that have been made during the last years of research. Figure 1.1 (c) is the most recent, being derived from (b) with just some small structural changes. Figure 1.1 (a) shows one of the earliest prototypes, which used wire bonding and had major structural changes since its design to become what is shown in Figure 1.1 (c). From the wire bond model in Figure 1.1 (a) subsequent models (b) and (c) used instead direct metallization layer contact connections. The first tests performed to these prototypes were dedicated mainly to find the best possible layout in order to reduce size without sacrificing its electrical performance.

(a) (b) (c)

Figure 1.1: Some of the different CPES active IPEM prototypes.

The process of IPEM manufacturing is explained in detail in [Liang and Lee, ‘01] and [Liang et al., ’03]-[,‘04]. Many trade-offs had to be made in order to comply with both goals due to the complex electro/thermal/mechanical interactions that arise inherently in such novel high-power-density designs. As an example, the two wire-bonded chips that can be seen in Figure 1.1 (a) are now completely embedded in the ceramic frame of modules (b) and (c). That major change is one of the reasons why prototype (a) was referred to as IPEM Generation I, and the ones with embedded semiconductors are referred to as IPEM Generation II. This second generation also had many changes. Notice how the gate driver was placed originally at the center in (b) and now is a little bit offset to the left. The module in (c) has now a polyimide coating on top, and the top copper traces are also wider. The gate driver connection leads located to the left (b) were also relocated in prototype (c). Generation II prototypes were also

redesigned internally many times. In fact, there are three models for this generation, referred to as A, B and C respectively. Figure 1.2 shows the reason for this referencing.



(a) (b) (c)

Figure 1.2: Different layout stages that identify the progress in the Gen. II IPEMs design.

To minimize the use of copper layering and specially the parasitic capacitances due to these close and wide conducting surfaces, the top copper portion of the DBC layer below the chips was reduced to a minimum from Gen. IIA to Gen. IIC [Chen et al., '02]. When electrical analysis also showed that it was necessary to include the bus capacitor to improve the output signal behavior, the top Cu layers on top of the chips had to be modified to provide more surface material to solder it to the IPEM leads. These changes can be seen in Figures 1.2 (a), (b) and (c), where the surrounding ceramic frame was removed to show the basic embedded elements in 3D.

The electrical structure of the active IPEM is that of a basic half-bridge, as shown in Figures 1.3 and 1.5. In terms of its physical components for thermal modeling purposes, the IPEM is quite simple: it consists mainly of two embedded power MOSFETs within a Al_2O_3 ceramic frame on top of a DBC layer, and a small gate driver circuit board composed of microelectronic components and chips attached to the module as an external SMT circuit, as shown in Figures 1.1 (a) to (c). In the first prototype the SMT gate driver is located to the left; in the other two it is located to the top. The MOSFETs are bare chips with 500V blocking voltage and a 24A current rating. They will be connected in such a way to create a half-bridge power stage structure with high- and low-side drivers that can be used as a standard component to implement more complex circuits. A schematic of this complete half-bridge structure for the active IPEM is shown

in detail in Figure 1.3. It was experimentally determined at VT that, as shown in the schematic, the total steady state power loss including conduction and switching losses was estimated as 19W for the complete half-bridge power stage: 12W were for the upper switch and 7W for the lower switch, this under typical working conditions. The gate driver dissipated 1W.

Most of the components shown in that schematic are part of the gate driver circuitry. Only the gate driver resistors *Rg1* and *Rg2*, and the bus capacitor *Cbus* are not included neither as an integral part of the gate driver SMT board nor the embedded MOSFETs structure. The bus capacitor can be easily seen on top of the IPEM structure in Figure 1.1 (c). A closer look of the hybrid gate driver components (but not connected to the resistors) can be seen in Figure 1.4. It consists basically of three chips (*U1, U2, U3* in Figure 1.3) for control processes and sensors, and discrete thin film coupling capacitors.

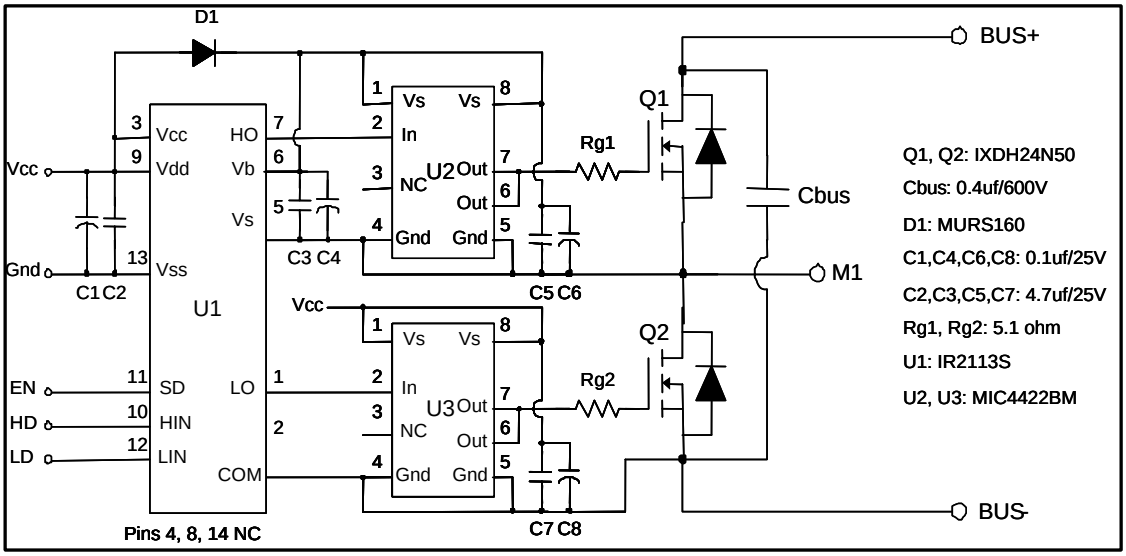


Figure 1.3: Schematic of the active IPEM.

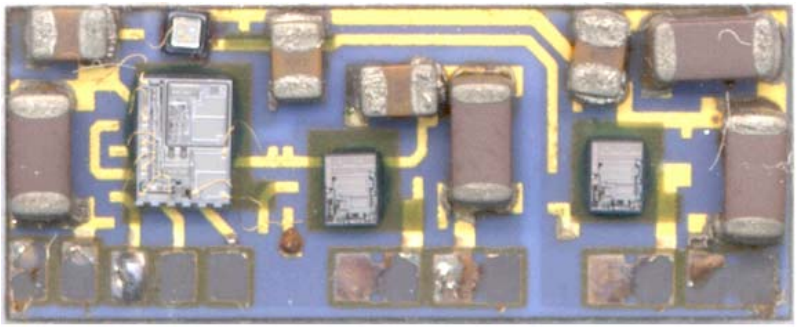


Figure 1.4: Close up of the gate driver showing its microelectronics circuitry.

The active IPEM is intended to work as part of a DC/DC converter having the specifications shown in Table 1.1 [Lee et al., '02]. A schematic of the proposed AHBC DC/DC converter being developed by CPES is shown in Figure 1.5, and an image of the actual device is shown in Figure 1.6. The specifications for the active IPEM are presented in Table 1.2. The intended operation of the 1kW DC/DC converter for DPS application is to have a 400V DC input bus voltage and 5A RMS current, operating at 200kHz.

Table 1.1
Specifications for the Proposed IPEM DC/DC Converter

Parameter	**Specification**
Input Voltage	300 V ~ 415 V
Output Voltage	48 V ± 10%
Output Voltage Ripple	480 mV
Isolation (output to GND)	> 10 kΩ
Output Power	1 kW
Operational Frequency	200 kHz

Table 1.2
Specifications for the Active IPEM

Parameter	Specification
DC Bus Voltage	400 V
Surge of DC Bus Voltage	415 V
Power Terminal Current	25 A
Junction Maximum Temperature	150 °C
Maximum Operating Junction Temperature	125 °C
Operating Case Temperature	-20 °C ~ +100 °C
Isolation Voltage	> 2500 V
Power Terminal Leakage Current	< 500 μA
Maximum Switching Frequency	500 kHz

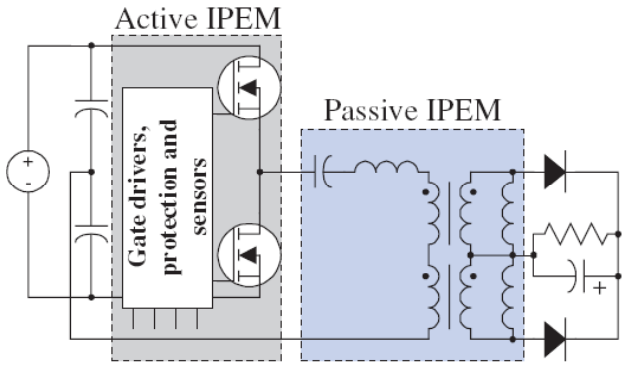


Figure 1.5: Schematic of an AHBC DC/DC converter based on IPEMs.

The passive IPEM, which is the central rectangular bulk in the converter shown in Figure 1.6, is also being developed with new planar technologies to improve its electrical characteristics and reduce its size. Details about its integration can be found in [Lee et al., '02]. The active IPEM circuitry can be seen placed in front of the device. These modular DC/DC converter prototypes have been tested to verify their electrical performance. Figure 1.7 shows a captured image of actual output waveforms under operational conditions [Liang et al., '03].

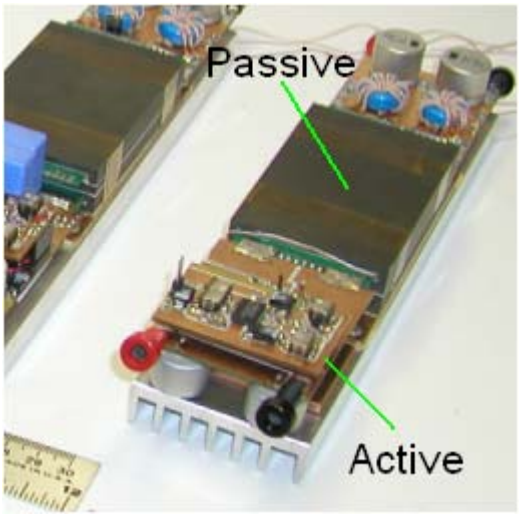


Figure 1.6: AHBC DC/DC converter. [Liang et al., '03]

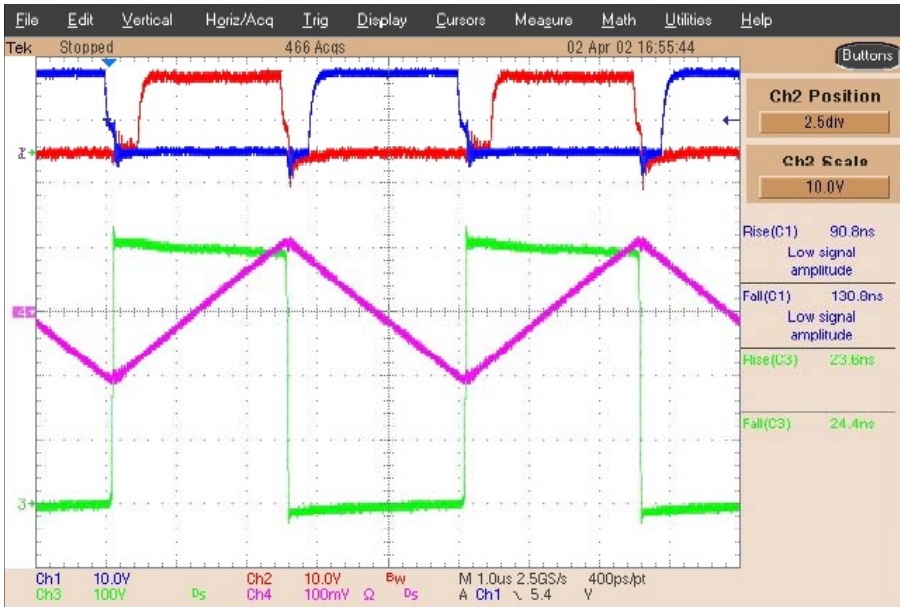


Figure 1.7: Output waveforms generated by the DC/DC converter with IPEMs. [Liang et al., '03]

1.2 PREVIOUS WORK ON THE IPEM THERMAL PROPERTIES

When the final prototype for the DC/DC IPEM (shown in Figure 1.1 (c)) was accepted, the next step in its design was to continue to analyze its reliability, especially its thermal behavior under full operational conditions. Different tools have been used to analyze the effect of thermal stresses in the embedded power module structure [Zhu et al., '03]. Some simulations were performed to analyze its thermal behavior through the use of specialized software tools, like FLOTHERM and I-DEAS [Chen et al., '00]. The IPEM thermal behavior was simulated and analyzed under different environments: being enclosed with cooling methods of forced convection [Liang et al., '04], free convection analysis, the use of different heat sink sizes (see Figure 1.8), the placement of components arranged in different locations of the cooling surface, etc. These results are presented in [Liang et al., '03] and [Chen et al., '00]. Samples of these results are shown in Figures 1.9, 1.10 and 1.11.

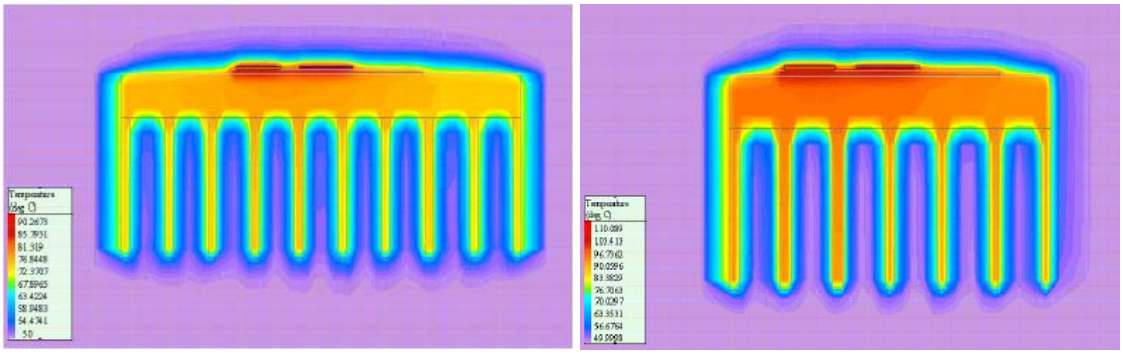


Figure 1.8: Different heat sinks FLOTHERM simulations used to analyze the IPEM thermal behavior. [Chen et al., '00]

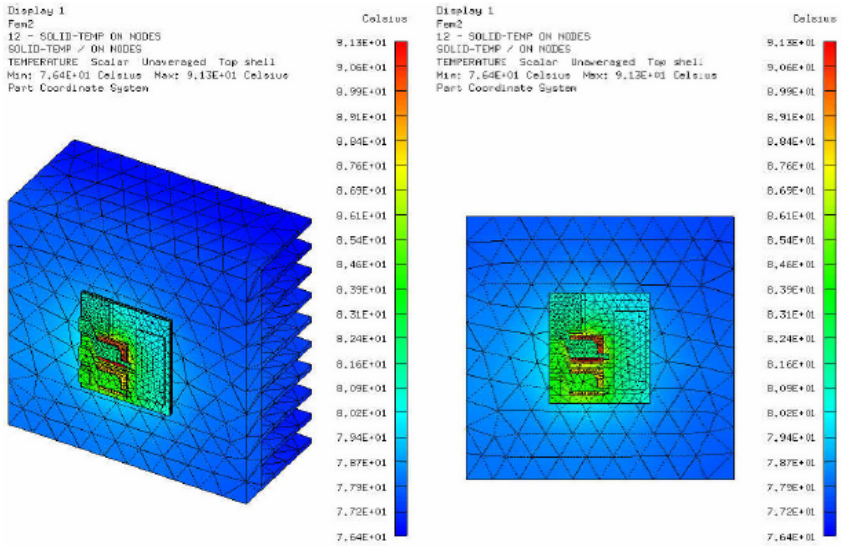


Figure 1.9: 3D temperature distribution at operational conditions simulated in I-DEAS. [Liang et al., '03]

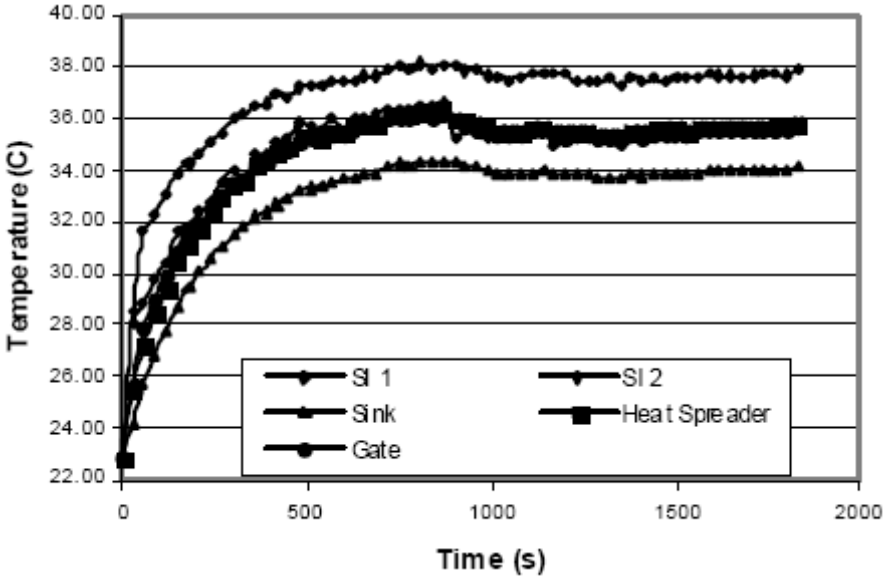


Figure 1.10: Slow-transient thermal results from VT tests. [Liang et al., '03]

As we shall see later, the experimental results shown in Figure 1.10 are very similar to the experimental results shown in Chapter 3 using the same method of measuring temperatures at various points in the IPEM with the aid of thermocouples. A description of that thermocouple experiment performed at UPRM is presented in Chapter 3. The only difference is that the VT experiment also included a measurement point in the heat sink structure, while the one performed at UPRM did not.

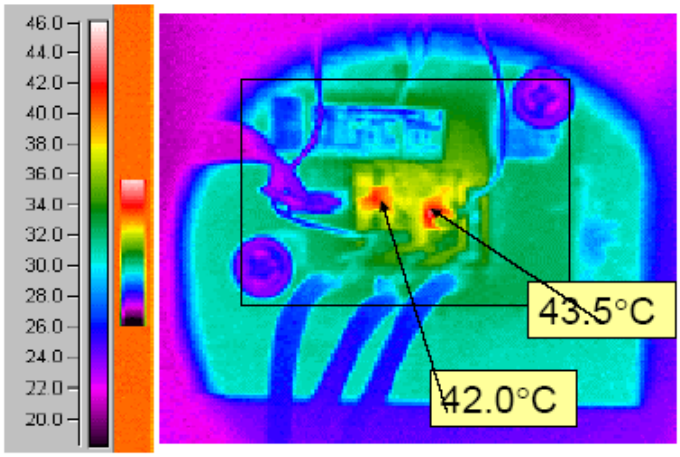


Figure 1.11: Thermal camera readings sample from the fully operational IPEM at VT. [Liang et al., '03]

The only problem with all the previous thermal tests performed to the IPEM is that none of them addresses the issue of what happens *internally* within the IPEM power stage structure itself. Although experimental characterization methods have been applied to verify the electrical parasitic components present in the internal IPEM structure [Yang et al., '03], the same has not been done from the thermal point of view. Most of the thermal measurements were taken on the surface of big elements like the heat sink and the heat spreader, which dominate the dynamics of heat transfer for slow-transient thermal behavior due to their shear bulk sizes, or on wide areas in contact with ambient temperatures and forced convection flows like the IPEM top surface.

The results shown in Figure 1.10 are showing the thermal behavior of the dominant dynamics of the heat sink. However, these measurements give no information about how the junction heat starts to spread within the different layers of the IPEM, how the heat being generated during the switching of one of the devices is affecting the other one, or which are the temperature gradients observed from the very small distance between the MOSFET junctions and the bottom Cu layer of the DBC. This is very important to analyze too because the power stage can be placed on top of different cooling arrangements, not necessarily the ones for which it has been tested. Modeling a complete recommended heat dissipation assembly does not necessarily provides enough information about the actual thermal behavior within the IPEM layers, except for slow-transient thermal conditions, like heating up to a steady room temperature after being

turned on for a while. In that case it is presumed that the whole IPEM is slowly warming up uniformly as the heat sink sets the whole assembly to a final steady state.

Apart from the temperature measurement problem, the fact that the IPEM is to become a standard module for future developments and designs implies that a fast model of its electro-thermal characteristics should be developed, as it has been done with many discrete power devices in the past once they have been introduced to the market. Being still a prototype under development, no model has been made for the CPES IPEM yet. Simply assembling a circuit similar to the one presented in the schematic in Figure 1.3 can simulate its electrical characteristics if needed. There are several power MOSFETs models and gate drivers already included in circuit analysis tools software libraries such as in PSpice, Cadence, SABER, etc. Nevertheless, the special thermal characteristics that the novel embedded IPEM structure possesses cannot be easily represented with the use of those discrete library components, even if they have their own electro-thermal equations integrated in their electrical response behavior. These equations usually represent the response of the discrete component under the ambient temperature influence, but have no way to incorporate thermal coupling with a nearby element attached to a different electrical network, or how to represent its thermal behavior if the element is surrounded in a non uniform way by layers of different materials with dissimilar thermal properties.

So, it is necessary to develop a method to represent, in a reliable way, the actual internal thermal behavior of the CPES IPEM under conditions other than the slow-thermal transient responses already analyzed. Excessive power being applied at a fast rate can burn the IPEM silicon devices before slow-transient models could show any potential thermal threat. If a good model is developed to show the actual internal thermal behavior of the embedded power stage under fast-transient high-power conditions, any potential hazard due to overheating could be detected with simulations, instead of sacrificing valuable prototypes.

1.3 PREVIOUS WORK ON POWER ELECTRONIC DEVICES MODELS

In order to develop a reliable electro-thermal model for the CPES IPEM, we will follow a general procedure suggested by many authors: (1) an experimental test should be performed to the IPEM to get enough data to obtain a precise temperature profile of its internal structure, and (2) a proven methodology to develop a computational model for a power device based on such data should be applied.

The first step depends on what type of profile we can get depending on the kind of test to be performed. In the case of the IPEM, the critical junction temperatures are specified in Table 1.2 for our module. Those peak temperatures will decrease as the generated junction heat is dissipated throughout the IPEM structure and towards the cooling assembly. It has been demonstrated in previous works like [Berning et al., '03] that one of the most recommended methods to generate a junction temperature profile for a power electronics device is to apply a train of high-frequency high-power pulses to it, or some other equivalent induced transient methodology like the one used by [Bagnoli et al. (a), (b), '98]. The purpose of the high-power pulse in Berning's work is to generate enough heat to get a noticeable temperature profile, usually trying to get temperatures as high as possible without overheating the device. On the other hand, the purpose of the high frequency is precisely to ensure that the effects of such high-power pulses stay on only for a very small fraction of time, enough to generate an optimal amount of heat, but avoiding overheating conditions.

Other works have also used thermal transient data to determine models for other semiconductor devices and power modules. In [Sofia, '95] the author develops a simple synthetic RC model for a packaged semiconductor from thermal step-response data, and suggests that simulation under non-uniform power conditions can completely describe the thermal performance of the device. The use of square-wave input with varying duty cycle is recommended because of being a typical power electronics waveform.

In [Yun et al., ‘01], the static and dynamic behavior of an IGBT module system mounted on a water-cooled heat sink is analyzed. They emphasize that, although 3D FEM analysis delivers very accurate results, an equivalent RC thermal network (RC Component Model (RCCM)) can predict the numerical solutions of the 3D FEM. The uniqueness of the RCCM is the introduction of the time constants based on the Elmore delay, which represents the propagation delay of the heat flux through the physical geometry of each layer. This offers insight into the physical layers and enables designers to couple the thermal prediction with a circuit simulator to analyze the complete electro-thermal behavior of the module. An electro-thermal model of the IGBT module simulated in SABER is presented.

Different thermal model approximations for the electro-thermal simulation of power semiconductor devices were compared in [Ammous et al., ‘99]. Useful analysis about the choice of the thermal model circuit networks is given. The discretization of the heat equation using FDM and FEM approaches is compared to obtain an analytic model developed by applying an internal approximation to the heat diffusion problem. The author emphasizes that his study on the adequate model selection is advantageous particularly for large surges of short time duration.

Typically, thermal effects are generally assumed static when circuits are designed, but in [Storti-Gajani et al., ‘01] the authors investigate some cases where the thermal and electrical quantities may have a strong nonlinear dynamic interaction, which could create “unexpected” oscillations. A mixed state-variable approach for common semiconductor devices embedded in simple circuits is used to show how the nonlinear effects may be significant in the analysis and design of many circuits.

In [Wünsche et al. (a), (b), ‘97] the authors present the use of different simulation tools coupled together so they can interchange calculated values to develop an electro-thermal circuit simulation for an integrated circuit. The interesting point is that the technique used is to couple ANSYS, which is a FEM computational tool, with SABER, a circuit simulator. SABER and ANSYS have the capability to send and receive calculated values from each other, and the method used was based on an automatic time step

algorithm, which is different from other known simulator couplings. The thermal modeling of the die/package structure and the extended modeling of the electronic circuit were discussed.

The analysis of the thermal behavior of an IGBT subjected to short power pulses of high amplitude is presented in [Rouve et al., '94], and the developed model is compared with simulations and experimental results. In this case, the applied power injections only last a few hundreds microseconds, so that heat does not have enough time to spread within the whole IGBT structure, but can damage the junction by overheating if not restricted. To test the validity of the model, electrical thermally dependent parameters were studied: the p-n junction threshold voltage V_o, and the gate threshold voltage V_{GSth}. A current impulse of 250 A heated the device during 470μs for the tests involving V_o, letting a low 5mA current cross the device to check the fall of temperature in the p-n junction. To test V_{GSth}, a power step of 30V – 20A is applied during 100μs to evaluate the temperature evolution in the inversion channel. The authors also make some tests and simulations under short-circuit conditions.

Another work related to the analysis of instantaneous junction temperatures for high-power devices is presented in [Profumo et al., 99]. In this work, high-power diodes are evaluated during current transients. First, the device transient impedance was obtained. Then it was reduced to a finite series of independent RC cells or nodes to obtain a thermal system transfer function based on the linearity properties of RC networks. Performing surge tests on the actual device and comparing the measured results with the simulated ones are used to validate the model.

Works on the dynamic electro-thermal modeling of power semiconductor devices, mostly for the IGBT, are presented in [Hefner and Blackburn, '93], [Hefner, '94], [Hefner and Blackburn, '94], and [Hefner and Diebolt, '94]. Dr. Hefner was one of the first researchers to perform a deep analysis on the electro-thermal behavior of the IGBT. Many of his power device models are now included in the libraries of circuit tools, like SABER. In this work, he couples a temperature-dependent IGBT electrical model with dynamic thermal models of the IGBT silicon chip, packages and heat sinks. These

dynamic thermal models are referred to as *thermal components*, and are derived from heat dissipation equations that are coded as templates in the SABER environment in order to create discrete library elements. These components can be connected to form a thermal network in the same way that electrical components are connected to form a circuit. The model was implemented in the SABER circuit simulator and the thermal network components were verified for a range of power dissipation levels important for power electronics systems. With his IGBT models, other more complex power electronics systems have been modeled using his thermal component approach, like the PWM inverter validated in [Mantooth and Hefner, '97].

An electro-thermal model of a PiN diode following the approach of [Hefner et al., '94] for the IGBT is presented in [Mawby et al., '01]. This type of diode can act as a variable resistor at RF and microwave frequencies. A physics-based compact electro-thermal model is developed and implemented in a circuit library as a component with thermal and electrical nodes in SABER, following Hefner's procedure for the IGBT. A SiC PiN and merged PiN Schottky power diode electro-thermal models also derived following Hefner's methods are presented in [McNutt et al., '01]. The dynamic electro-thermal models were implemented also in the SABER circuit simulator. In [Digele et al., 97] another fully coupled electro-thermal simulation on chip and circuit level is presented following similar approaches. The nonlinear thermal conductivity temperature dependence of silicon is taken in account to solve the nonlinear heat diffusion equation. An electrical current control circuit, built into a multi-watt package, is used to illustrate the electro-thermal simulation response using the SABER simulator. In this case, the author uses 792 thermal nodes for its model.

Hefner's approach was used in [Rodríguez et al., '02] to model a high power commercial IGBT module. The same physical-based thermal components modeling approach suggested by Hefner was used, and a computer-based system for experimental validation and calibration suitable to analyze other thermal models of multi-chip power electronics modules was developed [Parrilla et al., '02]. The experimental validation was for the slow-transient thermal behavior of the module. The developed test bed has the ability to select from an array of thermocouples which signals are of most interest to the

designer, and allows for performing a controlled test were the user can set the duration of the measurements and the sampling frequency. Depending on how the thermocouples were located in the module or modules, the user can also select to take measurements from the IGBTs only, the power diodes, or both. This environment was developed using GPIB instrumentation and a custom user interface was designed to manage the different measurement components. Once again SABER was the electric circuit tool used to generate the electro-thermal simulation results to be compared against the experimental measurements.

In [Hernández-Mora et al., '03] a different approach is taken to develop a model for the CPES IPEM. In this case, the authors describe a dynamic reduced electrothermal model based on the expanded Lumped Thermal Capacitance Method (LTCM). From this approach a simple, non-spatial, but highly non-linear model is obtained. While other methods are based on the three-dimensional heat diffusion equation, the LTCM allows for an unsteady heat transfer analysis dependant only on the time variable, and representing the spatial thermal distribution by the physical and thermal characteristics of the IPEM. The validity of the LTCM is based on the ratio between the internal conductive heat resistance to the convective one. This ratio is referred to as the dimensionless Biot number, and a small magnitude in this number is an indication of a very efficient conduction heat transfer, which happens in the IPEM. Each material is treated as a control volume, or lumped. The model calculates the energy balance of each lumped, resulting in a set of simultaneous non-linear ordinary differential equations. The validity of the LTCM was verified with a FLOTHERM™ simulation and with slow-transient experimental measurements. Experimental results showed good agreement with the model simulation.

1.4 THESIS OUTLINE

In this chapter, the CPES vision and virtual prototyping approach to develop and analyze the IPEM were presented. The IPEM was described in terms of its electrical functionality and its general material constituents, which are necessary to correctly develop the thermal model. Different approaches that various authors use to determine methodologies to develop thermal models for power electronic components were presented. The majority suggests the use of a thermal network based on developing an equivalent RC circuit to represent the thermal behavior of the power devices or components. The proven methodology described in the works related to thermal components modeling by Hefner was finally selected as the approach to follow to develop a thermal model for the CPES IPEM. The purpose is to improve the virtual prototyping thermal modeling step by introducing the thermal components model for a faster reduced-order simulation approach.

In the following chapters, the selected thermal modeling approach will be introduced, and the necessary 1D equations representing the thermal behavior of our module model will be presented. The IPEM will be examined to reveal its internal structure, dimensions, and the thermal properties of its materials, this to describe the procedure to decompose its structure into a series of thermal components needed to develop its equivalent RC thermal network. Two different experiments, needed to collect experimental measurements that will be used to validate the proposed model, will be explained in detail. Respective simulations will be performed to our model in order to compare and validate the obtained results. Finally, conclusions and suggestions to further improve the generated model will be presented.

CHAPTER 2

THE IPEM THERMAL MODELING

2.1 INTRODUCTION

From the works presented in Chapter 1, it can be found that practically all of them have certain things in common when it comes to generate a thermal model for an electronic package. The principal one is that the suggested model follows a current-power analogy. Heat dissipation behaves naturally as charge flow does in electrical circuits, heat capacity related to capacitances and heat dissipation to resistances. It is necessary to recognize the relevant heat-transfer mechanisms and their governing relations in order to understand the flow of heat within electronic systems. Three mechanisms can be considered for the IPEM: conduction, convection, and radiation. Heat conduction occurs when heat diffuses through a solid or a stationary fluid. In the IPEM, conduction will occur from the junctions through the solid module materials. Heat convection occurs when a fluid in motion assists heat transfer from a wetted surface. The heat sink performs this transfer from the module structure to the surrounding air. Heat radiation is termed for the heat exchange between surfaces o between a surface and a surrounding fluid if long-wave electromagnetic radiation is the transfer agent. Its contribution is more noticeable when high temperatures are present, but in the case of the IPEM conduction and convection practically dominate the whole process due to the allowed operational temperature range, which states that the junction temperatures must be less than 125°C.

Those characteristics make the modeling approach presented in [McNutt et al., ‘01], [Parrilla et al., ‘02], [Rodríguez et al., ‘02] and [Berning et al., ‘03] a suitable one for the CPES IPEM. They all have had results with good agreement with experimental measurements, and follow the same procedure presented by Hefner since it first works with thermal component models in [Hefner and Blackburn, ‘94]. All the necessary physical information about the IPEM thermal and dimensional characteristics will be

used to decide how to subdivide the IPEM structure into the necessary thermal components, and its equivalent RC network will be developed.

2.2 ONE-DIMENSIONAL MODELING APPROACH

Steady thermal transport through solids is governed by the Fourier equation [Kraus and Bar-Cohen, '95], which in one-dimensional form is expressible as

$$q = -kA\frac{dT}{dx} \qquad [\mathrm{W}] \tag{2.1}$$

where q is the heat flow, k is the thermal conductivity of the medium, A is the cross-sectional area for the heat flow, and dT/dx is the temperature gradient in the direction of the heat flow. Heat flow produced by a negative temperature gradient is considered to be positive, and that is the reason for the minus sign in the previous equation. The temperature difference resulting from a steady state diffusion of heat will be related to k, A, and the path length L by

$$\Delta T = (T_1 - T_2)_{cd} = q\frac{L}{kA} \qquad [\mathrm{K}]. \tag{2.2}$$

Ohm's Law governing electrical current flow through a resistance can be used as an analogy to define thermal resistance for conduction as

$$R_{cd} \equiv \frac{(T_1 - T_2)}{q} = \frac{L}{kA} \qquad [\mathrm{K/W}]. \tag{2.3}$$

It can be seen from these equations that, in terms of electrical circuit variables, temperature would be equivalent to voltage, and heat flow would be equivalent to current in a circuit. It is important to notice that, if no physical resistor is present as an available path, there will be no current flow in presence of a voltage potential, but that is not necessarily true in the thermal equivalent. Even if there is no material present with a difference in temperature between its extremes, heat flow can still be existent due to radiation effects when a temperature differential is present. That is how heat can flow even in vacuum conditions. Following the analogies, if a heat flow is equivalent to an electrical current, then instantaneous heat should be equivalent to electrical charge. Heat capacity, which is usually identified as the specific heat C_p times volume, is given in units

of [Joules/Kelvins/cm^3] and defined as the amount of heat necessary to raise the temperature of 1 unit mass of substance by 1°C. The total heat is then dependent of the amount of material available to store it (volume). The thermal flow associated with this quantity will be

$$q = (C_p V)\frac{dT}{dt} \qquad [\mathrm{W}]. \tag{2.4}$$

If the same electrical analogy must hold for the thermal case, then the thermal or heat capacitance associated with the heat conduction through the material volume will be given as

$$C_{cd} \equiv C_p V \qquad [\mathrm{J/K}]. \tag{2.5}$$

Table 2.1 summarizes part of the voltage-temperature analogy that will be helpful to develop the thermal components model.

Table 2.1
Electrical-to-Thermal Analogies

Electrical		Thermal	
Parameter	Units	Parameter	Units
Voltage	V	Temperature	K
Current	$A = \frac{C}{s}$	Heat Flow	$W = \frac{J}{s}$
Conductivity σ	$\frac{A}{V \times cm}$	Conductivity k	$\frac{W}{K \times cm}$
Stored Charge	C	Stored Heat	J
Electrical Resistance	$\frac{V}{A}$	Thermal Resistance	$\frac{K}{W}$
Electrical Capacitance	$\frac{C}{V}$	Thermal Capacitance	$\frac{J}{K}$

Suppose that heat is being applied to one extreme of a body made out of two different materials, and that ambient temperature is surrounding the rest of it. A one-dimensional thermal equivalent could be like the one shown in Figure 2.1(a). The thermal power source will deliver a certain amount of heat that will be distributed through the

entire body until a thermal equilibrium is reached. Figure 2.1(a) is not the only way to represent the thermal network using an RC equivalent. Some other variations are also presented. Figures 2.1(b), (c) and (d) are referred to as a Foster network, a Cauer network, and a Cauer network for a top-covered device, respectively [Bagnoli et al.(a), '98].

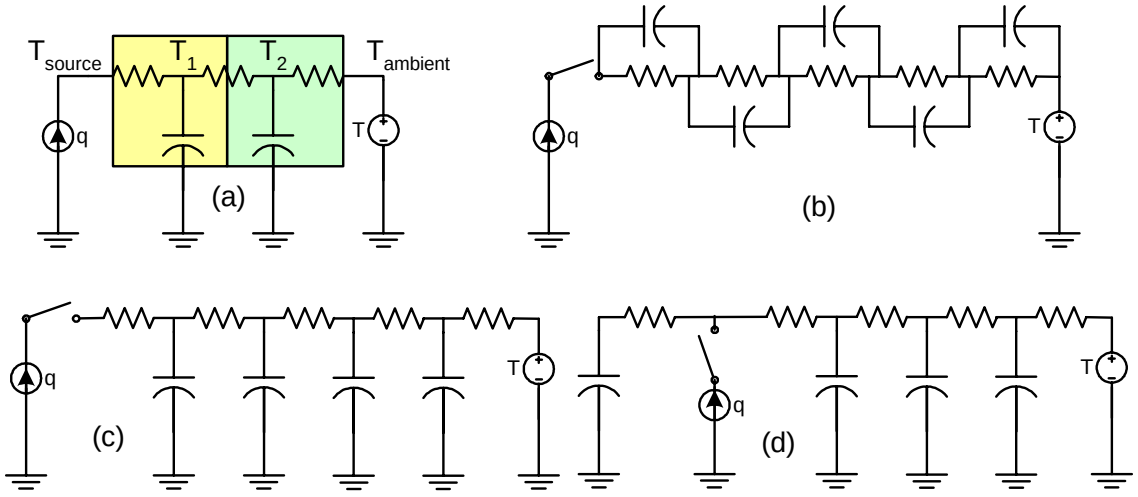


Figure 2.1: Example of one-dimensional thermal networks: (a) general approach; (b) Foster network; (c) Cauer network for a top uncovered device; (d) Cauer network for a top covered device.

It is also pointed out by [Bagnoli et al.(a), '98] that only the Cauer circuits are suitable for faithfully representing the system from the physical point of view. That happens because a dramatic physical nonsense occurs if the Foster network is applied for interpreting the dynamic thermal behavior of the internal points in the circuit. In the electrical circuit, the current flowing across the capacitor during a dynamic regime is the same on both sides of the device due to the symmetrical variation of the positive and negative electric charges. But thermal circuits have no quantities equivalent to negative electric charge. Only the heat flow on one side of the capacitor has a real meaning, and that is why the Cauer networks, with their capacitors grounded in one side, are more suitable as a thermal analogy. For that reason, a Cauer network was selected to develop the thermal model for the IPEM.

2.3 THE IPEM INTERNAL STRUCTURE

The IPEM is a body with different layers and materials of varying dimensions. In order to find the correct thermal resistances and thermal capacitances that would represent the IPEM model, it is important to know all the physical dimensions of the IPEM and the thermal characteristics of all the materials involved in its construction. Figure 2.2 shows an exploded view of the principal IPEM layers and components.

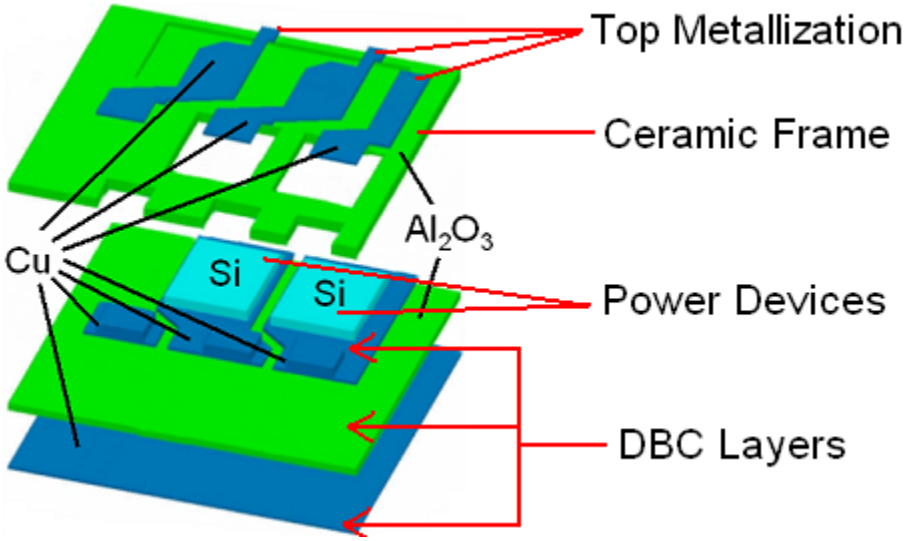
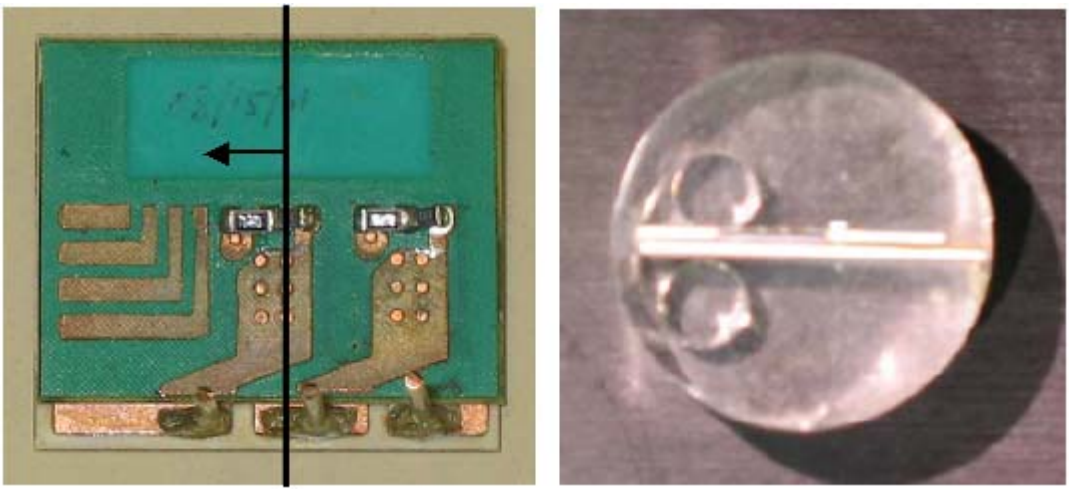


Figure 2.2: Exploded view of the CPES IPEM (Gen. II-C) layers and components.

The top copper metallization layers serve to interconnect the silicon devices. An Al_2O_3 ceramic frame surrounds both devices, which is also the same ceramic material of the DBC central layer. The DBC structure is composed of the bottom copper layer, the middle ceramic layer, and a reduced top copper layer designed just to make the necessary contact with the silicon devices and connection leads. The dimensions for the IPEM, principally the surface areas, are presented in Appendix A. Due to the fabrication process, some material thicknesses, like the solder layers for example, are difficult to set to a specific value because their final thickness will depend on the melting and solidification pattern that the mixture will adopt when heated or applied. To correctly identify the thicknesses of the different layers and materials, the IPEM was cut cross-sectionally to show its actual dimensions. Figure 2.3 shows how the procedure was performed at VT.



(a) (b)

Figure 2.3: IPEM cross-sectional cut procedure.

Notice that the IPEM shown in Figure 2.3(a) is for the Generation II-B, but its thicknesses are the same as for Generation II-C. A sample IPEM was immersed in a substance, which later hardened enough to support the IPEM structure during the cutting process. Figure 2.3(a) shows where the cut was made, and Figure 2.3(b) shows the cross-sectional view of the resulting piece. A close up of the IPEM layers and relative thicknesses is shown in Figure 2.4.

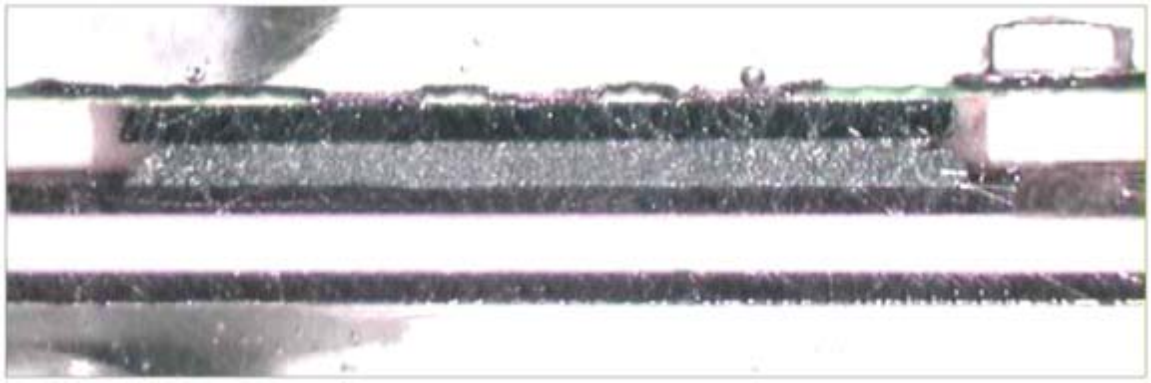


Figure 2.4: Cross-sectional view of the IPEM layers.

Figure 2.5 shows a portion of the image in Figure 2.4, now identifying each layer material and its thickness. Notice that the solder layer was not identified as part of the exploded IPEM in Figure 2.2.

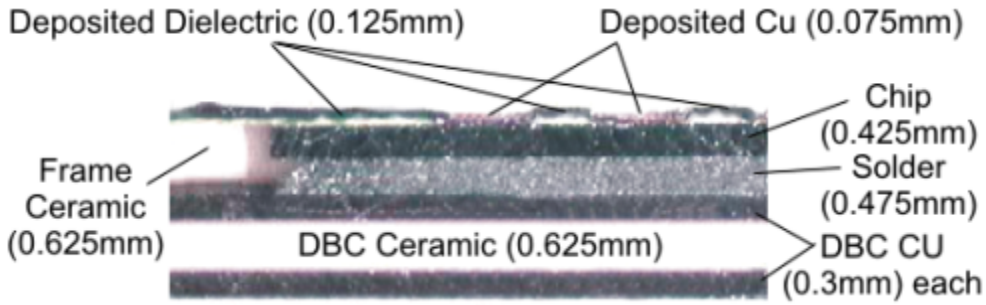


Figure 2.5: Identification of layer materials and thicknesses.

A closer look at the top deposited layers (too thin to be appreciated in Figure 2.5) is shown in Figure 2.6.

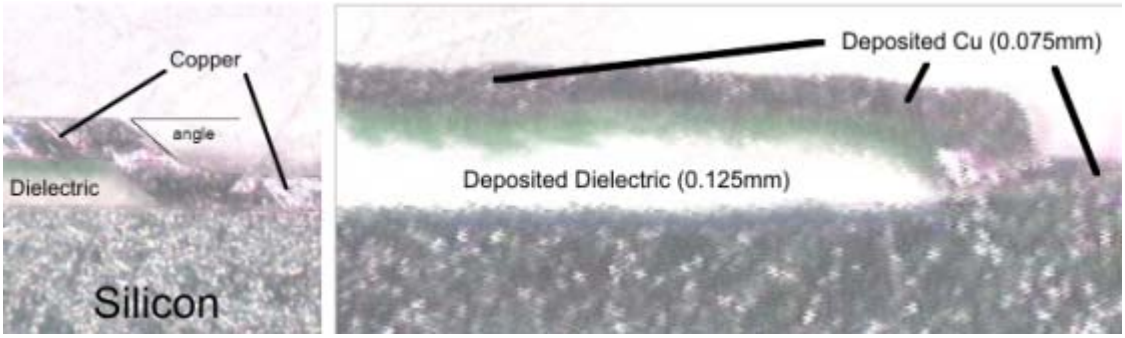
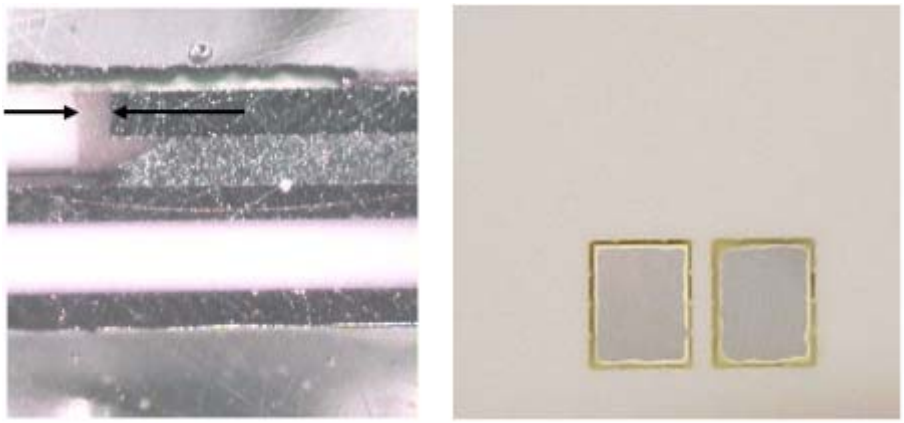


Figure 2.6: Close up of the deposited top copper metallization layer and dielectric.

The frame ceramic is cut with laser precision to provide space for the two embedded chips. Placing an epoxy layer around the chips holds them firmly in position. Part of this lateral epoxy layer can be seen in Figure 2.5 between the top ceramic frame layer and the chip and solder layers. Figure 2.7 (a) identifies the location of the epoxy layer as seen in Figures 2.4 and 2.5. Figure 2.7 (b) shows the back view of the frame ceramic layer when the chips are placed with the epoxy.



(a) (b)

Figure 2.7: Epoxy layer surrounding the silicon chips in the IPEM.

The thermal properties of the material used in the IPEM are shown in Table 2.2.

Table 2.2
Thermal Properties of IPEM Materials

Material	Thermal Conductivity [W/K/cm]	Heat Capacity [J/K/cm^3]
Silicon	1.5	1.6
Copper	4.0	3.4
Al_2O_3	0.2	3.2
Solder	0.6	1.3

2.4 THERMAL COMPONENTS DECOMPOSITION

The method of thermal components used by Dr. Hefner subdivides de structure of electronics devices in such a way that the heat dissipation is followed through the structure as it crosses a series of volumetric elements or thermal components, which start from the point where power is applied (the semiconductor junctions) toward the heat sink or any other heat-removing method present. The available path, in most cases, is from the silicon junction directly downward the DBC layers and ending in the heat sink structure, as it is the fastest and most efficient way to remove the device heat. Depending on the

thickness of the materials, the generated heat may be dissipated quickly like fast-transient pulses, where the pulses are so short that the junction returns to its initial temperature without the heat even getting noticed at the bottom layers or the DBC. If the pulse is longer (and the power level is very low so that it does not overheat the junction) heat will be present down to the heat sink itself, and any final state will take a long time to be reached like in the slow-transient experiment.

Since the heat starts emerging from the semiconductor junction, the silicon device is the first one to be modeled. Silicon has the property of varying its thermal conductivity in a nonlinear manner depending on the temperature. The silicon thermal components modeled for the semiconductor device must account for that effect, and Hefner included that behavior in the silicon chip model that he developed based in his analysis for the IGBT model [Hefner, ‘94]. He described all the governing electrothermal equations necessary to generate a model for the silicon power device of the IGBT, and that model is now implemented as a general silicon chip thermal element available for circuit simulation in the SABER thermal components libraries. His silicon chip model was used for the IPEM model development without other modification than the chip size parameters. His chip model is composed of two parts: the whole chip, divided in ten nodes, has an upper section that represents the top 20% of the full thickness, and it is there where he defines how the power is distributed to the rest of the structure from the silicon junction at the top through five nodes; the second portion of the model is represented by the remaining 80% of the full thickness, also divided into five thicker nodes that will uniformly handle the heat being dissipated downward to the device header. His model presumes that from the header on is where the geometry of the rest of the module will influence the final behavior of the heat response for the entire ensemble.

His approach is to continue with the silicon bottom area as the actual heat-generating surface, and then subdivide the remaining path into a series of thermal components with different thermal characteristics. Each new component starts as a uniform geometrical prism that must follow the shape of the heat-generating source, that is, the bottom area of the silicon chip. In his model, the chip is presumed not to let heat flow sideways from the silicon volume, but the following layers can start to spread the

heat to the periphery as it goes down. He suggests the use of a 45-degree angle in all directions from the starting point under the chip to represent this heat diffusion effect through the materials. Another suggestion is to select the sizes for each consecutive node following a quasi-logarithmic spacing sequence in order to represent a more "natural" curve behavior as the heat is dissipated further from its junction origin. Although the chip base is rectangular, the 45-degree angle tends to round the corners of the following nodes as they widen and get thicker the farther they are located. Figure 2.8 depicts the idea behind this thermal component subdivision, which is valid principally to verify the fast-transient experimental measurements since it only covers for the close layers below the silicon chip at this time.

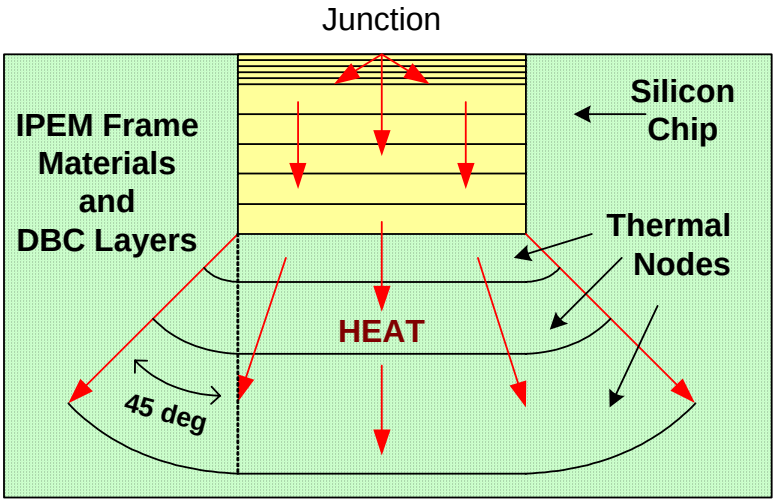


Figure 2.8: Thermal element decomposition of the IPEM into nodes.

Notice that the node in contact to the bottom of the chip (header) is the only one having a top area that is rectangular. The rest of them will have curved areas of contact between them due to the conical volumes that are added due to the presumed angular heat spreading. Figure 2.9 show a three-dimensional perspective of the adjacent nodes and a cross-sectional cut showing the form of the successive volume created for each node.

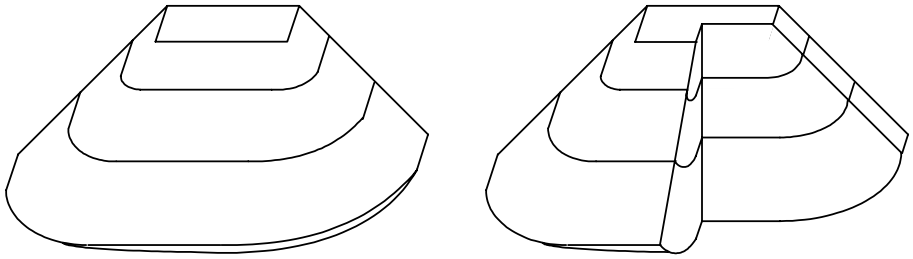


Figure 2.9: Three-dimensional perspective of the series of nodes from the chip down.

All these nodes contact areas and volumes are computed based only on the header area, the given angle (recommended to be 45° in this case) and the specified thickness for each node. The header area is known from the IPEM dimensions; the angle was recommended; but the thermal elements thicknesses have to be calculated from the total thickness to be modeled starting from the header down. The thickness of the layers below the chip are determined from the information obtained in Figure 2.5, which are the first solder layer and the DBC ones. Unfortunately, there is another solder layer located between the DBC and the heat spreader that is not described in the cross-sectional cut image of the IPEM, because the cut was made only for the isolated power stage of the module itself.

To represent the logarithmically spaced thermal components below the chip, the layers presumed to be always under the chip (that is, in case that some other element is used below the power stage instead of the heat spreader used in our experiments) would be taken as the DBC with the two solder layers. The chip has to be always soldered to the DBC, and the DBC has to be soldered to something else below it to spread the heat, otherwise the IPEM will burn out by overheating even with very low power levels due to its minimal thickness. According to the thickness of the last (bottom) node in the silicon chip, the next node below it (in the following solder layer) should be thicker. A quasi-logarithmic trend in thickness growth was chosen as a possibility to determine how each successive node will increase in relative thickness. If the total thickness of the five layers following the silicon chip is divided into ten logarithmically spaced thermal components, then the approximate location of their centers between the boundary surfaces of the different materials would be like the ones shown in Figure 2.10.

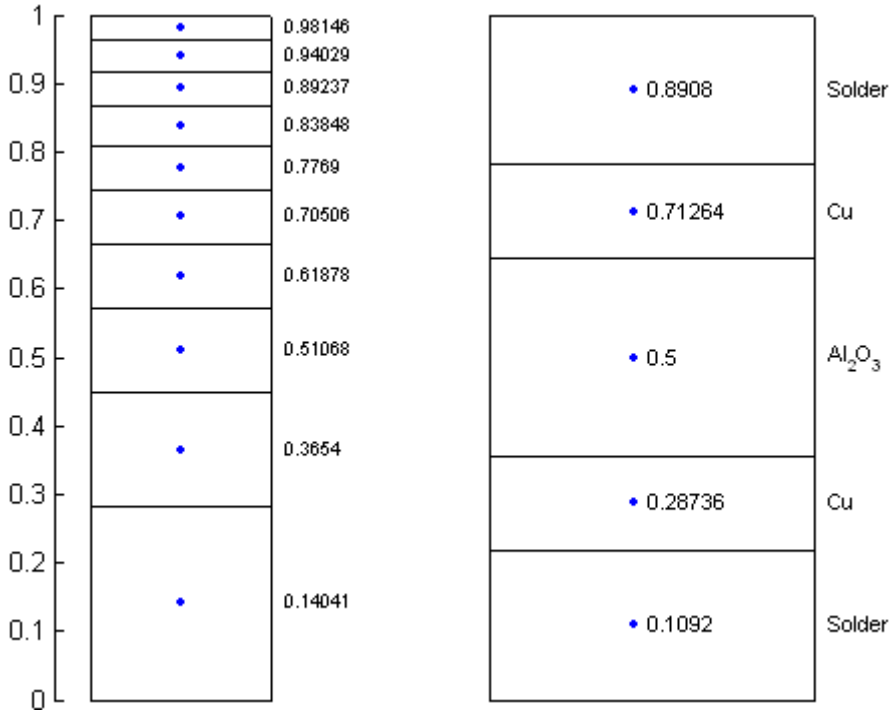


Figure 2.10: Relative location of the thermal components for the layers below the chip.

The left column in Figure 2.10 shows how the relative sizes of the ten thermal elements will look compared to the layer thicknesses in the right column. The five layers in the figure are proportionally scaled according to the dimensions given in Figure 2.5. Some thermal components were made of a single material, like the first four, which were represented as being pure solder. Others had to be computationally defined as a combination of two materials, and the percentage of material contributing to their thermal characteristics had to be computed carefully. For example, the last node is a mixture of some copper and a majority of solder, but the amount of each material will determine the overall thermal resistance and thermal capacitance assigned to it in the final RC network representation of the thermal model for the IPEM. Although the most significant part of the modeling is the path below the chips, the remaining volume of the DBC layer and the ceramic frame also had to be included as peripheral thermal components, because that remaining material also contributes to the behavior of the final model, especially when slow-transient power levels are applied. The thermal capacitances in the rest of the structure have enough time to accumulate heat coming from the coupling paths that they share with the fast-transient-determined thermal components. If this remaining portion

were not modeled, there would be no way to simulate the same location below the gate driver board where the thermocouple was placed to take its measurements during the slow-transient experiment.

Finally, with all the IPEM structural dimensions, the thermal properties of the materials, the designation of the thermal components thicknesses, and the aid of Equations (2-1) to (2-5) applied to the Cauer thermal circuit representation in Figure 2.1, it was proceeded to develop a computational model in SABER for the thermal behavior of the IPEM by coding all the previous information in form of a MAST ADHL template. An example of a SABER template is presented in Appendix B. The reason for the use of SABER as a tool to perform electro-thermal simulations by many authors is the ability of this software to combine different systems, like electric, mechanical, pneumatic, etc., into a single analysis environment when needed. For example, a full electrothermal analysis of the IPEM is possible by modeling the electric part of the IPEM like in any other circuit simulation tool and adding a thermal model of the IPEM, provided that the programmer allowed for the necessary interconnections between both systems in the analysis environment. That is, the electrical model of the power electronic silicon devices, which are the critical components affected by the generated heat, must include a thermal connection point to allow for representing how their electrical parameters or behavior will be affected or modified by the actual circuit environment temperature. In turn, the thermal model will use these connection points as thermal links to allow the proper interaction between the electrical behavior of the components and the surrounding thermal conditions, modifying their electrical performance accordingly.

The templates were coded so that the governing differential equations of the thermal model were represented and computed by the software in the same way that the circuit simulators do for the electrical ones. That is another reason to use an electrical model to represent the thermal behavior of the module. The software solved for the thermal model as if it were simply solving for an electric circuit, with the only difference that the programmer was the one who previously decided how the thermal model should be computed by the simulator using a series of templates to represent different portions of the physical structure of the module.

Each thermal component can be represented in SABER by a template. A template is composed of a series of variable declarations, parameter calculations, and energy balance equations that can be solved by the simulation tool like RLC circuits are solved based on Kirchoff's laws. Take for example the SABER thermal network shown in Figure 2.11. The two sources are part of the SABER thermal components library. But the two chip components and the DBC component are user-made components, coded in their respective templates by using MAST-AHDL. Appendix B shows a brief example of the main parts needed to develop a functional thermal component using SABER MAST-AHDL templates.

The thermal connections, or pins, are defined in the heading of the template. They identify these connections as thermal ones, and the simulator automatically creates references for the temperature and power magnitudes associated with them. If the component has its own internal components, like the DBC one, which has different nodes defined within, all the necessary variables must also be defined. To simplify the calculations, the necessary dimensions and thermal material properties are given first. Auxiliary temperature, energy and numerical variables are also defined initially.

With all these variables, a section in the template called the parameters section is used to calculate further quantities needed to solve the thermal equations governing the model. It is in this section that volumes, contact areas between nodes, and thermal resistances are calculated. The thermal resistances are found as stated in Equation (2.3), using only distances, areas, and thermal conductivities. It is then that the solver can find the temperature in the values section values at each node and connection pin. Temperature values are also needed to calculate the thermal capacitance values, thus they are also computed in the values section after the temperatures, using Equation (2.5).

The user is not allowed to set initial temperature values at the connection pins because a conflict with the values generated by the thermal sources connected to them could enter in conflict. But the internal nodes, being inaccessible by the sources, can be set to an initial temperature, like capacitors that are part of an electrical network can be set to an initial voltage during circuit simulation if they are not in contact with a voltage source. That initial temperature setting for the thermal nodes can be done in the

control_section section. Once all temperatures, thermal capacitances, and thermal resistances have been found, the simulator can solve the heat flow (power) equations in the equations section of the template. The simulator solves Equation (2.5) to calculate the stored heat at each node or volume, and the Fourier Equation (2.1) is solved to find the heat flow between nodes in the thermal network.

Different simulations were performed using SABER to verify the model behavior. First, the small single-chip circuit shown in Figure 2.11 was used to analyze how was the behavior of the right chip simulation alone against all the experimental data collected for that chip for the different power levels of the fast-transient test. Then, a second simulation for all the same power levels was tested again but this time using the two-chip coupled model shown in Figure 2.12, which is more representative of the actual IPEM model and more related to what the final completed model should be. Finally, a slow-transient simulation was performed with the circuit shown in Figure 2.13 to analyze the behavior against a couple of measurements of the UPRM experimental measurements data. These three figures represent how the thermal model actually looks in the SABER environment, and illustrate the concept of developing thermal components for the different IPEM structures and how they are connected to create a thermal network.

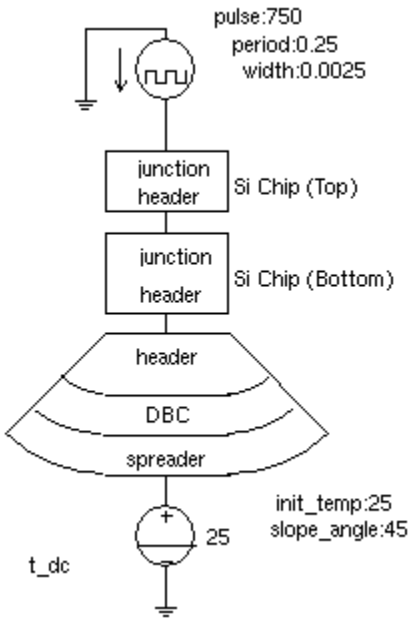


Figure 2.11: SABER single-chip simulation for the fast-transient test.

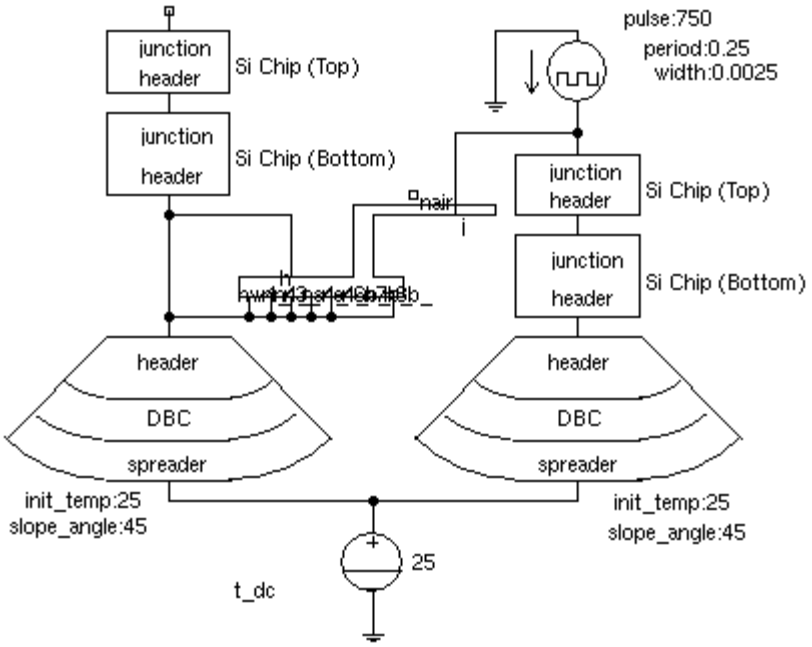


Figure 2.12: SABER double-chip simulation for the fast-transient test.

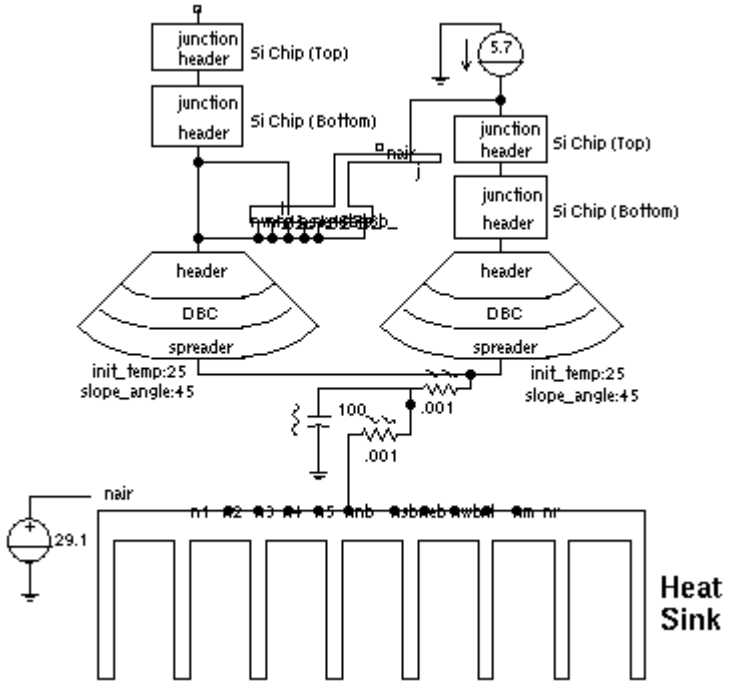


Figure 2.13: SABER simulation for the slow-transient test.

2.5 CONCLUDING REMARKS

In this chapter, the equations needed to develop the 1D approach for the IPEM thermal components model were presented. The IPEM structure was analyzed in more detail to reveal its actual dimensions and the thermal characteristics of its materials, which are necessary to correctly develop the thermal components for the desired model. The methodology used to subdivide the different IPEM layers into the necessary amount of thermal nodes and components was also explained. Finally, preliminary SABER thermal components networks that represent the conditions for slow- and fast-transient responses for the IPEM were developed and presented.

Simulation results differ from the final steady temperatures measured experimentally but for no more than 10°C. This was due to the fact that the ceramic layer surrounding the silicone power devices was not completely modeled below the gate driver location. The simulated results were also affected because the heat sink, included in the model, cannot be modeled using only conduction effects, since it is dominated by convective heat dissipation.

CHAPTER 3

THE UPRM SLOW-TRANSIENT EXPERIMENT AND MODEL VALIDATION

3.1 INTRODUCTION

The CPES IPEM is designed to manage high power density levels and, being so integrated, its generated heat can affect nearby components if placed close to its structure. Due to the high-speed switching during its full operation and the non-symmetrical placement of its components, different power levels are generated throughout the active electrical elements or circuits. Experiments performed at VT demonstrated that dissipated power levels during full half-bridge IPEM operation are approximately 1W for the complete gate driver circuitry, 7W for the innermost MOSFET (from hereon referred to as the "Left" or "L" device also), and 12W for the outermost one (from hereon referred to as the "Right" or "R" device also). This demonstrates the effect on power dissipation that arises from the non-symmetrical placement of these components, even when both MOSFETs are equal in dimensions and operate at 50%-50% duty. They are not really centralized, but rather placed close to one of the edges in the IPEM structure, and their electrical copper tracing connections are different in size and shape also.

For that reason, a slow-transient experiment was performed to measure the different temperatures arising from the non-uniform heat dissipation throughout the IPEM structure. These temperatures would give a thermal profile on how the IPEM heats up according to different power levels being applied at different locations, specifically, at each of the MOSFETs.

3.2 THE UPRM EXPERIMENTAL SETUP

According to the VT measurements, the UPRM slow-transient experiment (see Figures 3.1 and 3.2) had to be performed in such a way that similar power levels were generated by the devices without damaging them by overheating. During a visit to UPRM, two colleague investigators from VT, Ying F. Pang and Jonah Z. Chen, suggested the method to be used for such a test. The gate driver circuitry wire bond connections are extremely delicate and readily exposed to possible damage due to the shipping and handling of the prototypes from VT to UPRM. Because of that, the decision taken was not to implement a complete power circuit load for the IPEM to control in order to activate the module at full capacity and generate similar power dissipations like the ones obtained at VT, but to supply a direct amount of electrical power to the devices to generate the desired power dissipation.

The 7W and 12W dissipated power appeared when both devices were working intermittently at the same time. Both MOSFETs were working forward-biased as switches because they were operating as a half-bridge, but in our case, no load was present, so that arrangement could not be used to generate the desired power levels. The suggested method was then to apply a constant electrical low-power level to the protection diodes in each silicone device forward-biased, as shown in Figure 3.3. The current being conducted by each diode would generate the necessary heat, and the respective temperature levels would be measured with thermocouples located at five different locations.

Figure 3.1 shows the IPEM with the five thermocouples that were attached for this experiment, and the complete assembly used for the slow-transient experiment. The two thermocouples used to acquire the silicon devices temperatures have their tips glued on top of the metallization layers in the IPEM. They can be seen coming out from the center of the figure to the left, and then turning to the right at the bottom, as they are bend to join the remaining three thermocouples identified in the picture. The other thermocouple tips cannot be seen in Figure 3.1. One is glued beneath the gate driver board, but the location of the other two thermocouples tips can be shown before all the

IPEM layers were joined. These two thermocouples are shown in Appendix D, in Figures D.2 and D.3 respectively. Apart from having the five thermocouples attached to it, the main difference from the fast-transient experiment (which will be explained in more detail in the next chapter) is that the IPEM plus heat spreader were placed on top of a heat sink. This heat sink was selected at VT to dissipate the necessary amount of heat and keep the IPEM working at correct operational temperatures. Figure 3.2 shows the actual UPRM instrumentation setup. The IPEM and its heat sink are shown in front. To the right is a high-power controlled DC source. To the left are the thermocouple array switching device (top) and a multimeter (bottom) connected to it in series to interpret the array measurements.

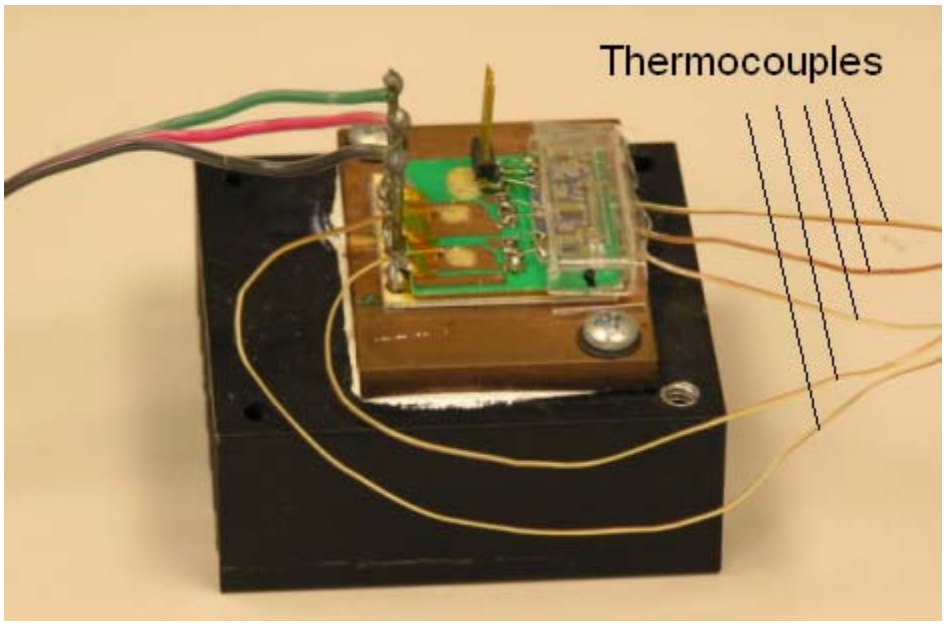


Figure 3.1: UPRM IPEM and heat sink experimental setup.

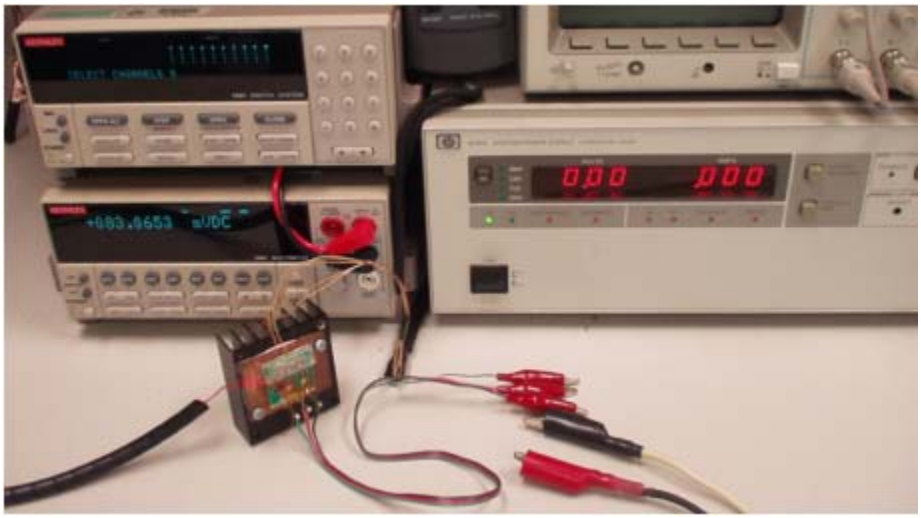


Figure 3.2: UPRM slow-transient test instrumentation and experimental setup.

3.3 THE EXPERIMENTAL PROCEDURE

The experimental setup for the slow-transient experiment can be seen in Figure 3.3. A Windows-CVI™ program was designed to perform automatically all the necessary measurements (See Appendix D, Figure D.8). The software allowed for the setting of the power level to be supplied, the selection of the desired temperature measurements, the time interval between each consecutive measurement, and the full time for the duration of the experiment. The first tests were performed using just a low power level to verify how much voltage needed to be applied in order to generate a certain amount of power to be dissipated by the diode. The diode conducts just with enough voltage to forward-bias it, usually just about 1.2V or so. So, in order to generate different power levels, the given command was to set a similar voltage at the DC power source and an initial current guess value.

The thermocouples are connected to an array card in a switching device, which in turn is connected to a multimeter capable of interpreting the thermocouples temperature-to-voltage tip measurements back to a temperature value to be recorded by the computer. Part of the required instrumentation for the actual UPRM setup can be seen in Figure 3.2. Once the software set on the power, the original voltage value would be maintained, but the diode would adjust its current automatically depending to the voltage level, and that

would generate a certain heat. There was no i_d vs. v_d table or graph available about the embedded diode to know how much current could be obtained with a certain voltage. That means that the power being applied to the device could not be directly specified, but rather "forced" to be set as close as possible by trial and error with the selected voltage value. In order to generate a certain amount of power individually at each device, the power source had to be connected respectively to one device only to avoid the simultaneous current conduction trough both diodes.

It was considered that the 1W dissipation of the gate driver circuitry was not high enough to affect adversely the electrical performance of the half-bridge structure. The supporting frame ceramic provided enough isolation from this 1W power level to reach the power semiconductors. Hence no test was performed to the gate driver during this experiment other than to measure the temperature that appeared at the point of contact between the driver board and the rest of the IPEM. The thermal effect of the power semiconductors on the board was more important. This was done to measure how much heat the devices were delivering to the gate driver and the possible effects that this may have on its electrical performance.

The computer managed the automated measurement process completely. Measurements would start at room temperature, and an additional thermocouple was placed apart form the IPEM sensors to measure the air temperature during the whole process to check for possible changes that could affect the rest of the measured values. Some fluctuations were seen during the first measurements due to the room temperature changes being produced by the air conditioning system. It was decided to shut down the air conditioning during the rest of the remaining tests in order to obtain more uniform transient curve measurements. Most of the tests were set to last about an hour and a half. This would allow the whole experimental setup to reach the necessary steady-state temperature values throughout the different layers once the applied power had been completely distributed. The system would then turn off all power sources automatically, display the final measured curves, and wait for the user to save them.

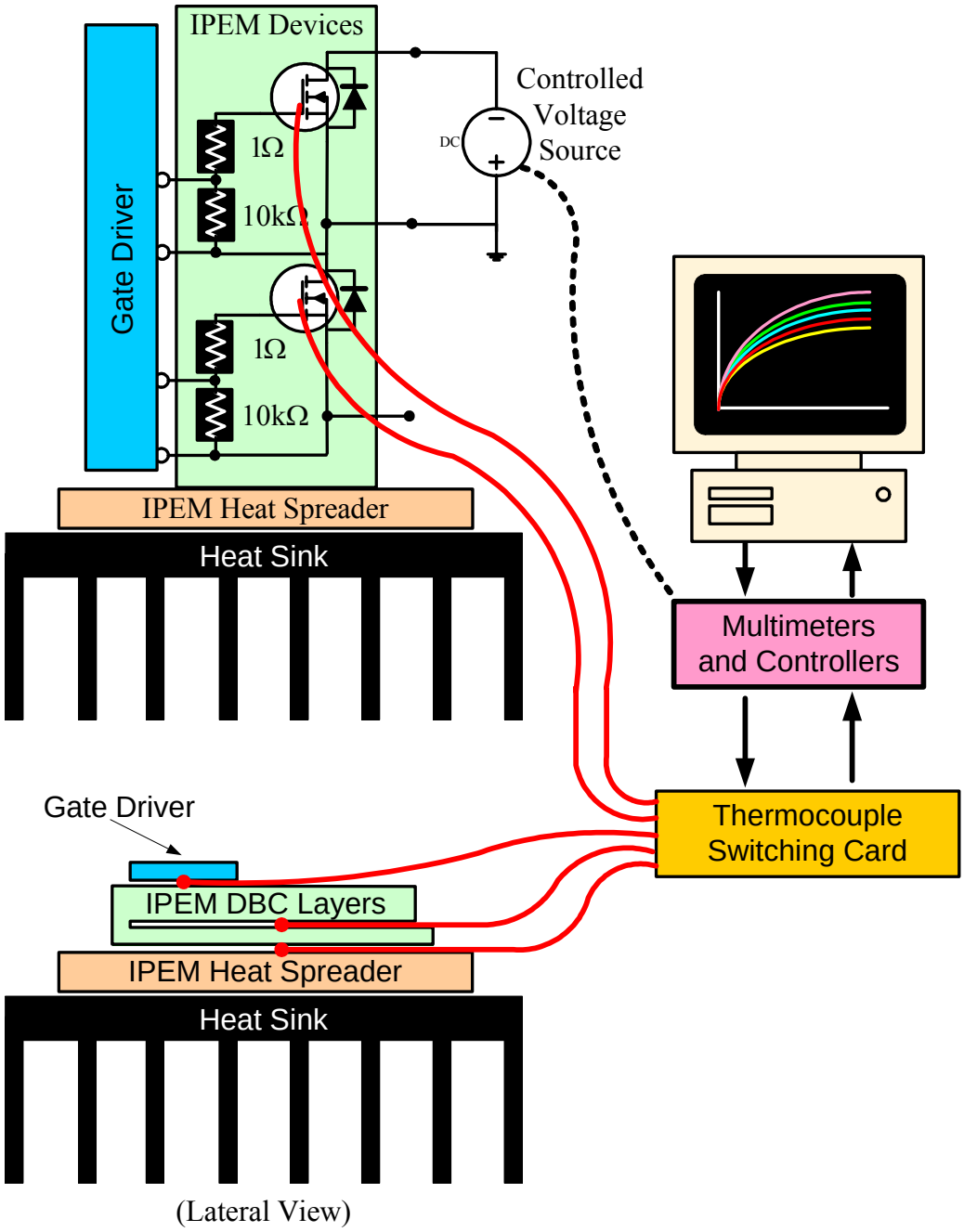


Figure 3.3: Slow-transient UPRM experimental setup.

Several tests were performed on each device with different power levels that never exceeded about 8W, this trying to stay below the 7W~12W levels measured at VT, as explained previously. There was a limitation between this experiment and the one performed at VT: the operating full-bridge of VT allows for a wider range of currents and voltages for the MOSFETs, thus, more and higher power levels could be obtained. At the other hand, diode power dissipation for our experiment depends on the forward-bias voltage applied to the diode. For conduction purposes, it can be set only to a small range of values, and the only other way to further modify the power levels was by including some external resistance to the current path, which was not done to avoid the interference of non-IPEM-related elements in the experimental measurements.

Figures 3.4 to 3.11 show some of the measurements for the different devices at different power levels. Notice that only the measurement closer to the device where the power is being applied will show a noticeable difference in temperature from the rest of the five IPEM signals. The other device will show values even lower than the ones for the layers beneath the powered device. This happens because heat flows better downwards in search of the most efficient heat-dissipation surface of the heat sink, and the contact areas in the heat flow path are wider also. In contrast, the IPEM dielectric offers a higher resistance than the bottom layers, thus the non-powered device will not heat up as fast as the rest of the layers which are in the way offering better conduction paths. The lateral conduction path from chip to chip is also very thin and, added to the low thermal conductivity of the dielectric, provides for a higher heat flow resistance. Nevertheless, being so thin, the layers of the IPEM show similar temperature readings regardless the temperature differential being managed between the powered junction and the heat sink. All power level values are approximate due to variations in the source.

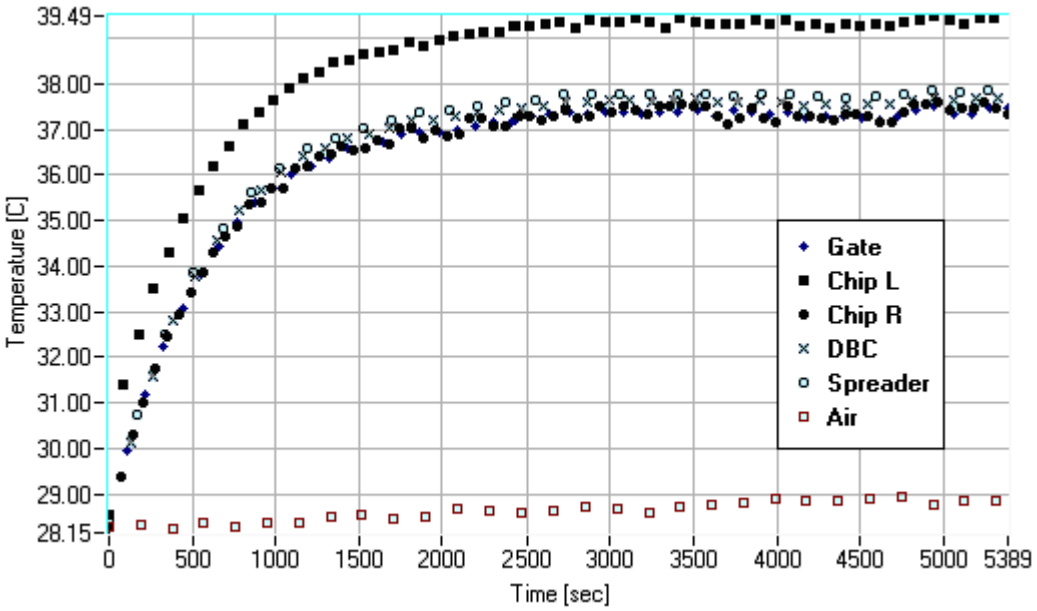


Figure 3.4: Experimental measurements in L with approx. 1.65W, 1.1V, 1.54A.

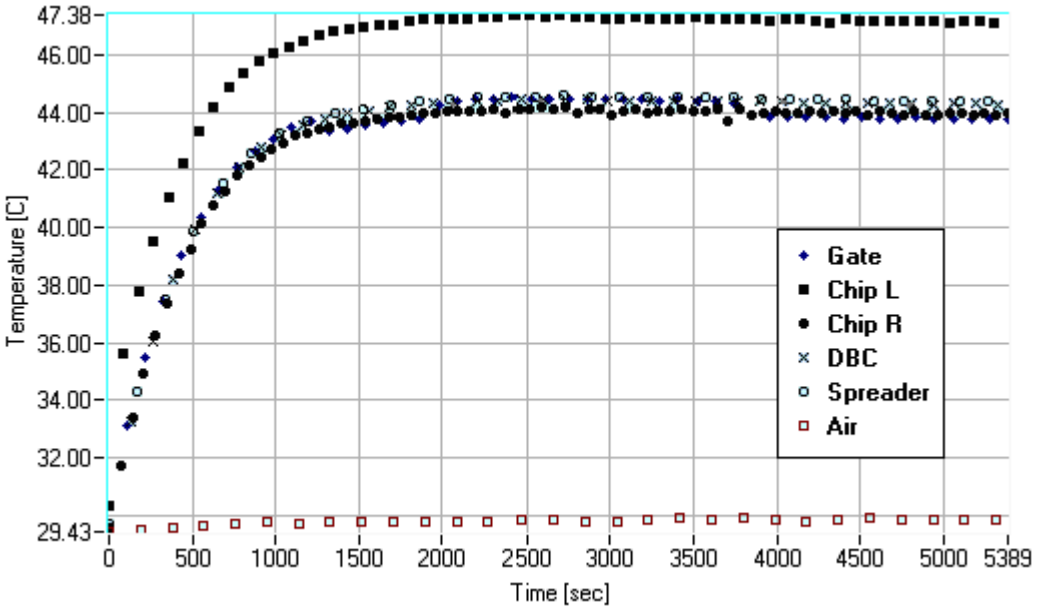


Figure 3.5: Experimental measurements in L with approx. 2.8W, 1.3V, 2.1A.

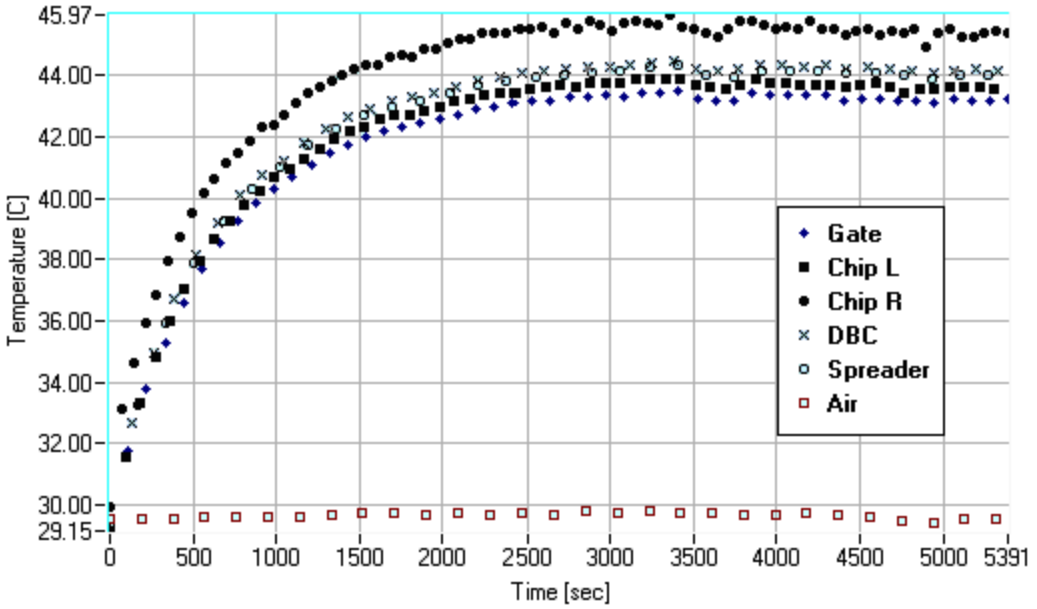


Figure 3.6: Experimental measurements in R with approx. 3.3W, 1.1V, 3A.

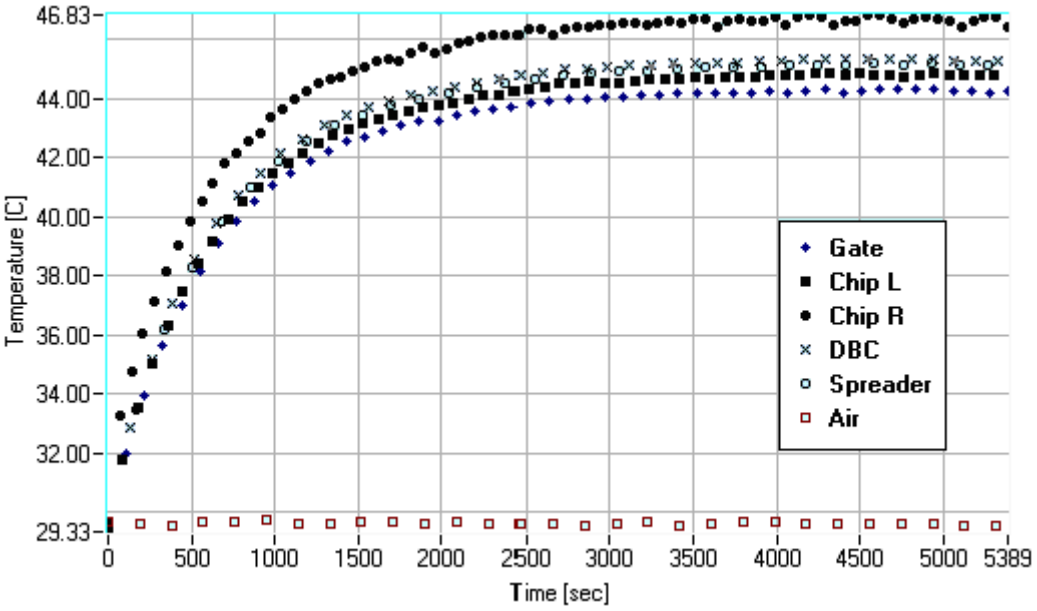


Figure 3.7: Experimental measurements in R with approx. 3.3W, 1.1V, 3A (#2).

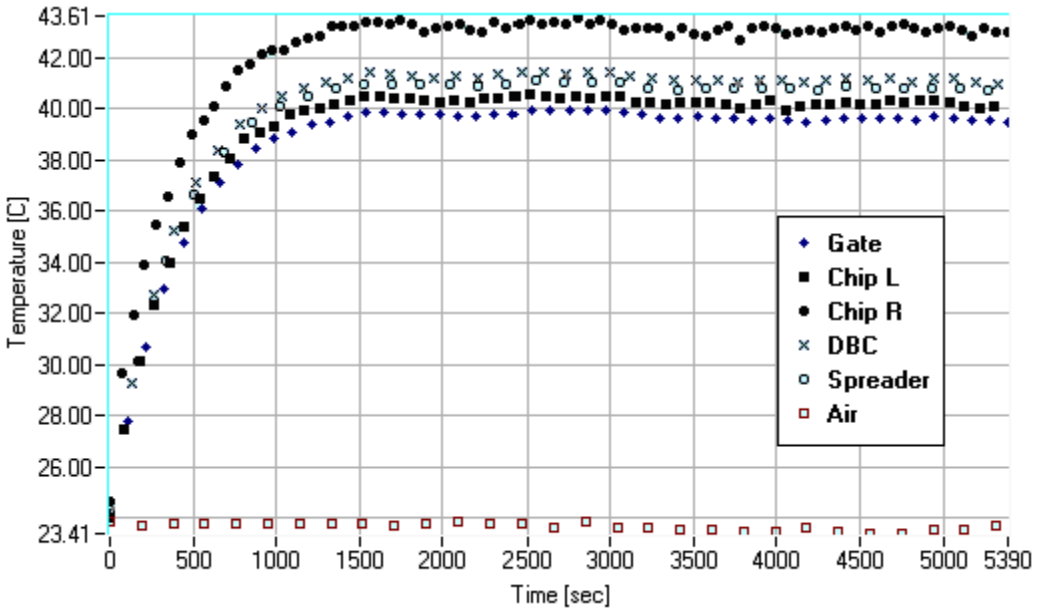


Figure 3.8: Experimental measurements in R with approx. 4.8W, 1.3V, 3.7A.

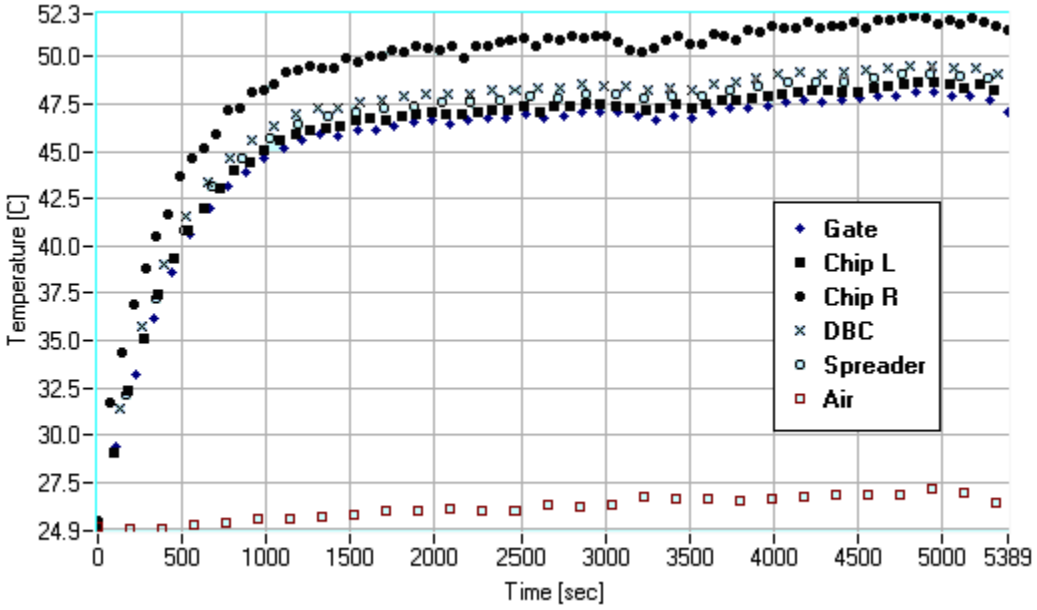


Figure 3.9: Experimental measurements in R with approx. 5.8W, 1.4V, 4.2A.

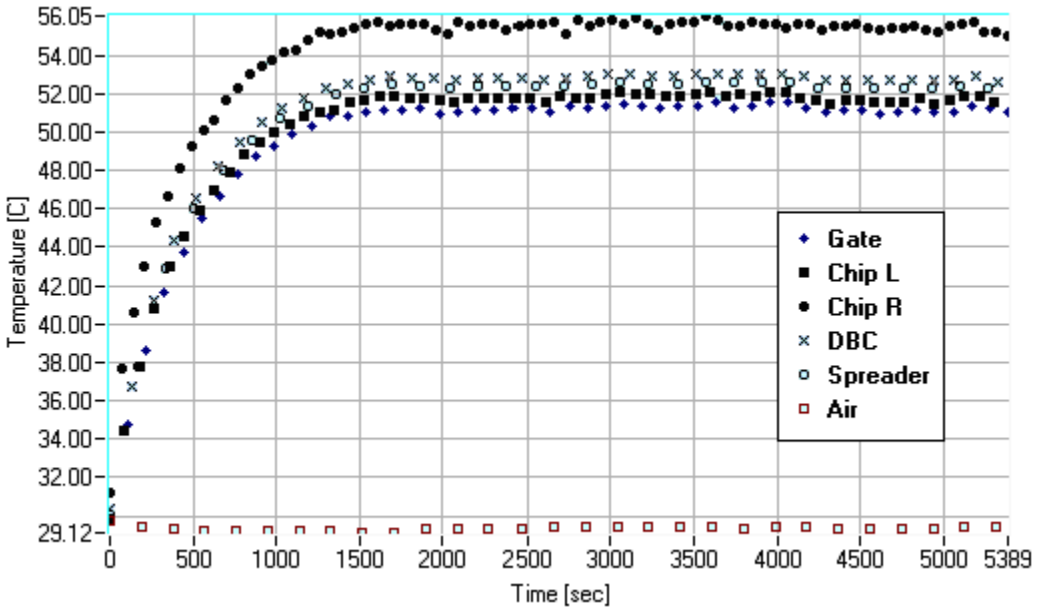


Figure 3.10: Experimental measurements in R with approx. 5.7W, 1.5V, 3.85A.

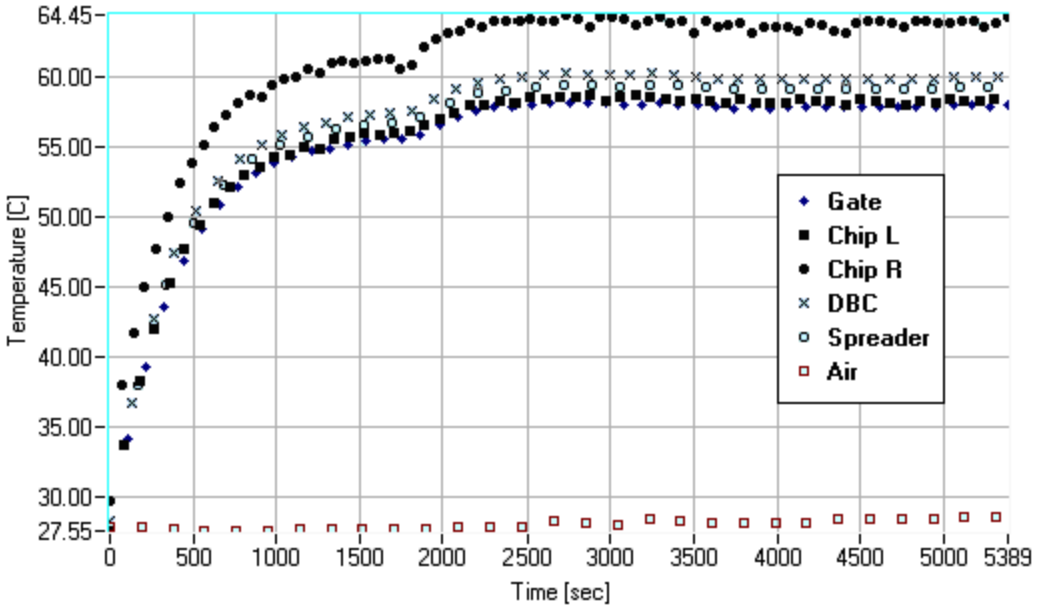


Figure 3.11: Experimental measurements in R with approx. 8~10W, 1.7V, 5.2A.

3.4 SLOW-TRANSIENT VALIDATION RESULTS

Figures 3.12 and 3.13 show simulations for two of the constant power experiments performed at UPRM for the slow-transient test. These results were obtained using the Figure 2.13 model that has the heat sink added to the two-chip model of Figure 2.12, plus a representative resistive path and a capacitance for the heat spreader copper bulk. Power levels and experimental measurements are approximate due to the constant variations measured from the thermocouples. Notice how noisy the waveforms for the two junctions are in the experimental measurements. That was due in part to the fact that the two junction thermocouples were at the surface of the IPEM, and hot air convection currents may have altered their readings, preventing them from being uniform.

In both cases the time constants present in the system behaved similarly in terms of how much time was needed to reach a thermal steady state. But the final constant values differ noticeably. It can be considered that it is better for the model to simulate that it heats more than the actual circuit, than letting the circuit overheat when its simulation shows lower than actual temperature values. It is important to mention that the temperature profile of a heat sink acts as a nonlinear thermal resistance. The heat sink cannot be modeled with the same thermal components approach used for the rest of the IPEM structure, because instead of conduction, convection effects govern the heat sink thermal profile. The present heat sink model is based on equations derived from examples in [Kraus and Bar-Cohen, ‘95] for a general finned heat sink.

3.5 CONCLUDING REMARKS

In this chapter, the slow-transient experiment and thermal model validation were presented. First, the UPRM slow-transient experimental setup was described, and then the complete experimental procedure was explained. A series of experimental measurements were shown to analyze the slow-transient behavior of the IPEM temperatures when constant low-power levels were applied. Finally, model simulation results were compared to the experimental measurements to validate the modeling approach under slow-transient power level conditions.

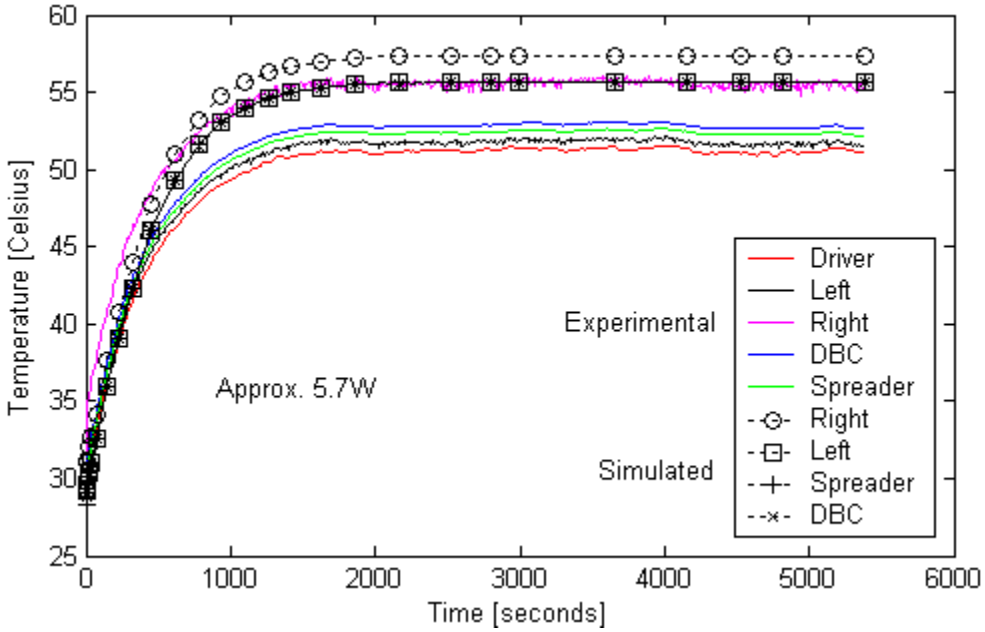


Figure 3.12: Slow-transient simulation results for 5.7W applied at the "right" chip.

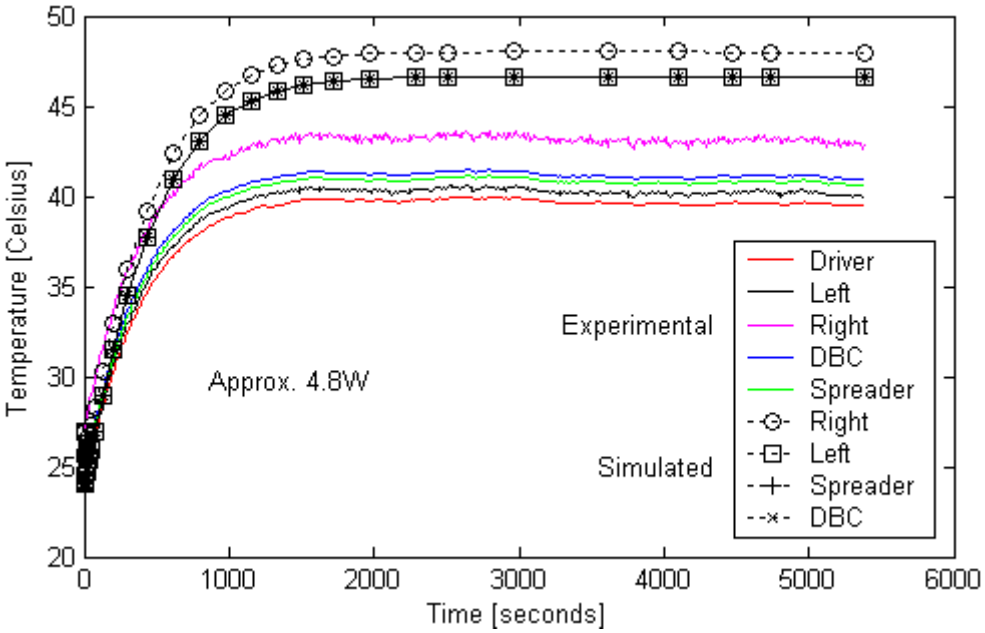


Figure 3.13: Slow-transient simulation results for 4.8W applied at the "right" chip.

CHAPTER 4

THE NIST FAST-TRANSIENT EXPERIMENT AND MODEL VALIDATION

4.1 INTRODUCTION

It is not possible to put thermal transducers like thermocouples to perform thermal measurements within the IPEM structure due to its reduced size and embedded architecture. Thermocouples can be attached to the IPEM's outer surface at different locations, but only the ones attached on top of the copper traces that make contact with the MOSFETs electrical connections can be presumed to be as close as possible to the junctions, which are the critical points to measure in the whole assembly. The highest temperatures will be located at the junctions, where the power is being applied. It takes time for any generated heat to spread within the IPEM structure before it reaches any of the attached thermocouples. The glued thermocouples, in turn, need to adjust their own tip temperatures before any measuring instruments can compute their voltage differential and convert them to equivalent thermal readings. Although the thermocouples are quite sensitive and this process takes only a very short time in our case, their thermal reaction time is not fast enough to reflect the actual junction temperatures.

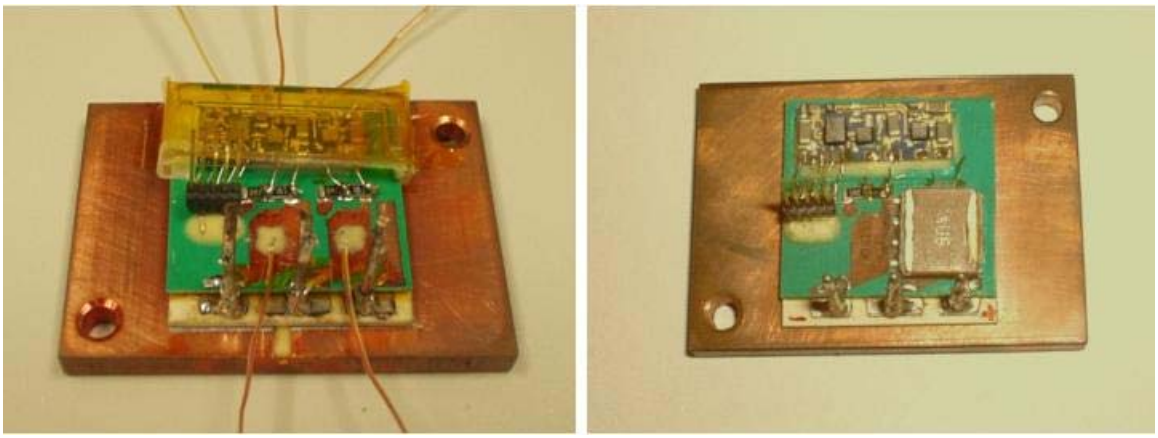
There are physical distances separating the junctions from the thermocouple tips, which affect the time that it takes for the generated junction heat to cross the material in order to be noticed in its true full magnitude. This problem is more evident if the power being delivered to the IPEM comes from fast high-power pulses, which could quickly heat up the junctions before the thermocouples could notice their actual temperature. This effect worsens as the transducers are placed farther from the heat source. For example, if a very high power pulse lasting just a few milliseconds or less is applied to one of the devices, a thermocouple attached at the top of the heat spreader would not even notice its presence until it had already burned the junction.

It is a known fact that the electric performance of most semiconductor devices can be noticeably affected by temperature changes. For example, in [Bagnoli et al. (2), '98] the p-n and Schottky junction voltages are treated as thermally sensitive electrical parameters suitable to be used as thermal sensors to characterize power electronic devices when an induced transient is applied. In the case of the IPEM MOSFETs, their gate voltage also changes as a function of the device temperature, and this voltage change can be easily measured. So, to cope with the fast-acting junction heat problem, the use of direct voltage readings from the silicon devices themselves can provide a fast-transient response profile of what is occurring in the close vicinity of their junctions. This method has proved to be useful for previous experiments on other devices ([Bagnoli et al. (2), '98], [Berning et al., '03]) and can be readily adapted for MOSFETs.

4.2 THE NIST EXPERIMENTAL SETUP

There were two IPEM prototypes available for this kind of electro-thermal experiment. Both were designed at VT. One of them has five thermocouples attached to it. A thermocouple was attached on top of the copper tracing of the each of the semiconductors in this particular IPEM. Due to the fact that the bus capacitor of the IPEM was obstructing the surface of one of the copper traces, this capacitor had to be removed prior to its shipping to UPRM in order to provide enough free space for the thermocouple to be glued. The other IPEM prototype has no thermocouples and came with its bus capacitor on place. This IPEM without thermocouples was used for the fast-transient experiment to avoid the disconnection and hassle of dealing with all the cabling that was already attached to the other one, and it was connected to all the instruments being used for the experimental setup in UPRM. Figure 4.1 shows these two prototypes; the five thermocouples cables can be seen in the left IPEM 4.1(a), and the location of the bus capacitor can be seen in the right one 4.1(b). The two thermocouples glued to the copper traces can be clearly seen in the left picture 4.1(a), with their cables coming out from the lower portion of the image. Only the left copper trace surface is easily accessible in the right IPEM 4.1(b) if a thermocouple were to be glued on it, but the capacitor is blocking the access to the other copper trace to the right because it is placed right on top

of it. Both IPEMs came with a small plastic cap to protect the gate driver circuitry, as shown in the left picture 4.1(b) at the top. The right one shows the driver board without it.



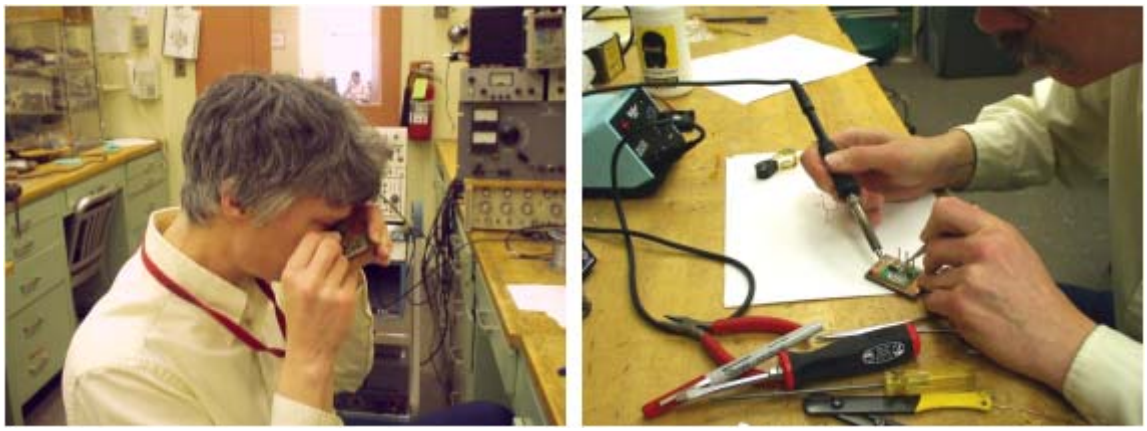
(a) (b)

Figure 4.1: The two IPEM prototypes available for the electro-thermal experiments.

Part of the instrumentation needed for the fast transient measurements was not readily available in UPRM when the decision to perform the fast-transient experiment was taken. Because of that, the chosen prototype was sent to the NIST facilities to undergo the measurements, all the process to be performed under the supervision of Dr. Allen R. Hefner and Mr. David W. Berning. They have performed and perfected the methodology for this fast-transient measurement procedure previously for other devices [Berning et al., '03].

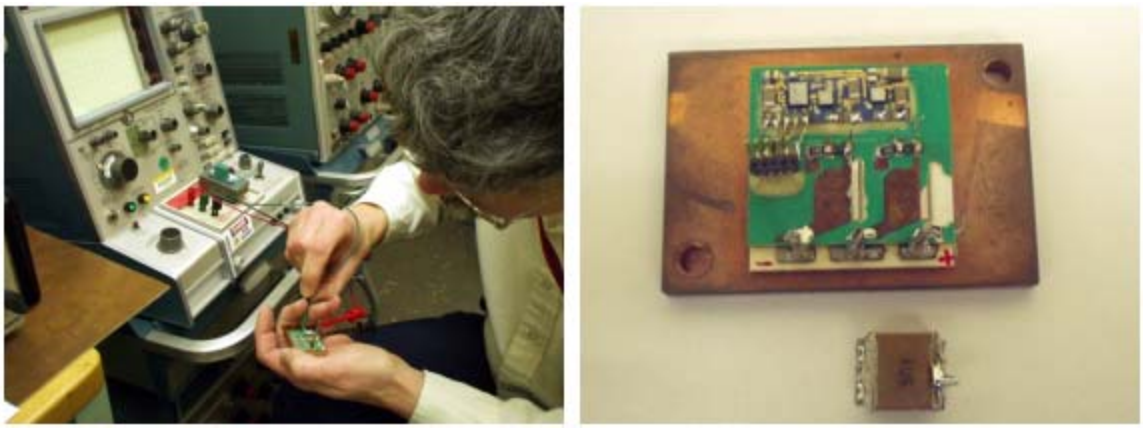
The first task performed was to visually analyze the provided IPEM prototype to check how to make the necessary connections to the silicon devices. After a quick revision with a magnifying glass (see Figure 4.2-a), it was determined that there were two thin film resistors connected to the gate of each device: one was approximately 10kΩ, and the other one about 1Ω. These findings were corroborated by means of a multimeter, after disconnecting the devices from the gate driver circuitry. It was also found that the bus capacitor would be interfering with the experimental process, and was removed from the IPEM (see Figure 4.2-b). This was necessary because the kind of electrical test to be performed requires both the semiconductor devices to be electrically isolated from any other electrical energy-storing elements. Finally, the isolated semiconductors were tested

with a curve tracer to be sure they were working properly. Figure 4.3 (a) shows this procedure, and the IPEM, as it came out of this inspection process and finally prepared for the experiment, is shown in Figure 4.3 (b).



(a) (b)

Figure 4.2: Visual inspection of the components (a), and bus capacitor unsoldering (b) for the IPEM.



(a) (b)

Figure 4.3: Curve tracer analysis (a), and bus capacitor already removed (b) from the IPEM.

An experimental setup was readily prepared to measure the many different devices and modules at NIST laboratory facilities. The NIST electro-thermal experiment can be separated into two main components: the electric circuitry and instrumentation used to perform and control all the necessary signals and voltage measurements, and the heating plate and temperature controller which are used to provide the necessary heating processes and temperature control characteristics for the experiment. There was no

evident problem with the connections or the settings for the electrical portion, but to ensure a good contact with the heating plate, a custom-made supporter to hold down the IPEM structure firmly was created. A piece of flat metal sheet was drilled in order to create a square hole from which the IPEM electrical connections could be accessible, but the metal sheet had to be wide enough to cover the IPEM heat spreader surface area to leave enough material to press it against the plate. Once the holding supporter was finished, a small electrical connections port was attached to allow for more available connection points firm and strong enough to withstand the manipulation of measurement cabling and the soldering of other discrete electrical components needed for the setup (see Figure 4.4). This had to be done to avoid damaging the delicate gate connections that came originally soldered to the IPEM.

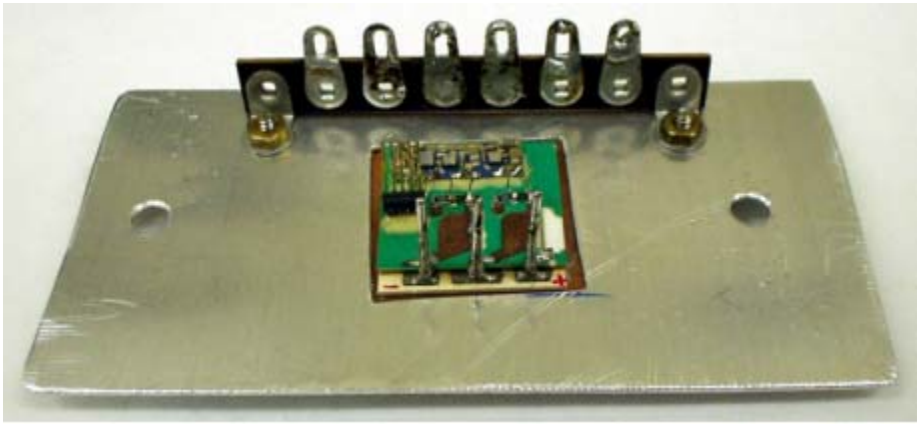


Figure 4.4: Drilled metal plate used as a supporter for more connections and to press down the IPEM.

The IPEM heat spreader was then impregnated with enough thermal grease before being mounted on the heating plate to improve the thermal contact between both elements. After this preparation, the IPEM was firmly attached to the heating plate, which is shown in Figure 4.5.

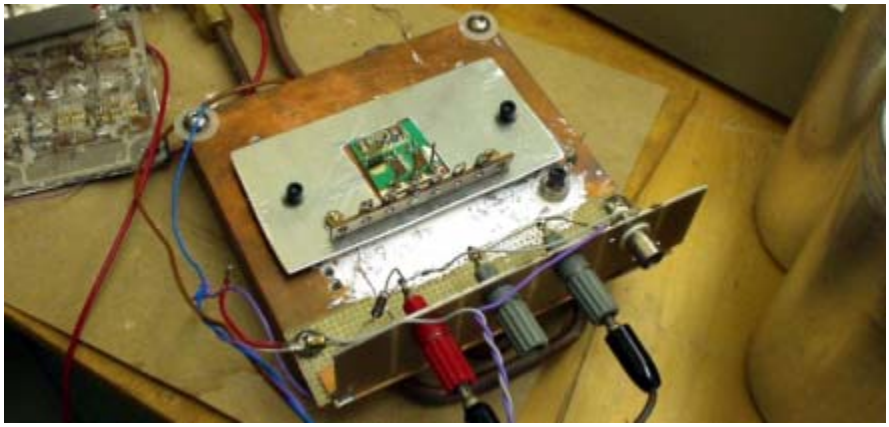


Figure 4.5: IPEM with holding metal sheet firmly positioned against the experimental heating plate.

The following step was to assemble the experimental electrical testing circuit. This circuit is simply a setup to provide for a series of testing power supply adjustments to the devices, provided that no adverse fluctuations could interfere with the measurement process. The circuit schematic and the testing instrumentation arrangement are presented in Figure 4.6. A high power DC voltage supply was used to provide the necessary voltage to the device, and a large bank of capacitors was held in parallel of it to control any possible voltage fluctuations and to ensure the availability of an electric charge supply if necessary. A custom-made current source, designed by Berning, was used to generate a train of pulses that would provide, together with the DC voltage source, the necessary power delivered to the MOSFETs junctions. The high power voltage source and the custom-made current source are shown in Figure 4.7. The bank of capacitors and most of the electrical instrumentation connections already placed can be seen in Figure 4.8.

The current source can attain currents of up to 20 amperes, and could be controlled by an external triggering signal to generate the train of pulses or to work as a DC current source if desired. The rest of the circuit provides for certain voltage adjustments and bypasses for the oscilloscope connection leads.

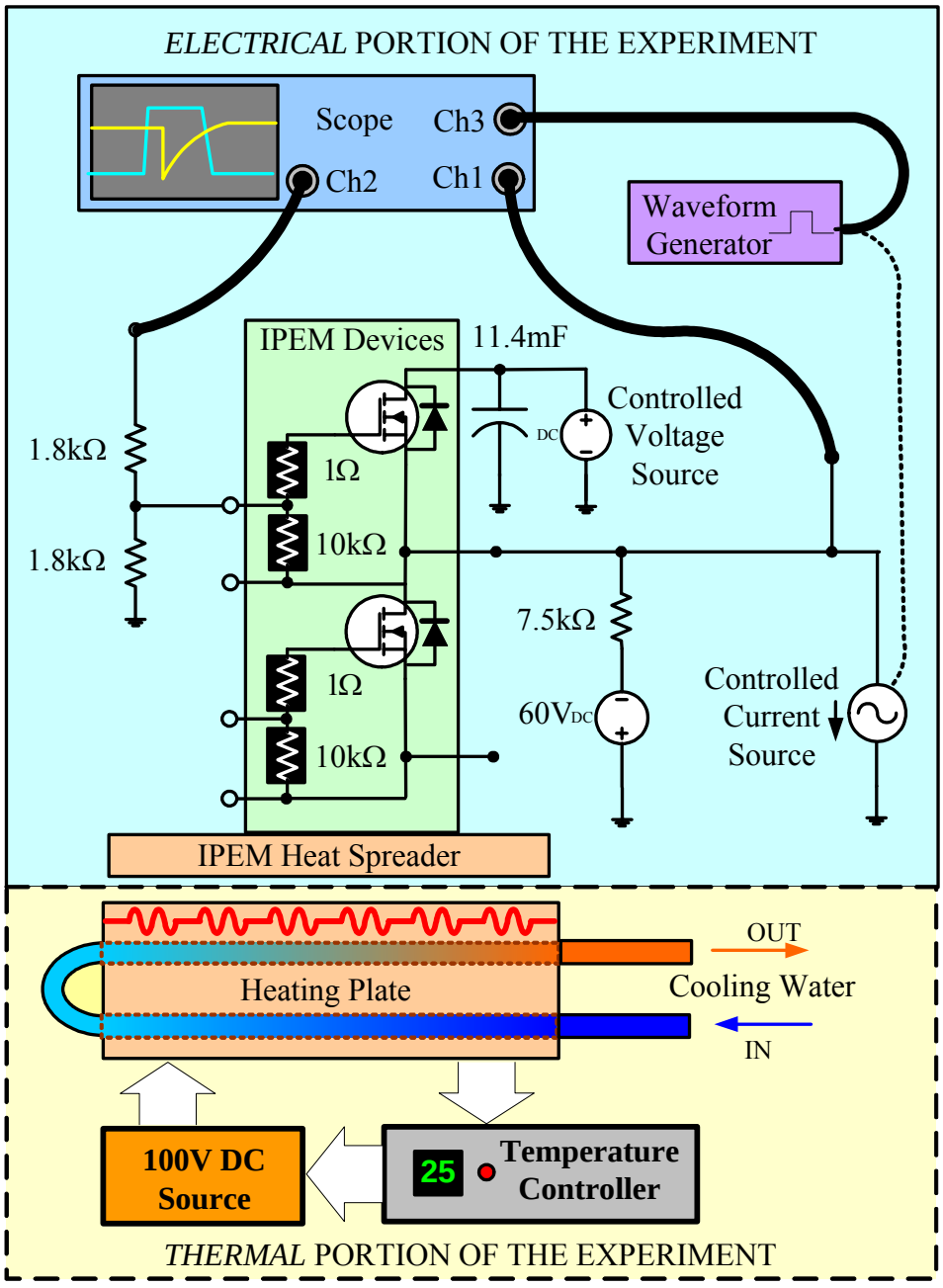


Figure 4.6: Schematic of the NIST experiment for the IPEM.

Figure 4.7: DC Voltage Source (left, bottom) and D. Berning's Current Source (right).

Figure 4.8: IPEM with all connections to the plate and bank of capacitors.

4.3 THE EXPERIMENTAL PROCEDURE

The same complete electro-thermal test had to be performed on each MOSFET individually; the left device was chosen to undergo the process first. Two main steps were required to make the complete fast-transient electro-thermal measurements:

1. Each device was slowly but uniformly heated within a certain temperature range to acquire its gate voltage as a function of temperature, thus creating a series of voltage-to-temperature experimental calibration curves for different tested power levels.

2. A series of power pulses, equal in magnitude to the ones used for the calibration curves, but with certain necessary frequency adjustments, were applied to the device to measure the electrical response at the gate. Then these responses were interpreted according to their respective calibration curves to obtain a temperature profile that appears at the gate during the pulse duration.

The tests were performed during a period of four days. The first day was devoted mostly to set all the experimental circuitry and instrumentation as shown in Figure 4.9, and to perform a couple of preliminary tests to check that the readings were properly working. The remaining days were used to acquire data and to analyze the circuit behavior in case that some adjustments were still necessary.

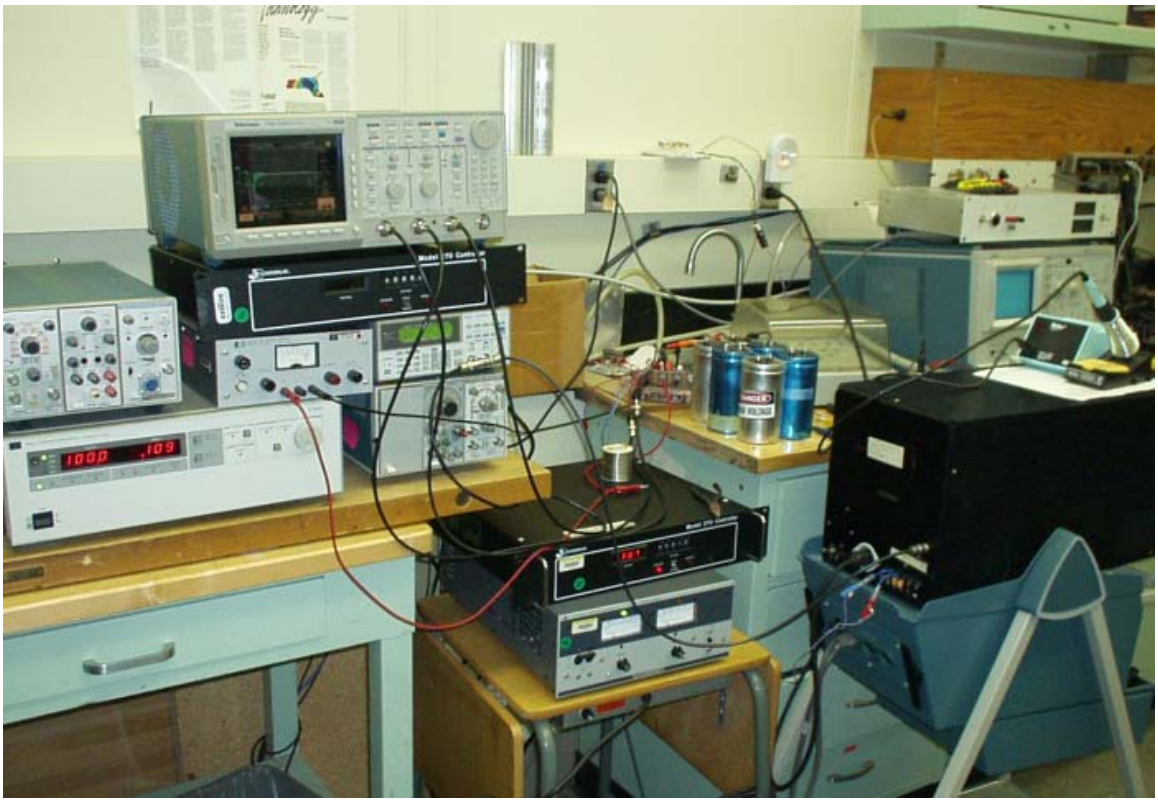


Figure 4.9: View of the complete fast-transient experimental setup at NIST.

4.3.1 DETERMINING THE JUNCTION TEMPERATURE CALIBRATION CURVES

A series of junction temperature calibration curves is needed to characterize how the gate voltage in the silicon devices changes according to the temperature of the device. The process to obtain these curves was simple, and most of the procedure was computer-controlled. The computer interface used to obtain the calibration curves can be seen in Appendix D, Figure D.7. Each test required a starting point at a temperature value lower than the temperature at which the first sample would be. For some of the first tests, the initial temperature was set to 20°C. The heating plate had to be cooled down below this temperature before starting the experiment. The mechanism used to cool down the plate was to let chilled water run through a series of embedded copper pipes within the plate. Part of this piping system can be seen in Figure 4.10. One of the internal coils is shown as it emerges to return again into the plate. The straight tubing for the input and output lines can also be seen to the right.

The cooling process was done manually because no automatic water flow control was available for the water chiller system valves. The temperature controller shown in Figure 4.11 can only be used to heat the plate but the temperature sensor was used in the cooling procedure.

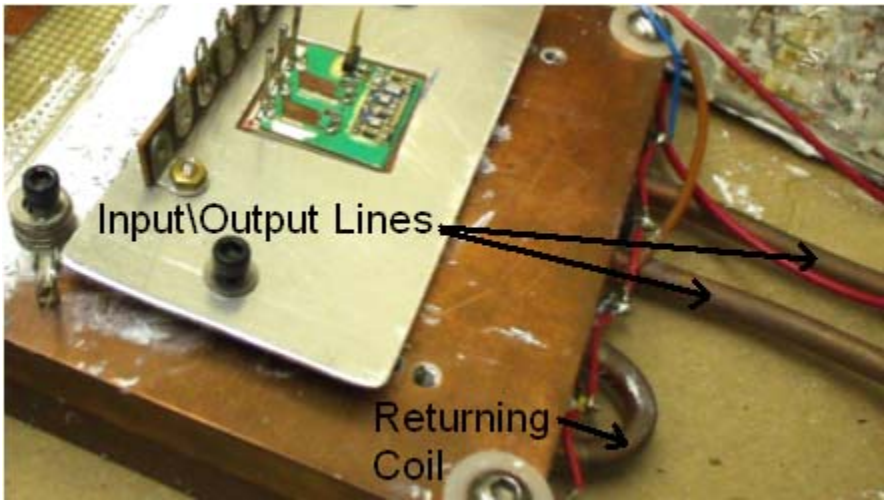


Figure 4.10: IPEM attached to the heat plate, showing part of the cooling pipes (right).

The controller temperature sensor was monitored to be sure that the temperature was well below the needed initial 20°C, usually down to about 13°C to 17°C. Once this happened, the water faucets were closed and the automatic computer control quickly turned on to perform the required measurements to avoid letting the ambient temperature heat up the plate again.

Figure 4.11: Temperature Controller (top) and 100V DC source (bottom) for the heating plate.

This test required an extremely short power pulse in comparison to the ones needed for the later *electrical* portion of the experiment. For all power combinations used to generate the calibration curves (for example 100V @ 2A, 200V @ 5A, etc.), the current source was triggered by a signal generator previously set to generate a 300Hz square pulse @ 1% duty and 5 V in magnitude. The current source would generate a similar pulsed signal, but its magnitude had to be set manually to the desired value before the experimental measurements could take place. Depending on the desired tests, source current values could be set from 2.5A up to sometimes 20A.

Once the initial setup was finished, the first step in the automatic part of the experiment was to command the temperature controller to raise the temperature of the heating plate to the desired initial 20°C. The computer monitored the controller until the desired temperature value was reached. The controller heated the plate by controlling a 100V DC source used to power up the resistive elements within the plate. At that moment, the gate voltage readings were collected using the oscilloscope. Then, the

incoming signal waveform read from the oscilloscope screen was averaged, and that value was recorded as being the 20°C voltage equivalent for the given power level.

This process was repeated at increments of 2°C up to 95°C. This high limit was chosen to prevent the water inside the heat plate pipes to reach the boiling point. In this case, the instruments would record up to the 94°C mark, and then stop the process turning off the high power DC voltage and the temperature controller. The process would be repeated for other power levels if needed.

Several curves were made for the *left* silicon device using this procedure. The collected data is presented in Figure 4.12. Some discrepancies were found between the curves obtained during the first day of measurements and the curves recorded during the following days for the same power combinations. An evident shifting occurred to the second day measurements, but Dr. Hefner recommended to take a couple of measurements more before performing the *electrical* part of the experiment to avoid losing valuable time. The calibration procedure was exactly the same for the *right* device, whose curves are presented in Figure 4.13. In both devices the use of higher current magnitudes produced curves with irregular behavior. Low-current and low-power measurements behaved accordingly to this expected trend. It was recommended by Dr. Hefner to use the low-amperage curves for the analysis of later experimental voltage readings, due to the uncertainty of the high-current results.

Polynomial curve fitting was applied to all the calibration curves in order to obtain equations to perform the transient voltage to transient temperature conversion by the test software. Quadratic fitting proved to be good enough to represent most of the data due to the smooth continuity and soft concavity of the recordings. Numerical approximation results are presented in Table 4.1. The shifting present in some curves measured initially could be due to the time needed for the instruments to set their internal temperature from the moment that they were turned on during the evening of the first day of measurements. The shaded values in the table represent curves that should be rejected for different reasons. Some of the curves that were generated by erroneous readings can be identified just by graphical inspection.

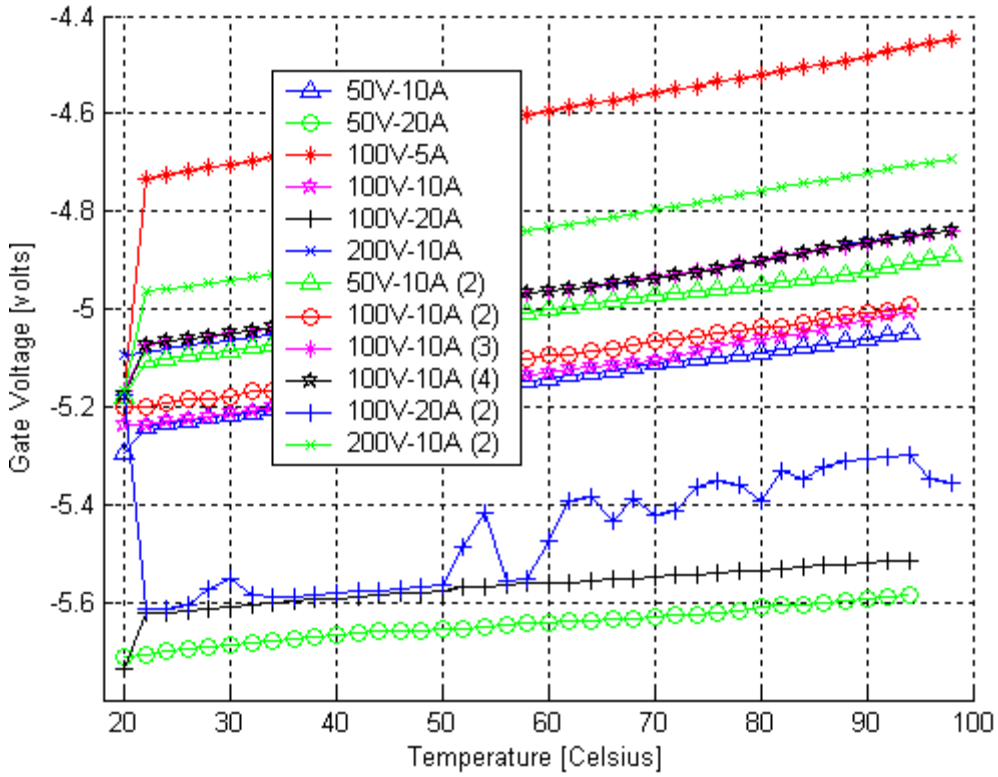


Figure 4.12: Experimental calibration curves for the *left* device at various power levels.

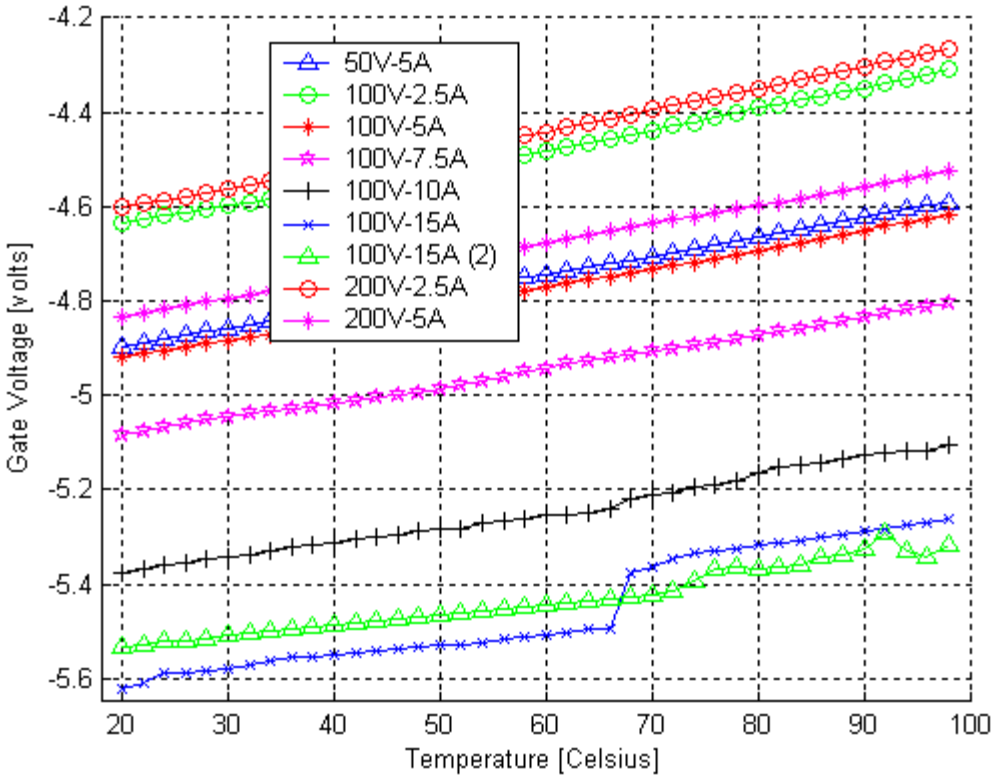


Figure 4.13: Experimental calibration curves for the *right* device at various power levels.

Table 4.1
Curve Fitting for all the Experimental Calibration Curves

$Vg(V,I,T) = a \times 10^{-5} T^2 + b \times 10^{-3} T + c$						
Voltage V (Volts)	Current I (Amperes)	Iteration #	*Left* Device			
			a	*b*	*c*	R^2 (%)
100	5	1	1.9263	6.6628	-4.7374	99.97
200	10	2	1.0336	6.8810	-4.9750	99.95
100	10	2	2.2724	4.7716	-5.2022	99.91
50	10	1	0.3091	5.0956	-5.2427	99.89
50	20	1	**-0.0998**	3.0794	-5.7021	98.85
200	10	1	1.0118	6.2225	-5.0948	99.84
100	20	1	**-1.7843**	3.6674	-5.6270	99.84
50	10	2	0.5929	5.3143	-5.1120	99.84
100	10	3	2.3388	5.1602	-5.0754	99.83
100	10	4	2.3386	5.1603	-5.0754	99.82
100	10	1	5.1678	4.2130	-5.2350	**99.71**
100	20	2	1.5910	8.5857	-5.6434	**88.24**
Voltage V (Volts)	Current I (Amperes)	Iteration #	*Right* Device			
			a	*b*	*c*	R^2 (%)
200	2.5	1	0.8123	3.3514	-4.6704	99.98
100	2.5	1	0.9052	3.0990	-4.6996	99.98
200	5	1	0.2079	3.7009	-4.9073	99.97
100	5	1	0.4101	3.3709	-4.9878	99.97
50	5	1	0.3118	3.5218	-4.9655	99.97
100	7.5	1	0.5342	2.9394	-5.1414	99.89
100	10	1	1.2862	1.9916	-5.4154	**99.48**
100	15	2	1.7054	0.8604	-5.5522	**97.68**
100	15	1	3.6191	0.7232	-5.6412	**94.02**

The extremely irregular curve shown at the bottom of the *left* calibration curves plot is a clear example of a bad reading. It was included on purpose to show some of the erroneous measurements that appeared sometimes. Many of these readings were aborted during the collection process. In other cases the errors were not so evident. For example, the "a" coefficient for some of the *right* device curves was negative for some of the quadratic fittings, although the curves look very smooth. That meant that those curves were concave, while the vast majority of the others had a positive "a" value. A value of R^2 lower than 99.8% was also a sign of recorded samples spreading away from their main series trend line. There were some curves that show many of their samples deviating from linear behavior. This disruption appeared, in particular, in most of the high-current measurements.

An inspection of the results shows that the best fittings were obtained for the measurements with the lower current ratings. Among them, the 2.5A were the lowest, and both were measured for the *right* device. But these two 2.5A curves were not enough to represent various power combinations needed to further validate our IPEM model. To solve this problem, both curves were used to derive a complete family of 2.5A calibration curves from voltages ranging between 50V to 300V, thus generating different supplied powers to analyze, ranging respectively from 125W to 750W. This was possible because both the measured curves were almost parallel, and the coefficients of the remaining curves could be found by means of interpolation, using the fitted coefficients of the two available curves. Following this approach, the whole family of 2.5A curves for the *right* device could be represented with a single voltage-dependent quadratic function, shown in Equation 4.1. The generated family of curves obtained from this numerical manipulation is shown in Figure 4.14.

$$Vg(V,T) \approx \left\{ \begin{array}{c} (0.998\times10^{-5} - 0.9287\times10^{-8}V)T^2 \\ +(0.0028 + 0.2523\times10^{-5}V)T \\ -4.7289 + 0.0003V \end{array} \right\} \Bigg| I = 2.5A \qquad (4.1)$$

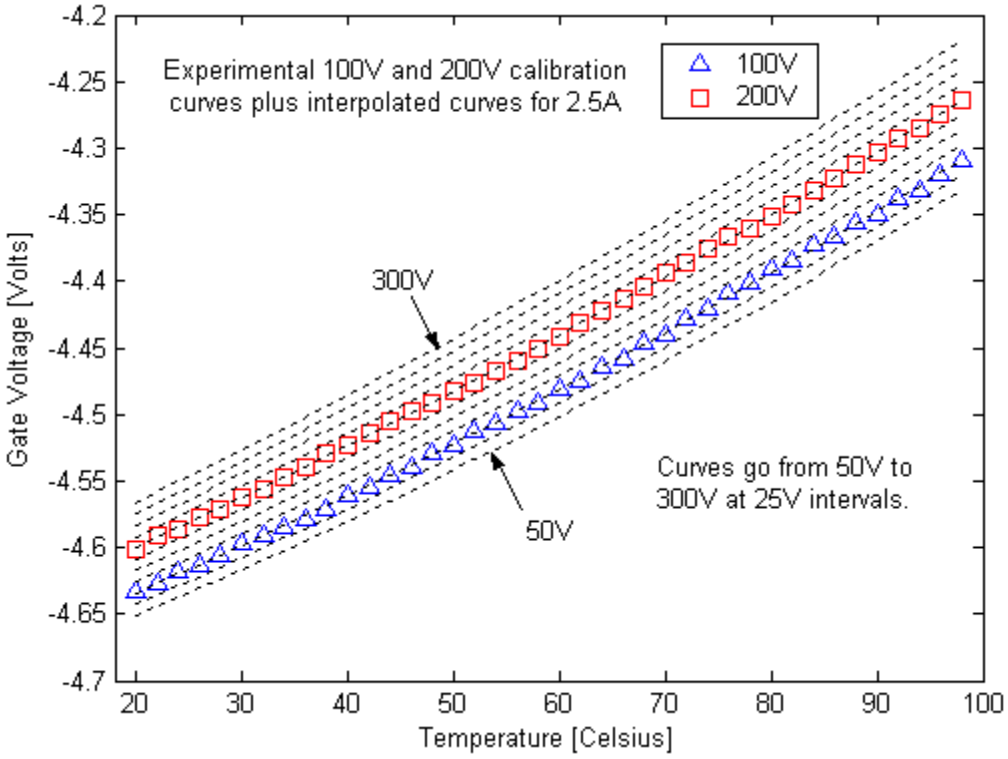


Figure 4.14: Generated family of 2.5A calibration curves for the *right* device.

4.3.2 THE ELECTRICAL PULSES MEASUREMENT

For the gate voltage pulse measurements in the *electrical* part of the experiment, the constant 300Hz pulse train triggering the current source was tuned according to the information provided by the calibration curves for the power level to be tested. The calibration curves show the gate voltage range that can be obtained for a particular current-voltage combination, all of them basically for the same temperature range. The maximum and minimum gate voltages attainable for each calibration curve are related to the temperature range shall we expect the device junction to heat up when a particular power pulse is applied to the device. To get sufficient thermal information from the electrical pulse test, we need to let the device heat up enough during the time that the pulse is kept on. Much care should be taken in order to avoid letting the pulse stay on for too long; otherwise, the device will exceed junction its temperature rating and burn off.

The way to avoid overheating was to initially set the applied power pulse with a frequency high enough to be sure that no excessive heating could be generated. For

example, 30Hz proved to be good enough as an initial guess. All tests would use again the same 1% duty for the triggering pulse square wave applied to the current source in the previous calibration measurements. Before making any recordings, the heat plate was set in manual mode at an almost constant 25°C temperature to use as a common base temperature for all the transient measurements to be performed. This would provide for a temperature control in the complete IPEM structure, which would only heat mainly at the silicon devices due to the applied pulses, and quickly restore its whole temperature back to the dominant 25°C of the experimental setting.

The question about how to determine the best pulse frequency for a particular power pulse can be answered by visually checking the gate voltage pulse-response waveform in the oscilloscope screen during the pulse duration. Its voltage extremes should be separated by no more than the voltage difference of the calibration curve extremes of its respective voltage-current calibration curve. For most of the calibration curves, the gate voltage difference between their minimum and maximum extreme values never exceeded 300mV. This can be seen by inspection of the calibration curves plot. For example, in the 200V calibration curve in Figure 4.14, the lowest and highest extremes are approximately located at (20°C, -4.6V) and (98°C, -4.275V) respectively. That means that heating up from 20°C to 98°C is equivalent to a 300mV difference between the initial and final points of the pulse voltage readings in the oscilloscope. Instead of being a perfectly square pulse, the gate voltage pulse-response waveform has a conspicuous exponential-shaped slope when allowed to heat up safely. As time went by during the on state of the pulse, the temperature of the device changed and the gate voltage also did accordingly.

The initial temperature at the rising corner of the pulse should be equivalent to the dominant 25°C of the heat plate, and just when the pulse goes off will reveal how much the device was heated up during the pulse duration. Comparing the final gate voltage value with its respective location in the corresponding calibration curve is the method used to find the temperature value. The power pulse frequency should be changed slowly and carefully, always checking that the final voltage of the pulse never exceeds the

maximum value that is equivalent for the highest temperature in its respective calibration curve. This would assure no junction overheating.

The fast-transient electrical measurements could finally be performed as long as those security steps were followed during the process. Figures 4.15 and 4.16 show some of the curves captured by the oscilloscope for the *left* device for current pulses of various frequencies and using different voltage combinations. Notice that as the pulse power increases so does the frequency to avoid overheating. Unfortunately, during the measurement process, a momentarily disruption of the triggering pulse signal to the current source left the latter acting as a constant DC signal and such high current immediately damaged the *left* device. The current source always remains turned on unless manually set off or at standby. No more fast-transient voltage curves could be retrieved other than the few ones shown in Figure 4.15 after that accidental surge.

Nevertheless, enough curves were collected for the *right* device to analyze the IPEM thermal behavior. It is interesting to observe that pulses of the same power but different voltage and current do not generate the same transient-voltage response, even when the same frequency is used. That can be clearly observed in both the 1Hz (250W) and both the 2Hz (500W) measurements shown in Figure 4.16. However, when using the corresponding calibration curves to compute the thermal transient, that effect is compensated. The transient temperature calculations are performed only with the curvilinear portions of the pulse responses. Figures 4.17 and 4.18 show these portions isolated from the rest of the oscilloscope flat readings, and time-shifted to set the initial corner of their curves to start at the origin in the time coordinate.

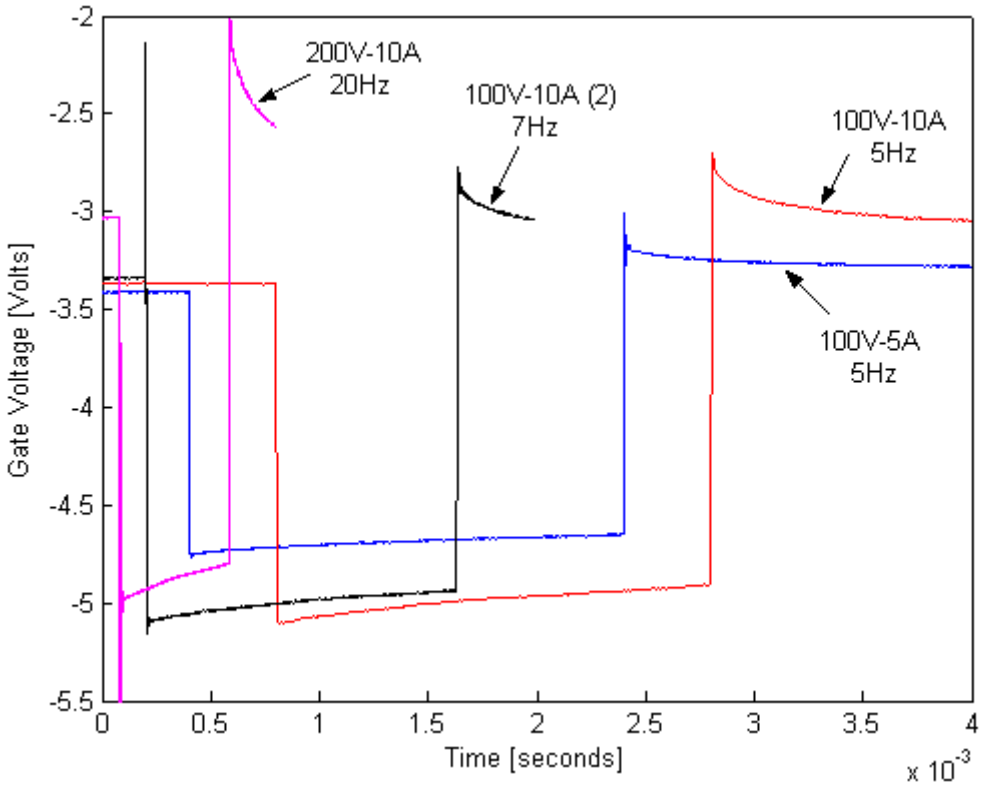


Figure 4.15: Left transient voltage curves for various powers and frequencies.

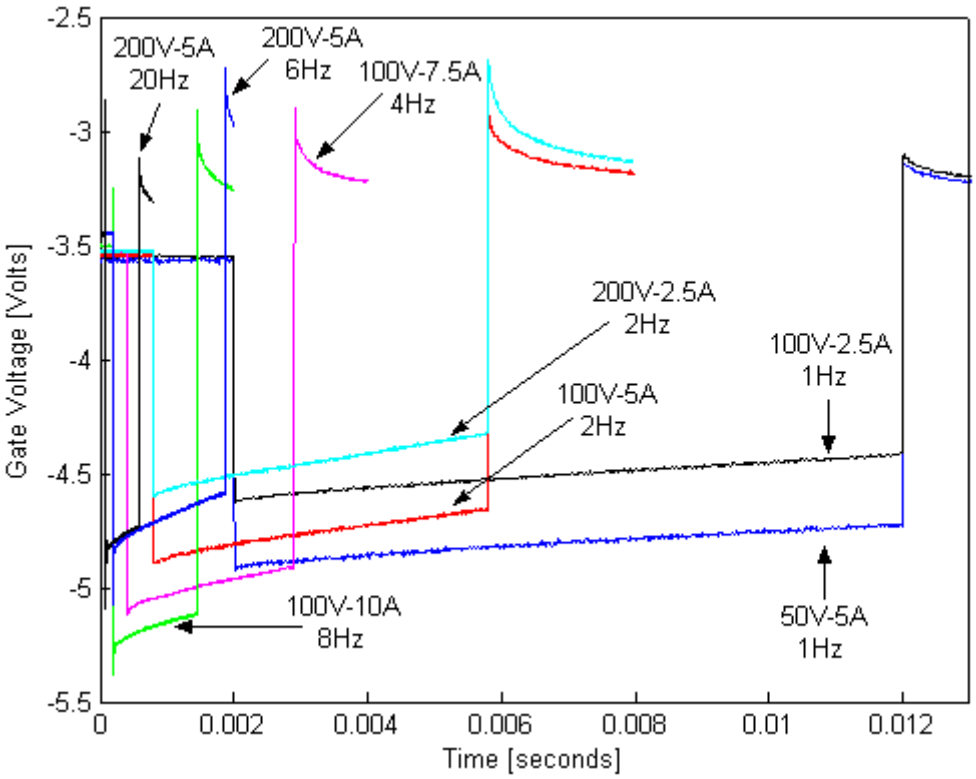


Figure 4.16: Left (top) and Right (bottom) transient voltage curves for various powers and frequencies.

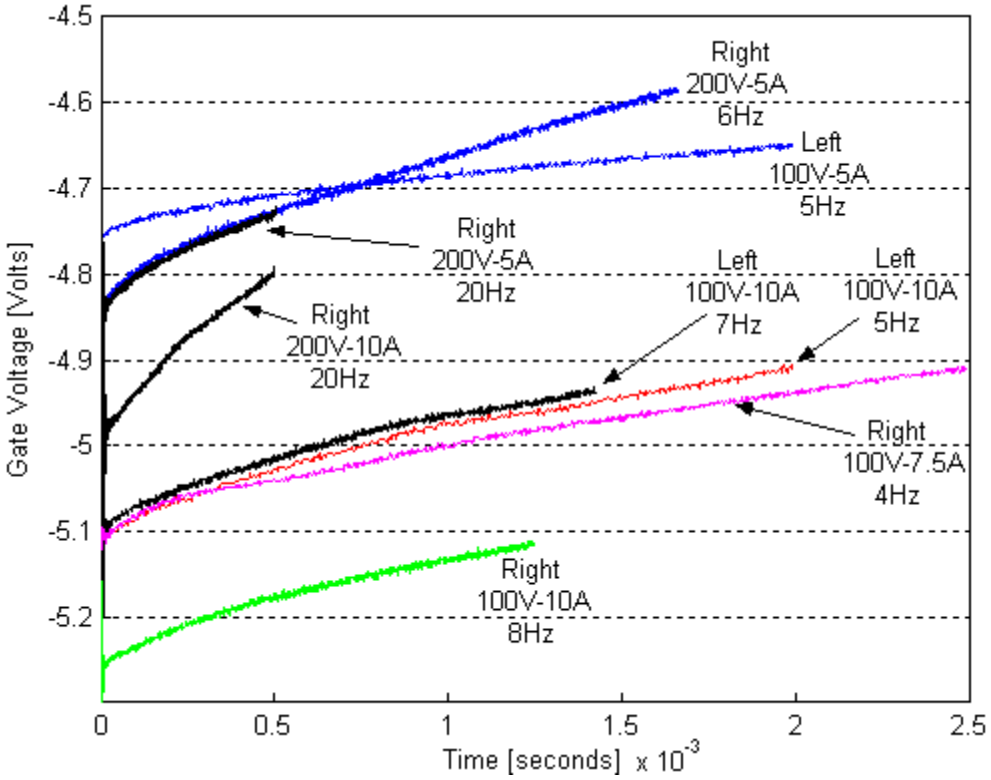


Figure 4.17: Isolated 4, 5, 6, 7, 8, and 20 Hz curvilinear pulse portions of the curves in Figure 4.16.

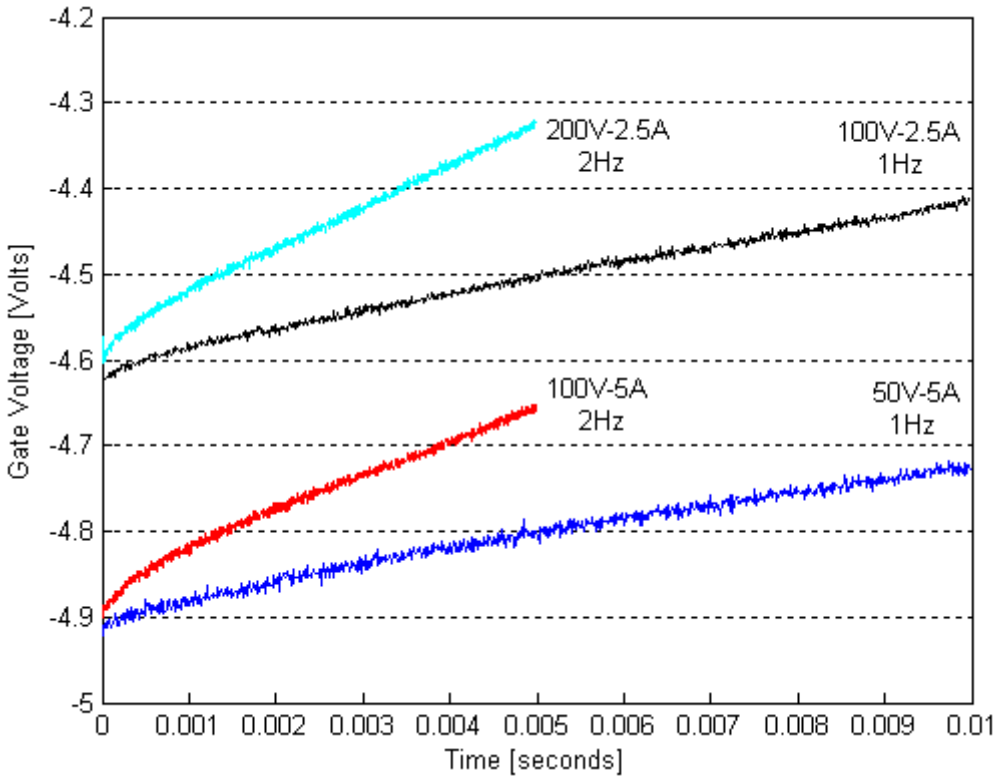


Figure 4.18: Isolated 1 and 2 Hz curvilinear pulse portions of the curves in Figure 4.16.

If these adjusted curves are transformed according to the voltage-to-temperature relationship determined from the calibration curves, a temperature response will be generated and shown in Figure 4.19. Once these temperature profiles are plotted together, the effect of the calibration curve shifting can be better understood. Since the base temperature for the whole setting was supposed to be set to approximately 25°C, is should be expected for all pulses to begin at that temperature. All the temperature curves having a starting point different from that base temperature are a possible product of a shifted calibration curve, like the ones starting approximately at 40°C, 60°C, and 90°C. The one staring below zero is even worse. The device has no way to be cooled down experimentally to such freezing temperatures. That curve is definitively unacceptable as a result.

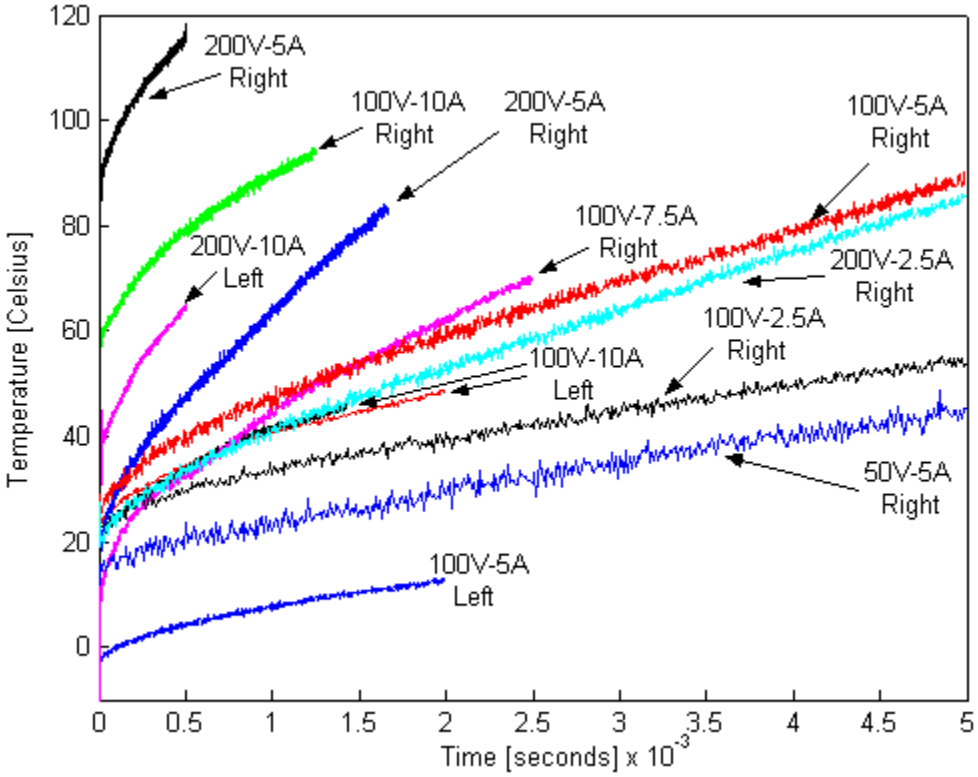


Figure 4.19: Temperature equivalents for the voltage curves shown in Figures 4.17 and 4.18.

If all the corresponding calibration curves were correct, instead of being all mixed and overlapped like shown in Figure 4.19, the temperature curves would look like the modified plot presented in Figure 4.20. The modification done on the curves was to adjust their initial measured value so that all temperatures would start from a similar point in the graph, this to show how curves at the same power should overlap.

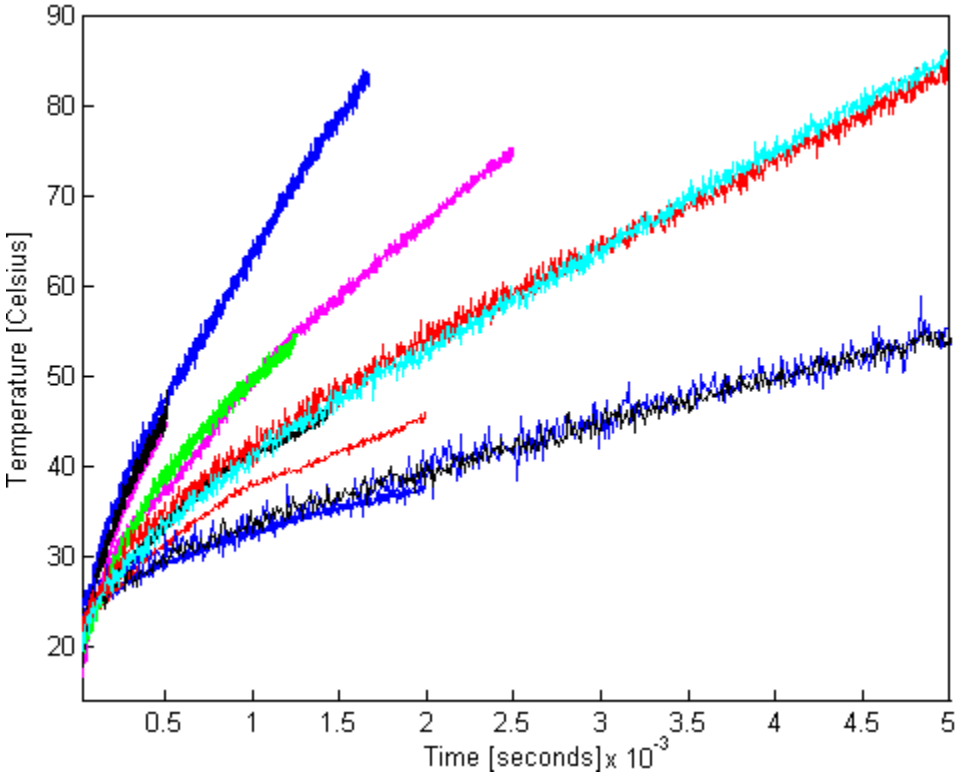


Figure 4.20: Ideal temperature results that were expected for the measurements obtained in Figure 4.16.

Nevertheless, it can be seen by inspection that most of the curves in Figure 4.19 still start close to the 25°C mark. Dr. Hefner analyzed all those curves and recommended the 2.5A curves for the IPEM model validation because they showed a uniform slope and coincided better at the origin than others. The process of obtaining the oscilloscope pulse responses generated the set of curves shown in Figure 4.21. By applying the interpolated family of curves from Figure 4.14 to the isolated curve portions in Figure 4.22, a final family of corresponding temperature profiles was obtained, shown in Figure 4.23.

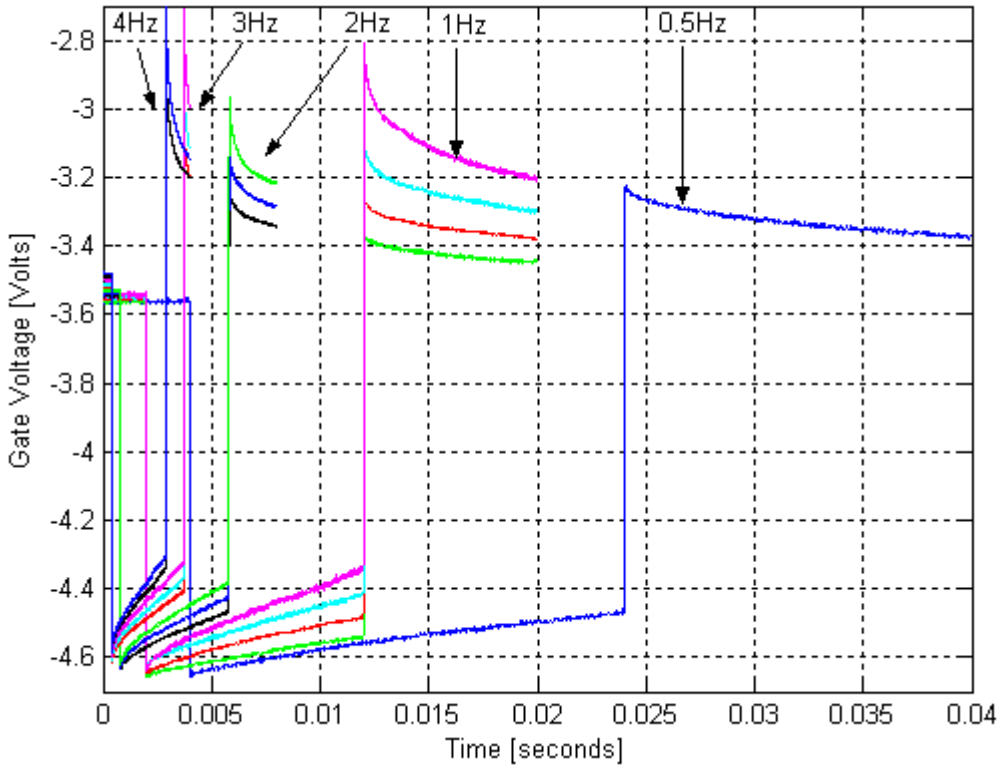


Figure 4.21: Oscilloscope readings for a family of 2.5A pulses at various frequencies.

All these pulses were generated under the same experimental conditions, during a short lapse of time. That is why the resulting curves behave as expected; that is, they all started almost at the same temperature and the pulse frequencies provided for enough heating time to allow the device to heat up almost to its maximum limit in many of the measurements.

With these final results, enough information was available to perform simulations with the same power variations used for the 2.5A experiments, and the temperature curves were long enough in terms of their time span to allow for graphical verification of the simulated values.

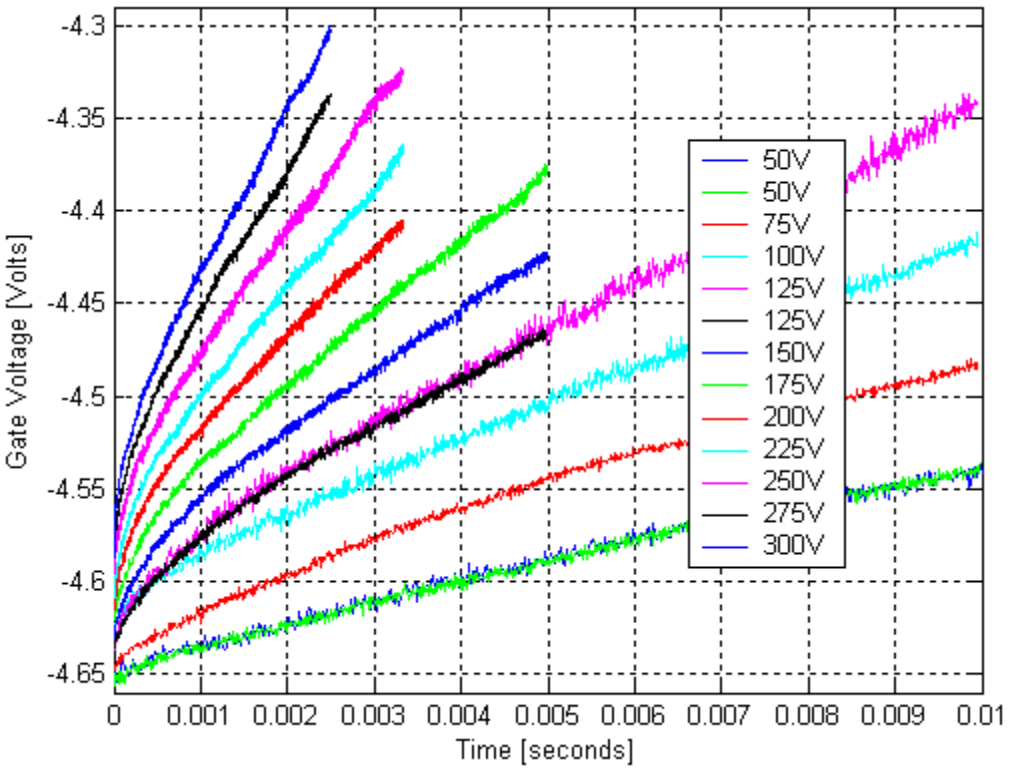


Figure 4.22: Isolated and identified curvilinear portions from Figure 4.21 readings.

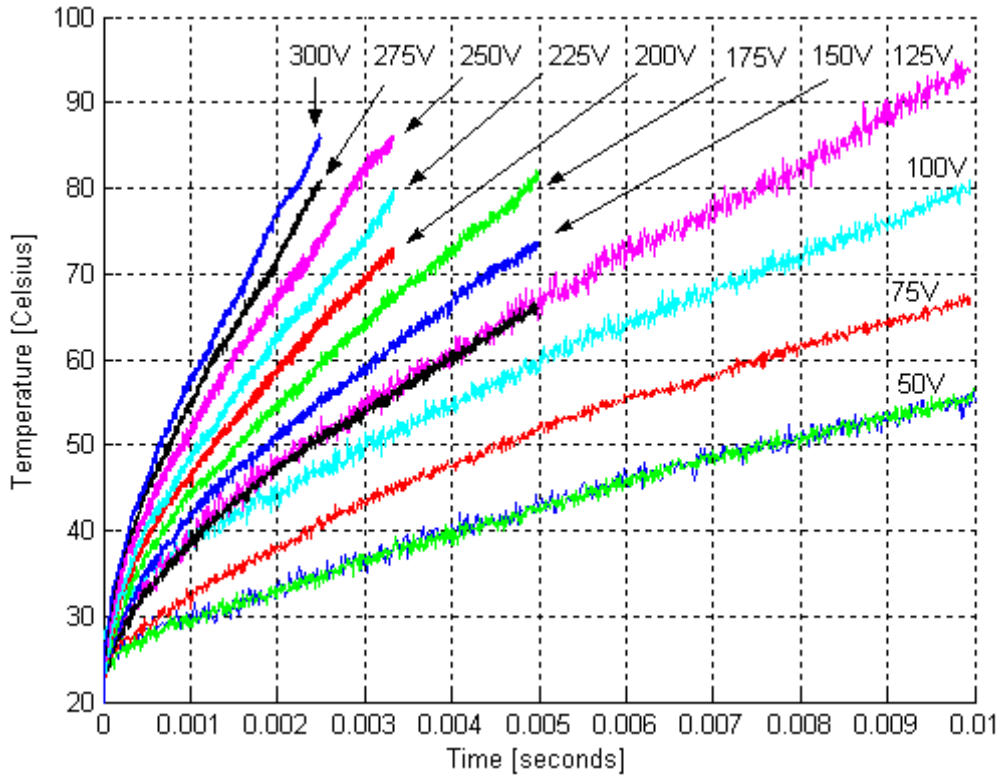


Figure 4.23: Equivalent temperature profiles for the gate voltage curves in Figure 4.22.

4.4 FAST-TRANSIENT VALIDATION RESULTS

Figures 4.24 to 4.26 are validation results obtained for the single-chip model presented in Figure 2.11 for the "right" chip. Figure 4.24 are the results obtained for the curves having 1Hz and 2Hz frequencies, which have the longest pulses from the measured data. These curves are the ones that represent how the heat reaches nodes located far away from the heat source, possibly down to the heat spreader. The 437W power level curve shows that our model is heating up faster at the beginning of the pulse, but then after about 2ms (for that specific level) it is not keeping the same temperature levels that the experimental data show. Apparently, it is cooling a little bit faster than expected as the pulse is reaching its end.

The same trend was found in all the other fast-transient simulations. The final temperature reached by the simulation falls almost 10°C below what is expected. This behavior was more noticeable with the lower power levels. The results obtained by [Berning et al., '03] also show a tendency in the simulated results to deviate from the experimental measurements with a tendency to cool faster than the actual device. Their work is based in the same model developed by Dr. Hefner that was used for the IPEM, but applied to an IGBT converter.

Figures 4.25 and 4.26 show the simulation results for the 3Hz and 4Hz frequency power levels respectively. It can be seen that, as the power level is increased, a better fit is obtained for the simulation results. But the same temperature trend is being noticed: the simulation heats up faster than the experiment at the beginning, and then cools down at the end of the pulse. This behavior could mean that the heat is encountering a higher thermal resistance than expected in the nodes close to the junction, where the heat is being generated, and that farther nodes are providing a better heat dissipation path than the corresponding actual IPEM layers, thus allowing for a faster cooling as the heat reaches deeper in the layers. It was expected for these simulated results to fit good enough to give an idea about the thermal behavior of the thermal component approach, but not to be very good since the model was not complete yet.

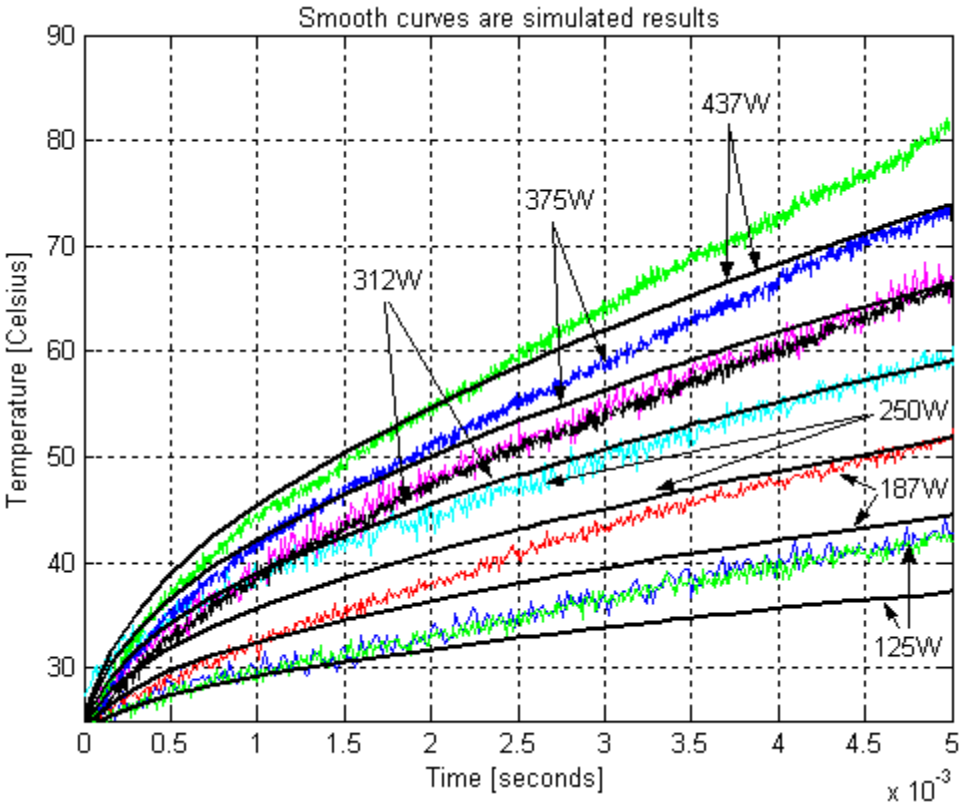


Figure 4.24: Single-chip results for the power levels with 1Hz and 2Hz frequencies.

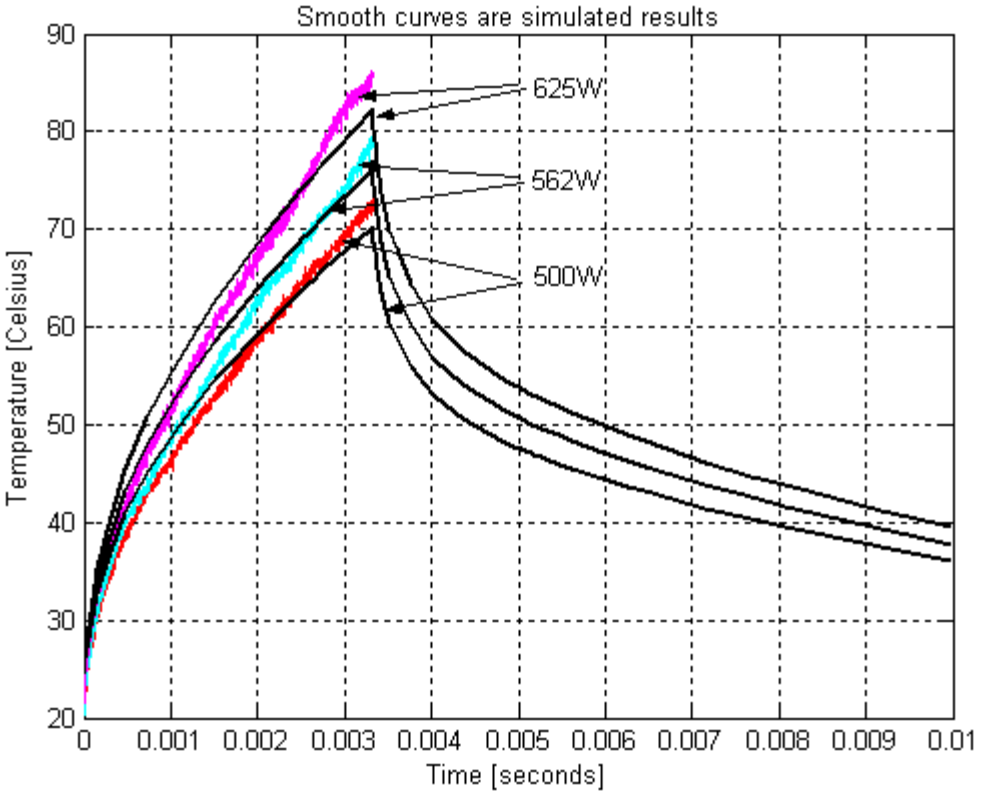


Figure 4.25: Single-chip results for the power levels with 3Hz frequency.

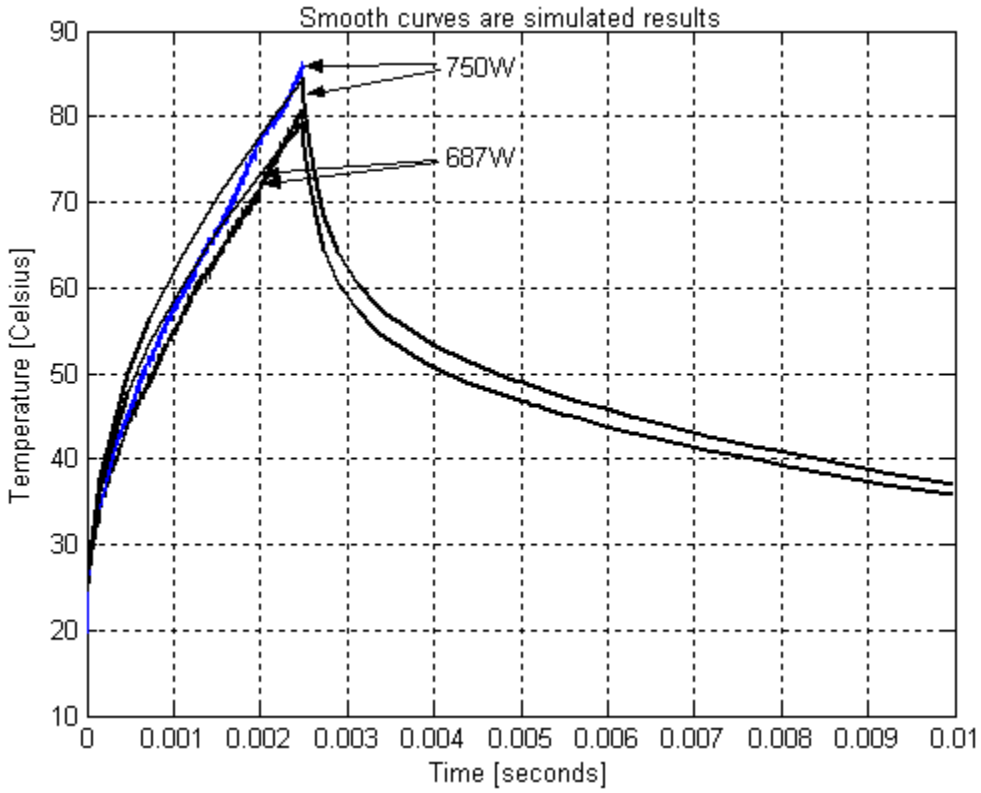


Figure 4.26: Single-chip results for the power levels with 4Hz frequency.

Figures 4.27 to 4.29 present validation results for the double-chip model of Figure 2.12. The curves show a better fit because the two-chip model is more representative of the actual IPEM, especially for the coupling that exists between the junction of the right chip and the header of the left chip due to the copper connection. This copper contact cools down the right junction slightly more by providing a direct path with better heat conduction than the silicon, and that is why the curves do not start with a steep slope as they did for the single chip-model. That can be seen when the curves in Figures 4.26 and 4.29 are compared. Nevertheless, the low power curves still deviate from their expected experimental slope by predicting lower temperatures from the beginning, only that this time some of the values had a better fit, like the 437W level in Figure 4.27.

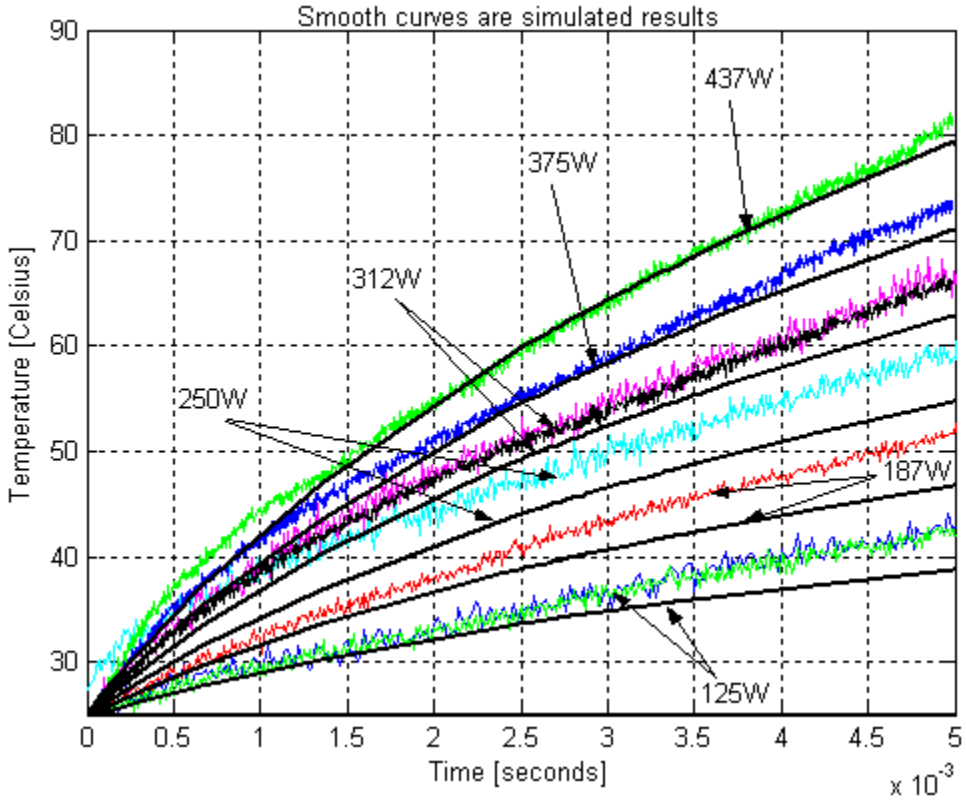


Figure 4.27: Double-chip results for the power levels with 1Hz and 2Hz frequencies.

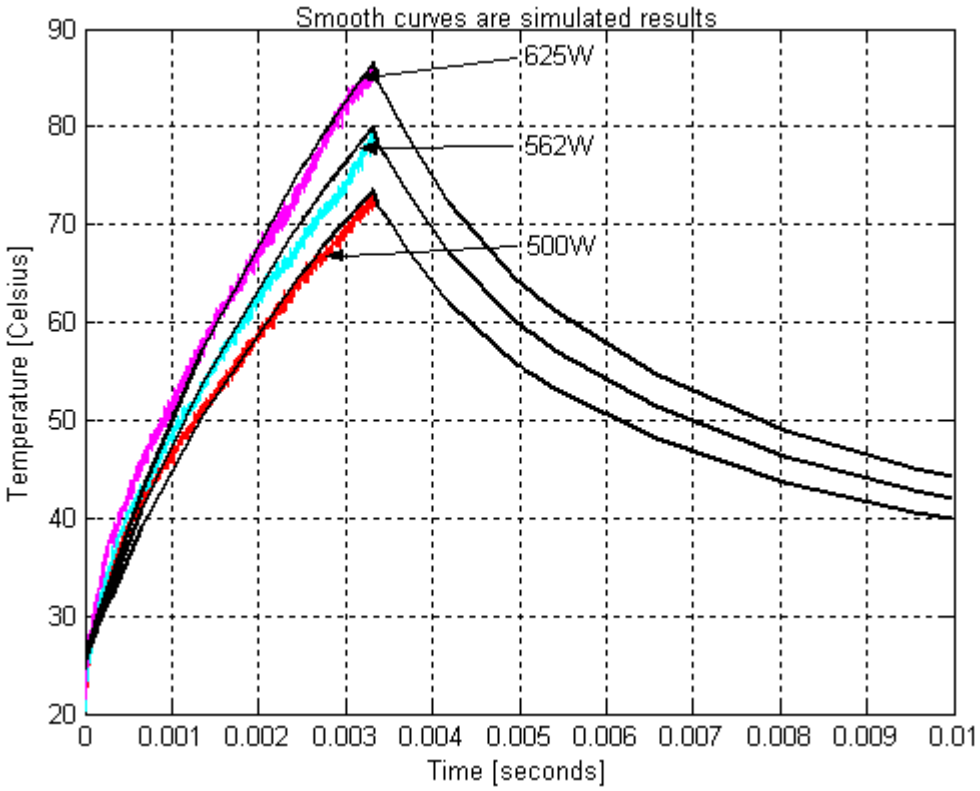


Figure 4.28: Double-chip results for the power levels with 3Hz frequency.

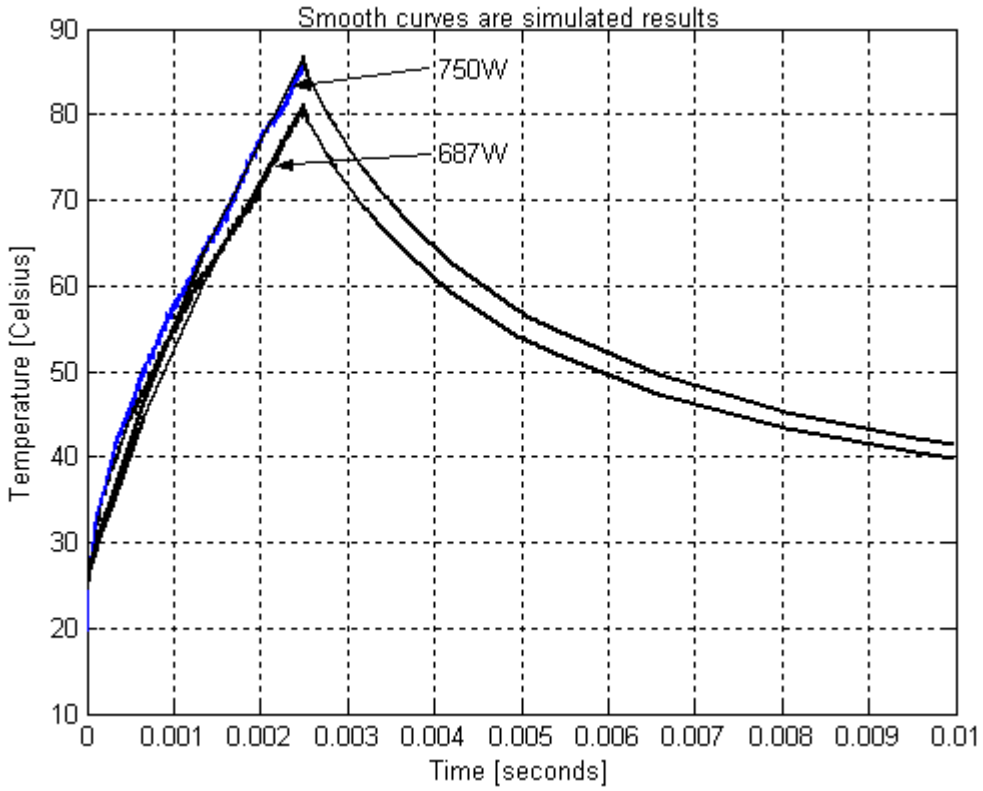


Figure 4.29: Double-chip results for the power levels with 4Hz frequency.

4.5 CONCLUDING REMARKS

In this chapter, the fast-transient experiment and thermal model validation were presented. First, the NIST fast-transient experimental setup was described, and then the complete experimental procedure was explained. The procedure to determine the necessary calibration curves and device voltages needed to generate the junction temperature profiles was described. A series of experimental measurements were shown to analyze the fast-transient behavior of the IPEM temperatures when fast high-power pulses were applied. Finally, model simulation results were compared to the experimental measurements to validate the modeling approach under fast-transient power level conditions.

The fast-transient model results generated temperature profiles comparable to the experimental measurements. These fast-transient simulated results had a better agreement with the experimental results in comparison to the slow-transient ones. Higher power levels showed a better response when simulated than low power levels. This can be due to the proximity of the high power levels dissipation to the device junction. The silicon device model developed by Hefner is more precise than the preliminary model for the remaining material in the IPEM layers.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 SUMMARY

A thermal model for the CPES IPEM was developed and validated. The chosen methodology was to follow a 1D thermal components network approach, based on the structural dimensions and thermal characteristics of the module. The model was generated and coded into SABER templates in order to validate its performance by comparing its behavior to acquired experimental measurements. Different power levels representing slow- and fast-transient responses were experimentally analyzed to validate the model behavior. The obtained model showed good agreement with the experimental measurements, especially when high-power levels were analyzed. Further modifications can be made to improve the low-power level behavior of the model.

5.2 CONCLUSIONS

It can be concluded that the thermal components method is suitable to model power electronic modules with an acceptable agreement when compared to experimental measurements when most of the material thermal characteristics and geometric information about the devices is known. In the case of the CPES IPEM, its non-symmetric construction was a challenging obstacle because the top metallization patterns were not parallel in terms of their relative placement with the top DBC layer counterparts, all metallic components were dissimilar on shape, and combined with the reduced IPEM size and high power density, made the resulting model very sensitive to errors in the CAD data.

The fast transient validation experiment, after measured, modeled, and simulated, showed an acceptable agreement. Since the heat spreader and heat sink dimensions can change due to the fact that they are not part of the actual IPEM, the DBC part of the

model can be kept as a good representation of its thermal behavior and later modified to accept other different cooling mechanisms if necessary. Table 5.1 summarizes the relative error between the experimental and simulated results for the fast-transient power levels. The table identifies where was the maximum error located, which was usually at the beginning of the pulse or at the final portion of it. The pulses for the low power levels were longer, and the figures do not show their full extension. That is why their errors are specified as being greater than the final values shown in the experimental results figures.

Table 5.1
Fast-Transient Simulation Results Summary

Power Level (W)	750	687	625	562	500	437	375	312	250	187	125
Maximum Error (°C, App.)	1.5	1	2	2	2	3	2.5	4	> 4	> 5	> 5
Maximum Error Pulse Location	Start	Start	Start	Start	Start	Start	Start	End	End	End	End

Finally, it can be concluded that, with minor modifications in the templates hierarchy, this model can be implemented as part of the automated process of virtual prototyping for the CPES IPEM. The software provides for the communication with other software tools, and the computational cost is much lower for this dynamical model than using finite 3D approaches as a thermal modeling option.

5.3 FUTURE WORK

It is recommended to further validate the developed model by:

1) Taking measurements of more modules to verify that, in general, they all perform similarly in terms of their thermal behavior under the same experimental power levels.
2) Making enough experimental measurements for both semiconductors in each IPEM to validate the full structure of the module. (The fact that during the experimental fast-transient measurements one of the chips was damaged makes it difficult to prove that the whole IPEM model is behaving adequately).
3) Changing the heat sink to check if under very low power levels the uniform heating of the whole module is being adequately modeled.

4) Using more thermocouples located at many different locations throughout the IPEM and heat spreader surfaces to validate the slow-transient model with more precision. The use of a thermal camera may also aid to verify these readings.
5) Performing an experimental slow-transient test with a fully functional IPEM driving a power load to obtain a more realistic thermal profile under operational conditions.
6) Changing the waveforms of the applied power pulses (to saw-toothed, rectified sinusoidal, exponential, etc.) to validate possible variations in the measurements.
7) Designing a method to capture the cooling profile of the thermal response, because it has valuable information about the thermal natural response of the module materials, which behaves very different in terms of the generated time constants from the forced function (power pulse) response. This was not done because the actual software that acquires the oscilloscope readings at NIST was programmed only to analyze the response for the flat portion corresponding the 1% heating portion of the complete period for the applied pulses, and not to acquire the remaining 99% corresponding to the cooling portion. Due to their different durations, that would require the software to change the time axis divisions in the oscilloscope and perform two measurements, so that at least one complete period could be recorded for every applied pulse. That procedure is being considered for future implementation.
8) Verifying the same thermal components modeling approach by modeling other IPEM prototypes, to see if their structural differences are satisfactorily simulated when compared to experimental measurements of the same kind performed to the final prototype.
9) It is recommended to verify the possible dependency between the error and the components discretization. This could help to find an optimal model.

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APPENDICES

APPENDIX A

IPEM STRUCTURAL DIMENSIONS

IPEM CAD layout schematic showing relative planar dimensions (transparent top view). See Table A.1 for mode details.

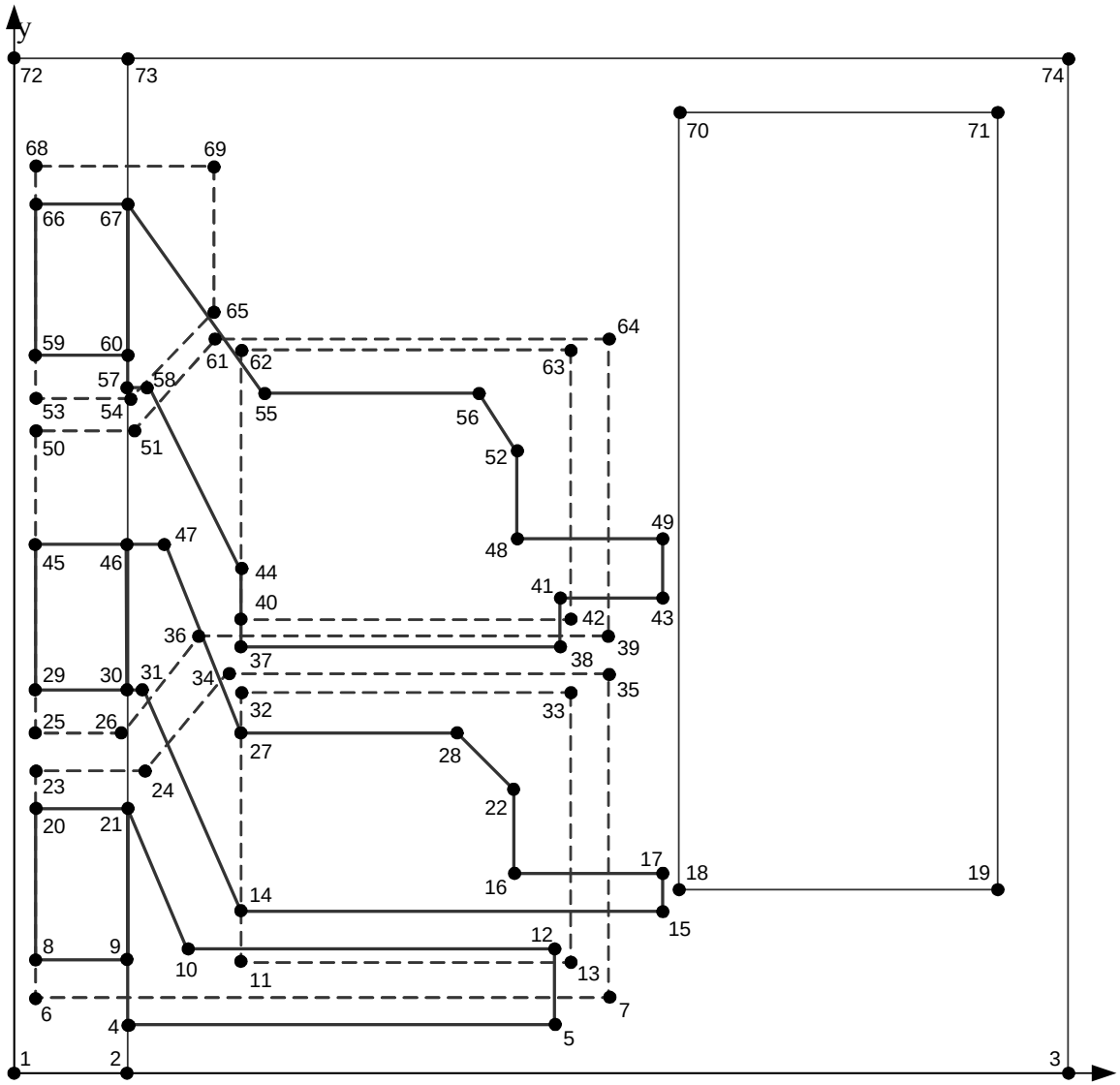


Figure A.1: IPEM structural schematic.

Table A.1

Coordinates (x, y, z) for the Maxwell grid locations of the IPEM layout schematic depicted in Figure A.1. (All dimensions are given in **centimeters**).

	Coordinates		
Point	**x**	**y**	**z**
1	0.0000	0.0000	0.0762
2	0.3048	0.0000	0.1892
3	2.8448	0.0000	0.1892
4	0.3048	0.1346	0.2159
5	1.4478	0.1346	0.2159
6	0.0508	0.2032	0.1029
7	1.5956	0.2032	0.1029
8	0.0508	0.3061	0.2159
9	0.3048	0.3061	0.2159
10	0.4572	0.3251	0.2159
11	0.6098	0.3048	0.1892
12	1.4478	0.3251	0.2159
13	1.4937	0.3048	0.1892
14	0.6096	0.4244	0.2159
15	1.7475	0.4244	0.2159
16	1.3462	0.5260	0.2159
17	1.7475	0.5260	0.2159
18	1.7983	0.4895	0.2527
19	2.6492	0.4895	0.2527
20	0.0508	0.7125	0.2159
21	0.3048	0.7112	0.2159
22	1.3462	0.7571	0.2159
23	0.0508	0.8147	0.1029
24	0.3567	0.8147	0.1029
25	0.0508	0.9197	0.1029
26	0.2911	0.9197	0.1029
27	0.6096	0.9146	0.2159
28	1.1887	0.9146	0.2159
29	0.0508	1.0213	0.2159
30	0.3048	1.0213	0.2159
31	0.3556	1.0213	0.2159
32	0.6098	1.0236	0.1892
33	1.4937	1.0236	0.1892
34	0.5588	1.0744	0.1029
35	1.5956	1.0744	0.1029
36	0.5047	1.1760	0.1029
37	0.6096	1.1491	0.2159

	Coordinates		
Point	**x**	**y**	**z**
38	1.4732	1.1491	0.2159
39	1.5953	1.1760	0.1029
40	0.6098	1.2268	0.1892
41	1.4732	1.2888	0.2159
42	1.4937	1.2268	0.1892
43	1.7475	1.2888	0.2159
44	0.6096	1.3472	0.2159
45	0.0508	1.4277	0.2159
46	0.3048	1.4277	0.2159
47	0.4064	1.4277	0.2159
48	1.3462	1.4412	0.2159
49	1.7475	1.4412	0.2159
50	0.0508	1.7363	0.1029
51	0.3184	1.7363	0.1029
52	1.3462	1.6698	0.2159
53	0.0508	1.8417	0.1029
54	0.3184	1.8417	0.1029
55	0.6604	1.8324	0.2159
56	1.2395	1.8324	0.2159
57	0.3048	1.8527	0.2159
58	0.3556	1.8527	0.2159
59	0.0508	1.9373	0.2159
60	0.3048	1.9373	0.2159
61	0.5348	1.9811	0.1029
62	0.6098	1.9456	0.1892
63	1.4937	1.9456	0.1892
64	1.5953	1.9811	0.1029
65	0.5348	2.0697	0.1029
66	0.0508	2.3437	0.2159
67	0.3048	2.3437	0.2159
68	0.0508	2.4513	0.1029
69	0.5348	2.4513	0.1029
70	1.7983	2.5977	0.2527
71	2.6492	2.5977	0.2527
72	0.0000	2.7315	0.0762
73	0.3048	2.7315	0.1892
74	2.8448	2.7315	0.1892

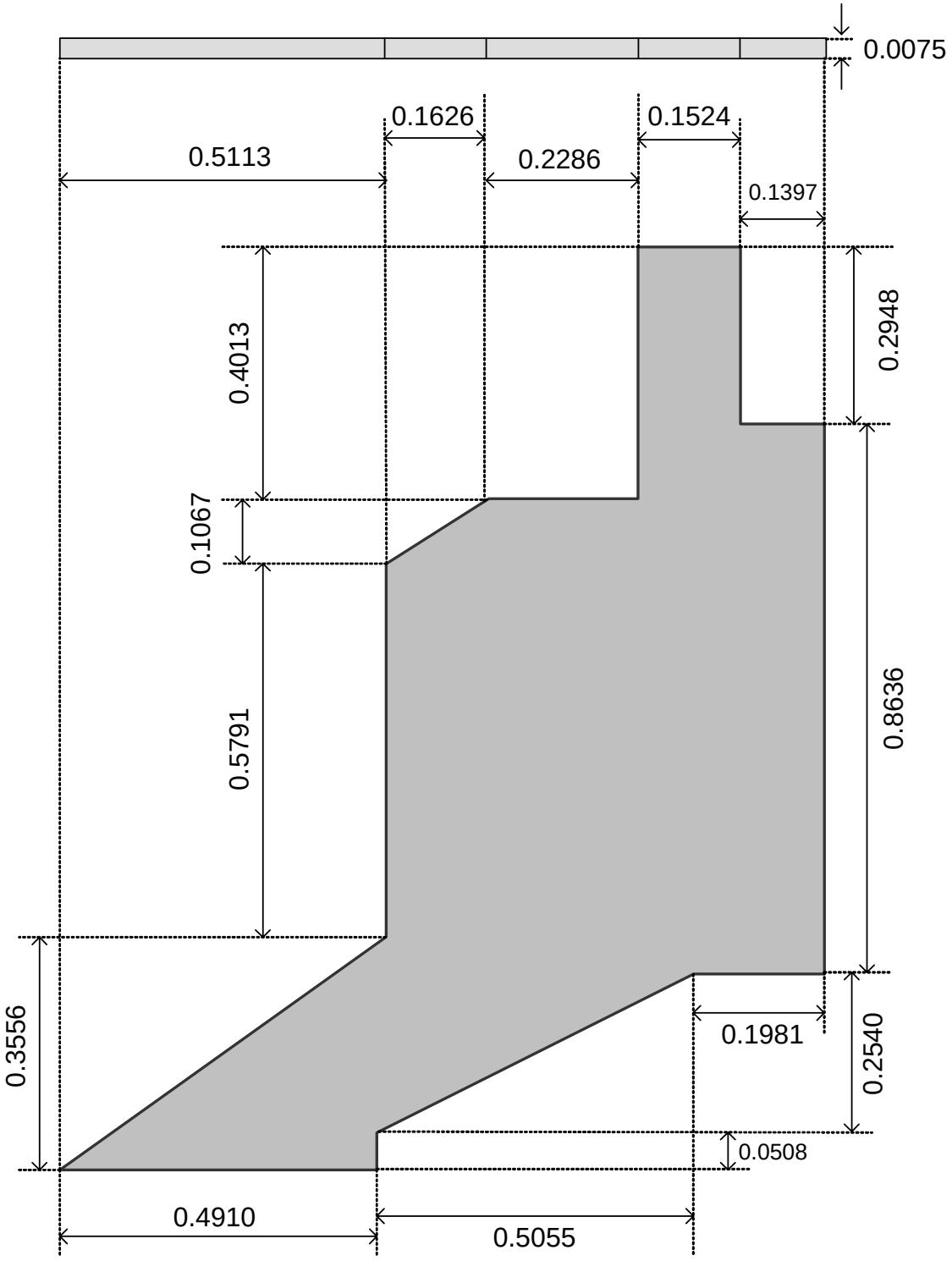


Figure A.2: Top middle copper metallization trace.

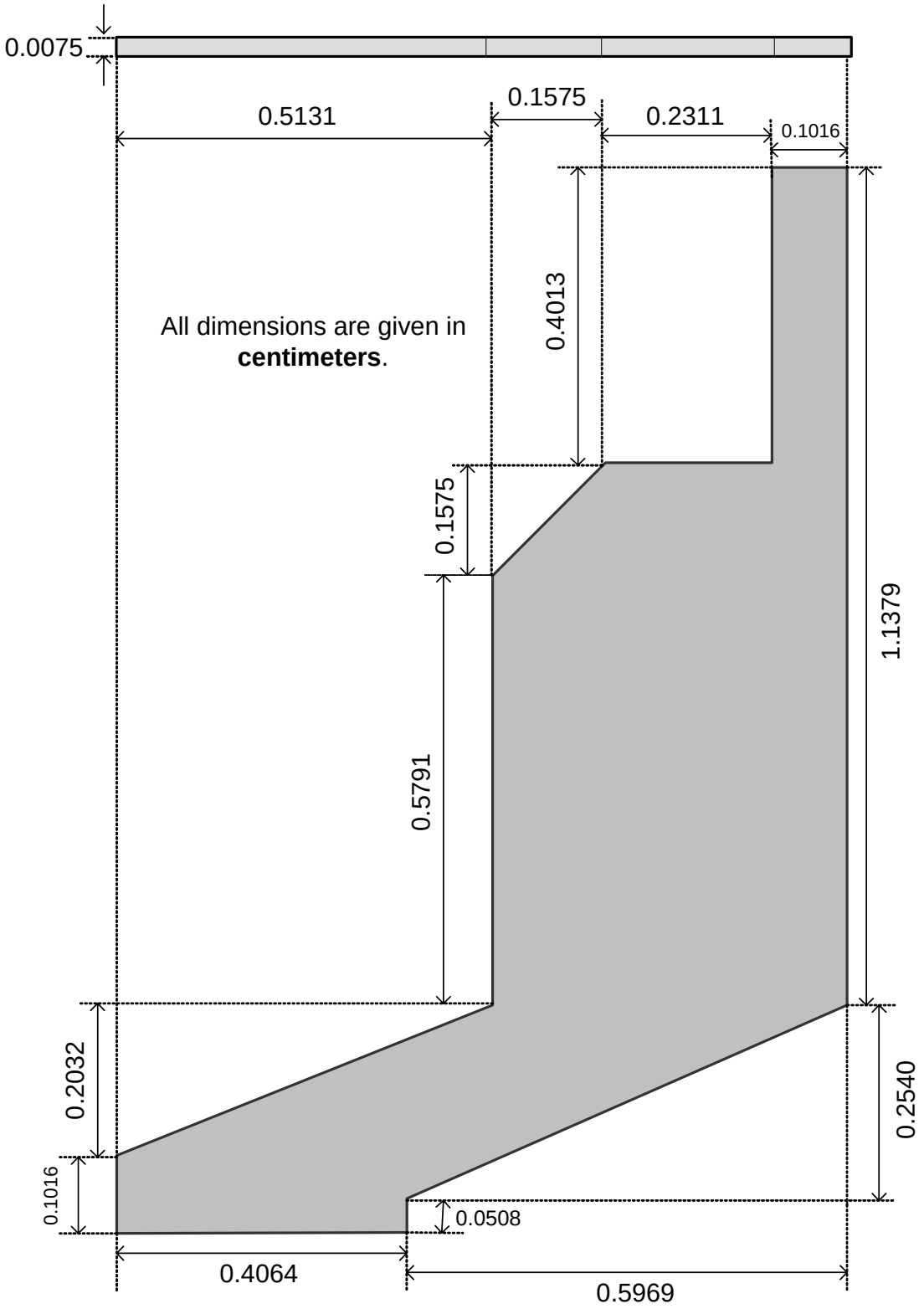


Figure A.3: Top left copper metallization trace.

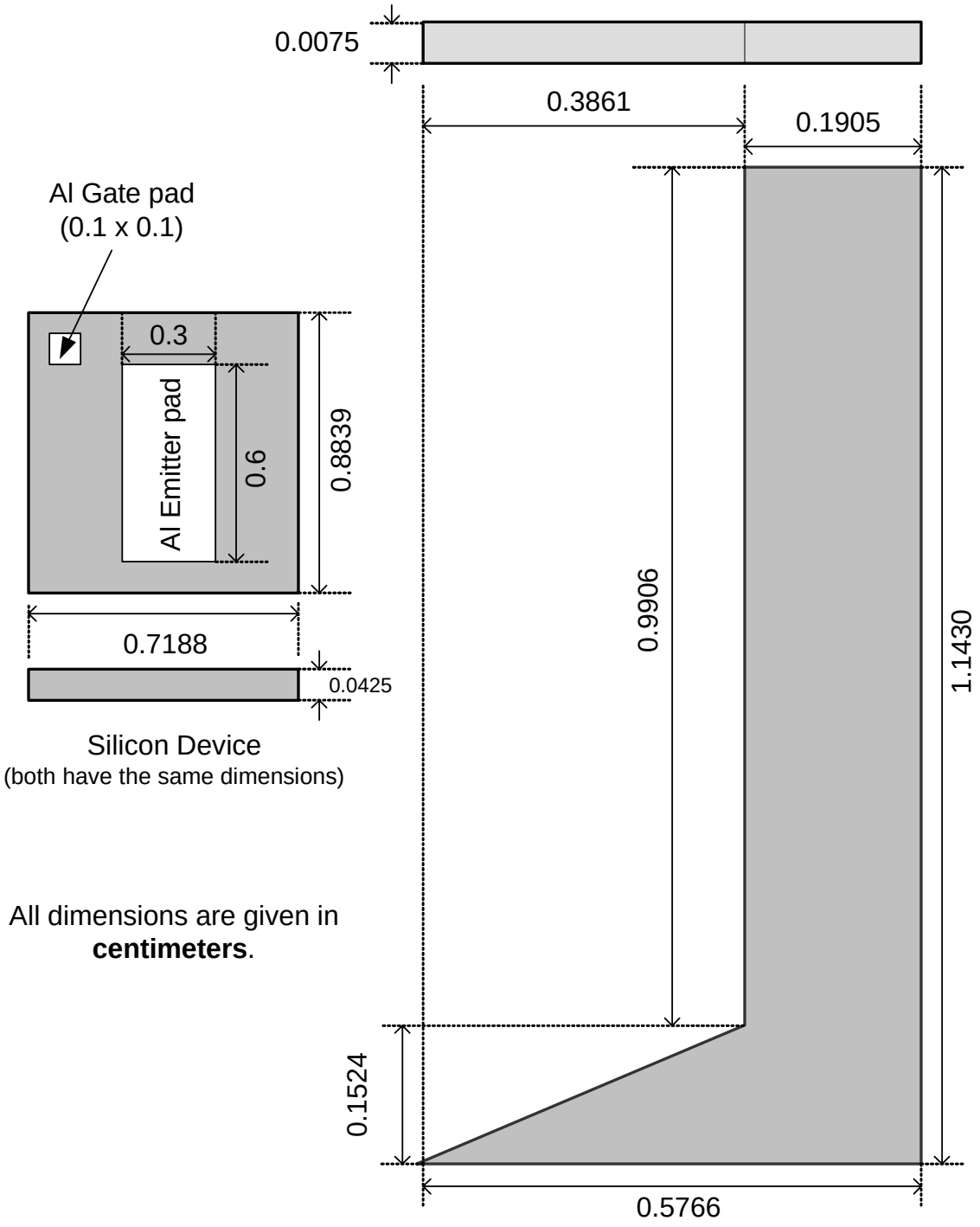


Figure A.4: Top right copper metallization trace and chips dimensions.

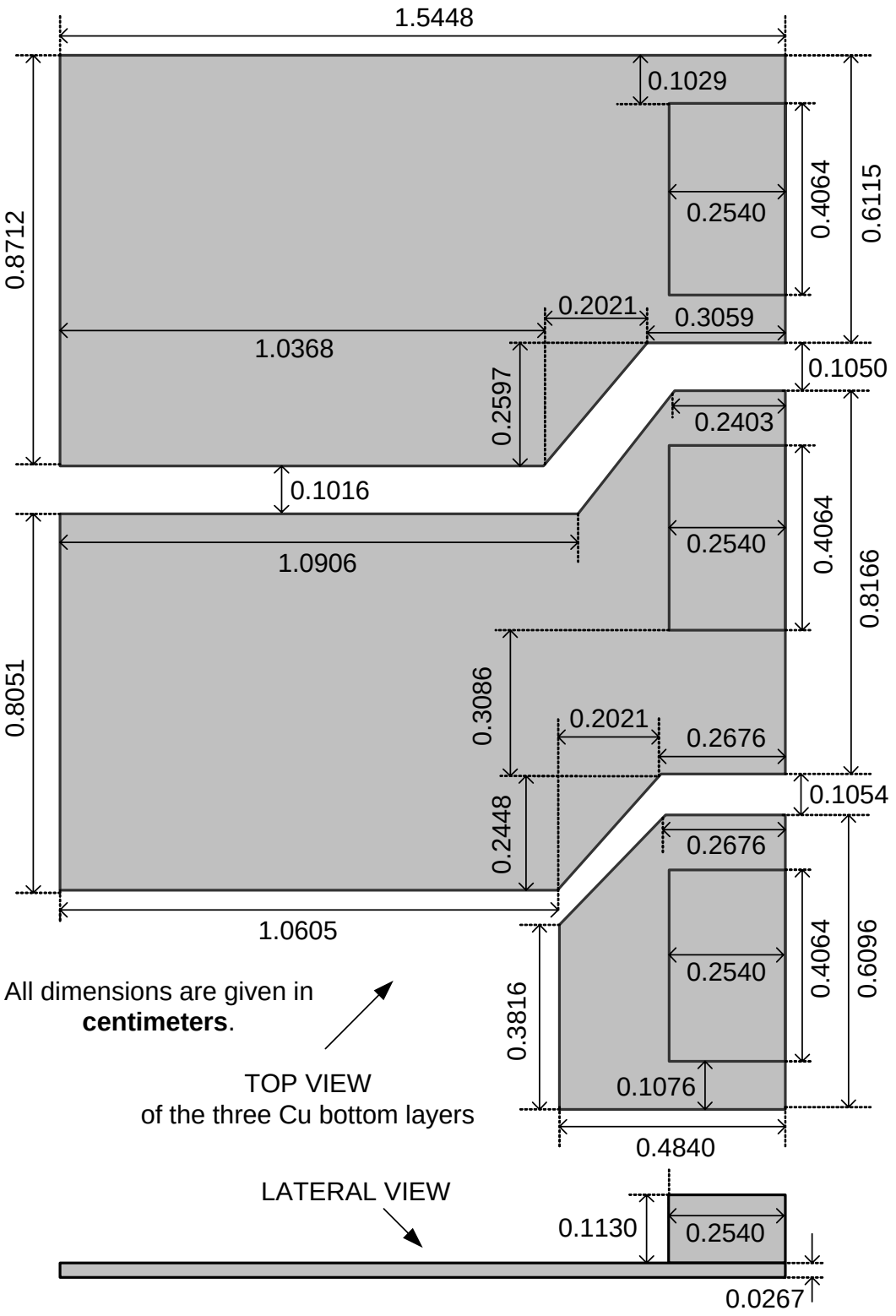


Figure A.5: Top DBC layer and contact leads.

APPENDIX B

EXAMPLE OF A SABER MAST-AHDL TEMPLATE

This template example is for illustrative purposes only. It shows the main subdivisions (identified as *sections*) coded in the actual IPEM thermal model templates. All the necessary sections are presented in their actual order. Template sections can be long if many parameters or variables need to be declared within them. In this template example each section shows only part of the variables and instructions to give an idea of how they are coded.

```
#=============================================================================#
# FILENAME: "cu_base.sin"                                                     #
#                                                                             #

#======================= Template and Header Declarations ======================
template cu_base  nlt nm3t nmnt nmst nmet nmwt nm6t nm7t nm8t nr3t nrnt

thermal_c  nlt, nm3t, nmnt, nmst, nmet, nmwt, nm6t, nm7t, nm8t,

number init_temp = undef

external number temp

#=============================================================================
#---------------------------- Template Body ----------------------------------
#=============================================================================
{#--------------------------- Local Declarations -------------------------------

number   Pi = 3.141592654

number LAB  = 0.2704,
MWBC = 0.8051,


# Physical properties of Al2O3
number ThermCondCu = 4   # Thermal Conductivity at 300K. (W/cm/K) "k"
number      DensCu = 8.92   # Density (g/cm^3)
number  SpcfHeatCu = 0.39   # Specific Heat (J/g/K)                  "Cp"

number HeatCapCu        # Heat Capacity = DensCu*SpcfHeatCu (J/cm^3/K)
number Ach

val tc     tlc,  tm3c, tmnc, tmsc, tmec, tmwc, tm6c, tm7c, tm8c,
           tr3c, trnc, trsc, trec, trwc, tr6c, tr8c

thermal_c  nlc,  nm3c, nmnc, nmsc, nmec, nmwc, nm6c, nm7c, nm8c,
           nr3c, nrnc, nrsc, nrec, nrwc, nr6c, nr8c

val joule  hl,  hm3, hmn, hms, hme, hmw, hm6, hm7, hm8,
           hr3, hrn, hrs, hre, hrw, hr6, hr8

number     vl,  vm3, vmn, vms, vme, vmw, vm6, vm7, vm8,
           vr3, vrn, vrs, vre, vrw, vr6, vr8

number temp_init
```

```
#-------------------------------------------------------------------------
#-------------------------- Parameters Section ---------------------------
#-------------------------------------------------------------------------
parameters {

     if (init_temp == undef){
                             temp_init = temp
                            }
     else{
           temp_init = init_temp
         }

     HeatCapCu = DensCu * SpcfHeatCu
     Ach = Wch * Lch

     vl  = LAB * ZCu

     vm3 = Ach * ZCu

     vm8 = MWB * MLB * ZCu

     vr8 = RLB * RWB * ZCu

     rr6  = (1/2)*ZCu / ThermCondCu / (vr6/ZCu)
     rr8  = (1/2)*ZCu / ThermCondCu / (vr8/ZCu)

}#-- End of Parameters Section ---------------------------------------------

#-------------------------------------------------------------------------
#----------------------------- Values Section ----------------------------
#-------------------------------------------------------------------------
values {

       tlt   = tc(nlt)  #+ 273.15
       tr8b  = tc(nr8b) #+ 273.15

       hl   = HeatCapCu * (tlc  + 273.15) * vl
       hr8  = HeatCapCu * (tr8c + 273.15) * vr8


}#-- End of Values Section -------------------------------------------------

#-------------------------------------------------------------------------
#---------------------------- Control Section ----------------------------
#-------------------------------------------------------------------------
control_section{
                initial_condition(tlc,  temp_init)
                initial_condition(tr8c, temp_init)

}#-- End of Control Section ------------------------------------------------

#-------------------------------------------------------------------------
#--------------------------- Equations Section ---------------------------
#-------------------------------------------------------------------------
equations {

       p(nlt  -> nlc)   += (tlt  - tlc)   / rll
       p(nr6t -> nr6c)  += (tr6t - tr6c)  / rr6
       p(nr8t -> nr8c)  += (tr8t - tr8c)  / rr8

       p(nrwc)  += d_by_dt (hrw)
       p(nr6c)  += d_by_dt (hr6)
       p(nr8c)  += d_by_dt (hr8)

}#-- End of Equations Section ----------------------------------------------

}#========================== End of Template Body ============================
```

APPENDIX C

SEMICONDUCTOR CHARACTERISTICS

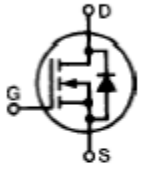
IXYS

MegaMOS™FET

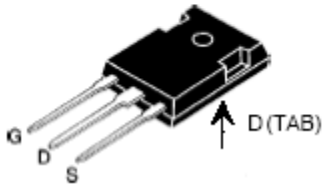
N-Channel Enhancement Mode

V_{DSS}	I_{D25}	$R_{DS(on)}$
500 V	21 A	0.25 Ω
500 V	24 A	0.23 Ω

IXTH / IXTM 21N50
IXTH / IXTM 24N50



TO-247 AD (IXTH)



TO-204 AE (IXTM)

G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		500	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	21N50	21	A
		24N50	24	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	21N50	84	A
		24N50	96	A
P_D	T_C = 25°C		300	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
M_d	Mounting torque		1.13/10	Nm/lb.in.
Weight			TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s			300	°C

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 µA		500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	V_{DS} = 0.8 • V_{DSS}	T_J = 25°C			200	µA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.5 I_{D25}	21N50			0.25	Ω
		24N50			0.23	Ω
	Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %					

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 • I_{D25}, pulse test	11	21		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4200		pF
C_{oss}			450		pF
C_{rss}			135		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 I_{D25}		24	30	ns
t_r			33	45	ns
$t_{d(off)}$	R_G = 2 Ω, (External)		65	80	ns
t_f			30	40	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 I_{D25}		160	190	nC
Q_{gs}			28	40	nC
Q_{gd}			75	85	nC
R_{thJC}				0.42	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0	21N50			21	A
		24N50			24	A
I_{SM}	Repetitive;	21N50			84	A
	pulse width limited by T_{JM}	24N50			96	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				1.5	V
t_{rr}	$I_F = I_S$, -di/dt = 100 A/µs, V_R = 100 V			600		ns

APPENDIX D

ADDITIONAL IPEM IMAGES

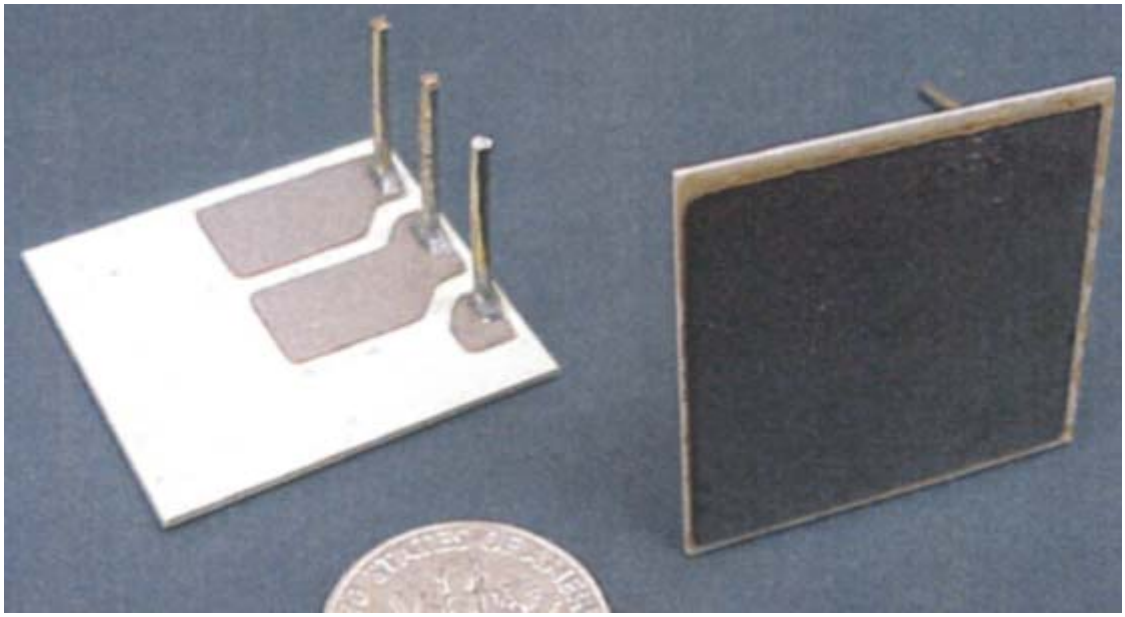


Figure D.1: DBC top metallization (left) and bottom soldering layer (right).

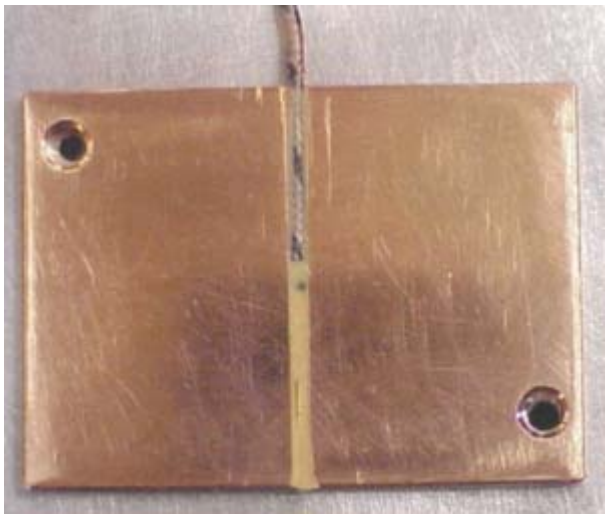


Figure D.2: Thermocouple placement for the heat spreader.

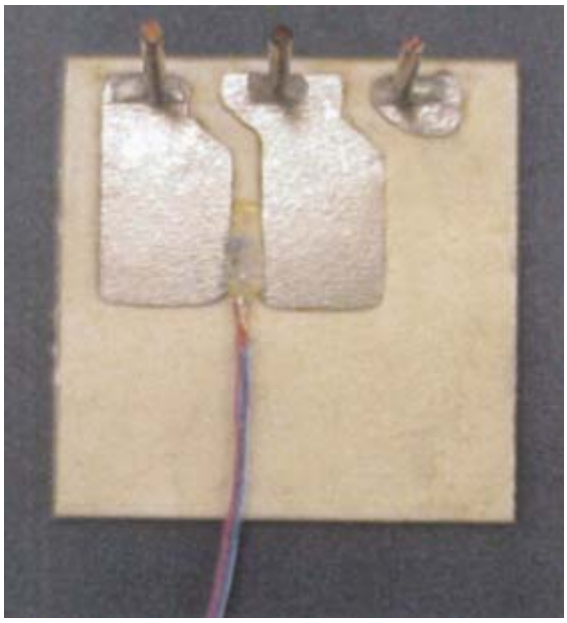


Figure D.3: Thermocouple placement for the DBC between chips.

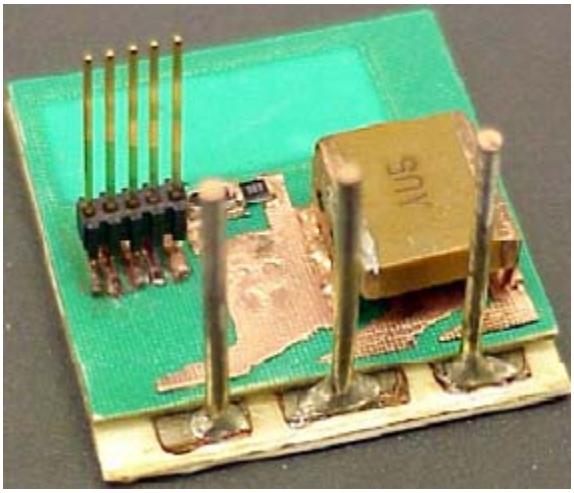


Figure D.4: Bus capacitor placement before gate driver addition.

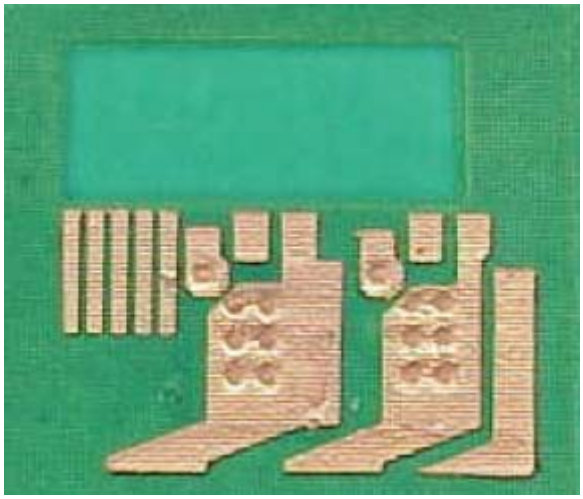


Figure D.5: Top metallization layer layout before any connections are made.

Figure D.6: CPES brochure cover being inserted through the air gap in the IPEM.

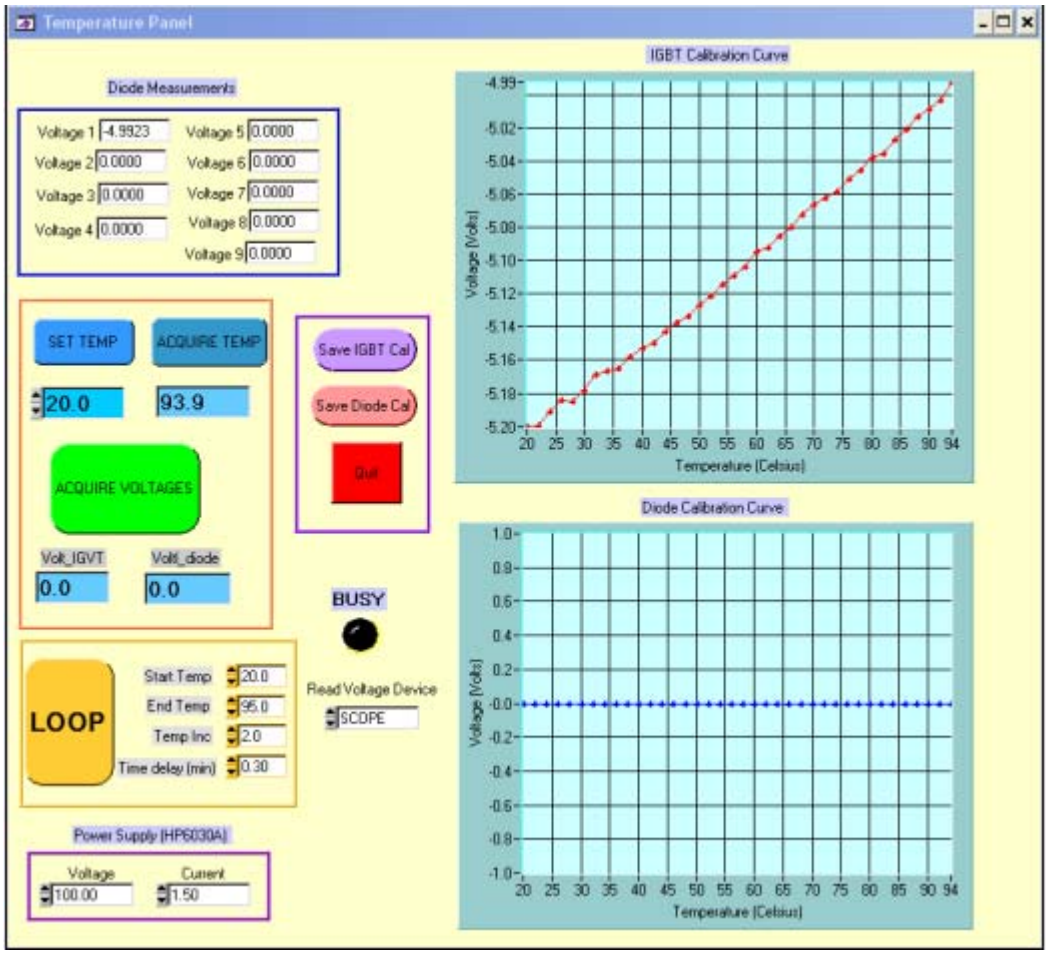


Figure D.7: Calibration curve acquisition tool environment. (For the fast-transient experiment)

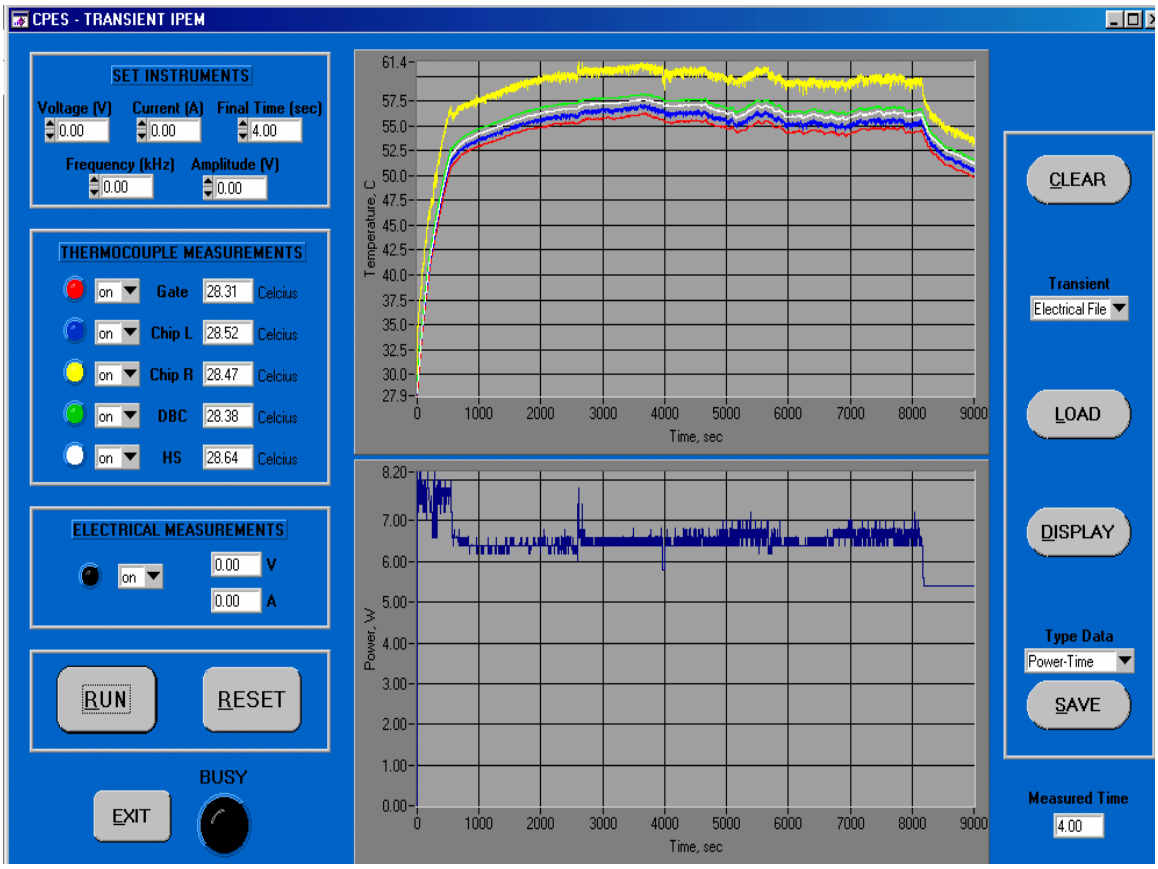


Figure D.8: Data acquisition system for the slow-transient experiment.