DESIGN AND IMPLEMENTATION OF A FOUR TERMINAL FLOATING AMPLIFIER AND ITS APPLICATION IN ANALOG ELECTRONICS

By

José A. García Rivera

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Approved by:

_____	_____
Dr. Rogelio Palomera García President, Graduate Committee	Date
_____	_____
Dr. Manuel Jiménez Cedeño Member, Graduate Committee	Date
_____	_____
Nicolas Salamina, MS Member, Graduate Committee	Date
_____	_____
Dr. Dorothy Bollman Representative of Graduate Studies	Date
_____	_____
Dr. Isidoro Couvertier Chairman of the Department	Date

ABSTRACT

DESIGN AND IMPLEMENTATION OF A FOUR TERMINAL FLOATING AMPLIFIER AND ITS APPLICATION IN ANALOG ELECTRONICS

By

José A. García Rivera

The field of analog electronics has developed and matured for the past two decades. Within this field, design of analog amplifiers has received attention due to changes in technology. Amplifier circuits, considered analog devices, are found anywhere in many house electronic appliances. A variety of these devices such as the Operational Amplifier, a dominant one, Fully Differential Amplifiers, Current Feedback, and Current Conveyors are found wide spread in the integration of these electronic appliances. However, the operational amplifier is not the only device available for design and integration of complex systems. Different systems implementations call for different analog devices that suite a particular specification.

This thesis presents the design and implementation of a rare, analog amplifier, active device: The Four Terminal Floating Nullor. A brief history and development of this device is presented. Circuit blocks and schematic representation from literature are shown to illustrate the different ways it has been design. Different approaches for these devices are presented with their corresponding SPICE simulations. Also, a wide variety of applications are presented where this device performs as a replacement of the Operational Amplifier.

RESUMEN

DESIGN AND IMPLEMENTATION OF A FOUR TERMINAL FLOATING AMPLIFIER AND ITS APPLICATION IN ANALOG ELECTRONICS

El campo de la electrónica análoga ha estado en desarrollo y constante cambio en las últimas dos décadas. Dentro de este campo, el diseño de amplificadores análogos ha recibido atención debido a los cambios en tecnología. Los amplificadores, considerados dispositivos análogos, pueden encontrarse en muchos de los equipos electrónicos de un hogar. Una variedad de estos dispositivos tales como el Amplificador Operacional, uno de los más dominantes en el mercado, "Current Feedback" y "Current Conveyor" ha encontrado una integración amplia en los equipos electrónicos de hoy día. Sin embargo, el amplificador operacional no es el único dispositivo activo disponible para el diseño e integración de sistemas complejos.

Esta tesis presenta el diseño e implementación de un amplificador análogo: Amplificador Operacional de Salida Flotante. Una breve historia y desarrollo de este dispositivo se presenta. La representación esquemática de la literatura se demuestra para ilustrar las diversas maneras que se ha puesto en ejecución. Una variedad de circuitos de estos dispositivos es presentada con sus simulaciones correspondientes en SPICE. También, una gran variedad de aplicaciones son presentadas donde este dispositivo se usa como reemplazo del amplificador operacional.

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Chapter 1 Introduction

1.1 Historical notes

The first operational amplifier was designed in the 1940's by Loebe Julie [40], then a student working with Prof. John R. Ragazzini at Columbia University. The term operational amplifier was coined by Ragazzini himself in a seminar paper where it was demonstrated that mathematical simulation could be done electronically using this amplifier. The first commercial operational amplifier was introduced to the market in 1952 by the company George A. Philbrick Researches. Since then, much progress has followed, triggered first by the now almost disappeared analog computer industry, and later on by integrated circuit technology.

On other venue, theoretical studies had been associated with the modeling of electronic circuits. The search of appropriate models for vacuum tubes first, and later on for transistors, triggered much research in the apparently unrelated quest of a complete set of elements for modeling circuits, a topic more related to a mathematical application activity than to technological one. In this path, several theoretical concepts were developed, such as the unitor [7], ideal amplifiers [3], nullator, norator and nullor [1]. The nullor concept was shown to be closely related to Tellegen's ideal amplifier. Modeling of ac ideal transistors with nullator and norator, together with the proof that the nullator and norator, with resistances and capacitances, constituted a complete set, gave rise to the development of synthesis and analysis methods for electronic circuits [4, 8, 9]. Also, the association of nullor with grounded output to the ideal operational amplifier proved to be a powerful tool for the design and compensation of electronic circuits,

solving different problems associated to the parasitics of real amplifiers, and providing a link between apparently unrelated designs [4,41]. The development of current conveyors [11] and other building blocks further triggered the interest in this topic. An interesting overview of the nullor concept and relations to the different operational amplifiers can be found in [6].

The limitation of practical operational amplifiers to have a grounded output became limiting obstacle for practical applications where simpler developments would require a floating output. This problem triggered the search for the development of practical operational amplifiers with floating output [20]. Terms, such as Four Terminal Floating Nullor (FTFN), Operational Floating Amplifiers (OFA), and Four Terminal Floating Amplifier (FTFA) were coined. Nowadays, there is much activity in this area.

1.2 Project objective

The objective of this work is to design two FTFA or FTFN circuits. After a theoretical review of the ideal concepts associated to operational amplifiers, some previous works of integrated circuit realizations is presented. Two basic topologies, the so called telescopic and the folded-cascode ones, are selected for the proposed designs. These were chosen because they have been readily proven in previous designs. Key design parameters to be used in this work are the FTFA gain, frequency response and phase margin. Although the basic block topology follows the same patterns as previous works, some variations in the techniques were introduced.

For the telescopic type FTFN, a gain enhancing procedure using negative conductances, which had been used by R. Geiger [35] in switched capacitor circuits, was used instead of the usual boosting method. Unlike the boosting method, negative conductances tend to eliminate poles, thereby improving the frequency response and phase margin when compared to previous realizations. Also a higher gain is achieved. A phase margin of 64° with a 115 dB was measured in simulation.

In the case of the folded-cascode type amplifier, a feedforward technique was used together with a compensation scheme. The feedforward methods are usually not applied to circuits containing feedback, and in particular, to this author's knowledge, have not been used at all in previous works on FTFN's. Improvement in performance was obtained too. A phase margin of 65º with a 91 dB gain was measured in simulation.

The designs were initially intended to be fabricated and tested experimentally using MOSIS AMIC5N 0.6 u. All the simulations were done using this technology. Although for practical reasons the fabrication of the designed circuits has been left for future work, simulated applications using these designs are provided.

1.3 Thesis description

This work begins treatment on chapter 2 with theory and concepts of nullator, norator and nullor; definitions and properties are also discussed. To introduce its use as a modeling device, several examples are presented. Also, some block equivalencies are introduced with respect to known circuit blocks such as the operational amplifier and current conveyor. Finally, an implementation of a nullor, the Four Terminal Floating Nullor (FTFN) is presented. Antecedents motivated by the use of the FTFN started to search for a physical implementation and this is the topic of chapter 3. From class A and

class AB implementations bases on operational amplifiers to transistor level implementations, a full range of circuit variations are presented. Based on previous publications some considerations are presented prior to the design of the proposed FTFN. Specific techniques such as gain-enhanced negative conductance and feedforward techniques are discussed in chapter 4. To verify the design characteristics, Spice simulations of parameters such as gain, phase margin, etc., are provided with a respective testbench is presented in chapter 5. Chapter 6 presents some enhancements done to the basic designed. To validate the circuit design, linear and nonlinear applications are used to demonstrate the versatility. This is the topic of chapter 7.

Appendices A to C review some theoretical concepts such as linearity, distortion, noise, etc. References are provided separately for each appendix. The rest of the appendices provide technical details and further simulation results.

Chapter 2 The Nullor Concept

2.1 The Nullator, Norator and Nullor

The nullator and norator are theoretical active devices that have been used in the analysis, design and synthesis of linear circuits. Known since the 1950's, these are concepts that, in spite of their enormous potential for the design of electronic circuits, have not been considered widely within text books. One of the possible reasons is that, unlike others like the resistance and capacitance, these elements do not respond to the idealization process of any physical device.

Carlin [1] made an attempt to use both nullator and nullator as single terminal active devices, but proved instead that they are not physically realizable. Later, Tellegen [2] also showed these devices were mathematical concepts without a physical content. Carlin on the other hand, proposed the combination of nullator and norator, which resulted in an accepted physical device, the nullor. This is so because the nullor has two ports and is characterized by two equations. The nullor was shown to be related to the ideal amplifiers previously proposed by Tellegen [3].

2.1.1 Definitions

Figure 2.1 shows a two terminal nullator which does not allow current flow through it, and the voltage across its terminals is zero under all conditions.

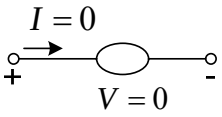


Figure 2.1 Nullator symbol representation

On the other hand, a norator, as shown in Figure 2.2 has an arbitrary voltage and current across its terminals. This element has no constitutive equation.

Figure 2.2 Norator symbol representation

Together, both nullator and norator form the nullor, as shown in Figure 2.3. It is

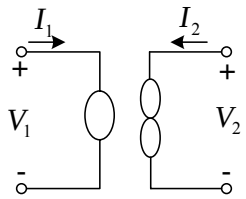


Figure 2.3 Two-port nullor symbol

defined as a two-port network element, whose transmission matrix [4] is the null matrix, that is,

$$\begin{bmatrix} V_1(s) \\ I_1(s) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2(s) \\ -I_2(s) \end{bmatrix} \tag{2.1.1}$$

A characteristic that makes the nullor attractive is that it is a universal active element. This concept means that together with capacitors and resistors we can implement a maximum number of functions (ideally all) with the minimum number of such devices [3, 5, 6]. That is, if a suitable set of linear and nonlinear passive elements is available, then no active elements other than nullors are needed to implement any linear or nonlinear circuit function. In particular the nullor, resistance and capacitance form a complete set for linear circuits.

2.1.2 Equivalence and properties of nullators and norators

Figure 2.4 shows equivalencies of combinations of nullators and norators. By connecting these two elements with others, and making use of these properties, it is shown the potentiality and usefulness of the nullor for analysis, realization and design of electric circuits. Various circuit elements such as the ideal transistor and operational amplifier can be modeled with such equivalences.

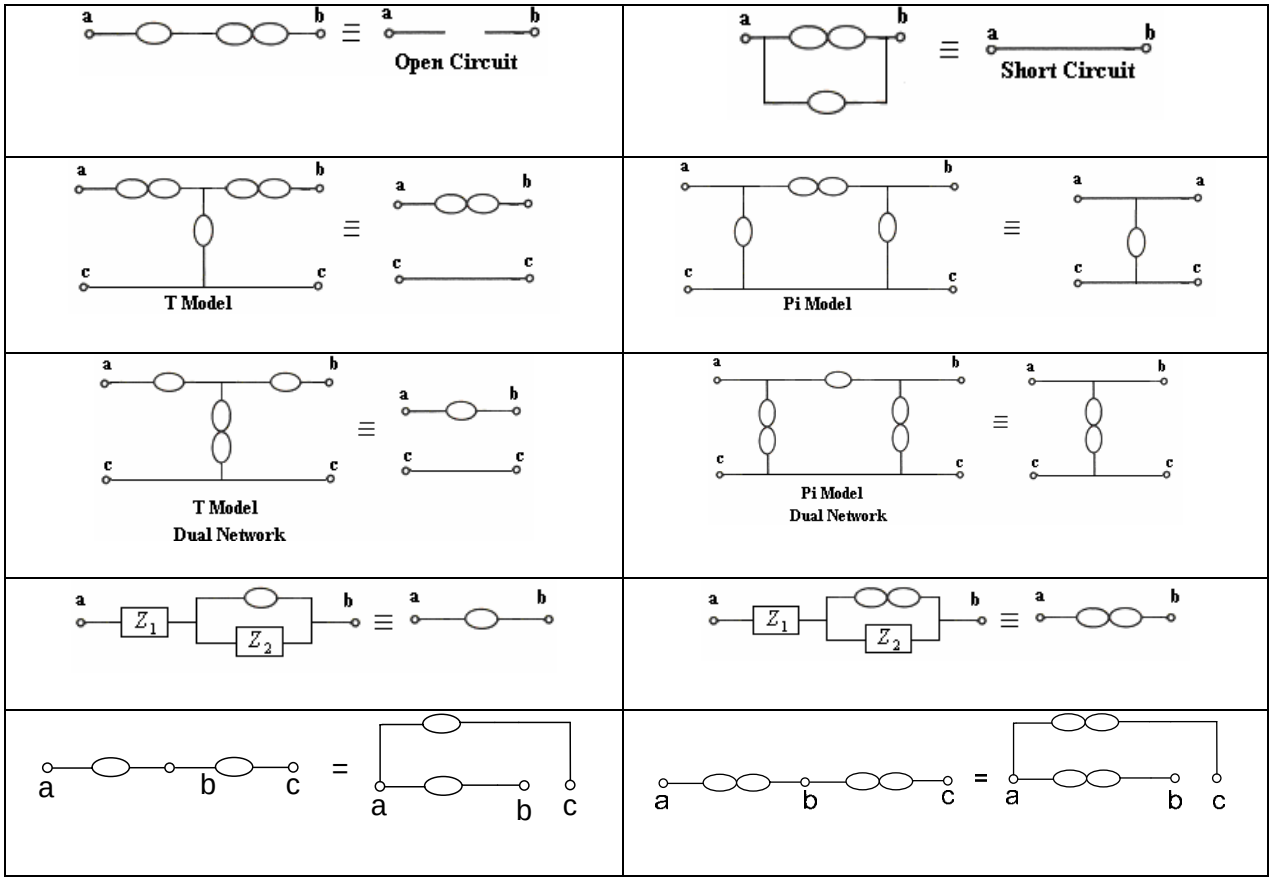


Figure 2.4 Nullator and norator equivalences

2.2 Nullor as a modeling device

The nullor has been used extensively as a modeling device in linear circuits. An example of this arouse from circuits realized with triodes with difficulties on device

modeling. To overcome this modeling difficulty, the unitor was proposed [7]. The unitor, in Figure 2.5 is defined as a floating three terminal element which acts as a unilateral unity-gain voltage transfer element from 1 to 2, with 3 as a common node, and as a unilateral unity-gain current transfer element from 2 to 3 with 1 as a common node.

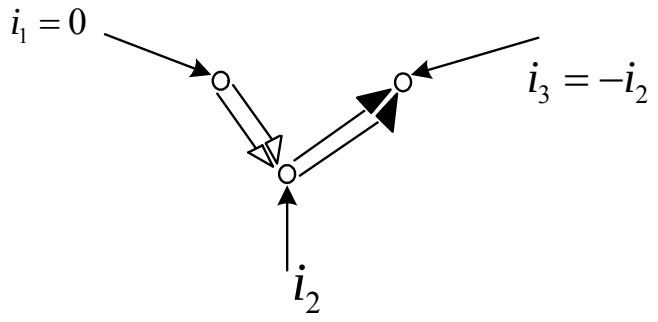


Figure 2.5 Unitor and its port description

The corresponding equations are:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$
$$\textit{Unity} - \textit{gain} \qquad \textit{Unity} - \textit{gain} \tag{2.2.1}$$
$$\textit{voltage transfer} \qquad \textit{current transfer}$$

This representation gave recognition to the ac modeling of ideal transistors by means of nullor devices as shown in Figure 2.6. Thus, a unitor is equivalent to a three terminal nullor. Due to the already mentioned fact, that a complete set is composed by an interconnection of resistances, capacitances and nullors, several synthesis and design methods using the equivalent transistor models were presented in [8].

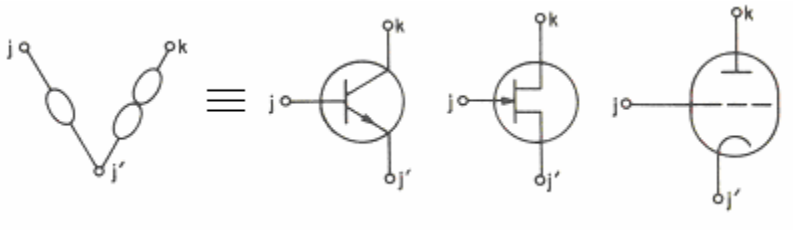


Figure 2.6 AC modeling of transistors and triodes by a unitor, or three terminal nullor

2.2.1 Nullors and transistors

Ideal AC transistors can be modeled by a nullor in which the nullator and norator share a common terminal [4, 9], as shown in Figure 2.6. The equivalent model for single transistors shown in Figure 2.6 can be used to form four terminal elements with transistors, using equivalencies applicable to the two terminal elements of nullators and norators. Such equivalencies were shown in Figure 2.4 while Figure 2.7 shows the realized nullor. Hence, it can be said that the simplest ac nullor consists of two transistors.

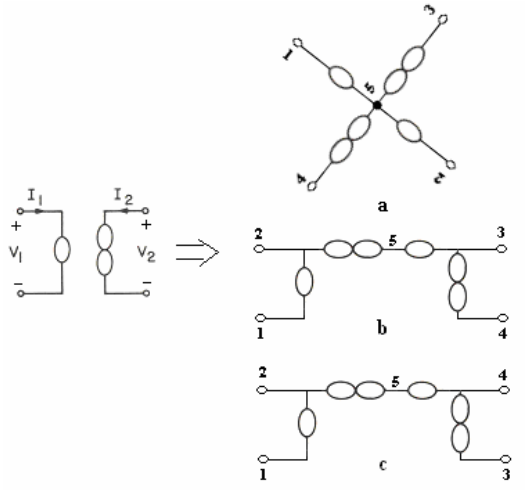


Figure 2.7 Composite transistor representations for a four terminal nullor.

2.2.2 Operational Amplifier, Current Conveyor and Nullor

The current conveyor and the operational amplifier have been two dominant active devices in the analog market. An operational amplifier is considered a voltage-mode device whereas the current conveyor a current-mode active device. Both devices can be represented by means of nullor equivalent circuits.

An Operational Amplifier is a voltage amplifier with high gain. The symbol for the ideal and non-ideal operational amplifier is shown in table 2.1.

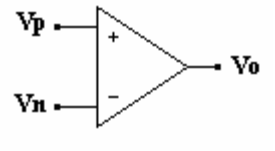
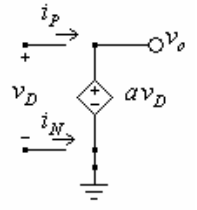
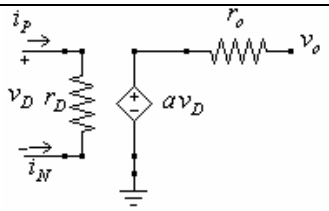
Symbol	Ideal Finite Gain Model	Basic Model
		

Table 2.1 Operational Amplifier symbol, ideal and non-ideal model

The ideal terminal conditions of the operational amplifier are [10]:

$$\begin{aligned} &\textit{Voltage gain}: a \to \infty \\ &\textit{Differential} \text{ resistance}: r_d = \infty \\ &\textit{Output} \text{ resistance}: r_o = 0 \\ &\textit{Differential Voltage } v_D \to 0 : v_N = v_P \end{aligned} \tag{2.2.2}$$

It is observed from these terminal conditions and the ideal model that an operational amplifier is realized by a voltage-controlled voltage source. That is, an infinite gain operational amplifier is a special case realization of a nullor.

In the same way as the operational amplifier, the Current-Conveyor (CCII) introduced by Sedra and Smith [11] in 1970 can be used to implement many analog

signal processing functions. Figure 2.8 shows the current-conveyor symbol. The definition of the CCII is shown in matrix form equation (2.2.3)

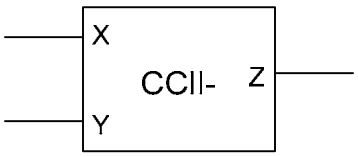


Figure 2.8 Current-conveyor circuit symbol

$$\begin{bmatrix} i_X \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_Y \\ v_Z \end{bmatrix} \tag{2.2.3}$$

In other words, the terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits zero input impedance. The current supplied to X is conveyed to the high-impedance output terminal Z where it is supplied with either positive polarity (CCII+) or negative polarity (CCII-). Thus, a simplified version of equation (2.2.4) results in:

$$i_X = 0, v_X = v_Y, i_Z = \pm i_Y \tag{2.2.4}$$

These conditions cast light on the relation on CCII, unitor and nullors. Equation (2.2.4) describes the behavior of a unitor, that is, unity-gain voltage transfer ($v_X = v_Y$) and unity-gain current transfer ($i_Z = \pm i_X$). As a result of this, a CCII is equivalent to a unitor, and to the already mention three terminal nullor. In chapter 3, it will be demonstrated that two current conveyors form a nullor. This is also demonstrated by the use of two AD844 integrated circuits.

A brief review on the relation between CCII, OpAmp's and nullors is presented in table 2.2. It is seen here that circuits containing Operational Amplifiers and Current Conveyor's are also realized by nullors.

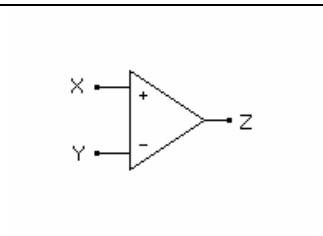
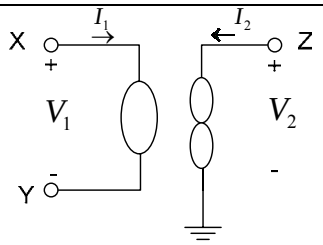
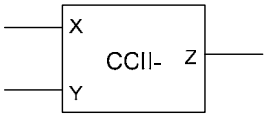
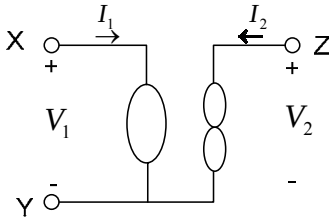
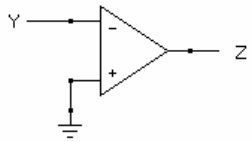
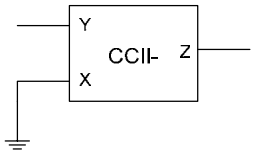
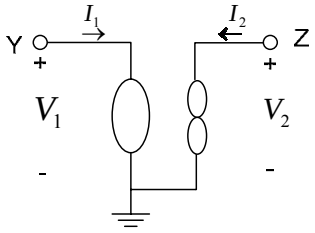
Operational Amplifier Circuit	Current Conveyor Circuit	Nullor equivalent
		
		
		

Table 2.2 Current Conveyor, Operational Amplifiers and Nullor equivalents

2.2.3 Controlled sources and nullor equivalencies

The four types of controlled sources, shown in table 3.3, are used extensively in the analysis and synthesis of RC-active networks.

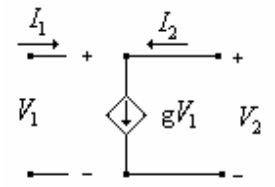
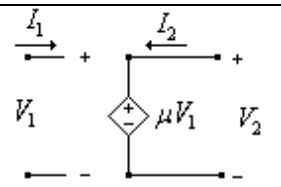
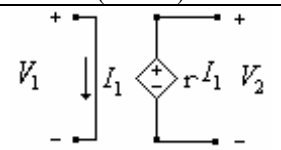
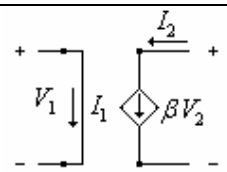
Symbol	Definition
 Voltage-Controlled Current Source (VCCS)	$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{g} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$
 Voltage-Controlled Voltage Source (VCVS)	$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \frac{1}{\mu} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$
 Current-Controlled Voltage Source	$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \frac{1}{r} & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$
 Current-Controlled Current Source (CCCS)	$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{\beta} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$

Table 2.3 Controlled Sources and Definitions

It is possible to obtain any of the four controlled sources by means of R-nullor equivalencies. Let us demonstrate the realization of a Voltage-Controlled Current Source. Figure 2.9 shows the R-nullor equivalent of the VCCS. At the input port, I_1 is zero by definition of the nullator port. The norator yields V_2 arbitrary, defined by external connections.

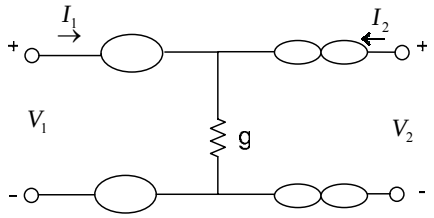


Figure 2.9 Voltage-Controlled Current Source R-nullor equivalent

A voltage equation shows that $V_g = V_1$ and the current passing through I_2, is

$$I_2 = gV_1 \tag{2.2.5}$$

In a similar way, the other types of controlled sources are realized by means of R-nullor equivalent networks. A set of realization is shown in table 2.4

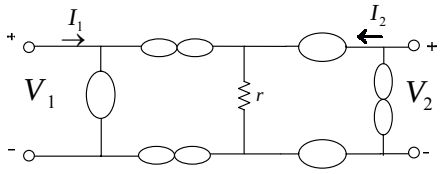
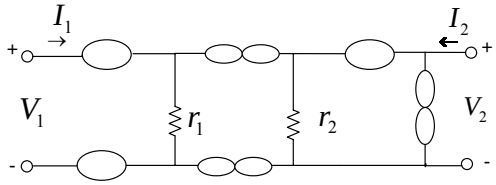
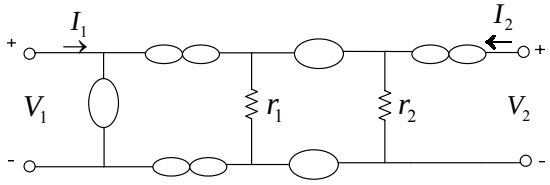
Constraints	Equivalent Nullor Network	Type
$V_1 = 0$ $I_2 = arbitrary$ $V_2 = rI_1$ Gain: r		CCVS
$I_1 = 0$ $I_2 = arbitrary \;\; Gain: \mu = -\frac{r_2}{r_1}$ $V_2 = -\frac{r_2}{r_1}V_1$		VCVS
$V_1 = 0$ $V_2 = arbitrary$ $I_2 = \frac{r_1}{r_2}I_1$ $Gain: \beta = \frac{r_1}{r_2}$		CCCS

Table 2.4 Controlled-Sources Nullor Equivalent

It is a particularly useful result that an infinite-gain controlled source or any of the four types is exactly equivalent to a nullor. To verify this statement we will make use of Figure 2.10

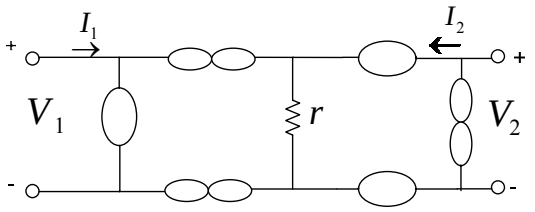


Figure 2.10 Current-Controlled Voltage Source R-nullor equivalent

The definition of current at the output port results in:

$$V_2 = rI_1 \tag{2.2.6}$$

Infinite gain is realized by setting the resistance $r = \infty$. As Figure 2.11 shows, an equivalent open-circuit nullor network is formed.

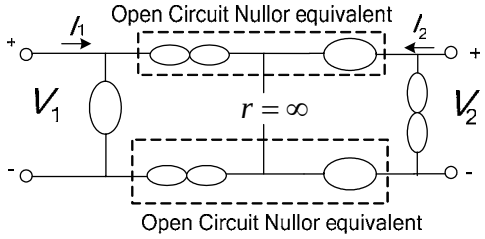


Figure 2.11 Current-Controlled Current Source R-nullor equivalent with infinite gain

Finally, the resultant circuit reduces to that of a single nullor as shown in Figure 2.12

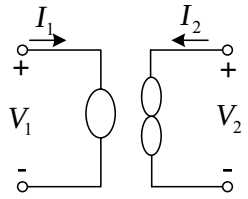


Figure 2.12 Nullor resulting from CCVS

2.3 Nullor as theoretical synthesis and design element

Several publications based on nullors as synthesis devices are known [8,12]. Most of them resulted in equivalent generated transistors and operational amplifier circuits. The nullor modeling for ac ideal transistors has long been recognized [4, 9]. This ac modeling of transistors with nullors has been used to successfully generate by hand several composite transistors configurations through the application of nullator-norator transformations and equivalences [13]. The same concept was applied to automatically generate composite transistors with any number of transistor components [14].

On the other hand, nullor based operational amplifier circuits resulted in impedance circuits suitable for filter implementations [4].

2.3.1 Transistor level implementation based on nullors.

Figure 2.13 shows an example on the use of nullors to obtain equivalent circuits. An equivalent short circuit nullor is inserted between base and emitter resulting in a composite transistor illustrating the final step with two NPN transistors. However, up to 16 combinations can be considered. Figure 2.14 shows the admittance parameters for the 16 possible results obtainable from Figure 2.13. Each row in this figure represents four cases, since ac is being analyzed and the only difference arises from bipolar or MOS

nature of the transistor, and not of the type.

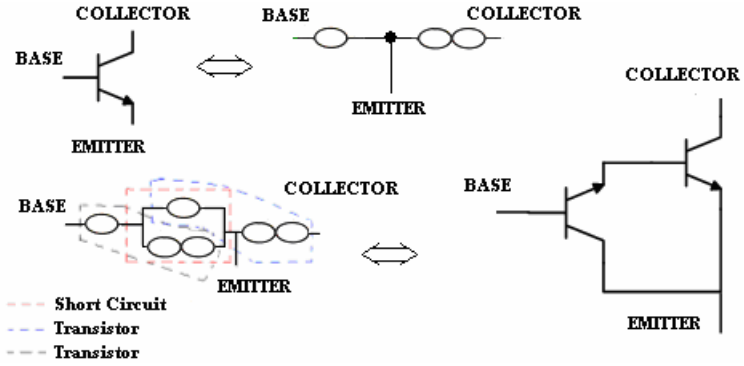


Figure 2.13 Example of a composite transistor generation

	y_{11}	y_{12}	y_{21}	y_{22}
Base, Collector, Emitter				
NPN,PNP	$\frac{g_{\pi 1}(g_{o1}+g_{\pi 2})}{g_{\pi 1}+g_{m1}+g_{o1}+g_{\pi 2}}$	0	$\frac{g_{\pi 1}(g_{o1}+g_{\pi 2})}{g_{\pi 1}+g_{m1}+g_{o1}+g_{\pi 2}}$	g_{o2}
NMOS,NPN	0	0	$\frac{g_{m2}g_{m1}}{g_{o1}+g_{\pi 2}}$	g_{o2}
NPN,NMOS	$\frac{g_{o1}g_{\pi 1}}{g_{m1}+g_{\pi 1}+g_{o1}}$	0	0	g_{o2}
NMOS,NMOS	0	0	$\frac{g_{m1}g_{m2}}{g_{o1}}$	g_{o2}

Figure 2.14 Admittance Parameters

While there is no difference in ac models for NPN and PNP transistors, DC biasing requirements are different. Figure 2.15 shows examples of biased configurations for different combinations derived from the process illustrated in Figure 2.13.

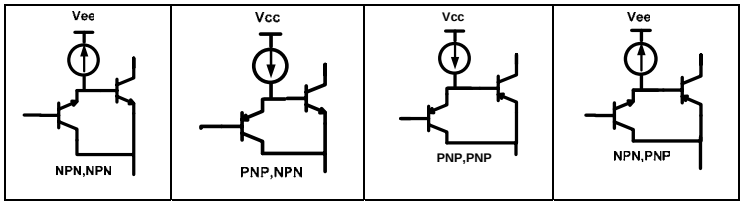


Figure 2.15 Examples of biasing for different combinations

Another example results from the derivation of a transistorized CCCS from a nullator-norator CCCS circuit. A procedure similar to that in Figure 2.13 follows except that in this case an open-circuit equivalent is inserted between 1' and the intersection node of R_1 and R_2. This is shown in Figure 2.16. Additional circuitry is needed for bias purposes.

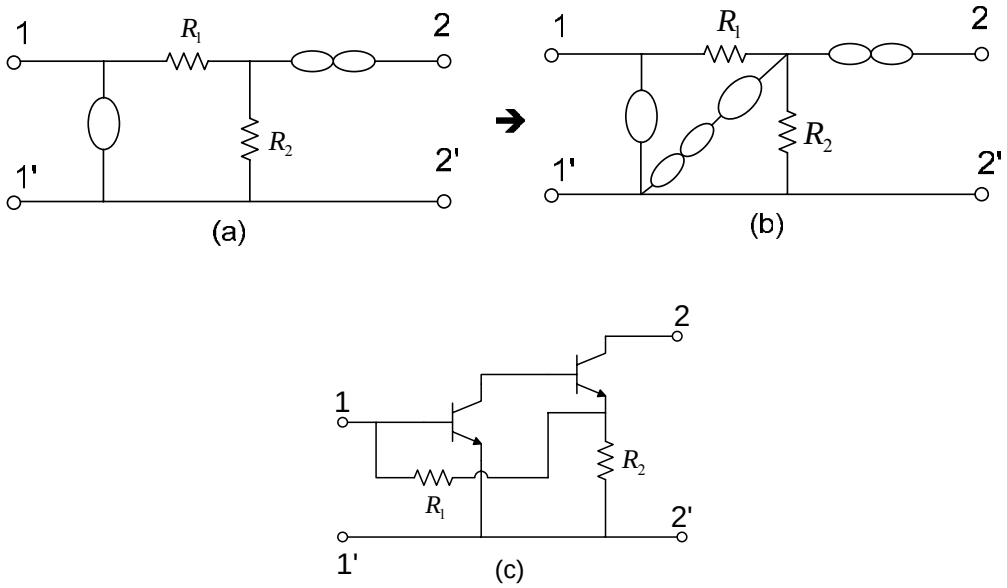


Figure 2.16 Process conversion of CCCS nullor to transistor equivalent

Another realization based on nullor equivalencies is the realization of active inductances by means of gyrators [9]. An ideal gyrator is a two-port network characterized by an admittance matrix:

$$[y] = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix} \tag{2.3.1}$$

Thus, in terms of the y-paramters, we have,

$$I_1 = gV_2 \tag{2.3.2}$$

$$I_2 = -gV_1 \tag{2.3.3}$$

where g is the gyration conductance. Its symbol is shown in Figure 2.17.

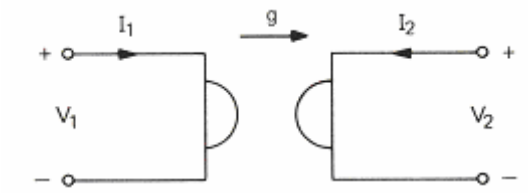


Figure 2.17 Ideal gyrator symbol

One way to realize a gyrator is by means of controlled sources. Expressing the y matrix of an ideal gyrator as the sum of two y matrices yields,

$$[y] = \begin{bmatrix} 0 & g_1 \\ -g_2 & 0 \end{bmatrix} = \begin{bmatrix} 0 & g_1 \\ 0 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -g_2 & 0 \end{bmatrix} \tag{2.3.4}$$

If let $[y_A] = \begin{bmatrix} 0 & g_1 \\ 0 & 0 \end{bmatrix}$ and $[y_B] = \begin{bmatrix} 0 & 0 \\ -g_2 & 0 \end{bmatrix}$ a gyrator is design realizing $[y_A]$ and $[y_B]$ separately and then connect resulting network in parallel. From the defining equations, $[y_A]$ and $[y_B]$ represent a positive and a negative voltage-controlled voltage source respectively. Connecting these two VCCS in parallel, an equivalent gyrator representation is obtained as shown in Figure 2.18.

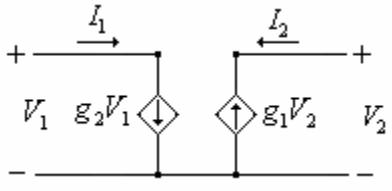


Figure 2.18 Equivalent gyrator circuit based on controlled sources

The admittance resultant matrix equation yields,

$$[y] = \begin{bmatrix} 0 & g_1 \\ -g_2 & 0 \end{bmatrix} \tag{2.3.5}$$

Using the nullor equivalencies based on controlled sources, an equivalent nullor network based on the VCVS results for the realization and is shown in Figure 2.19.

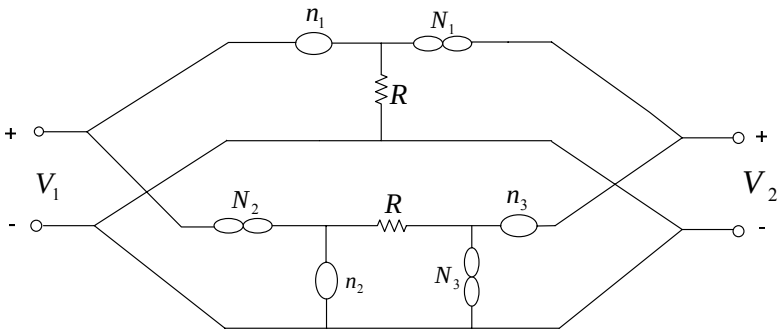


Figure 2.19 Nullor realization of VCCS gyrator based circuit

It is clearly identified that three pairs of transistors are generated. These are (n_1, N_1), (n_2, N_2) and (n_3, N_3). One of the possible transistorized implementations is shown in Figure 2.20.

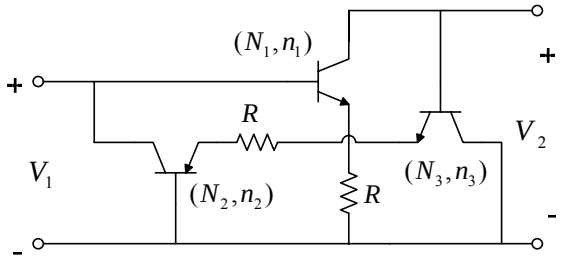


Figure 2.20 Transistorized generated circuit based on nullors

An equivalent active inductance is realized by connecting a capacitor at the gyrator output. This is shown in Figure 2.21.

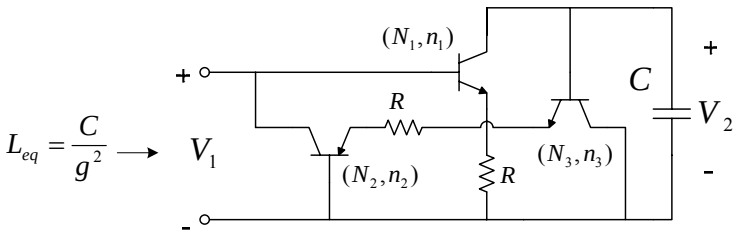


Figure 2.21 Transistor realization of an active inductance

2.3.2 Operational Amplifier realizations based on nullors

Figure 2.22 shows a nullor based general immittance converter (GIC). It can transform to an impedance or admittance with a terminated load.

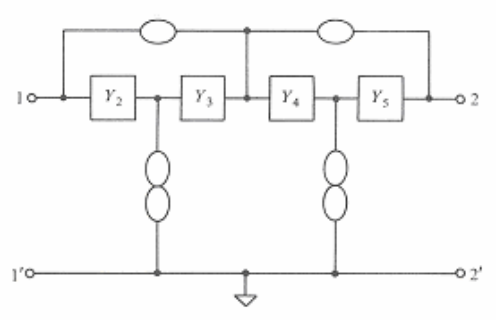


Figure 2.22 Nullor based general immittance converter

If, for example terminals 2-2' are terminated with conductance G_6, the driving-point admittance Y_{1d} for $Y_2 = G_2, Y_3 = sC_3, Y_4 = G_4$ *and* $Y_5 = G_5$ is calculated as:

$$Y_{1d} = \frac{G_2 G_4 G_6}{s C_3 G_5} \tag{2.3.6}$$

One of the main applications of GIC's is the inductance simulation. The general idea of inductance simulation is simply to replace the inductance elements of a passive LC filter by GIC-simulated inductances. As one would expect, the nonideal performance

of the simulated inductance becomes of critical importance on most active filters that are designed this way.

Figure 2.23 shows the equivalent operational amplifier network of Figure 2.22. Each admittance has been replaced by either a conductance (G_2, G_4, G_5, G_6) and by a capacitance C_3. The equivalent inductance value is:

$$Z_{1d} = \frac{1}{Y_{1d}} = s\frac{C_3 G_5}{G_2 G_4 G_6} \tag{2.3.7}$$

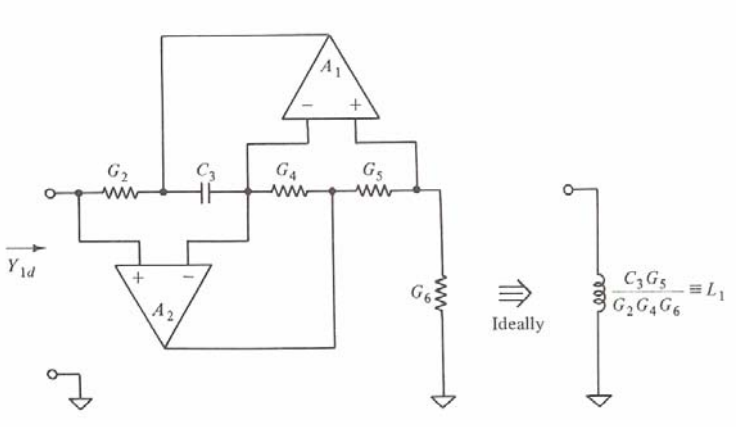


Figure 2.23 Equivalent GIC using operational amplifiers

2.4 Four Terminal Floating Nullor (FTFN)

A nullor approximation with both input and output ports floating is called a Four Terminal Floating Nullor (FTFN). An approximation of the FTFN as in [6] is shown in Figure 2.24.

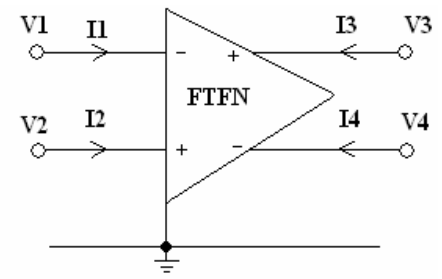


Figure 2.24 Four Terminal Floating Nullor block representation

At the input the nullator is defined by

$$\begin{aligned} I_1 &= -I_2 \\ I_1 &= 0 \\ V_1 - V_2 &= 0 \end{aligned} \tag{2.4.1}$$

and the norator by:

$$I_3 = -I_4 \tag{2.4.2}$$

The equation $I_3 = -I_4$ makes the FTFN fulfill Kirchhoff current law, $I_1 = -I_2$ is the equation added to the all-zero chain matrix (2.1.1). From these equations it is seen that the FTFN accurately equates two voltages connected to the terminals of the input port, like a standard operational amplifier, but in addition, it accurately equates two currents connected to the terminals of the output port. That is why some researchers claim that an FTFN combining both voltage and current mode capabilities is a more versatile analog building block than the operational amplifier or second-generation current conveyor [1, 15, 16]. For such purpose, different physical realizations of a nullor have been proposed and some of these are presented next.

Chapter 3 Antecedents of nullor realizations

It has been shown in Chapter 2 how nullors were employed as elements in circuits. Specifically, theoretical reference and modeling were given deep treatment. In this chapter, antecedents motivated by its use, started to search for a physical implementation and some of these are shown next.

3.1 Monolithic Nullor

The first floating output operational amplifier implemented with a nullor in mind was proposed by Huijsing and Korte in 1977 with their monolithic nullor [17]. The circuit is shown in Figure 3.1. A brief description follows. The input stage consists of a differential-pair amplifier (Q_{19}, Q_{20}) and is provided with circuit for input current cancellation, reducing the input bias current. A symmetrical voltage level shift stage (Q_{29}, Q_{30}) couples the input and output stages.

The output stage consists of a differential-pair and a Darlington connected transistors $Q_1 - Q_4$. On the other hand, the current source load, composed of Q_9 and Q_{13}, are enlarged by feedback of the base currents into the emitters by the NPN Q_{10} and Q_{14}. Miller compensation is performed to guarantee stability when connected in a feedback loop. Finally, external nulling of the input offset voltage can be provided at the external emitter connections of Q_{29} and Q_{30}. A drawback of this circuit is that the condition of arbitrariness of the output is pursued separately for each voltage node. This leads to an asymmetry in the device [5].

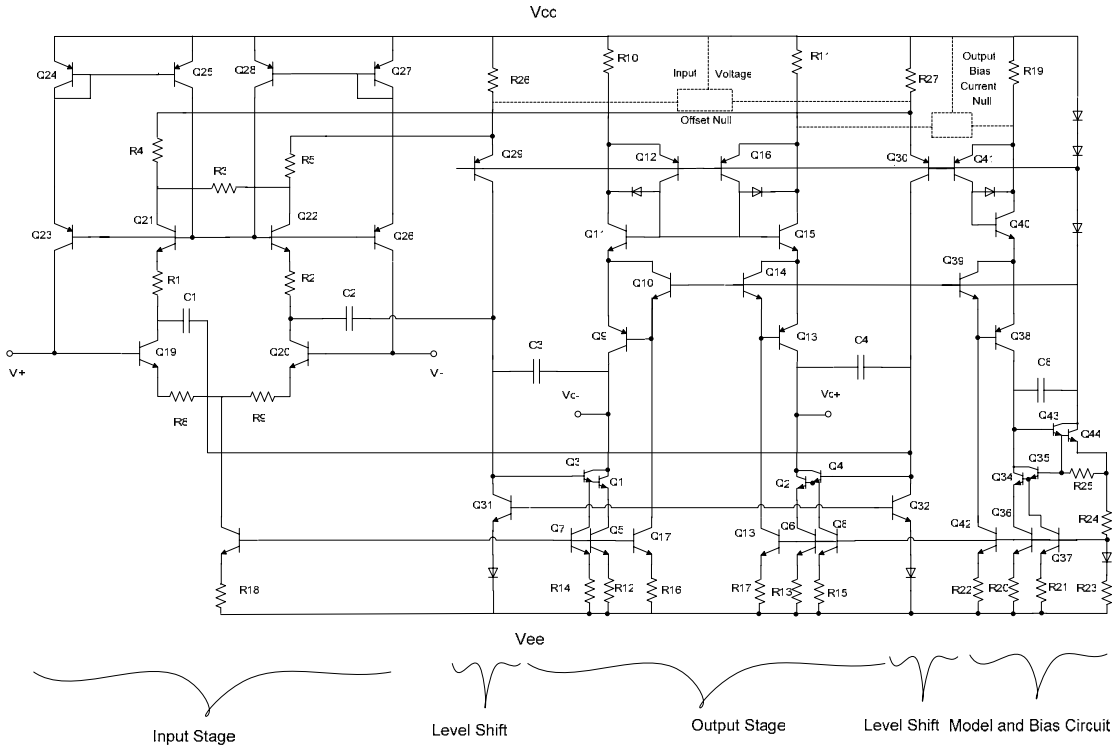


Figure 3.1 Monolithic Nullor

3.1.1 Operational Amplifier and Operational Floating Amplifier approach to a nullor realization

Even though a realization of a nullor had been proposed, the device itself was not quite accepted. A different approach to the realization of a nullor using cross-couple current mirrors technique was proposed [18]. A major contribution resulted from the above mention technique and a nullor based on an operational amplifier resulted as shown in Figure 3.2.

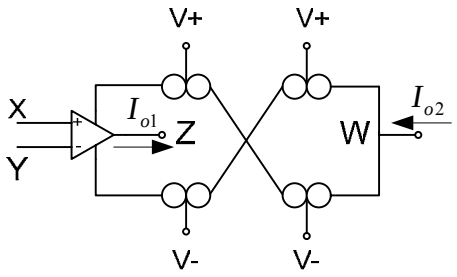


Figure 3.2 FTFN approach based on Operational Amplifier and Current Mirrors

This implementation exhibits low and high impedances at the output formed with terminals Z-W respectively. Therefore, it allows both voltage and current mode applications. If the output signal is desired to be in voltage mode, it can be obtained directly from the low impedance terminal whereas if the output signal is current it can be provided by the high impedance terminal. The main limitation of this FTFN type is that feedback can be established only between the voltage output while the current at the novel terminal cannot be established by feedback [19]. The performance is also limited by critical op-amp specifications.

A turning point to the nullor concept occurs when Huijsing proposed the Operational Floating Amplifier (OFA) [20]. The OFA concept is equivalent to a FTFN. A different approach from the presented above technique was the introduction of class A and class AB operation. These are now presented starting with the former classification. It is important to notice that the change in name from nullor to OFA, attracted more attention.

3.1.2 Class-A OFA with current source isolation of floating output

A class-A OFA design is achieved with the output currents satisfying the following relation:

$$I_{o1} = -I_{o2} \tag{3.3.1}$$

This can be achieved by a floating, or isolated output stage [21]. A class-A output stage with current source isolation of floating output port is shown in Figure 3.3. If we follow the output signal current I_{o1}, it is blocked by the current source I_1 from flowing to the positive supply. I_{o1} is forced to flow into M_1 and M_2 to the other output terminal as $-I_{o2}$. On its way it encounters I_3, I_4 and I_2, blocking the way towards the supply rail. Note that Q_1 and Q_2 formed a differential-pair providing good output common-mode rejection in the same way as input stage. A disadvantage of this circuit is that only half of the total output bias current $I_1 + I_2$ and $I_3 + I_4$ can be used for one output current I_{O1} and I_{O2}. Also, class A output stages provide a poor power efficiency and also low dynamic current range, expressed by the ratio between maximum output current and output-bias and output-bias-noise current [20].

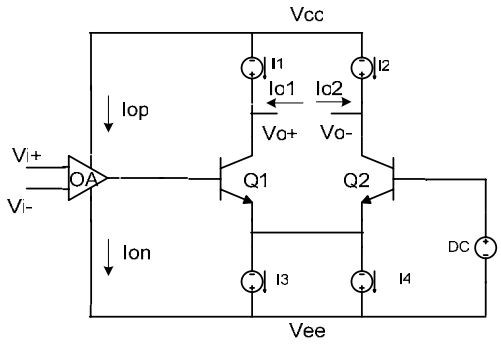


Figure 3.3 Class-A OFA with current source isolation of floating output port

3.1.3 Class-AB with supply current equalization

To surpass the problems of the class A OFA, a class-AB OFA would be a better choice. In this case it is made with the supply-current equalization method and is shown

in figure 3.4 [21]. If the total positive and negative supply currents are equal, the common-mode output current $I_{oc} = \frac{I_{o1} + I_{o2}}{2}$ must be zero, and thus the OFA requirement is fulfilled such that $I_{o1} = -I_{o2}$. The diodes D_1 and D_2 measure the positive and the negative total supply current I_{sp} and I_{sn}. These currents are mirrored to Q_5 and Q_6 at the same time being reduced by the $\left(\frac{1}{N}\right)$ ratio. The second opamp senses the differences in I_{Q5} and I_{Q6} at its positive input terminal. The output of this opamp is driven such that currents I_{Q5} and I_{Q6} are equal, so I_{sp} and I_{sn}.

A MOS version of this circuit is shown in Figure 3.5. A problem arises by the fact that the transistors $M_1 - M_4$ are not perfectly scaled, or will have different drain-source voltages, or different threshold voltages. The same problem is present in the bipolar case. This results in a non-linear current transfer. If such an OFA is used for audio signals, a noticeable distortion will be heard.

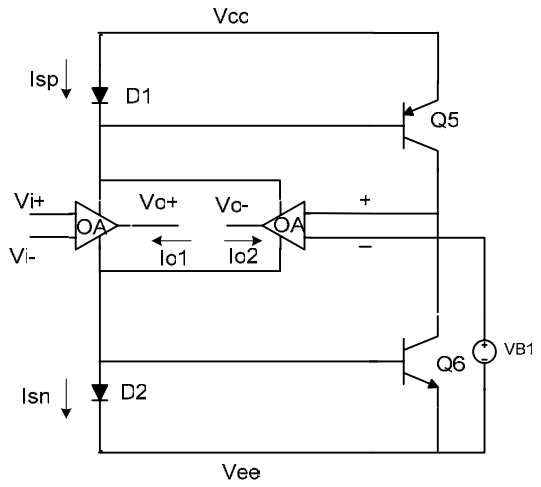


Figure 3.4 Class-AB with supply current equalization

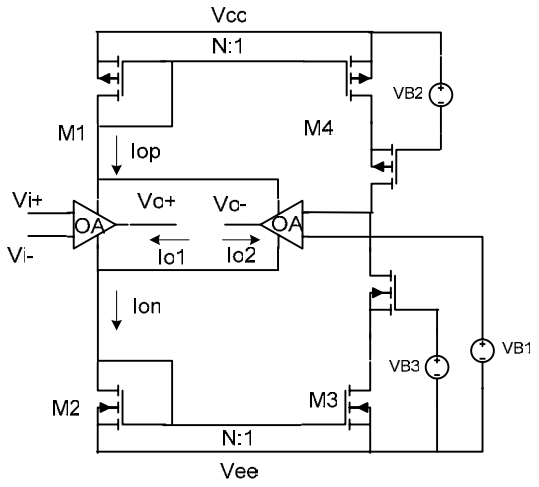


Figure 3.5 Class AB OFA realization with total-output supply current equalization

3.2 Current Conveyor approach to a FTFN realization

Another way to implement a nullor has been by means of current conveyors. The theory behind this approach is based on the representation of any kind of floating controlled source (VCVS, VCCS, CCVS, and CCCS) in terms of nullors. Let us demonstrate an example of a FTFN realization. Figure 3.6, which is a VCCS, is used as the starting point.

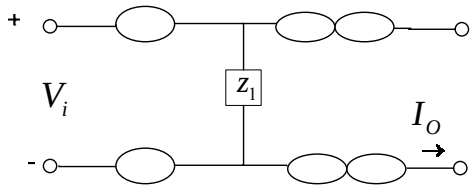


Figure 3.6 Voltage-Controlled Current Source nullor realization

Recall from Chapter 2 that a current conveyor is equivalent to a three terminal nullor. Thus, in this circuit two current conveyors are identified. This is shown in Figure 3.7.

Changing both equivalencies by that of current conveyors and letting $z_1 = 0$ a FTFN CC based realization is obtained as Figure 3.8 shows.

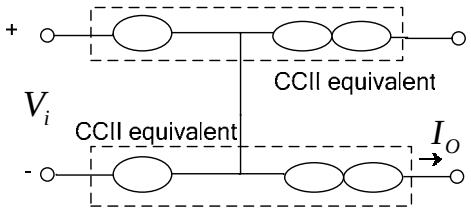


Figure 3.7 CCII equivalent embedded in nullor network when Z1=0 for infinite gain.

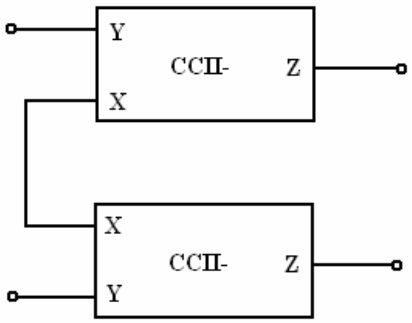
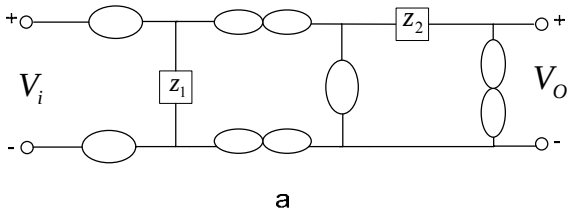


Figure 3.8 CCII- realization from nullor network

Other configurations can be considered using other controlled-source nullor realizations. Table 3.1 shows the nullor equivalence of the controlled sources.

Controlled Source	Nullor realization
VCVS	

a

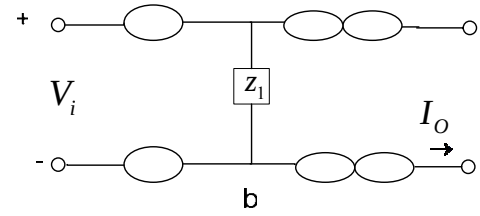
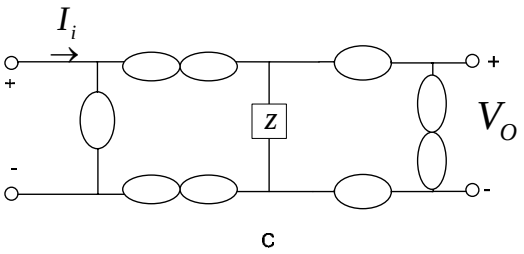
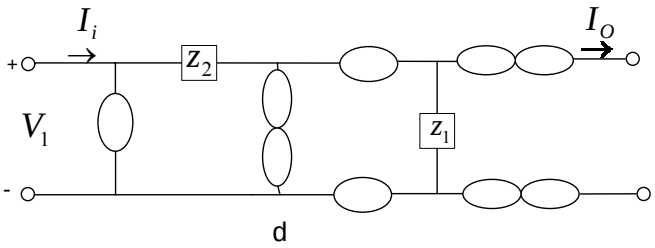
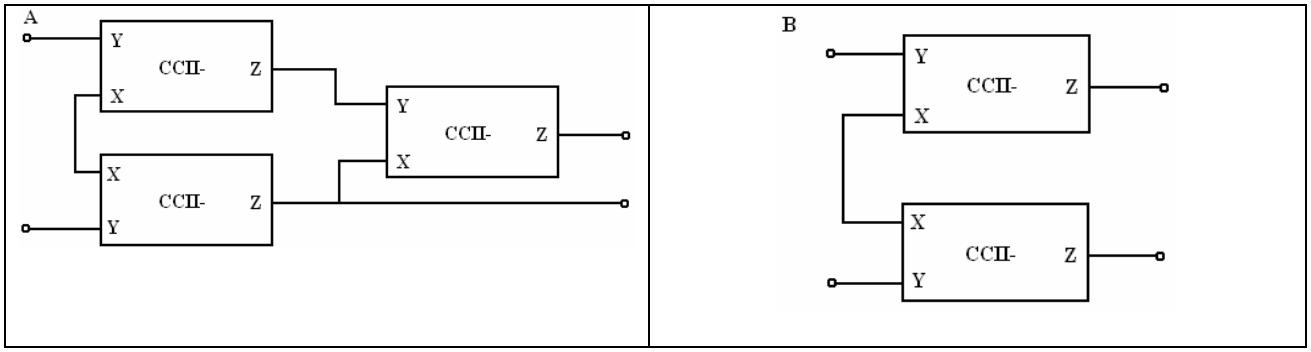
VCCS	
CCVS	
CCCS	

Table 3.1 Controlled Source realization based on nullors

From the dependent sources, four possible nullor implementations are obtained as shown in Figure 3.9.



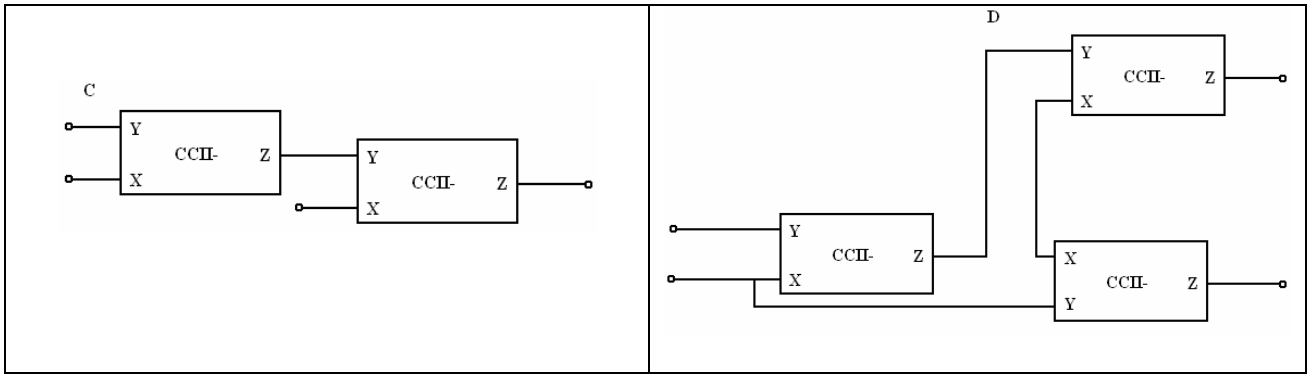


Figure 3.9 Current Conveyor FTFN realizations

These four nullor implementations although ideally equal, differ in practice due to the influence of the internal parasitic impedances and the different nature of input and output terminals with their corresponding impedance levels. Figure 3.9B is the most used approach to realize FTFN behavior and can be implemented in breadboard by connecting two AD844, current feedback op-amp IC's.

3.3 Other FTFN transistor based implementations

A growing interest in the realization of FTFN was mostly of its potential and versatility in the analysis, synthesis and design of electric circuits. Because of this, several FTFN based on transistors have been proposed. Some representating ones are now discussed.

3.3.1 Folded Cascode implementation of FTFN

To achieve high dc gain and fast settling, a folded-cascode operational amplifier is used in many modern analog IC designs. A four terminal floating nullor was proposed in [22] using a folded-cascode. The circuit proposed combines the advantages of a cascade of common-source and common-gate amplifiers and a floating current source. The common-source and common-gate, also known as folded-cascode is shown in Figure

3.10. Transistor $M_1 - M_{11}$ performs the common-source and common-gate amplification which provide large voltage gain over a wide frequency range. This voltage is converted into two balance output currents by the floating current source, formed from $M_{12} - M_{17}$ transistors, which require no transistor matching constraint unlike the current mirrors structure. Essentially, this stage consists of two matched CMOS inverters biased by two current sources and operates as an analogue transconductor stage. Note that transistors $M_8 - M_{11}$ perform an improved Wilson current mirror.

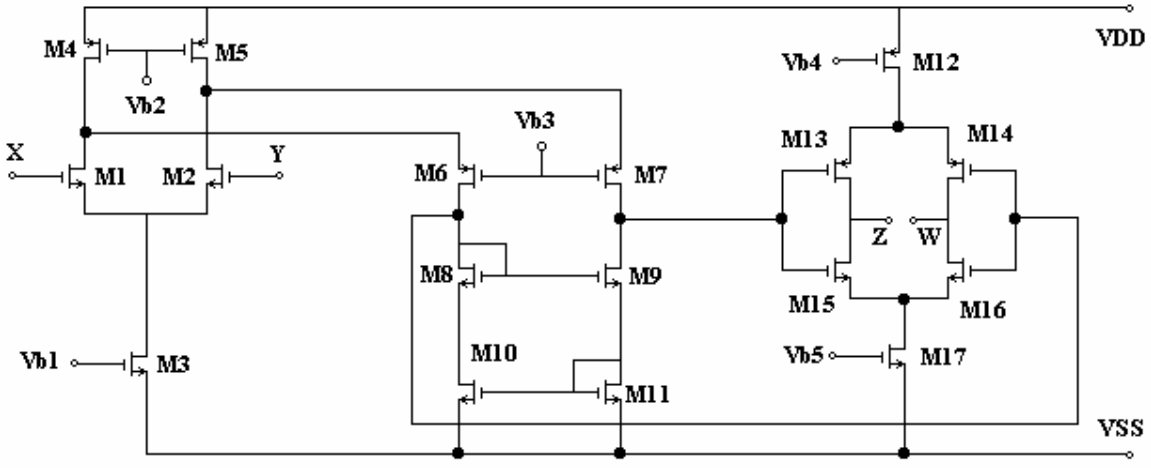


Figure 3.10 Common-source, common-gate FTFN

3.3.2 Balanced FTFN implementations

In modern systems, analog and digital signals are implemented in the same integrated circuit (IC) chip. Therefore, it is required to implement the analog part using fully-balanced architectures. Fully-balanced systems are more immune to digital noise and are used to increase the dynamic range, reduce harmonic distortion, and minimize the

effect of coupling between various blocks [23]. A fully-balanced FTFN (FBFTFN) circuit block and transistor-level circuit are shown in Figure 3.11 and 3.12 respectively.

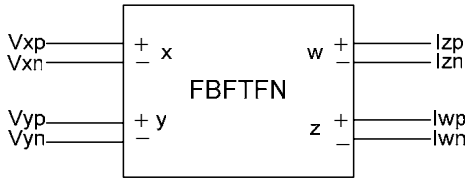


Figure 3.11 Fully-Balanced FTFN

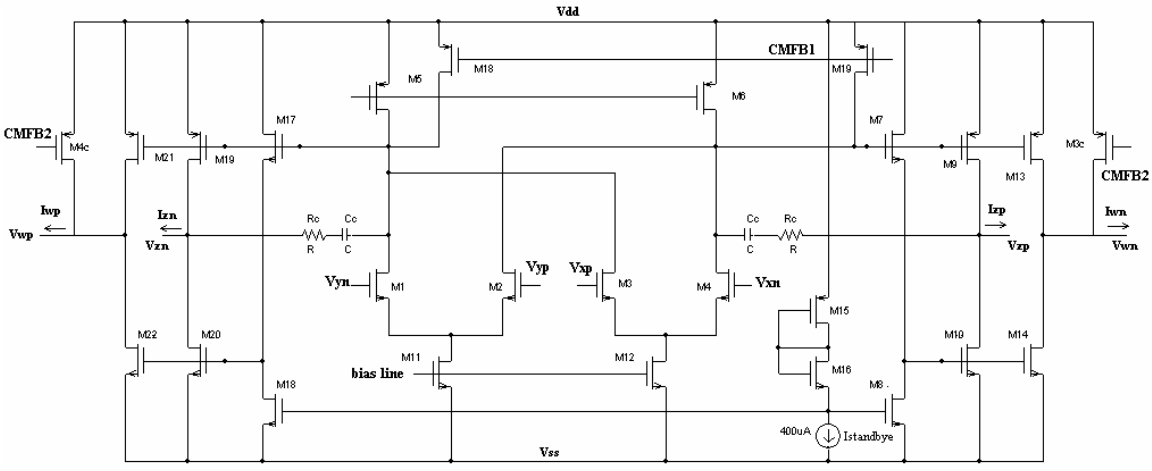


Figure 3.12 Fully-Balanced FTFN

The input stage uses two differential-pairs, each with a current source active load. A common-mode feedback is used at the input stage to maintain the common-mode voltage at a specific dc level. The second stage consists of class AB output stage. This particular circuit achieves well determined low standby power consumption with good output current driving capability instead of the conventional class A counterparts. Also, another common-mode feedback at the output is needed to maintain dc common-mode voltage at a desired level. This type of circuit to, unlike the op-amp, can be configured as an inverting voltage-controlled voltage source with infinite input impedance.

3.3.3 CMOS FTFN based on translinear cells

CMOS translinear loops have been used widely in design of current-mode circuits. A CMOS FTFN based on translinear cells proposed in [24] is shown in Figure 3.13. Transistors $M_1 - M_8$ perform the two mixed translinear-loops. The loops are biased by constant current source I_b creating equivalent high input impedance at both inputs $V_i +$ and $V_i -$. The output currents are created with cascode current mirrors and formed by transistors $M_9 - M_{24}$. Both of these cascode current mirrors form the $V_O +$ and $V_O -$ output port.

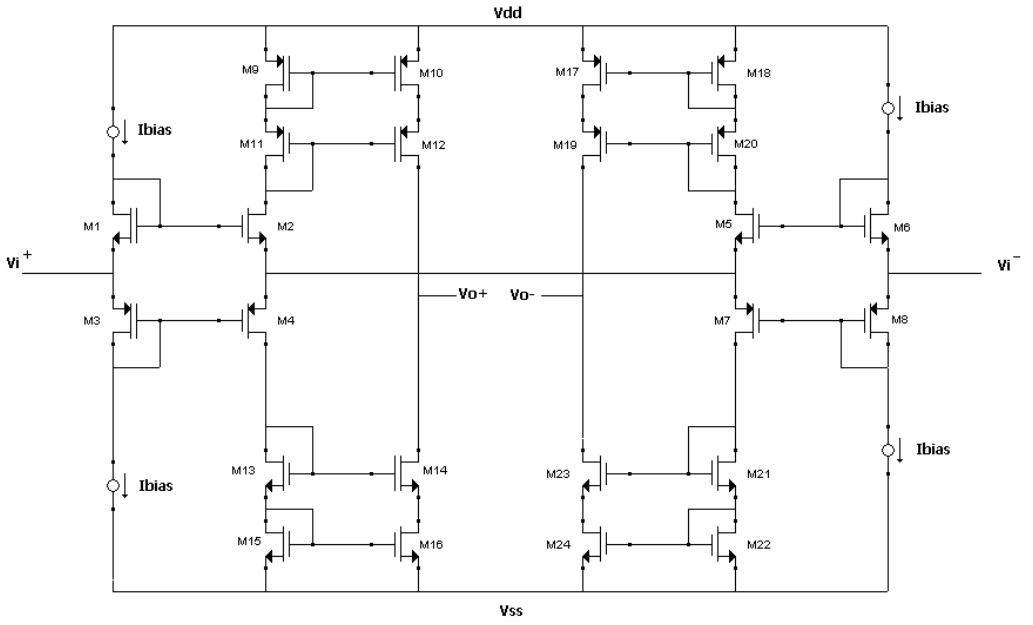


Figure 3.13 FTFN based on translinear cell

Based on all the implementations so far, specific considerations to the design of the FTFN proposed here are presented next.

Chapter 4 Design of an FTFN or floating amplifier circuit device

In this chapter, a design approach to an FTFN is presented. Specific considerations are first introduced to get grasp of the desired properties of such device. Based on this, a block diagram is presented where each of the block components are explained in detail. Emphasis is made on the technique used in each block, and if possible, mathematical background is considered.

4.1 FTFN design considerations

Specific considerations on the "universal" active device are necessary to establish a global vision of some desirable characteristics for the implementation of an actual "universal" amplifier as follows [25]:

1. The device must be a truly four terminal device, where no particular connection either to ground or between two terminals is a priori assumed.
2. For any practical implementation, the input and output sections do not present zero (arbitrary) current and voltage respectively. The ideal conditions

$$\begin{aligned} I_{in}^{+} &= I_{in}^{-} = 0 \\ I_{o}^{+} &= I_{o}^{-} \end{aligned} \tag{4.1.1}$$

although not achievable for real practical implementations, should be pursued to achieve a performance closer to that of the ideal FTFN. These conditions are presented within figure 4.1 [5].

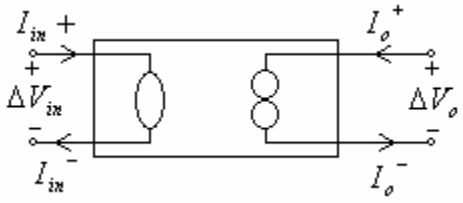


Figure 4.1 Real behavior of FTFN

where $I_{in}^{+} = I_{in}^{-}$ and $I_o^{+} = I_o^{-}$ are the input and output currents respectively. Also, a differential voltage at the input and output must be pursued. However, at the output the condition of arbitrariness must be pursued as a differential voltage ΔV_{no}, not separately for each terminal voltage.

3. The condition of arbitrariness of either voltage or current at the output section and the null value at the input section is usually achieved by producing a high gain (also transconductance or transimpedance) in combination with feedback.

One possible representation of the FTFN based on the above considerations is shown in figure 4.2. The input section consists of two voltage buffers whose outputs are connected through a resistor r_x which is the joint effect of the connection. To approach an ideal performance, this resistance should be low enough such that the condition of $\Delta V_i = 0$ and $I_i = 0$ is satisfied. At the output section we have two CCCS whose currents are, with opposite direction, copies of the current flowing from one buffer to the other. In practice, these two currents can be obtained by either mirroring the output stages of the two buffers or mirroring only one of them.

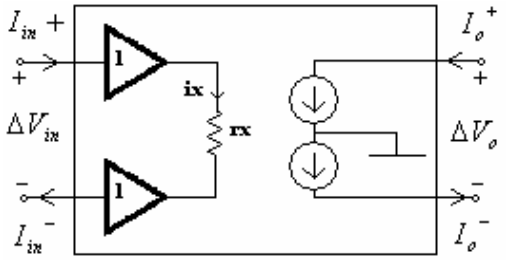


Figure 4.2 Transconductor representation of an FTFN

In general, any configuration that corresponds to the behavior of the four controlled sources in a differential way is an approximation of FTFN's. Thus, fully differential circuits are recommended for designing FTFN's.

4.2 General description of FTFN

4.2.1 FTFN block diagram

A possible block diagram for the realization of an FTFN is shown in Figure 4.3. It consists of a self-bias circuit, input, level shift and output stage. Finally, two common-mode feedback (CMFB) schemes are also included as part of the design.

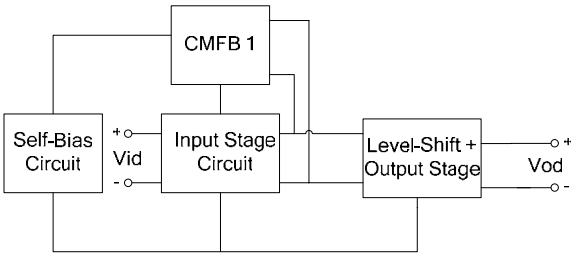


Figure 4.3 FTFN block level diagram

Another configuration posssible for the implementation of an FTFN is shown in Figure 4.4.

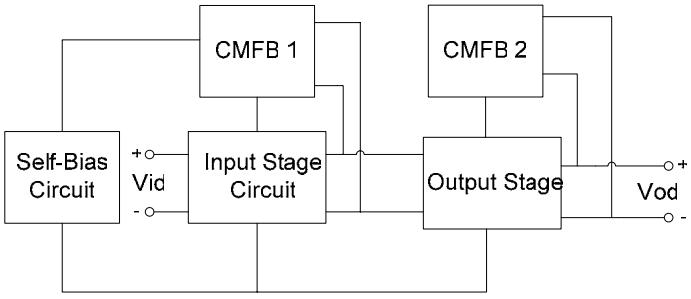


Figure 4.4 Second approach to design an FTFN

Instead of using only one CMFB at the input, an additional CMFB scheme is used at the output. Since these configurations will be used in this work, each block will be succinctly described.

4.2.2 Self-Bias Circuit

Power-supply sensitivity can be greatly reduced by the use of the so-called bootstrap bias technique, also referred to as self-biasing [27]. Instead of connecting a resistor to the supply, the input current is made to depend directly on the output current of the current source itself. Figure 4.5 shows the block diagram of the biasing scheme.

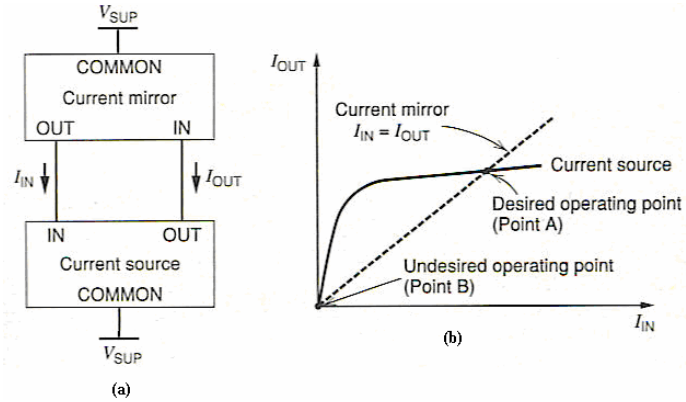


Figure 4.5 Block representation transfer curve for bias circuit

If the output current increases for any reason, the current mirror increases the input current by the same amount because the gain of the current mirror is assumed to be unity. As a result, the current source increases the output current by an amount that depends on the gain of the current source. Therefore, the loop responds to an initial change in the output current by further changing the output current in a direction that reinforces the initial change. The connection of a current source and current mirror form a positive feedback loop, and the gain around the loop is the gain of the current source. From the standpoint of the current source, the output current is almost independently of the input current. On the other hand, the current mirror sets I_{IN} equal to I_{OUT} as the mirror presents unity gain. The operating point of the circuit must satisfy both constraints and these are achieved at the intersection of the characteristics shown in figure 4.5b.

A self-biasing V_t reference circuit shown in Figure 4.6 is the selected configuration for biasing the FTFN [27].

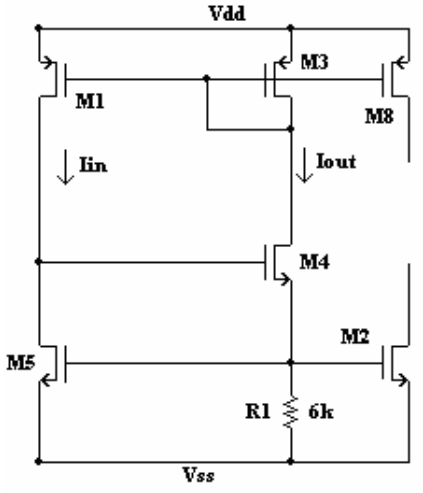


Figure 4.6 Self-biasing Vt reference

Transistors M_1 and M_3 form a current mirror and transistor M_4 and M_5 form a current source. On the other hand, transistors M_2 and M_8 are used to distribute the currents to other blocks. The output current calculated from figure 4.4 results in:

$$I_{OUT} = \frac{V_{GS5}}{R_1} = \frac{V_{tn} + V_{ov5}}{R_1} = \frac{V_t + \sqrt{\frac{2I_{in}}{k'\left(\frac{W}{L}\right)_5}}}{R_1} \tag{4.2.1}$$

where $V_{ov5} = V_{GS5} - V_{tn} = \sqrt{\frac{2I_D}{k'\left(\frac{W}{L}\right)}}$ is the overdrive voltage of transistor M_5

It is important to keep the gain of the feedback loop less than unity for proper operation [27]. Since the current mirror is assumed to be unity, the current source must compensate for this gain.

The self-biasing V_t reference circuit does not guarantee proper operation by itself. The addition of a start-up circuit as shown in figure 4.7 is necessary for the circuit to work properly. Additionally, this circuit must not interfere with the normal operation of the reference once the desired operating point is reached. Transistors M_6, M_7 and M_9 form such circuit. If the circuit is in the undesired zero-current state, the gate-source voltage of M_5 would be less than a threshold voltage. As a result, M_6 is off and M_7 operates in the triode region, pulling the gate-source voltage of M_9 up to V_{DD}. Therefore, M_9 is on and pulls down on the gates of M_1 and M_3. This action causes current to flow in M_1 and M_3, avoiding the zero-current state.

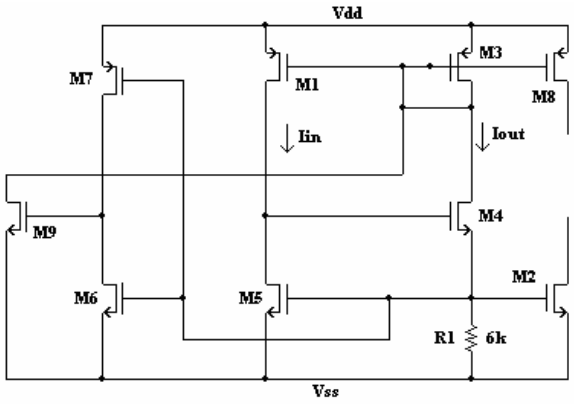


Figure 4.7 Self-biasing Vt reference with start-up circuit

In steady-state, the gate-source of M_6 rises to $I_{out} R$, which turn-on M_6 and reduces the gate-source voltage of M_9. In other words, M_7 and M_6 form a CMOS inverter whose output falls when the reference circuit turns on. Since the start-up circuit should not interfere with normal operation of the reference in steady state, the inverter output should fall low enough to turn M_9 off in steady state. Therefore, the gate-source voltage of M_9 must fall below a threshold voltage when the inverter input rises from zero to $I_{out} R$. In practice, this requirement is satisfied by choosing the aspect ratio of M_6 to be much larger than that of M_7.

4.2.3 Common-Mode Feedback (CMFB)

A Common-Mode Feedback (CMFB) block diagram is shown in Figure 4.8. It averages both differential output voltages to produce a common-mode voltage V_{CM}. This operation is executed at the Common-Mode Detector (CMD). Voltage V_{CM} is then compared to a desired reference common-mode voltage, V_{CMR}, usually equal to the

average of the two power supplies, or analog ground. The difference between V_{CM} and V_{CMR} is amplified and this error voltage is used to change the common-mode bias current of the amplifier to force V_{CM} and V_{CMR} to be equal.

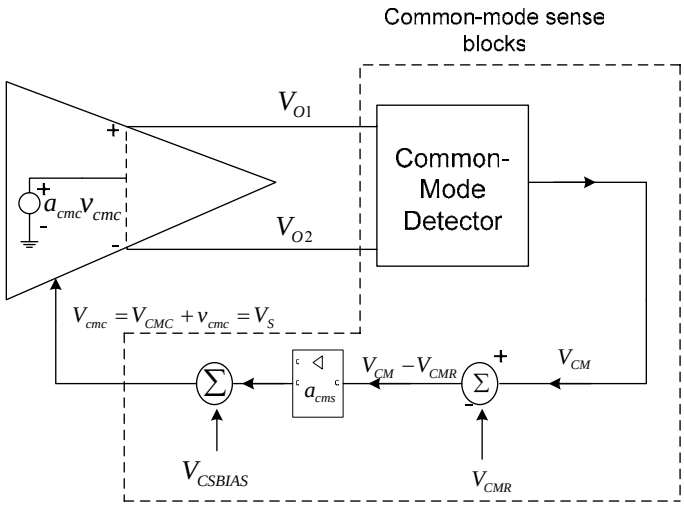


Figure 4.8 General block diagram of CMFB

The voltage V_{cmc} used as common-mode control is calculated from Figure 4.8 as:

$$V_{cmc} = a_{cms}(V_{CM} - V_{CMR}) + V_{CSBIAS} \tag{4.2.2}$$

A dc voltage V_{CSBIAS} is added such that when $V_{CM} \approx V_{CMR}$ then $V_{cmc} \approx V_{CSBIAS}$.

To demonstrate the use of the CMFB, we will use Figure 4.9 which shows the connection between a current-mirror differential amplifier and its CMFB circuitry [28]. The CMFB control voltage V_S changes the common-mode bias current of the op-amp by controlling the gate to source voltage of M_3 and M_5. As V_S increases, the bias current being sunk into the drain of M_3 and M_5 also increases, causing an equal reduction in the voltage of

nodes V_O^+ and V_O^-, thereby decreasing V_{CM}. As V_S decreases, the bias current sunk into the drain of M_3 and M_5 decreases thereby increasing V_{CM}.

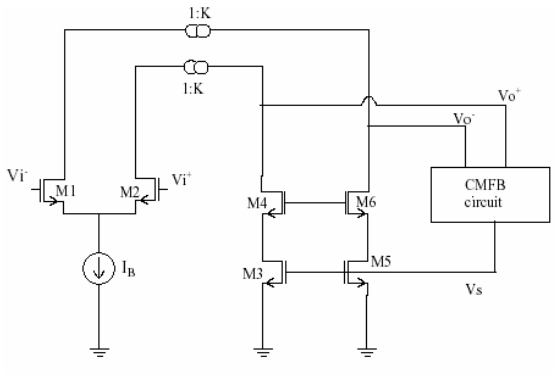


Figure 4.9 Current-mirror op-amp with CMFB circuit

Most CMFB circuits can be divided into 3 general categories: Differential difference amplifier (DDA) CMFB circuits, Switched-Capacitor (SC) CMFB circuits, or resistor-averaged CMFB circuits. The major distinction between these three categories is the technique used to average the differential output voltages to produce the common-mode voltage V_{CM}. Only the DDA will be discussed here. Prior to the considerations of the CMFB structures, several issues should be taken in design of these circuits [29]:

1. The CMFB has to center the common-mode output signal to a fixed but arbitrary chosen reference voltage. For maximal output swing half of the supply voltage is preferred.
2. The common-mode DC output voltage V_{CM} must be well stabilized and predictable, i.e., independent of matching between transistors, temperature, etc.

3. The bandwidth of the CMFB has to be greater than the bandwidth of the differential amplifier in order to ensure stable biasing conditions for all frequencies of interest up to GBW_D, where GBW_D corresponds to the differential amplifier gain-bandwidth product.
4. The differential input range of the CMFB has to be greater than the differential output range of the differential amplifier.

4.2.4 Differential Difference Amplifier (DDA) CMFB Circuits

Differential Difference Amplifier (DDA) CMFB circuits average two differential signals and compare that average to a reference common-mode voltage (V_{CMR}) in a single stage by using 4 identical transistors configured into 2 diff-pair structures [28]. One of the two transistors in each diff-pair is connected to V_{CMR} and the other two transistors are connected to the differential signals that are being controlled.

A straightforward implementation of this technique is shown in Figure 4.10. Assuming the differential signals, V_O^+ and V_O^-, are balanced with a common-mode voltage, V_{CM}, equal to V_{CMR}, we will have the same differential voltage in both differential pairs.

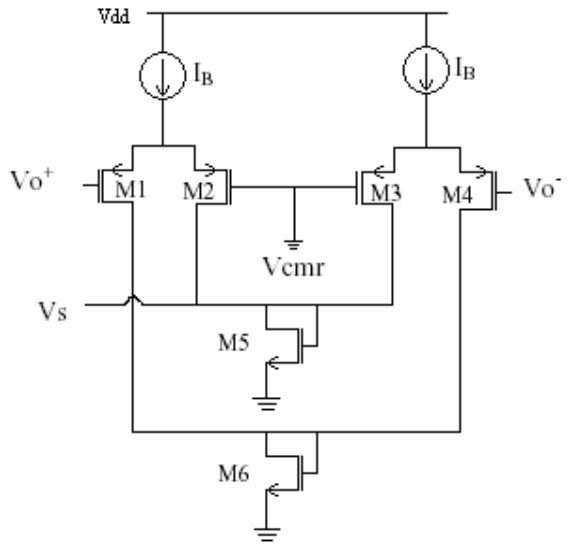


Figure 4.10 Differential Difference Amplifier CMFB Circuit

The following equations show the resulting drain currents (I_D) through transistors M_1 and M_4.

$$\begin{aligned} I_{D1} &= \frac{I_B}{2} - \Delta I \\ I_{D2} &= \frac{I_B}{2} + \Delta I \\ I_{D3} &= \frac{I_B}{2} - \Delta I \\ I_{D4} &= \frac{I_B}{2} + \Delta I \end{aligned} \tag{4.2.3}$$

where ΔI is the large-signal current change in I_{D2}. The current I_{D1} equals I_{D3} and, similarly, I_{D2} equals I_{D4}. The following relations hold for current I_{D5}:

$$\begin{aligned} I_{D5} &= I_{D2} + I_{D3} \\ I_{D5} &= (\frac{I_B}{2} + \Delta I) + (\frac{I_B}{2} - \Delta I) \\ I_{D5} &= I_B \end{aligned} \tag{4.2.4}$$

The size of transistor M_5 must be chosen so that when $I_{D5} = I_B$, which implies that V_{CM} of the differential outputs equals V_{CMR}, the value of the control voltage V_S being fed back to the differential amplifier establishes the correct common-mode output currents in the output stage of the amplifier to keep the common-mode output voltage at V_{CMR}.

Now assume that the differential signals, V_O^+ and V_O^-, are balanced with V_{CM} greater than V_{CMR}. Currents I_{D1} and I_{D4} will decrease, causing currents I_{D2} and I_{D3} to increase as shown in the following relations:

$$\begin{aligned} I_{D1} &= \frac{I_B}{2} - \Delta I_{CM} - \Delta I \\ I_{D2} &= \frac{I_B}{2} + \Delta I_{CM} + \Delta I \\ I_{D3} &= \frac{I_B}{2} + \Delta I_{CM} - \Delta I \\ I_{D4} &= \frac{I_B}{2} - \Delta I_{CM} + \Delta I \end{aligned} \tag{4.2.5}$$

The current increase through diode-connected transistor M_5 will cause voltage V_S to increase. As shown in Figure 4.6, this increase in V_S is applied to the gate of M_3 and M_5, which is part of the amplifier output stage current sink. The current being sunk into the drain of M_3 and M_5 will increase causing a reduction in the voltage of nodes V_O^+ and V_O^- thus reducing the common-mode output voltage V_{CM}. An analysis parallel to the one just presented can be used to describe the behavior of the CMFB circuit when the differential signals, V_O^+ and V_O^-, are balanced with V_{CM} smaller than V_{CMR}.

The main drawback of this CMFB implementation is a limited input range and the non-linear behavior of the differential pairs. If current source I_B is a simple current source consisting of a single active-mode PMOS transistor, the common-mode voltage at the input of each diff-pair is constrained to be less than $V_{DD} - V_{effB} - (V_{effD} + V_{tp})$, where V_{effB} is the effective voltage of the current source PMOS, V_{effD} is the effective voltage of the diff-pair transistors, and V_{tp} is the threshold voltage of the diff-pair transistors. Thus, this architecture can limit the maximum common-mode voltage to ~1.2 V below the positive supply.

If a cascaded current source is needed for output impendence enhancement, such as the wide-swing cascode current source, the allowable voltage swing will be reduced by more than 1.2V. For this reason, DDA CMFB implementations are suitable for circuits with small voltage swings and where V_{CM} is well below the positive supply.

4.3 FTFN Differential Input Stage: The negative-conductance gain-enhancement approach.

The differential amplifier is among the most important circuit inventions in analog electronics. Offering many useful properties, the differential operation has become the dominant choice in today's high-performance analog and mixed-signal circuits. An important advantage of differential operation is higher immunity to "environmental" noise. Also, maximum voltage swings are achieved with differential amplifier configurations.

High gain, accuracy and high speed are the two most important properties of analog circuits. The task of building such devices with high gain, high speed is a difficult problem. High accuracy requires high DC gain. On the other hand, the settling behavior of the differential amplifier determines the accuracy and the speed that can be reached. Fast settling requires single pole settling behavior and a high gain-bandwidth- product [30]. The high DC-gain differential amplifier can be implemented using one or more of the following techniques: gain-boosting technique, cascading stages, and positive-feedback gain enhancement, also known as negative-gain conductance approach.

Gain boosting technique is one of the most successful ways of boosting amplifier gain, even though boosting amplifier adds their own poles and zeros to the final amplifier, which affects amplifier settling slow [31],[32]. On the other hand, cascading two stages or more will result in a very high DC-gain. However, proper compensation for stable operation in cascading technique seriously limits the high frequency performance [33], [34]. Also limited output swing is obtained.

Another rare method to boost the gain is known as positive feedback technique or gain-enhanced negative conductance [35]. Positive feedback offers the ability of obtaining a very high DC-gain without affecting high frequency performance. In general, a negative resistance generated by feedback from the output node is used to compensate some positive resistance at the output to achieve a very high DC-gain.

The basic concept of gain enhancement by negative conductance compensation is shown in Figure 4.11. A negative resistance R_n is placed in parallel with the output impedance of the basic amplifier. A small signal analysis shows the dc gain of the amplifier to be:

$$A_V = \frac{V_O}{Vi} = \frac{-g_{M1}}{g_{ds1} + \frac{1}{R} + \frac{1}{R_n}} \text{ where } \frac{1}{R_n} = -(\frac{1}{R} + g_{ds1}) \qquad (4.3.1)$$

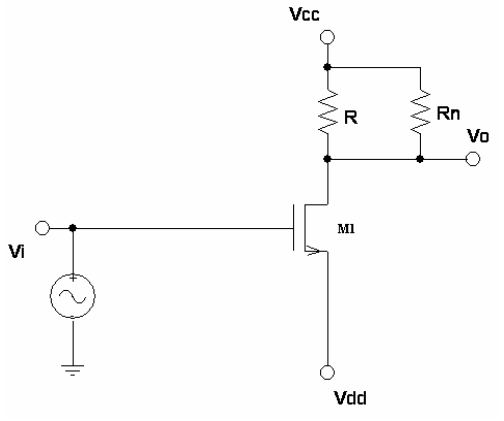


Figure 4.11 Basic Gain enhancement representation

The DC gain becomes theoretically, infinite when equation (4.3.1) is satisfied. Note there are no additional poles added, thus, the high-frequency response of the basic amplifier it's not adversely reduced and wide bandwidth is realized.

A simplified input stage is shown in Figure 4.12. Transistors M_1 and M_2 form a differential pair. The signal goes to M_3 and M_4, which are cascaded to M_1 and M_2. Connected to the source of is M_3 and M_4 the gate of M_5 and M_6 respectively. This is where the negative gain-enhancement takes place. These transistors form the group where the signal is processed. Transistor pairs M_7 and M_{23} are used as current sources. Bias voltages V_{bias1} through V_{bias5} are DC generated voltages. Finally, transistor M_{22} serves as the bias current source for the differential pair M_1 and M_2.

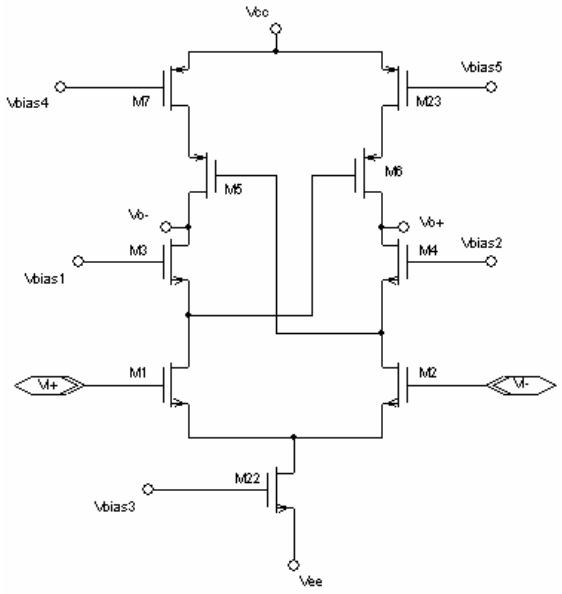


Figure 4.12 Simplified FTFN Input Stage

The complete input stage is shown in Figure 4.13. A Widlar current source is formed by transistors M_{11}, M_{12} and, M_{27}, M_{28} with a 3 kΩ resistor. This current source type is used to decrease the current by half in order to match the current passing through M_1 and M_2. Transistors M_3 and M_4 are biased by diode connected transistor M_{20} of the common-mode feedback. Three transistors receive a current from the bias circuitry.

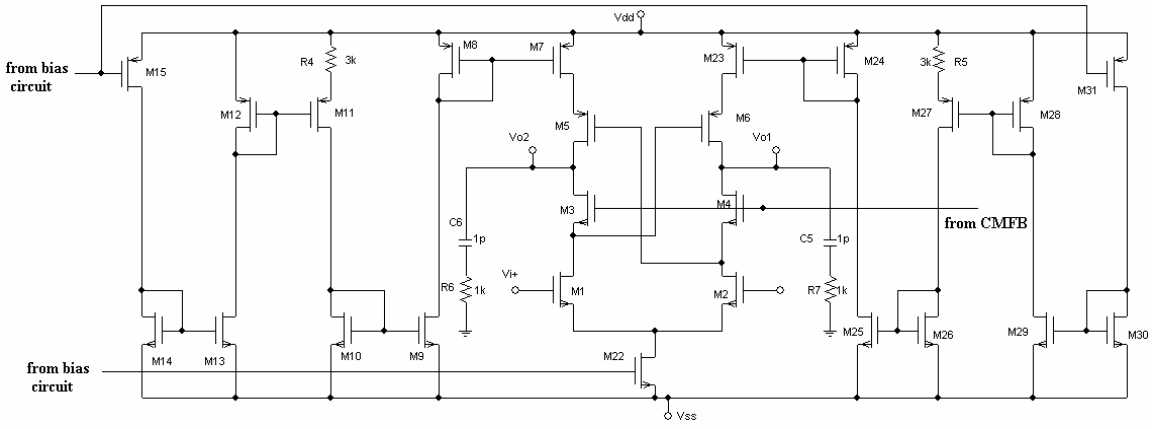


Figure 4.13 Complete input stage circuit

Compensation is realized by means of pole-zero compensation schemes. A capacitance of 1pF in series with a resistance of 1kΩ connected to the high impedance node forms the compensation scheme.

A problem arises with this circuit. First the output swing is limited and the output current is too low to drive a resistive load. Since the amplifier has a differential nature, two high-impedance nodes are recognized and a common-mode feedback structure is needed to control the output common-mode level.

To compensate for the output swing limit, an additional class AB output stage is used. It is shown in Figure 4.14. Class AB output stages are used to achieve well determined low standby power consumption with good output current driving capability instead of the conventional class A. For this FTFN, two rail-to-rail output stages are incorporated [23]. The first output stage consists of transistor $M_{90}, M_{93}, M_{94}, M_{97}$ and the second of transistors $M_{95}, M_{96}, M_{98}, M_{99}$. To bias both stages, transistors M_{88} and M_{89} are used as reference voltage generator. Considering the first output stage, its operation can be described by the following two translinear loops equations:

$$V_{SG94} + V_{GS97} + V_{GS90} = V_{dd} - V_{ss} \tag{4.3.2}$$

$$V_{SG98} + V_{GS89} + V_{GS93} = V_{dd} - V_{ss} \tag{4.3.3}$$

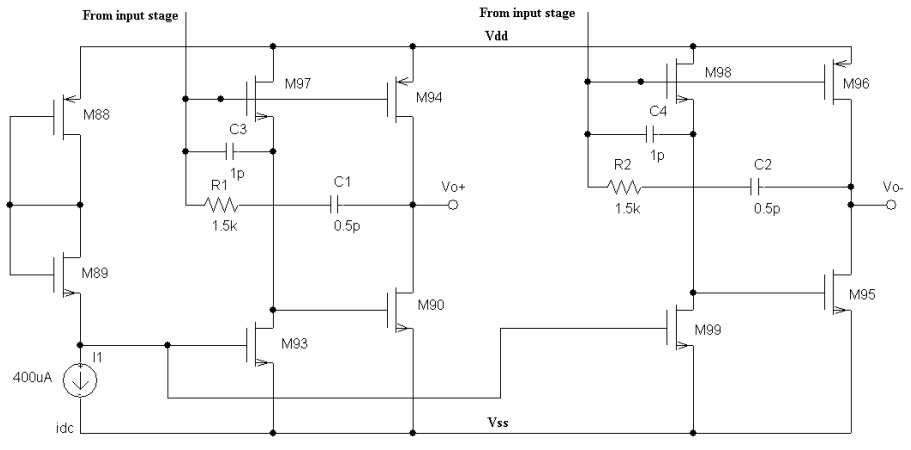


Figure 4.14 Rail-to-Rail Class AB output stage

Since transistors M_{93} and M_{97} have the same size and carry the same current, they have the same gate-source voltage:

$$V_{SG94} + V_{GS90} = V_{SG88} + V_{GS89} = \text{constant} \tag{4.3.4}$$

During standby-mode, no current is withdrawn from the output terminal and the currents of M_{94} and M_{90} are equal. Therefore, the current of the output transistors is equal to the standby current, which equals 400μA. When the circuit is supplying, transistor M_{94} will be fully conducting while M_{90} will be almost off. On the other hand, when the circuit is sinking current, M_{90} starts supplying while M_{94} will be almost off.

The complete circuit diagram is shown in Figure 4.15. The gain of this amplifier is composed of two stages: the input stage, the second stage, which is part of the translinear loop with the output stage. Using the half circuit analysis, the right half of the circuit is considered due to its symmetry nature. An approximated value of this gain resulted in:

$$A_V = A_1 A_2 \tag{4.3.5}$$

$$A_1 = \frac{g_{m1} g_{m5} g_{o4} (g_{o4} + g_{o6})}{(g_{m4} g_{o6} - g_{m3} g_{o4})} \tag{4.3.6}$$

$$A_2 = g_{m48} (r_{o96} \parallel r_{o95}) \tag{4.3.7}$$

The effect of negative-conductance gain enhancement is seen in the denominator of equation 4.3.6. To satisfy the condition of infinite gain the following condition must be pursued:

$$g_{m4} g_{o6} = g_{m3} g_{o4} \tag{4.3.8}$$

Finally, a Miller compensation scheme is added for pole-splitting. Also, a feedforward path is established by inserting a capacitor from gate to source to the common-drain transistors. A disadvantage on the previous configuration stems from the current mirror of bias current. Matched current mirrors are needed in order to keep equal input-output current relation.

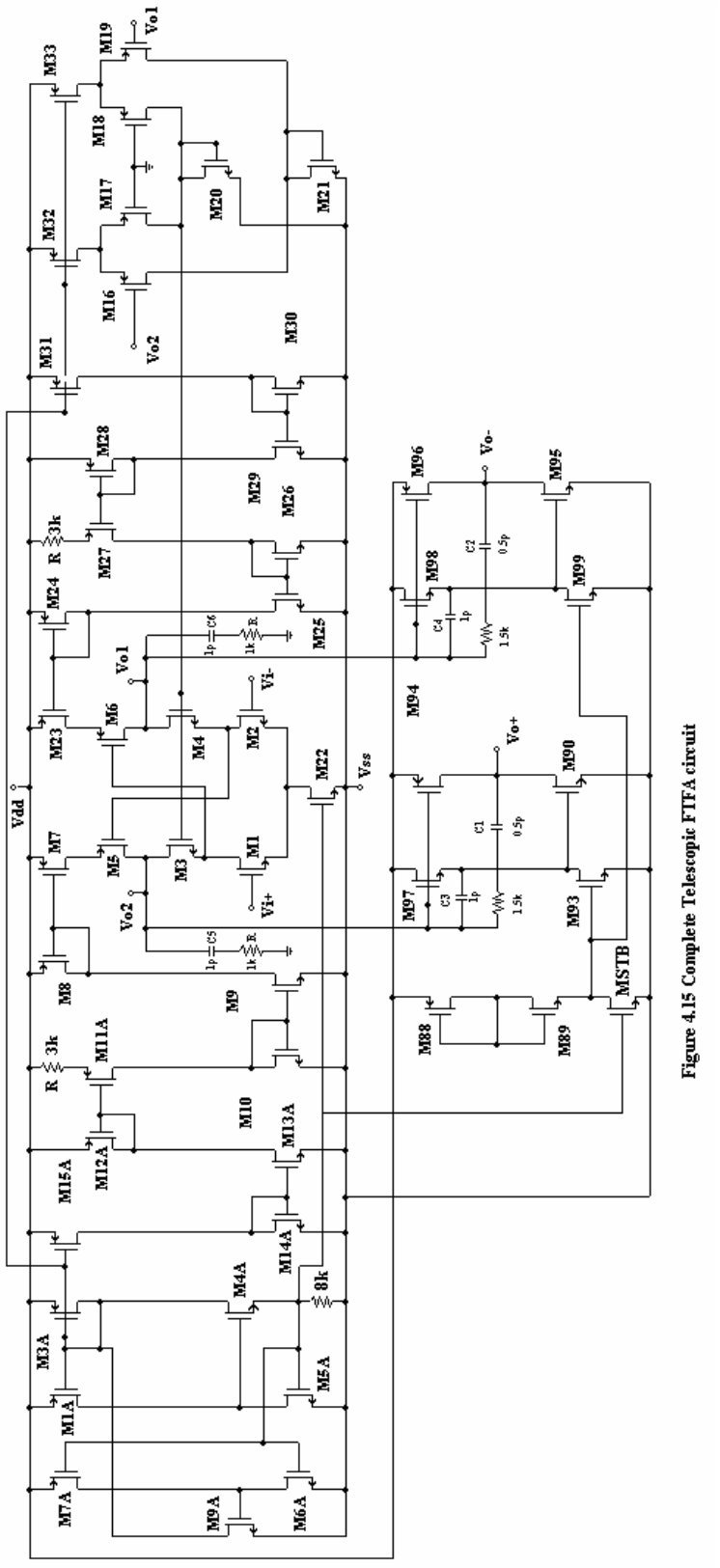


Figure 4.15 Complete Telescopic FTFA circuit

4.4 Folded-Cascode technique for high-frequency operation

A simple circuit design approach suitable for low-voltage and high frequency operation involves a folded-cascode with a feedforward path [36]. By introducing a zero at the non-dominant pole position, phase compensation is obtained, thereby enhancing high frequency response.

To get a grasp of this benefit, let's start with a simple folded-cascode small signal analysis. Figure 4.16 shows the circuit schematic and the high frequency circuit model. Analysis of the small signal of the circuit, which includes a load compensation capacitor yields:

$$\frac{V_o}{V_{in}} = \frac{\dfrac{g_{m2}C_{gd1}}{C_L C_{gs2}}\left(s - \dfrac{g_{m1}}{C_{gd1}}\right)}{s^2 + s\left(\dfrac{g_{m2}}{C_{gs2}}\right) + \left(\dfrac{1}{r_{o1}r_{o2}C_L C_{gs2}}\right)} \tag{4.4.1}$$

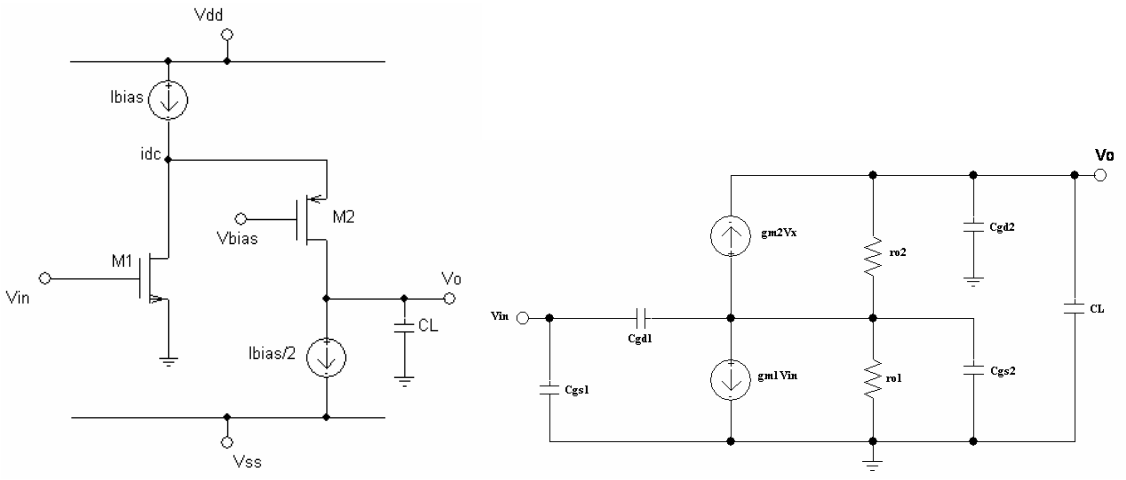


Figure 4.16 Folded-cascode circuit schematic and ac equivalent

Analysis of the small signal of the circuit, which includes a load compensation capacitor yields:

$$\frac{V_o}{V_{in}} = \frac{\frac{g_{m2}C_{gd1}}{C_L C_{gs2}}\left(s - \frac{g_{m1}}{C_{gd1}}\right)}{s^2 + s\left(\frac{g_{m2}}{C_{gs2}}\right) + \left(\frac{1}{r_{o1}r_{o2}C_L C_{gs2}}\right)} \tag{4.4.2}$$

These simplify expression is obtained using proper assumptions:

$$C_L >> C_{gd2},\ C_{gs2} >> C_{gd1} \text{ and } g_{m2}r_{o2} >> 1 \tag{4.4.3}$$

Equation 4.4.2 results in a two-pole, one-zero transfer function where:

$$p_1 = -\frac{1}{g_{m2}r_{o2}r_{o1}C_L} \qquad p_2 = -\frac{g_{m2}}{C_{gs2}} \qquad z_1 = \frac{g_{m1}}{C_{gd1}} \tag{4.4.4}$$

and p_1, p_2 and z_1 are the dominant pole, non-dominant pole and zero respectively. For better high frequency operation, pole p_2 must be as large as possible. To achieve this, transistor size ratio (W/L) must be increased. If minimum size lengths are used, only W is increased. The result of this will be an increase in gate-source capacitance which results in no overall change in pole p_2.

Another way to increase the magnitude of pole p_2 is by increasing the bias currents. However, this results in a power consumption increase. Notice that because of these trade-offs there's an upper limit for the non-dominant pole.

To overcome this limitation, a folded-cascode with feedforward is presented [36] in Figure 4.17. Here the gate of M_1 is also connected to the gate of M_2.

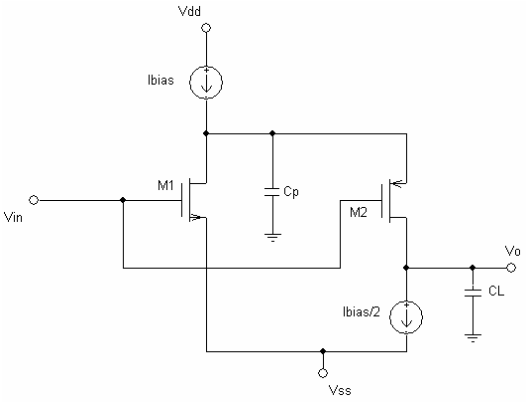


Figure 4.17 Folded-cascode with one-stage feedforward

The small signal analysis of this circuit yields the following:

$$\frac{V_o}{V_{in}} = \frac{\dfrac{C_{gd2}}{(C_L + C_{gd2})}\left\{ s^2 + s\left[\dfrac{g_{m2}(C_{gd2} - C_p)}{C_{gd2}(C_{gs2} + C_p)}\right] - \dfrac{g_{m1}g_{m2}}{(C_{gs2} + C_p)C_{gd2}}\right\}}{s^2 + s\left(\dfrac{g_{m2}}{C_{gs2} + C_p}\right) + \dfrac{1}{r_{o2}r_{o1}(C_{gs2} + C_p)(C_L + C_{gd2})}} \tag{4.4.5}$$

Suppose for an instant that $C_p = 0$. Then, the poles and zero values are calculated as:

$$\begin{aligned} p_1 &= -\frac{1}{g_{m2}r_{o2}r_{o1}C_L} & p_2 &= -\frac{g_{m2}}{C_{gs2}} \\ z_1 &= -\frac{g_{m1}}{C_{gd2}} & z_2 &= \frac{g_{m2}}{C_{gd2}} \end{aligned} \tag{4.4.6}$$

On the other hand if C_p is included, the pole and zero values are calculated as:

$$\begin{aligned} p_1 &= -\frac{1}{g_{m2}r_{o2}r_{o1}C_L} & p_2 &= -\frac{g_{m2}}{C_p + C_{gs2}} \\ z_1 &= -\frac{g_{m1}}{C_p - C_{gd2}} & z_2 &= \frac{g_{m2}(C_p - C_{gd2})}{C_{gd2}(C_p + C_{gs2})} \end{aligned} \tag{4.4.7}$$

If $C_p >> C_{gs2}$ and C_{gd2}, the coefficient of the **s** in the transfer function numerator changes from being positive to being negative. This results in the right hand plane zero now

occurring at higher frequencies and the left hand plane zero occurring at a frequency very close to that of the non-dominant pole such that cancellation can occur.

The improvement in high frequency behavior stems from the fact that, the non-dominant pole and the left-hand plane zero cancel exactly, and to obtain this cancellation the following condition must be satisfy:

$$p_2 = z_1 \tag{4.4.8}$$

Solving and rearranging algebraically for C_p yields:

$$C_p = \frac{g_{m1}C_{gs2} + g_{m2}C_{gd2}}{g_{m2} - g_{m1}} \tag{4.4.9}$$

It follows that to meet the condition 4.4.9, then g_{m2} must be greater than g_{m1} and their differences small enough such that $C_p >> C_{gs2}$ and C_{gd2}. In a no-load condition, pole p_1 will change its location to:

$$\mathrm{p}_1 = -\frac{1}{g_{m2}r_{o2}r_{o1}C_{gd2}} \tag{4.4.10}$$

Since $C_p >> C_{gd2}$, this indicates that pole p_1 moved to higher frequency. The magnitude of p_1 is still lower than p_2 and p_3 , thus their calculated positions are still valid.

A second folded-cascode stage has been added to increase gain. The same compensation scheme as explained above is considered. In this case, the compensation capacitance is realized by capacitor connected transistor that realizes an equivalent 0.1 pF capacitor. Once again, a combination of Miller-zero and feedforward compensation is used. The complete circuit schematic is shown in Figure 4.18. To verify the

performance of each circuit, SPICE simulations will be performed. This is the topic of chapter 5.

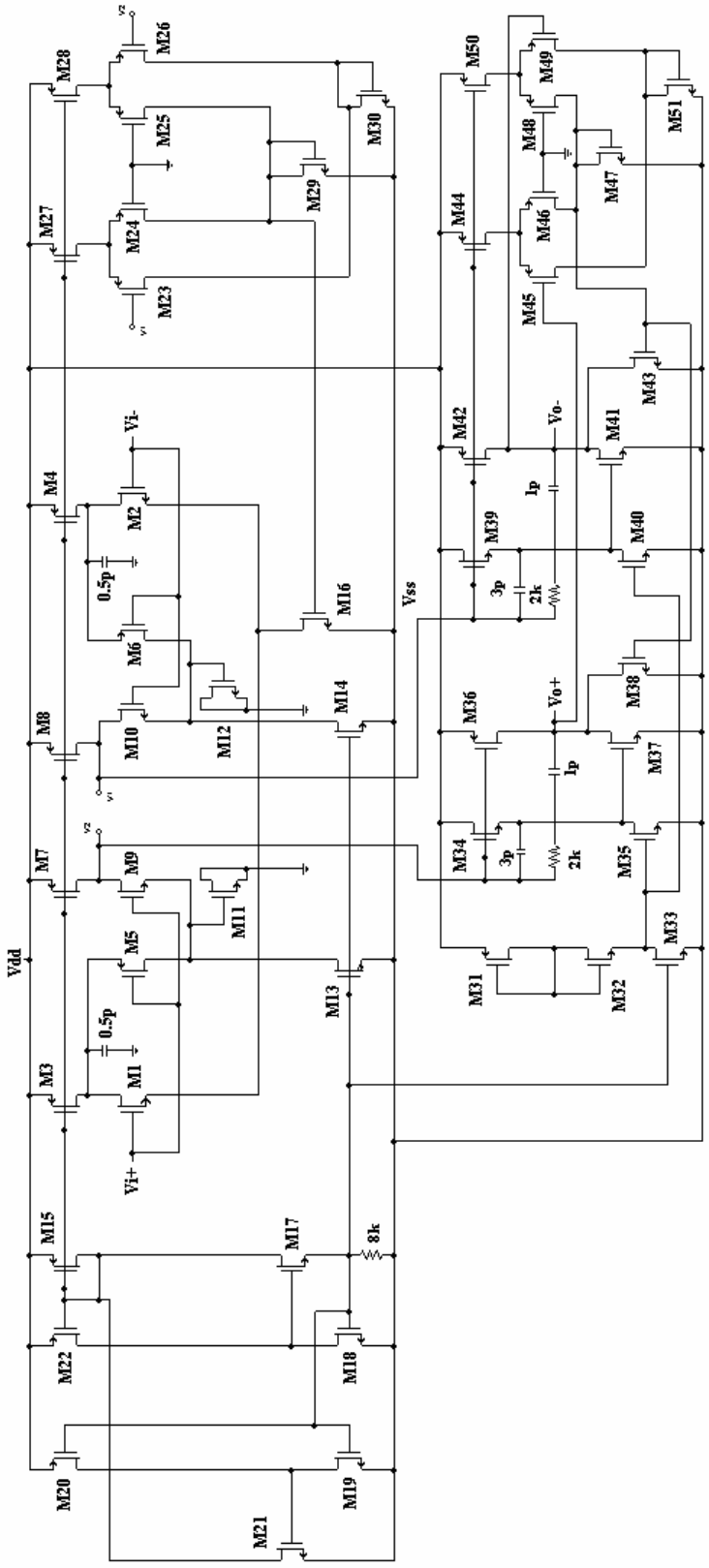


Figure 4.18 Complete schematic circuit for folded-cascode FTFA

Chapter 5 Characterization of Operational Floating Amplifier using PSPICE

To verify the performance of the proposed FTFN configurations, a series of simulations using Pspice were performed. Typical simulation setups such as DC Gain, Common-mode Rejection Ratio (CMRR), are within the various test configurations. Level 49 transistor models for AMIC5N 0.6u technology, which is a 5 volt n-well process, were used in each design. Typical values from simulations of the Telescopic and Folded-Cascode FTFN's are presented. The former is treated first. The setups for the designed circuits were done following references [42], [43] and personal communication with Dr. Gladys O. Doucoudray.

5.1 Simulated measurements

5.1.1 Open-loop gain, Phase Margin, Unity-gain and 3dB frequency

The first test setup measures open-loop gain, phase margin, unity-gain and 3db frequency parameters. Figure 5.1 shows the schematic testbench and figure 5.2 show the ac plot, with each design parameter identified.

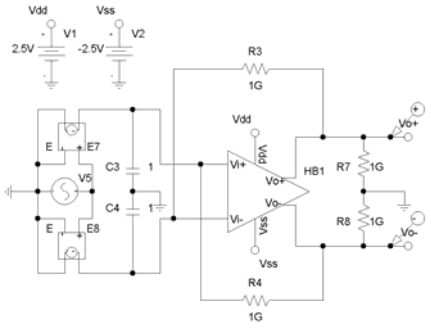


Figure 5.1 Testsetup for open-loop gain, phase margin, unity-gain and 3dB frequency

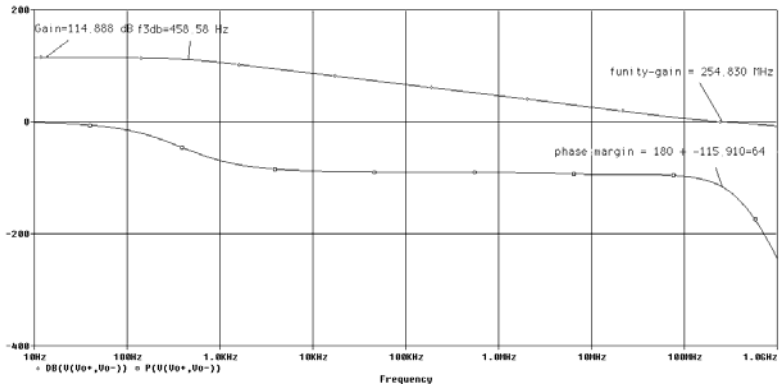


Figure 5.2 Gain and phase plots for Telescopic FTFN

5.1.2 Input Common-mode Range, DC Transfer Characteristic and power dissipation

The input common-mode range, DC transfer characteristic and power dissipation are measured in DC mode. The first test setup for measurement of input common-mode range is shown in figure 5.3.

Common-mode Input Range (CMIR) is defined as the maximum common-mode signal over which the differential voltage gain of the amplifier remains constant. The CMIR was measured by sweeping the input voltage from V_{SS} toV_{DD}. In the unity gain configuration, however, the linear portion of the curve represents the CMIR of the amplifier. In other words, in the unity gain configuration does not go to a rail due to the large gain of the amplifier. The output voltage is plotted against the input voltage as it varies from -2.5V to 2.5V. Figure 5.4 shows the dc plot.

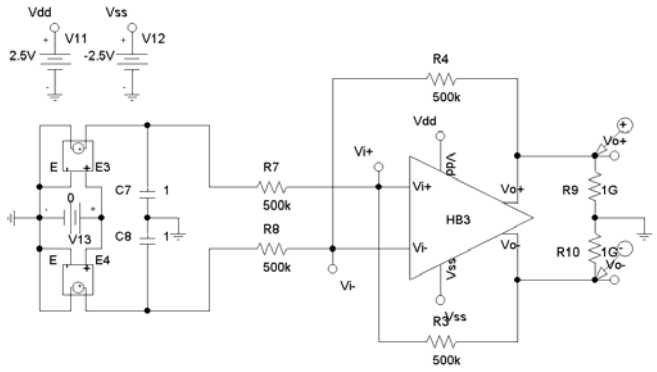


Figure 5.3 Input Common-mode range test setup

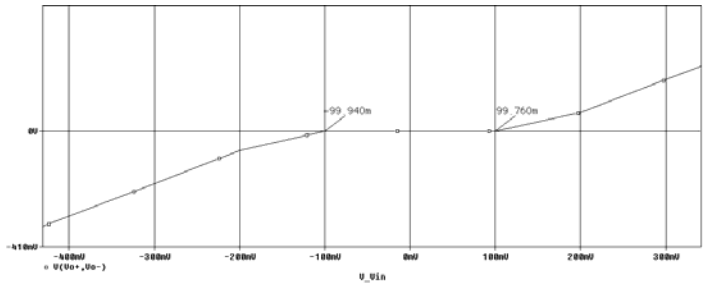


Figure 5.4 Input common-mode range plot

The second test performed was a DC transfer characteristic. This is done in open loop configuration as shown in Figure 5.5 and Figure 5.6 shows the plot. In addition, the DC transfer test allowed the power dissipation to be determined. It is calculated as

$$P_D = (V_{dd} - V_{ss}) * I_Q \qquad 5.2.1$$

where I_Q is the quiescent current.

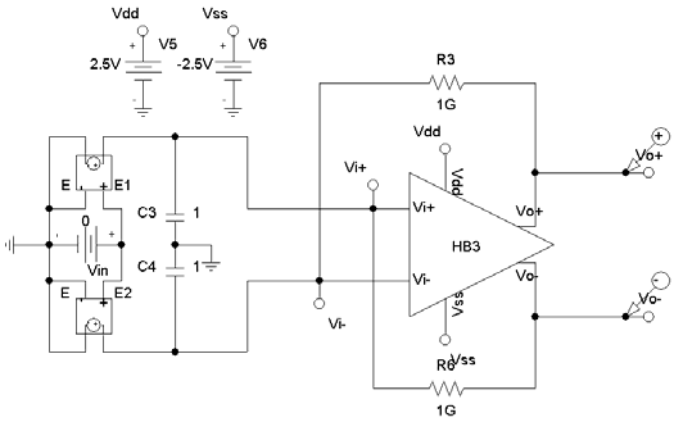


Figure 5.5 DC Transfer Characteristic and Power Dissipation Setup

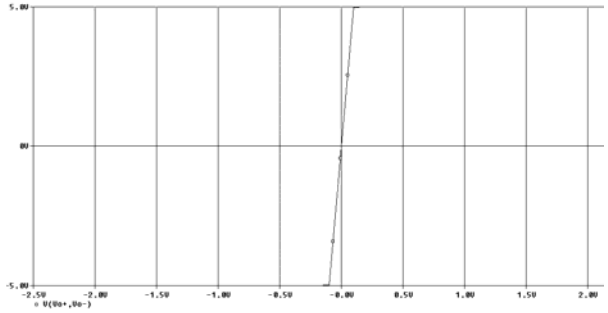


Figure 5.6 DC transfer characteristic for Telescopic FTFN

5.1.3 Offset-voltage measurement

A test setup to measure offset-voltage is shown in Figure 5.7. A unity-gain feedback loop circuit is used. A 0V voltage is set at the input to directly obtain the offset at the output voltage. An offset $V_{OS} = 659.47\,\mu V$ was obtained for the Telescopic amplifier.

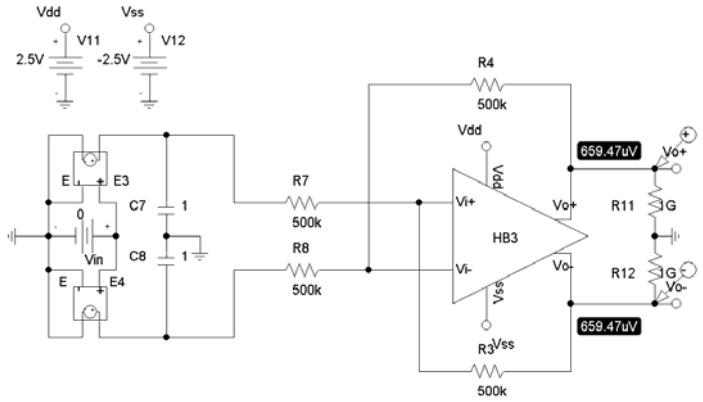


Figure 5.7 Offset-voltage calculation circuit

5.1.4 Output Swing

The circuit of Figure 5.8 was used to measure the output swing of the amplifier. In the unity gain configuration the linearity of the transfer curve is limited by the CMIR. Using this configuration of higher gain, the linearity region of a plot of V_O *vs* V_{IN} corresponds to the output swing of the amplifier. This configuration was chosen so the input voltage could be swept over a wider range of values without saturating the amplifier.

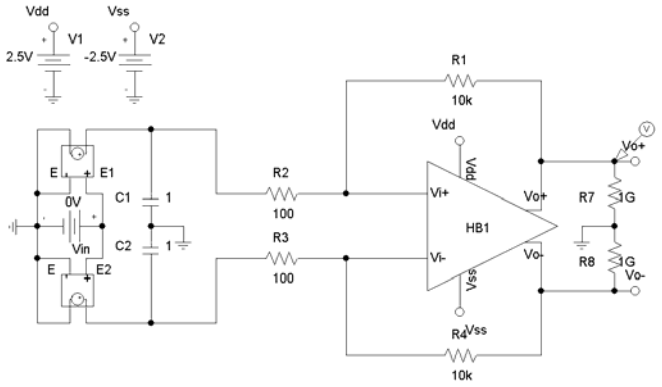


Figure 5.8 Output Swing test setup

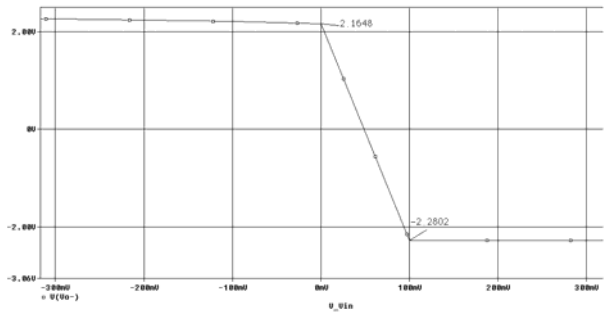


Figure 5.9 Output Swing for Telescopic FTFN test setup

5.1.5 Settling Time

The configuration in Figure 5.10 was used to measure the settling time of the final design and was used for accuracy in settling the output voltage range. The settling time to 0.1% for the amplifier is 52 ns for a 0 to 1V output step and 51.69ns for 0 to -1V output step. The slew rate is calculated as the slope of the output from 30% to 70%.

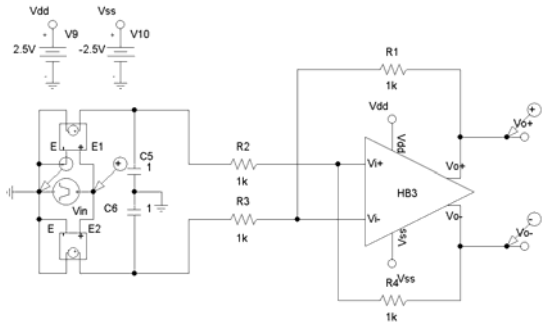


Figure 5.10 Settling time test setup

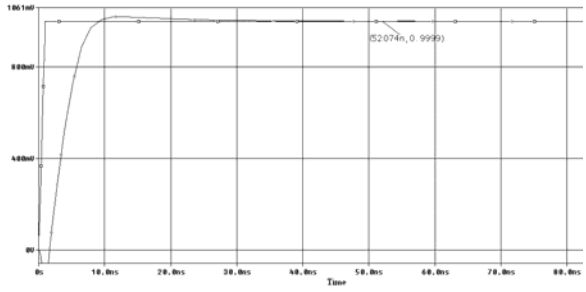


Figure 5.11 Positive slew-rate plot for the telescopic FTFA

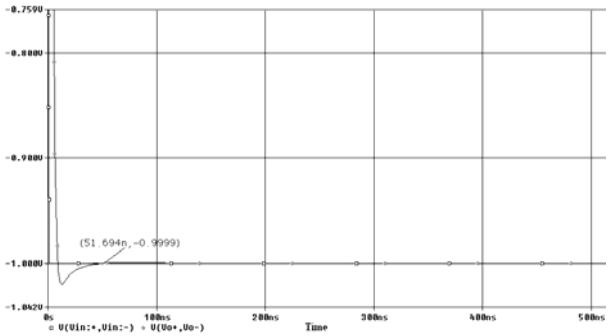


Figure 5.12 Negative slew-rate plot for the FTFA

5.1.6 Common-Mode Rejection Ratio (CMRR)

To measure the Common-mode Rejection Ratio (CMRR), the circuit of Figure 5.13 was used. This configuration provides a method to directly calculate CMRR by finding the ratio $\frac{V_{c\min} + V_{cref}}{V_o}$. This direct calculation of CMRR is very beneficial because it can then be plotted directly in the frequency domain to obtain the CMRR frequency response. Figure 5.14 shows the CMRR.

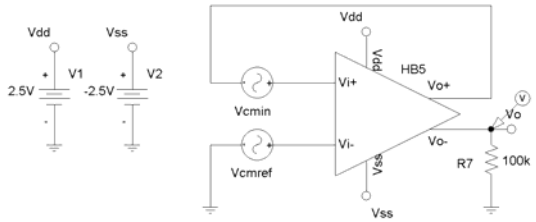


Figure 5.13 Common-mode rejection ratio test setup

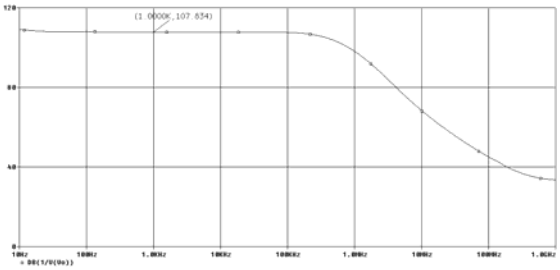


Figure 5.14 Common-mode rejection ratio plot

5.1.7 Equivalent Input-Referred and Total output noise

Figure 5.15 shows the circuit setup to measure input referred and total output noise. These parameters are measure in open-loop mode. Spice provides a noise analysis Option and it measures both input and output noise.

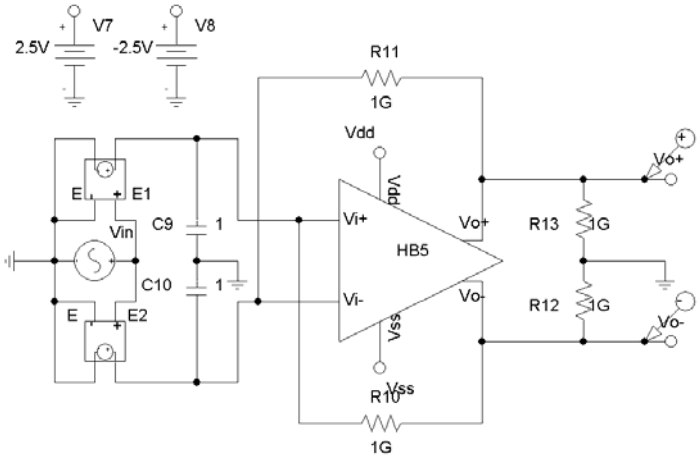


Figure 5.15 Equivalent input-referred and total output noise

A portion of the output file is shown in Figure 5.16 showing results for the input referred and total output noise.

```
TOTAL OUTPUT NOISE VOLTAGE         =  7.364E-06 SQ V/HZ
                                   =  2.714E-03 V/RT HZ

EQUIVALENT INPUT NOISE AT V_Vin =  9.774E-09 V/RT HZ

    JOB CONCLUDED
    TOTAL JOB TIME            5.06
```

Figure 5.16 Output result for input-referred offset voltage and total output noise

5.1.8 Total Harmonic Distortion measurement

The total harmonic distortion (THD) setup is shown in Figure 5.17. An inverting configuration is used in addition of a sine wave at the input is used in this testbench.

Spice provides fourier analysis and in this case test 9 harmonics, with a fundamental frequency of 1Khz.

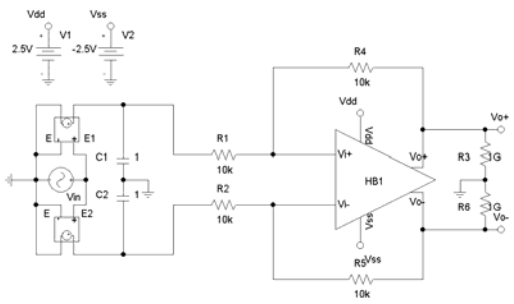


Figure 5.17 Total harmonic distortion setup

The THD is a measure of the percentage of the signal power due to the unwanted harmonics with respect to the fundamental signal power. Figure 5.18 shows the percentages corresponding to 2.523E-01 % for V_O^+ and 2.4132E-01 for V_O^-.

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = 1.898869E-03

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.974E-01	1.000E+00	-1.800E+02	0.000E+00
2	2.000E+03	1.252E-03	2.518E-03	-8.685E+01	2.731E+02
3	3.000E+03	3.389E-05	6.815E-05	-1.089E+02	4.311E+02
4	4.000E+03	2.790E-05	5.609E-05	-8.828E+01	6.317E+02
5	5.000E+03	3.203E-05	6.440E-05	-9.779E+01	8.022E+02
6	6.000E+03	3.148E-05	6.330E-05	-9.515E+01	9.848E+02
7	7.000E+03	3.183E-05	6.399E-05	-9.706E+01	1.163E+03
8	8.000E+03	3.068E-05	6.169E-05	-9.812E+01	1.342E+03
9	9.000E+03	3.201E-05	6.436E-05	-9.853E+01	1.521E+03

TOTAL HARMONIC DISTORTION = 2.523311E-01 PERCENT

****

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

DC COMPONENT = 1.934310E-03

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.974E-01	1.000E+00	3.376E-03	0.000E+00
2	2.000E+03	1.198E-03	2.409E-03	-9.093E+01	-9.094E+01
3	3.000E+03	2.916E-05	5.864E-05	6.674E+01	6.672E+01
4	4.000E+03	2.806E-05	5.643E-05	9.359E+01	9.358E+01
5	5.000E+03	2.600E-05	5.228E-05	7.951E+01	7.949E+01
6	6.000E+03	2.480E-05	4.986E-05	8.547E+01	8.545E+01
7	7.000E+03	2.539E-05	5.105E-05	7.886E+01	7.883E+01
8	8.000E+03	2.547E-05	5.120E-05	8.180E+01	8.177E+01
9	9.000E+03	2.465E-05	4.956E-05	7.757E+01	7.754E+01

TOTAL HARMONIC DISTORTION = 2.413267E-01 PERCENT

Figure 5.18 Fourier components of transient response

5.1.9 Open-loop gain, Phase Margin, Unity-gain and 3dB frequency.

The first test setup measures open-loop gain, phase margin, unity-gain and 3db frequency parameters. Figure 5.19 shows the schematic testbench and figure 5.20 show the ac plot with each design parameter identified.

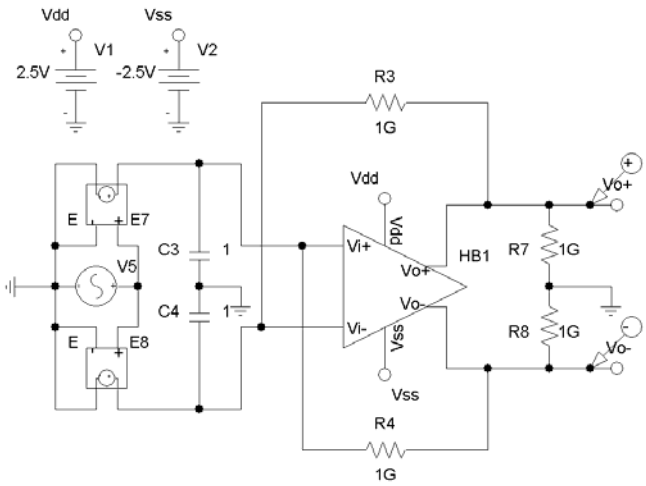


Figure 5.19 Testsetup for open-loop gain, phase margin, unity-gain and 3dB frequency

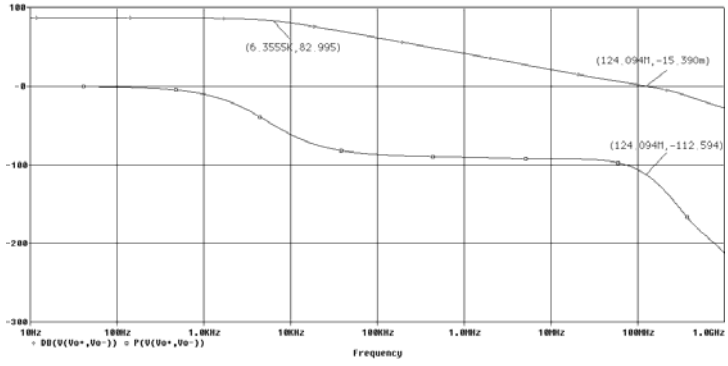


Figure 5.20 Gain and phase plots for Folded-Cascode FTFN

5.1.10 Input Common-mode Range, DC Transfer Characteristic and power dissipation

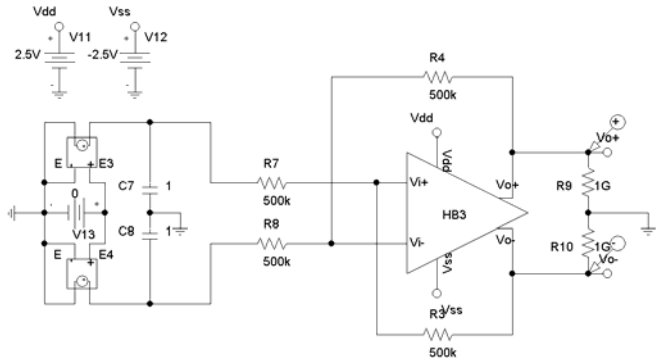


Figure 5.21 Input Common-mode range test setup

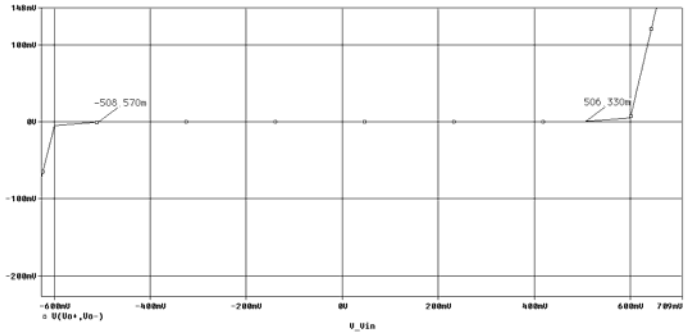


Figure 5.22 CMIR plot for Folded-Cascode FTFN

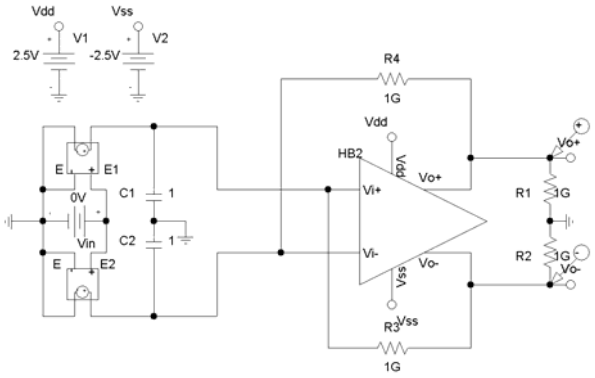


Figure 5.23 DC Transfer Characteristic and Power Dissipation Setup

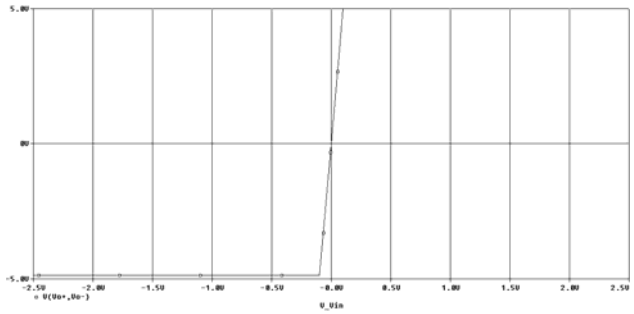


Figure 5.24 DC transfer characteristic for Folded-Cascode FTFN

5.1.11 Offset-voltage measurement

A test setup to measure offset-voltage is shown in Figure 5.25. A unity-gain feedback loop circuit is used. A 0V voltage is set at the input to directly obtain the offset at the output voltage. An offset voltage $V_{OS} = 869.25\,\mu V$ was obtained for the Folded-Cascode amplifier. This setup is different from the first one in that lower resistors are used. In this way, the offset does not trip the output transistors to go to either rail.

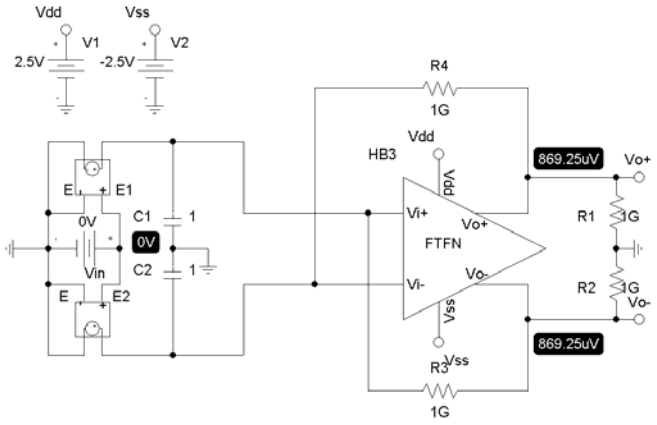


Figure 5.25 Offset-voltage calculation circuit

5.1.12 Output Swing

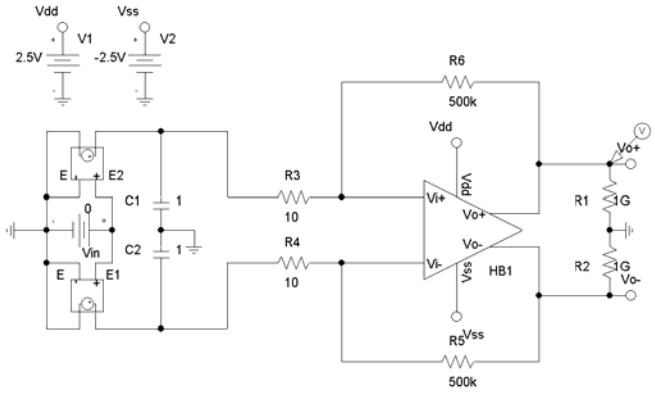


Figure 5.26 Output Swing test setup

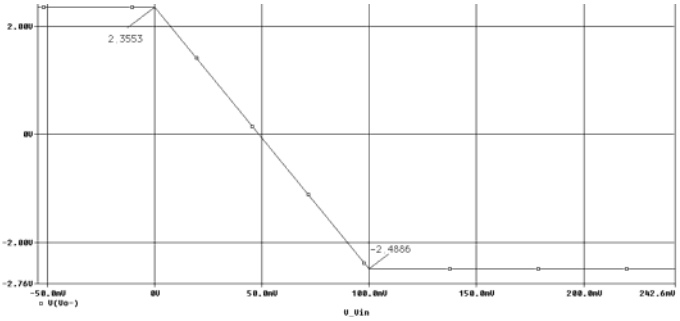


Figure 5.27 Output Swing output waveform

5.1.13 Settling Time

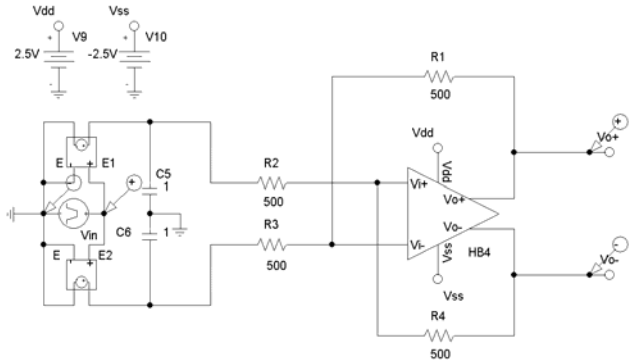


Figure 5.28 Settling time test setup

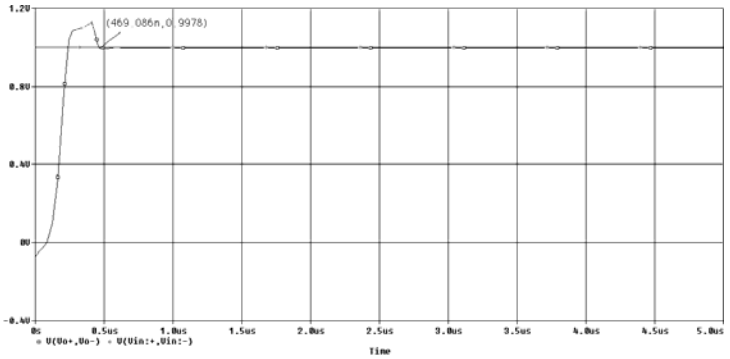


Figure 5.29 Positive slew-rate plot for the folded-cascode FTFA

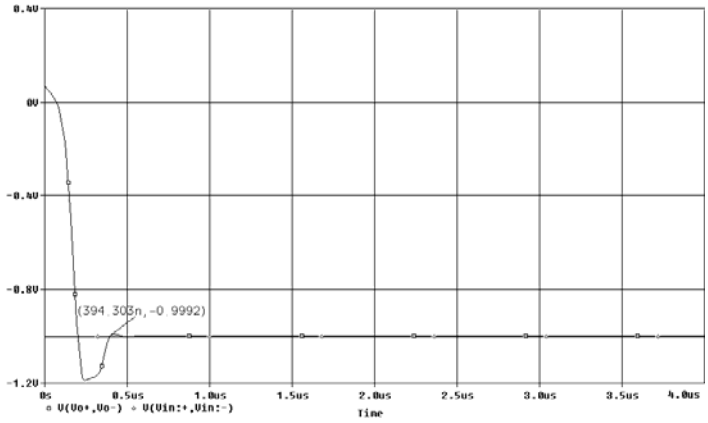


Figure 5.30 Negative slew-rate plot for the folded-cascode FTFA

5.1.14 Common-Mode Rejection Ratio (CMRR)

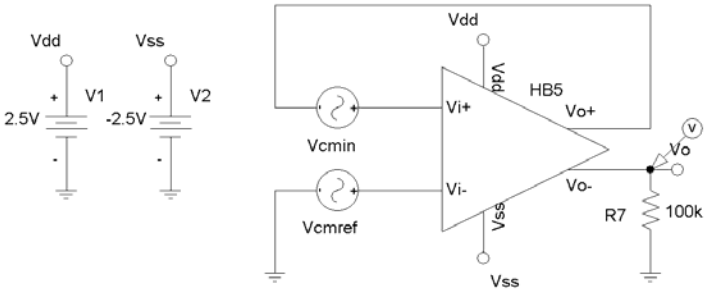


Figure 5.31 Common-mode rejection ratio test setup

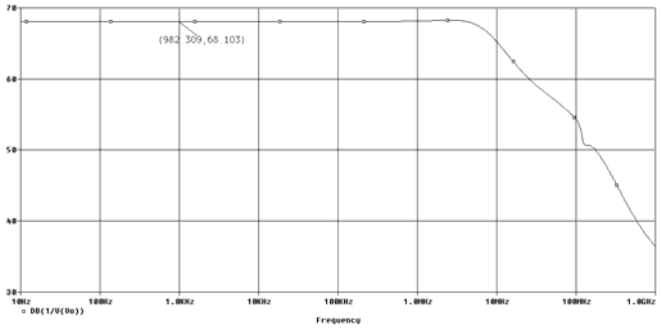


Figure 5.32 Common-mode rejection ratio plot

5.1.15 Equivalent Input-Referred and Total output noise

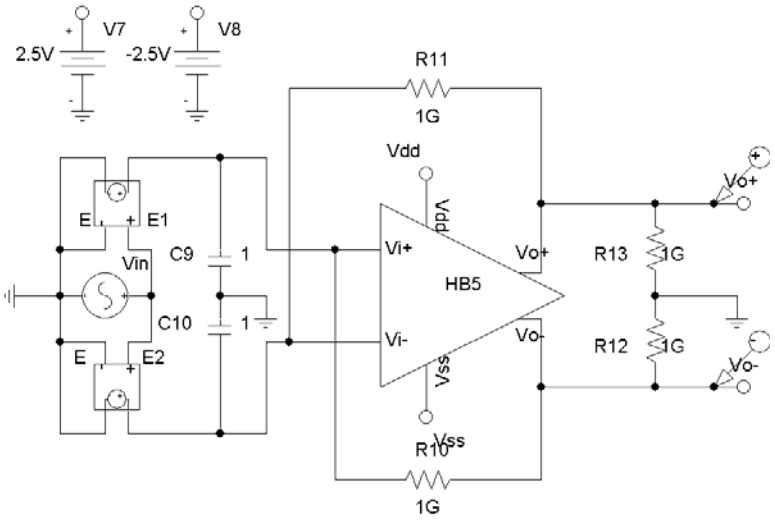


Figure 5.33 Equivalent input-referred and total output noise

A portion of the output file is shown in Figure 5.34 showing results for the input referred and total output noise.

```
TOTAL OUTPUT NOISE VOLTAGE          =  9.470E-09 SQ V/HZ
                                    =  9.731E-05 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  1.120E+04
EQUIVALENT INPUT NOISE AT V_Vin =  8.690E-09 V/RT HZ
```

Figure 5.34 Output result for input-referred offset voltage and total output noise

5.1.16 Total Harmonic Distortion measurement

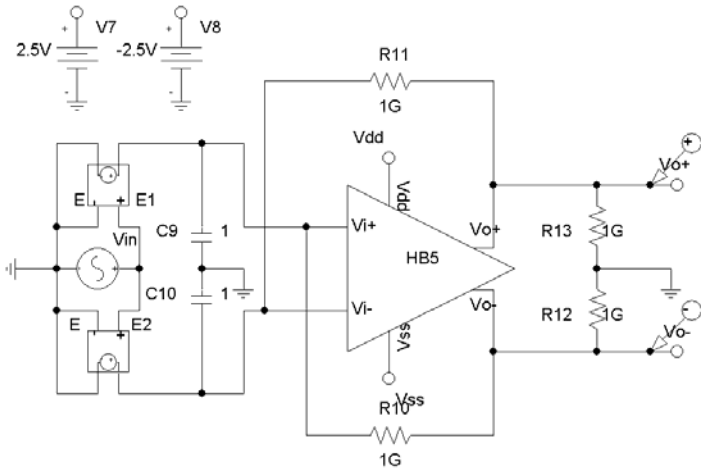


Figure 5.35 Total harmonic distortion setup

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.627E-03	1.000E+00	-1.499E-03	0.000E+00
2	2.000E+03	7.576E-07	4.657E-04	1.005E+02	1.005E+02
3	3.000E+03	3.963E-08	2.436E-05	6.374E+01	6.375E+01
4	4.000E+03	1.858E-08	1.142E-05	6.711E+01	6.712E+01
5	5.000E+03	7.718E-09	4.744E-06	1.369E+02	1.369E+02
6	6.000E+03	6.186E-09	3.803E-06	6.357E+01	6.358E+01
7	7.000E+03	1.380E-08	8.483E-06	-8.055E+01	-8.054E+01
8	8.000E+03	3.912E-08	2.404E-05	1.221E+02	1.221E+02
9	9.000E+03	4.429E-09	2.722E-06	-2.252E+01	-2.250E+01

TOTAL HARMONIC DISTORTION = 4.671961E-02 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	7.890E-04	1.000E+00	1.800E+02	0.000E+00
2	2.000E+03	6.039E-08	7.653E-05	-3.404E+01	-3.940E+02
3	3.000E+03	2.701E-08	3.424E-05	1.700E+02	-3.699E+02
4	4.000E+03	3.360E-08	4.259E-05	7.556E+00	-7.124E+02
5	5.000E+03	5.515E-08	6.990E-05	-1.793E+02	-1.079E+03
6	6.000E+03	2.229E-08	2.825E-05	-1.302E+02	-1.210E+03
7	7.000E+03	8.040E-09	1.019E-05	-1.036E+02	-1.364E+03
8	8.000E+03	3.233E-08	4.098E-05	-6.621E+01	-1.506E+03
9	9.000E+03	2.160E-08	2.737E-05	-1.533E+02	-1.773E+03

TOTAL HARMONIC DISTORTION = 1.306140E-02 PERCENT

Figure 5.36 Fourier components of transient response

5.2 Summary of design parameters

Table 5.1 shows a summary of the simulated parameters for both Telescopic and Folded-Cascode FTFA.

Parameter	Telescopic FTFA	Folded-Cascode FTFA
Open-loop gain	114 dB	86 dB
Phase Margin	64º	72 º
Unity-gain	254 MHz	124 MHz
3dB frequency	456 Hz	6.35 KHz
Input Common-Mode Range	$-100mV \le V_{CMIR} \le 100mV$	$-508mV \le V_{CMIR} \le 506mV$
Power Dissipation	45mW	79mW
Offset Voltage	659.47 µV	869.256 µV
Output Swing	$-2.280V \le V_{OSW} \le 2.16V$	$-2..48V \le V_{OSW} \le 2.35V$
Settling Time	$S^+ = 52ns \; S^- = 51.69ns$	$S^+ = 469ns \; S^- = 394ns$
Slew Rate	$SR^+ = 189\frac{V}{\mu s}$ $SR^- = 186dB$	$SR^+ = 9.29\frac{V}{\mu s}$ $SR^+ = 10.67\frac{V}{\mu s}$
Common-mode Rejection Ratio	111 dB	68 dB
Input-referred noise	$9.77\frac{nV}{\sqrt{Hz}}$	$8.69\frac{nV}{\sqrt{Hz}}$
THD@1KHz	$V_o^+ = 2.52E-1\%$ $V_o^- = 2.413E-1\%$	$V_o^+ = 4.679E-2\%$ $V_o^- = 1.306E-2\%$

Table 5.1 Design parameters for telescopic and folded-cascode FTFA

5.3 Worst Case Simulations

Using alternative models for the designed circuits to simulate worst case situations, the results of table 5.2 are obtained.

Parameter	Telescopic FTFA	Folded-Cascode FTFA
Open-loop gain	87 dB	92 dB
Phase Margin	79º	77 º
Unity-gain	86 MHz	125 MHz
3dB frequency	456 Hz	4.13 KHz
Input Common-Mode Range	$-422mV \le V_{CMIR} \le 422mV$	$-498mV \le V_{CMIR} \le 498mV$
Power Dissipation	67mW	77mW
Offset Voltage	1.46 mV	1.24 mV
Output Swing	$-2.48V \le V_{OSW} \le 2.02V$	$-2..47V \le V_{OSW} \le 2.37V$
Settling Time	$S^+ = 457ns \; S^- = 457ns$	$S^+ = 312ns \; S^- = 312ns$
Slew Rate	$SR^+ = 27.70\frac{V}{\mu s} \quad SR^- = 27.67\frac{V}{\mu s}$	$SR^+ = 15.98\frac{V}{\mu s} \; SR^+ = 14.75\frac{V}{\mu s}$
Common-mode Rejection Ratio	109 dB	65 dB
Input-referred noise	$8.19\frac{nV}{\sqrt{Hz}}$	$7.10\frac{nV}{\sqrt{Hz}}$
THD@1KHz	$V_o^+ = 3.90\%$ $V_o^- = 2.93\%$	$V_o^+ = 6.54E-1\%$ $V_o^- = 4.02E-1\%$

Table 5.2 Worst case simulation results

It is seen that the performance suffers enormously. Improved versions for these designs are given in the following chapter.

Chapter 6 Extending FTFA operating range using a complementary Common-Mode Feedback (CCMFB)

It has been stated that a Common-Mode Feedback controls the common-mode output voltage and provides control within a specific voltage range. To improve CMFB operating range, a Complementary Common-Mode Feedback (CCMFB) is added at the output. Figure 6.1 shows the circuit block.

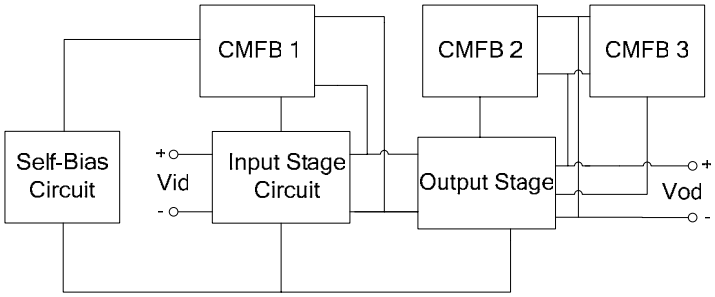


Figure 6.1 FTFA circuit block with complementary common-mode feedback

Common-mode feedback 2 and 3 forms the CCMFB. Both CMFB are shown in figure 6.2

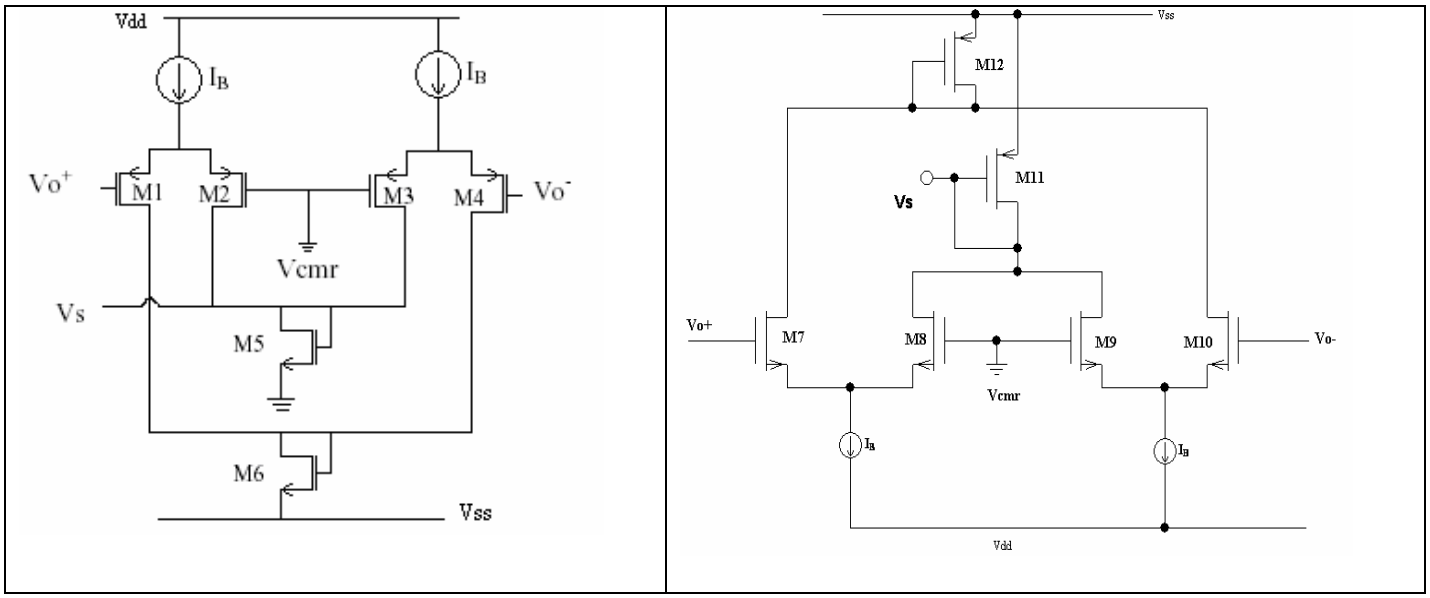


Figure 6.2 Complementary Common-mode feedback

The operation of the CCMFB, as the name implies, is the same an input complementary differential pair. One stage is processing the signal while the other is completely off. To appreciate the extended voltage range at the output, the equations will be decomposed within the operation of the circuits. First, the P-type shown in the right of Figure 6.2 results in:

$$V_{GS4} + V_{BIAS} \leq V_{CM} \leq V_{GS1} + V_{BIAS} \qquad 8.1.2$$

On the other hand, N-type results in:

$$V_{GS10} + V_{BIAS} \leq V_{CM} \leq V_{GS10} + V_{BIAS} \qquad 8.1.3$$

Results for the Telescopic and Folded-Cascode FTFA using this technique are shown in table 6.1 and 6.2 respectively. Also, both schematics are shown in Figure 6.84 and 6.85.

6.1 Simulated results

Simulation results for Improved FTFA Telescopic using typical models

1. Open-loop gain, 3dB-frequency and phase margin

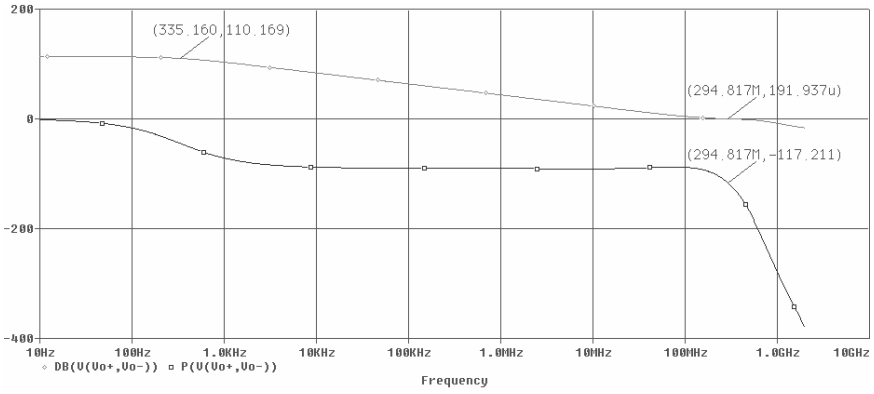


Figure 6.3 Gain and phase plots for Telescopic FTFN

2. Input Common-mode Range

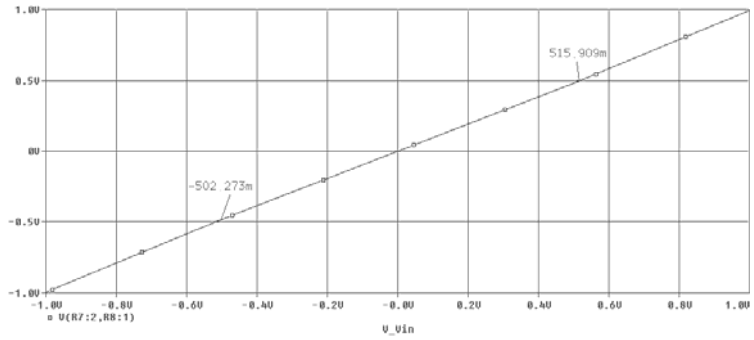


Figure 6.4 Input common-mode range plot

3. DC Transfer Characteristic

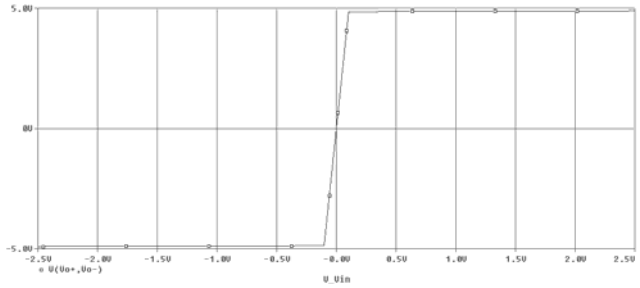


Figure 6.5 DC transfer characteristic for Telescopic FTFN

4. Offset Voltage

For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively.

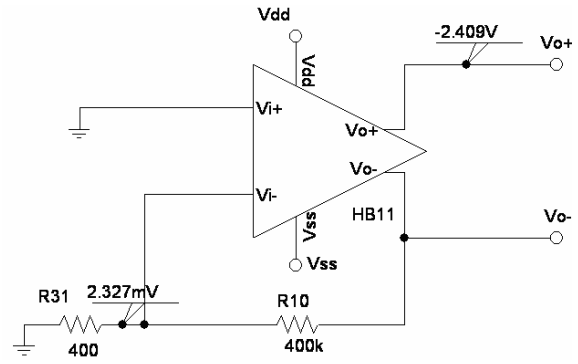


Figure 6.6 Offset-voltage calculation circuit

In this case the offset resulted as follows:

$$V_{off} = -\frac{1+\frac{4000}{446683.59}}{4000}(2)(-2.409V) = 1.22\,mV$$

5. Output Swing

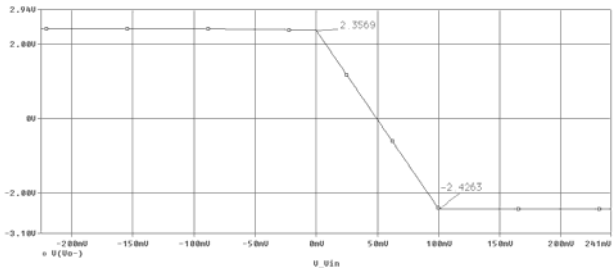


Figure 6.7 Output Swing for Telescopic FTFA

6. Settling Time

A. Positive Settling

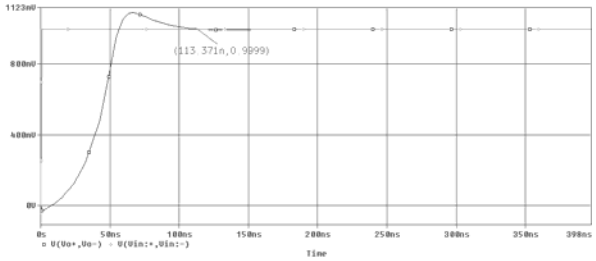


Figure 6.8 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling

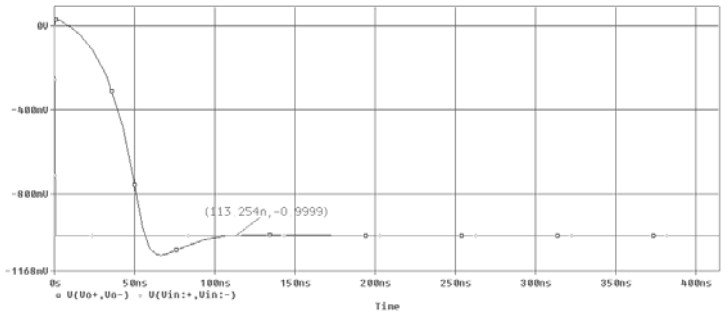


Figure 6.9 Negative slew-rate plot for the FTFA

7. Common-Mode Rejection Ratio

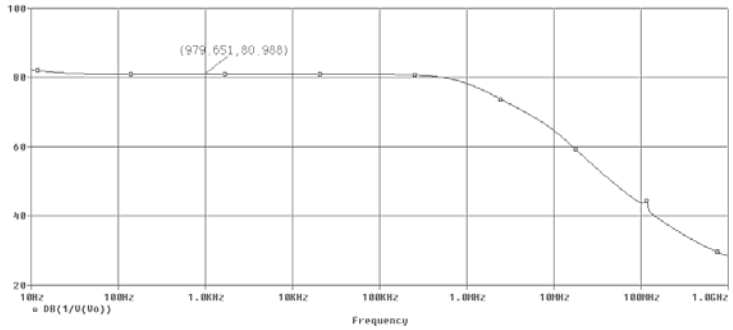


Figure 6.10 Common-mode rejection ratio plot

8. Input Referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE          =  3.600E-06 SQ V/HZ
                                    =  1.897E-03 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  2.275E+05
EQUIVALENT INPUT NOISE AT V_Vin =  8.340E-09 V/RT HZ
```

Figure 6.11 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = 2.293416E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	3.715E-02	1.000E+00	3.280E-03	0.000E+00
2	2.000E+03	1.211E-03	3.260E-02	8.989E+01	8.989E+01
3	3.000E+03	1.996E-05	5.374E-04	1.664E+02	1.664E+02
4	4.000E+03	7.876E-06	2.120E-04	-9.470E+01	-9.471E+01
5	5.000E+03	4.041E-06	1.088E-04	1.301E+02	1.301E+02
6	6.000E+03	3.266E-06	8.794E-05	8.842E+01	8.840E+01
7	7.000E+03	3.413E-06	9.189E-05	8.799E+01	8.796E+01
8	8.000E+03	3.453E-06	9.295E-05	9.021E+01	9.018E+01
9	9.000E+03	3.354E-06	9.029E-05	9.145E+01	9.142E+01

TOTAL HARMONIC DISTORTION = 3.261073E+00 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

DC COMPONENT = -2.394950E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.728E-02	1.000E+00	-1.800E+02	0.000E+00
2	2.000E+03	4.784E-04	2.768E-02	-9.005E+01	2.699E+02
3	3.000E+03	7.975E-05	4.614E-03	-1.786E+02	3.614E+02
4	4.000E+03	6.627E-06	3.834E-04	-8.822E+01	6.318E+02
5	5.000E+03	2.401E-06	1.389E-04	-3.734E+01	8.626E+02
6	6.000E+03	2.564E-06	1.484E-04	-9.116E+01	9.888E+02
7	7.000E+03	1.614E-06	9.337E-05	-7.803E+01	1.182E+03
8	8.000E+03	1.518E-06	8.784E-05	-9.124E+01	1.349E+03
9	9.000E+03	1.544E-06	8.936E-05	-8.886E+01	1.531E+03

TOTAL HARMONIC DISTORTION = 2.806551E+00 PERCENT

Figure 6.12 Fourier components of transient response

<u>Simulation results for Improved FTFA Telescopic using slow-slow models</u>

1. Open-loop gain, 3dB-frequency and phase margin

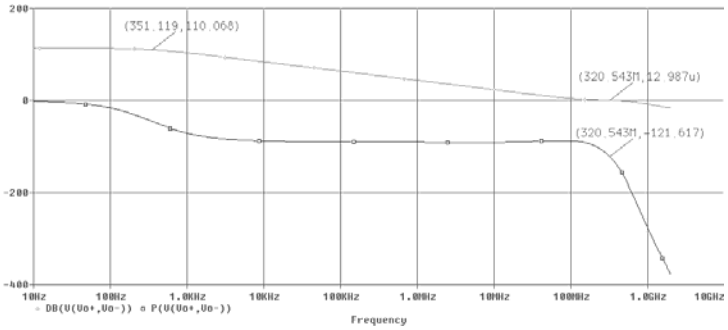


Figure 6.13 Gain and phase plots for Telescopic FTFN

2. Input Common-mode Range

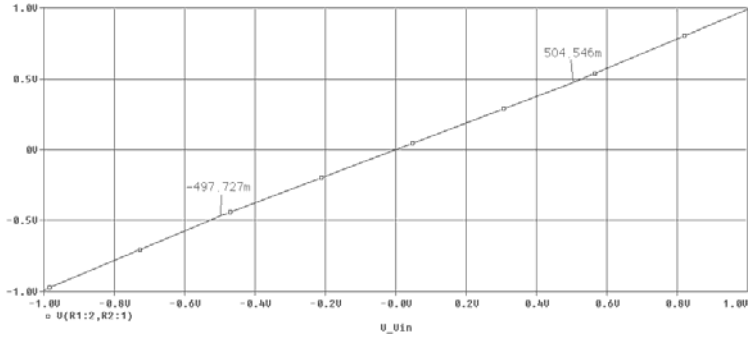


Figure 6.14 Input common-mode range plot

3. DC Transfer Characteristic

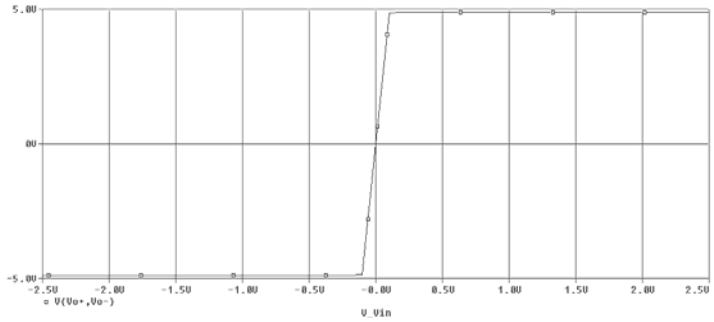


Figure 6.15 DC transfer characteristic for Telescopic FTFN

4. Offset Voltage

For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively.

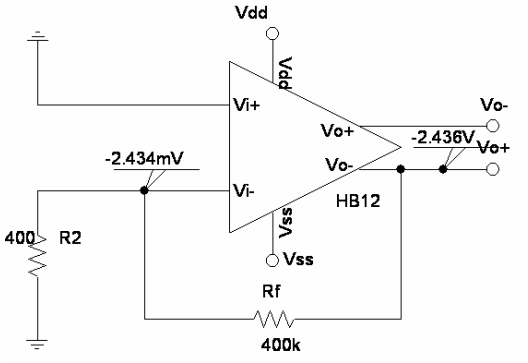


Figure 6.16 Offset-voltage calculation circuit

In this case the offset resulted as follows:

$$V_{off} = -\frac{1+\frac{4000}{446683.59}}{4000}(2)(-2.436V) = 1.22\,mV$$

5. Output Swing

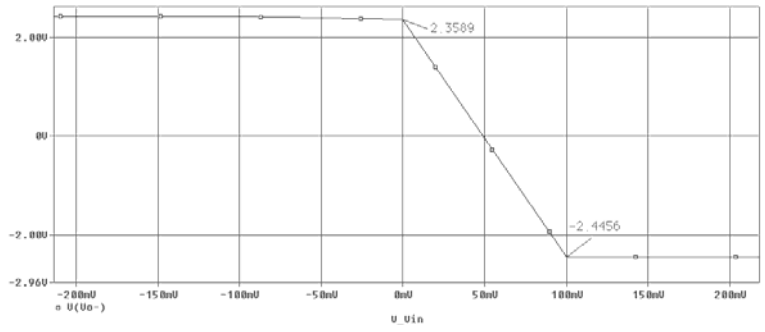


Figure 6.17 Output Swing for Telescopic FTFN test setup

6. Settling Time

A. Positive Settling

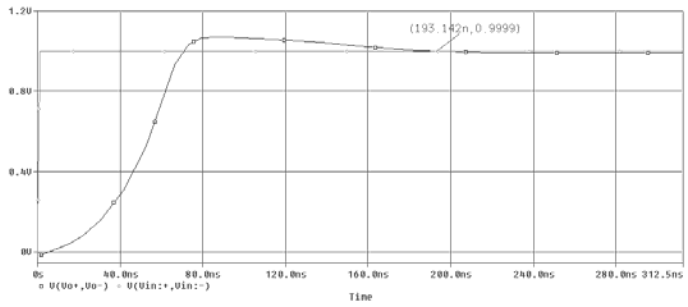


Figure 6.18 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling

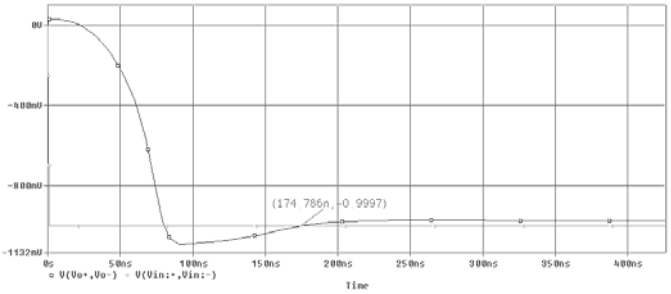


Figure 6.19 Negative slew-rate plot for the FTFA

7. Common-mode Rejection Ratio

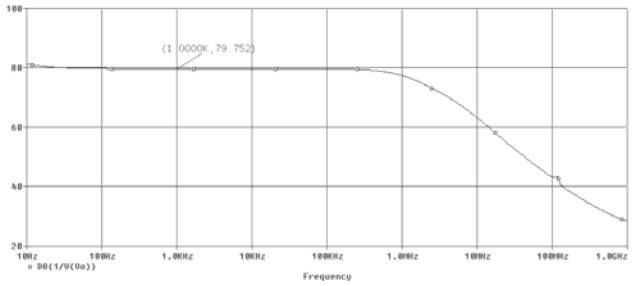


Figure 6.20 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE          =  3.451E-06 SQ V/HZ
                                    =  1.858E-03 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                      =  2.267E+05
EQUIVALENT INPUT NOISE AT V_Vin =  8.194E-09 V/RT HZ
```

Figure 6.21 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = -2.146742E-01

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.984E-01	1.000E+00	1.799E+02	0.000E+00
2	2.000E+03	3.118E-01	6.256E-01	8.969E+01	-2.701E+02
3	3.000E+03	1.566E-03	3.141E-03	8.531E+01	-4.544E+02
4	4.000E+03	9.188E-03	1.843E-02	8.759E+01	-6.320E+02
5	5.000E+03	7.596E-04	1.524E-03	5.657E+01	-8.429E+02
6	6.000E+03	2.699E-02	5.416E-02	-9.063E+01	-1.170E+03
7	7.000E+03	6.565E-04	1.317E-03	-3.805E+01	-1.297E+03
8	8.000E+03	1.053E-02	2.113E-02	-9.097E+01	-1.530E+03
9	9.000E+03	2.723E-04	5.464E-04	-1.446E+02	-1.764E+03

TOTAL HARMONIC DISTORTION = 6.285708E+01 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.985E-01	1.000E+00	1.921E-01	0.000E+00
2	2.000E+03	3.123E-01	6.265E-01	8.965E+01	8.926E+01
3	3.000E+03	1.405E-03	2.818E-03	1.002E+02	9.967E+01
4	4.000E+03	9.379E-03	1.882E-02	8.713E+01	8.636E+01
5	5.000E+03	1.292E-03	2.593E-03	6.479E+01	6.383E+01
6	6.000E+03	2.662E-02	5.341E-02	-9.081E+01	-9.196E+01
7	7.000E+03	6.164E-04	1.237E-03	2.079E+01	1.944E+01
8	8.000E+03	1.003E-02	2.012E-02	-9.014E+01	-9.168E+01
9	9.000E+03	3.528E-04	7.078E-04	3.157E+01	2.984E+01

TOTAL HARMONIC DISTORTION = 6.294073E+01 PERCENT

Figure 6.22 Fourier components of transient response

Simulation results for Improved FTFA Telescopic using sf models

1. Open-loop gain, 3dB-frequency and phase margin

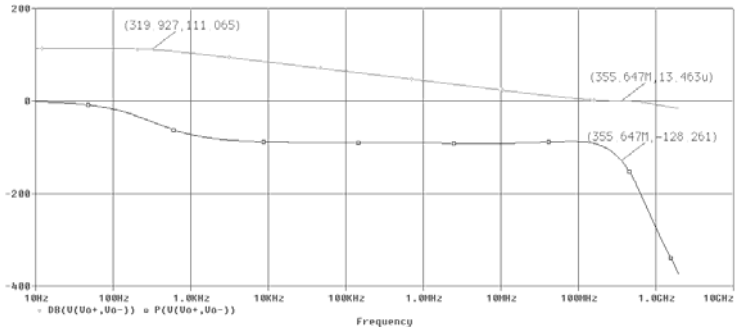


Figure 6.23 Gain and phase plots for Telescopic FTFN

2. Input Common-mode Range

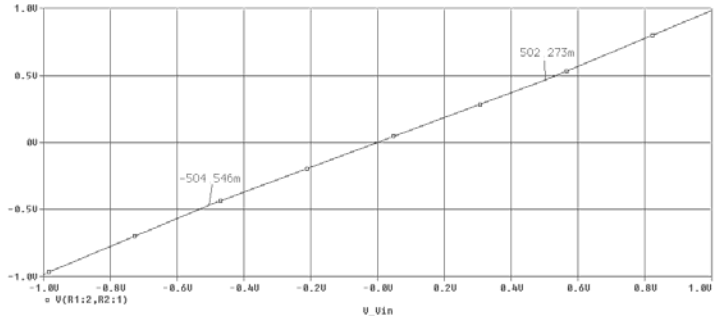


Figure 6.24 Input common-mode range plot

3. DC Transfer Characteristic

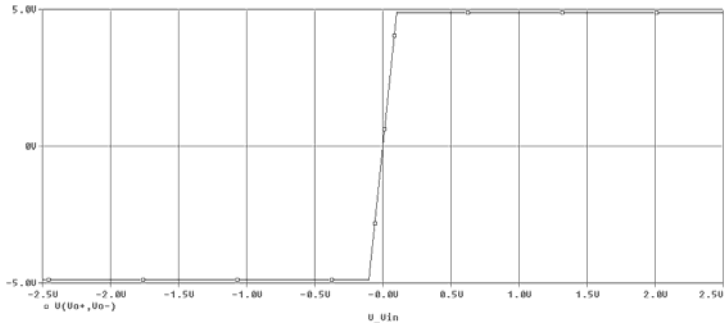


Figure 6.25 DC transfer characteristic for Telescopic FTFN

4. Offset Voltage

For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively.

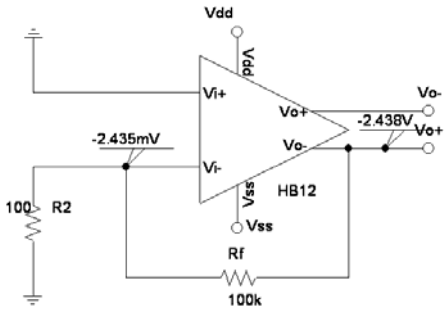


Figure 6.26 Offset-voltage calculation circuit

In this case the offset resulted as follows:

$$V_{off} = -\frac{1+\frac{4000}{446683.59}}{4000}(2)(-2.438V) = 1.22\,mV$$

5. Output Swing

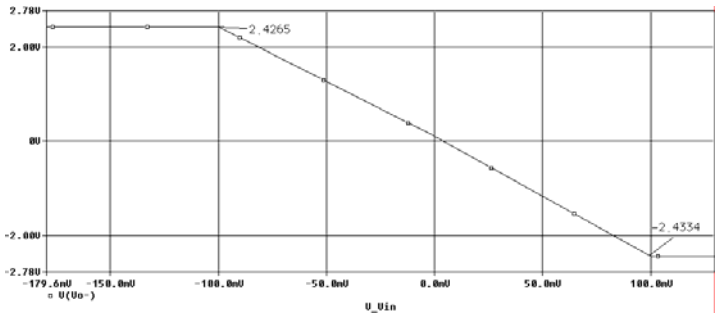


Figure 6.27 Output Swing for Telescopic FTFN test setup

6. Settling Time

A. Positive Settling

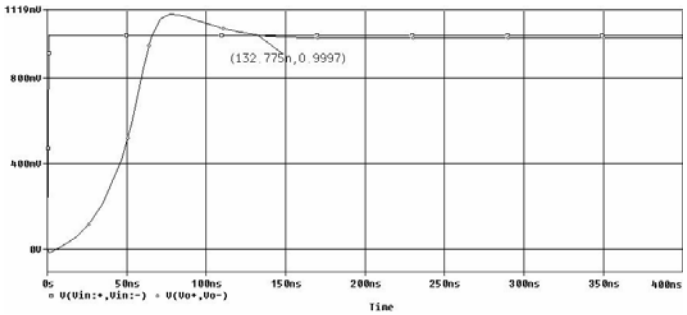


Figure 6.28 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling

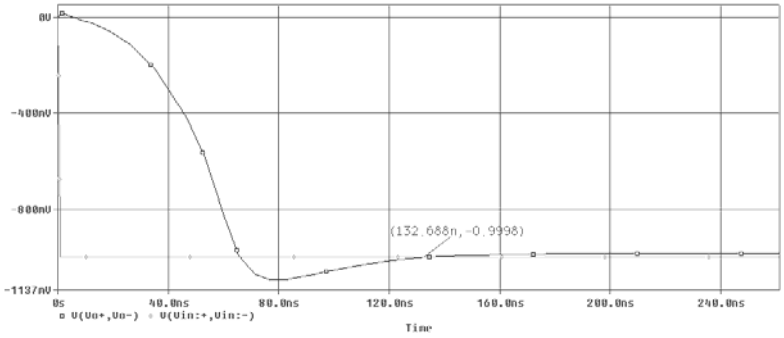


Figure 6.29 Negative slew-rate plot for the FTFA

7. Common-Mode Rejection Ratio

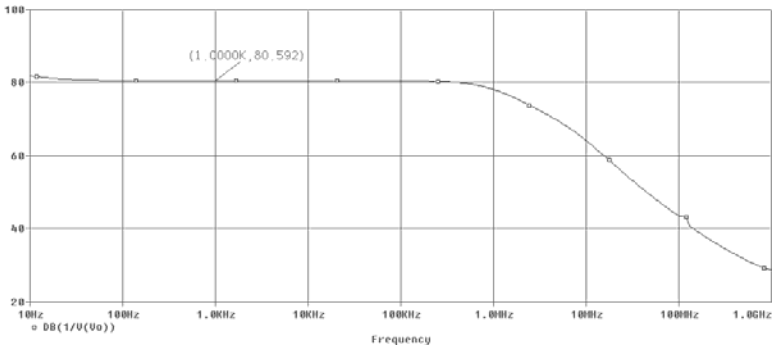


Figure 6.30 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE         =  4.149E-06 SQ V/HZ
                                   =  2.037E-03 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  2.532E+05
EQUIVALENT INPUT NOISE AT V_Vin =  8.046E-09 V/RT HZ
```

Figure 6.31 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	2.727E-01	1.000E+00	9.438E-03	0.000E+00
2	2.000E+03	1.344E-02	4.926E-02	-8.988E+01	-8.990E+01
3	3.000E+03	1.940E-03	7.111E-03	-1.795E+02	-1.795E+02
4	4.000E+03	9.626E-04	3.529E-03	8.994E+01	8.990E+01
5	5.000E+03	2.538E-04	9.305E-04	-2.380E+00	-2.427E+00
6	6.000E+03	2.015E-04	7.390E-04	-8.898E+01	-8.903E+01
7	7.000E+03	1.129E-04	4.140E-04	-1.744E+02	-1.744E+02
8	8.000E+03	8.756E-06	3.210E-05	-6.290E+01	-6.297E+01
9	9.000E+03	2.605E-05	9.551E-05	-1.558E+02	-1.559E+02

TOTAL HARMONIC DISTORTION = 4.991475E+00 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	3.733E-01	1.000E+00	1.800E+02	0.000E+00
2	2.000E+03	2.578E-02	6.907E-02	8.996E+01	-2.700E+02
3	3.000E+03	4.768E-03	1.277E-02	1.364E-01	-5.399E+02
4	4.000E+03	1.205E-03	3.227E-03	-9.052E+01	-8.105E+02
5	5.000E+03	1.485E-04	3.980E-04	1.700E+02	-7.300E+02
6	6.000E+03	9.390E-05	2.516E-04	-9.328E+01	-1.173E+03
7	7.000E+03	8.321E-05	2.229E-04	1.636E+02	-1.096E+03
8	8.000E+03	2.580E-05	6.913E-05	9.993E+01	-1.340E+03
9	9.000E+03	3.437E-05	9.206E-05	1.463E+02	-1.474E+03

TOTAL HARMONIC DISTORTION = 7.031398E+00 PERCENT

Figure 6.32 Fourier components of transient response

Simulation results for Improved FTFA Telescopic using fs models

1. Open-loop gain, 3dB-frequency and phase margin

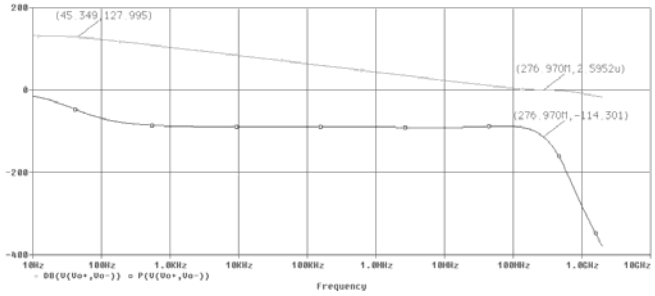


Figure 6.33 Gain and phase plots for Telescopic FTFN

2. Input Common-mode Range

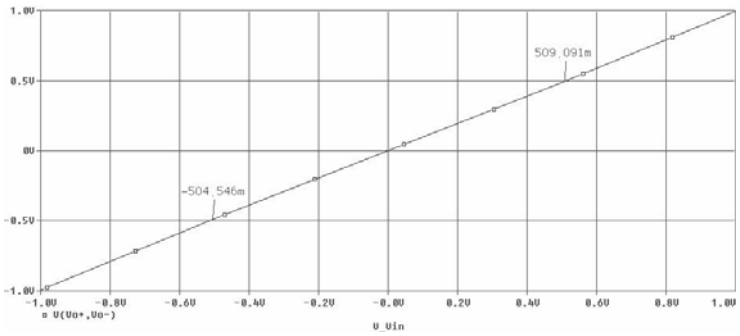


Figure 6.34 Input common-mode range plot

3. DC Transfer Characteristic

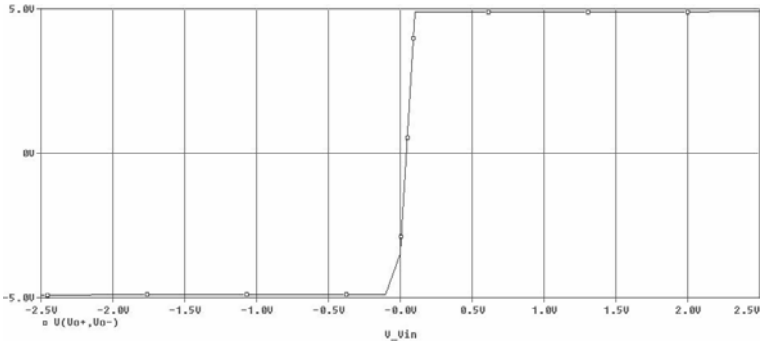


Figure 6.35 DC transfer characteristic for Telescopic FTFN

4. Offset Voltage

For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively.

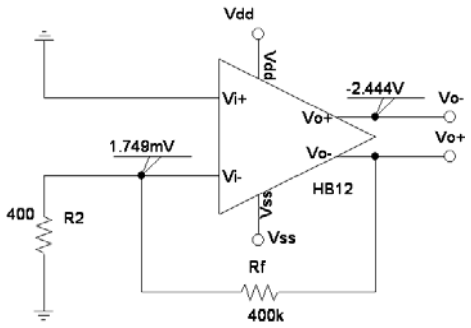


Figure 6.36 Offset-voltage calculation circuit

In this case the offset resulted as follows:

$$V_{off} = -\frac{1+\frac{4000}{3162277.66}}{4000}(2)(-2.444V) = 1.23\,mV$$

5. Output Swing

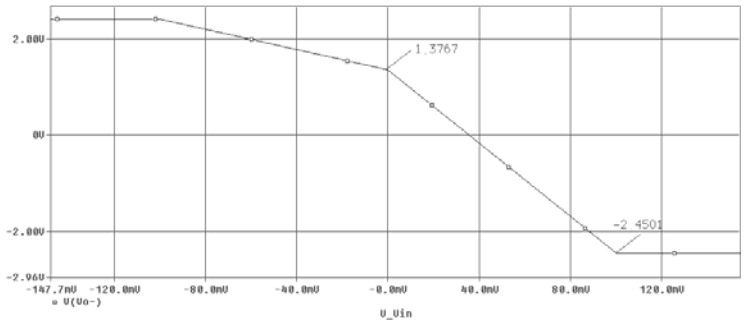


Figure 6.37 Output Swing for Telescopic FTFN test setup

6. Settling Time

A. Positive Settling Time

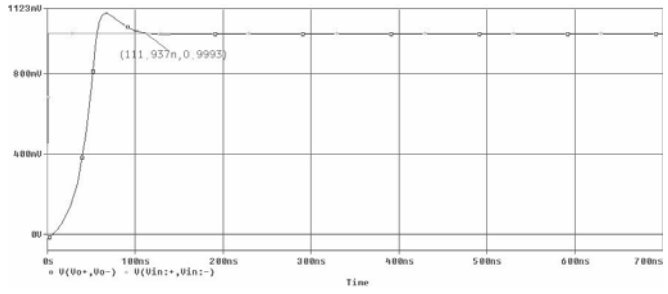


Figure 6.38 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling

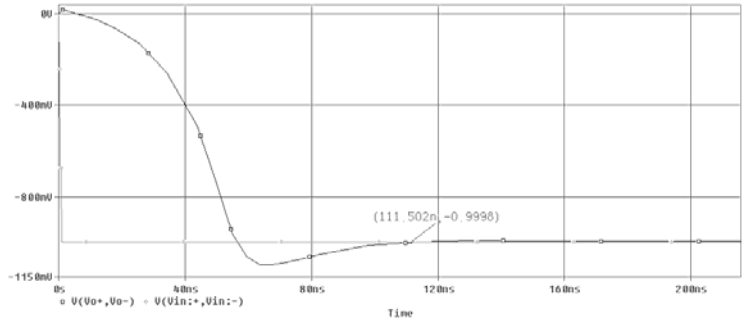


Figure 6.39 Negative slew-rate plot for the FTFA

7. Common-mode Rejection Ratio (CMRR)

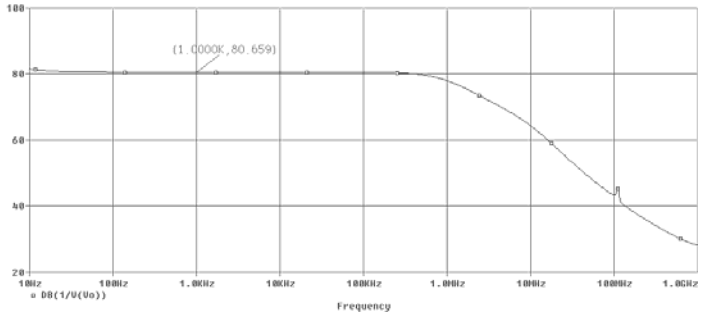


Figure 6.40 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE         =  3.255E-04 SQ V/HZ
                                   =  1.804E-02 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  1.870E+06
EQUIVALENT INPUT NOISE AT V_Vin =  9.647E-09 V/RT HZ
```

Figure 6.41 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.413E+00	1.000E+00	-4.602E+01	0.000E+00
2	2.000E+03	6.065E-02	4.292E-02	-1.589E+02	-6.688E+01
3	3.000E+03	3.721E-01	2.633E-01	1.776E+02	3.156E+02
4	4.000E+03	2.802E-02	1.983E-02	7.295E+01	2.570E+02
5	5.000E+03	2.228E-01	1.577E-01	5.344E+01	2.835E+02
6	6.000E+03	2.242E-02	1.587E-02	-6.285E+01	2.133E+02
7	7.000E+03	1.594E-01	1.128E-01	-6.995E+01	2.522E+02
8	8.000E+03	2.022E-02	1.431E-02	1.670E+02	5.352E+02
9	9.000E+03	1.241E-01	8.782E-02	1.669E+02	5.810E+02

TOTAL HARMONIC DISTORTION = 3.425341E+01 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.414E+00	1.000E+00	1.341E+02	0.000E+00
2	2.000E+03	4.901E-02	3.466E-02	-1.244E+02	-3.926E+02
3	3.000E+03	3.722E-01	2.633E-01	-2.064E+00	-4.043E+02
4	4.000E+03	2.659E-02	1.881E-02	1.509E+02	-3.854E+02
5	5.000E+03	2.229E-01	1.577E-01	-1.259E+02	-7.963E+02
6	6.000E+03	2.117E-02	1.498E-02	4.238E+01	-7.621E+02
7	7.000E+03	1.595E-01	1.128E-01	1.110E+02	-8.276E+02
8	8.000E+03	1.944E-02	1.375E-02	-7.180E+01	-1.144E+03
9	9.000E+03	1.241E-01	8.779E-02	-1.200E+01	-1.219E+03

TOTAL HARMONIC DISTORTION = 3.414055E+01 PERCENT

Figure 6.42 Fourier components of transient response

Simulation for FTFN Folded-Cascode using typical models

1. Open-loop gain, 3dB frequency, unity-gain frequency and phase margin

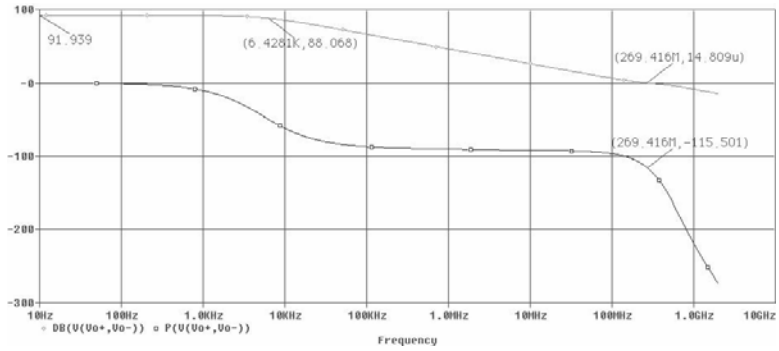


Figure 6.43 Gain and phase plots for Telescopic FTFN

2. Common-mode Input Range

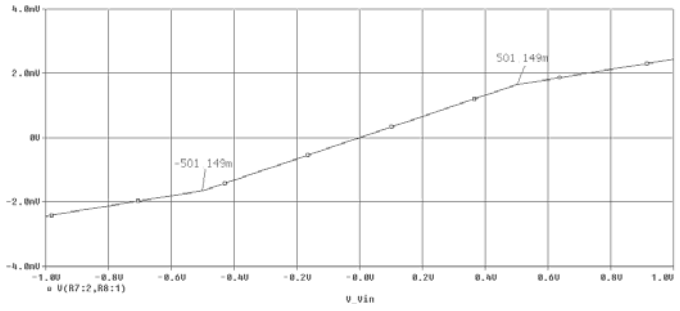


Figure 6.44 Input common-mode range plot

3. DC Transfer Characteristic

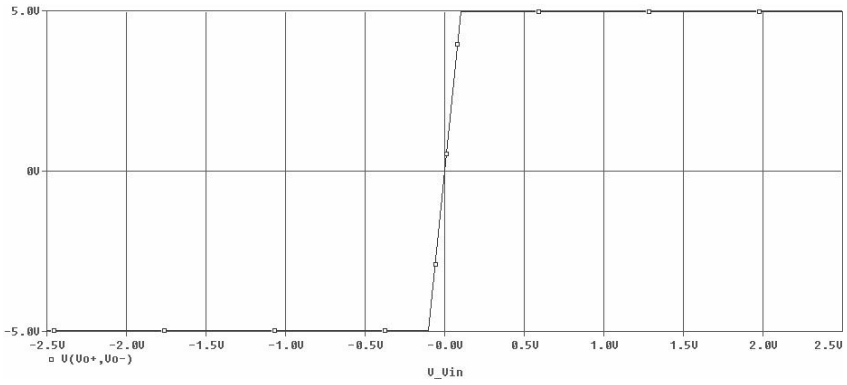


Figure 6.45 DC transfer characteristic for Telescopic FTFN

4. Offset Voltage

4. For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively

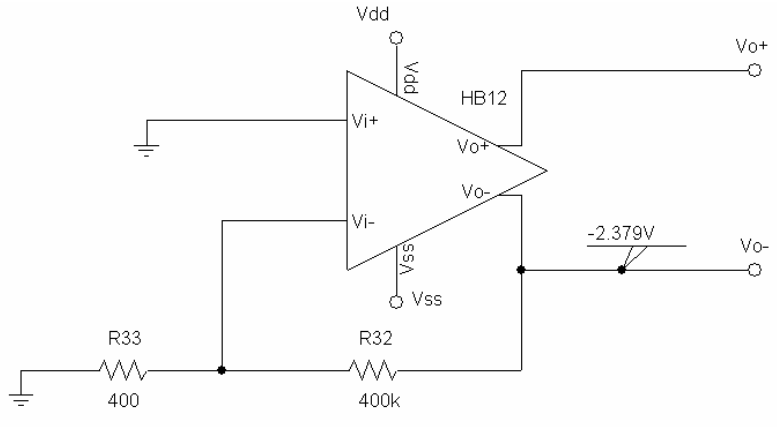


Figure 6.46 Offset-voltage calculation circuit

The offset results in:

$$V_{off} = -\frac{1+\frac{4000}{35481.33}}{4000}(2)(-2.378V) = 1.32\,mV$$

5. Output Swing

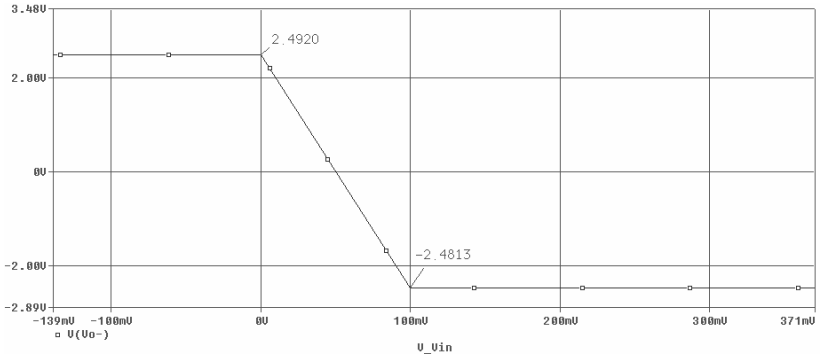


Figure 6.47 Output Swing for Telescopic FTFN test setup

6. Settling time

A. Positive Settling Time

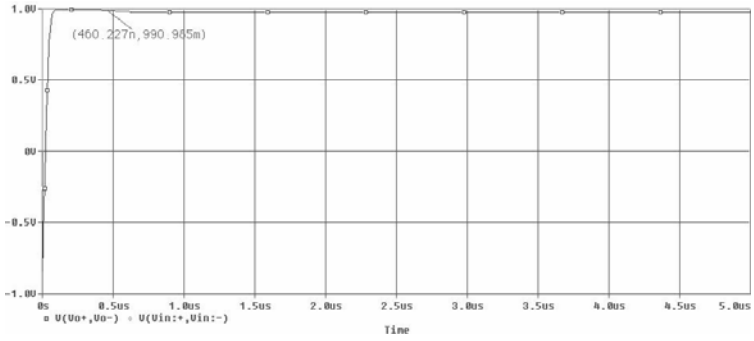


Figure 6.48 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling Time

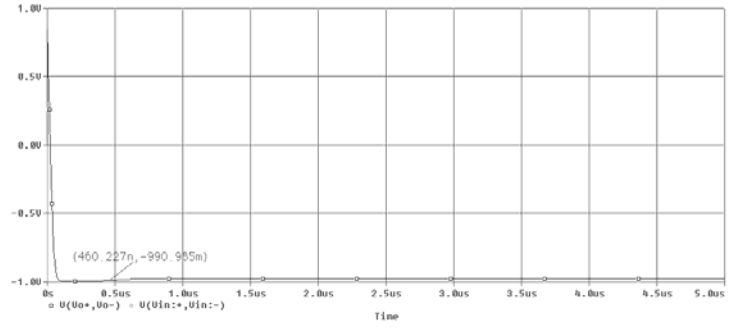


Figure 6.49 Negative slew-rate plot for the FTFA

7. Common-mode Rejection Ratio

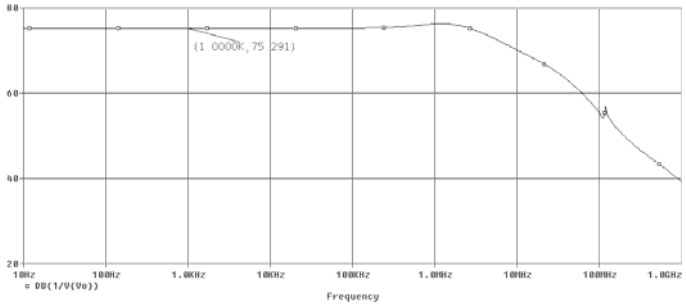


Figure 6.50 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE          =  2.032E-08 SQ V/HZ
                                    =  1.425E-04 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  1.977E+04
EQUIVALENT INPUT NOISE AT V_Vin =  7.212E-09 V/RT HZ
```

Figure 6.51 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = -1.301160E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.987E-01	1.000E+00	-1.800E+02	0.000E+00
2	2.000E+03	4.279E-02	8.581E-02	-8.991E+01	2.701E+02
3	3.000E+03	1.076E-05	2.158E-05	-1.247E+02	4.153E+02
4	4.000E+03	1.682E-04	3.374E-04	-7.762E+01	6.423E+02
5	5.000E+03	3.228E-05	6.473E-05	1.450E+02	1.045E+03
6	6.000E+03	7.707E-06	1.545E-05	-1.056E+01	1.069E+03
7	7.000E+03	2.649E-05	5.311E-05	6.813E+01	1.328E+03
8	8.000E+03	3.967E-05	7.954E-05	-1.320E+02	1.308E+03
9	9.000E+03	3.741E-05	7.501E-05	-1.278E+00	1.619E+03

TOTAL HARMONIC DISTORTION = 8.581552E+00 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

DC COMPONENT = -1.301229E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.987E-01	1.000E+00	1.363E-02	0.000E+00
2	2.000E+03	4.287E-02	8.596E-02	-9.007E+01	-9.010E+01
3	3.000E+03	6.793E-05	1.362E-04	-1.508E+01	-1.512E+01
4	4.000E+03	1.438E-04	2.884E-04	-1.315E+02	-1.316E+02
5	5.000E+03	1.152E-04	2.309E-04	-5.659E+01	-5.665E+01
6	6.000E+03	1.399E-04	2.806E-04	9.891E+01	9.883E+01
7	7.000E+03	1.153E-04	2.312E-04	-1.043E+02	-1.044E+02
8	8.000E+03	9.905E-05	1.986E-04	4.685E+01	4.674E+01
9	9.000E+03	1.043E-04	2.092E-04	-1.544E+02	-1.546E+02

TOTAL HARMONIC DISTORTION = 8.596524E+00 PERCENT

Figure 6.52 Fourier components of transient response

Simulation for FTFN Folded-Cascode using slow-slow models

1. Open-loop gain, 3dB frequency and phase margin

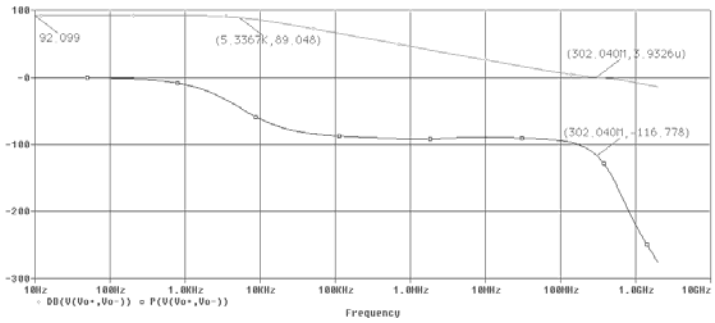


Figure 6.53 Gain and phase plots for Telescopic FTFN

2. Common-mode Input Range

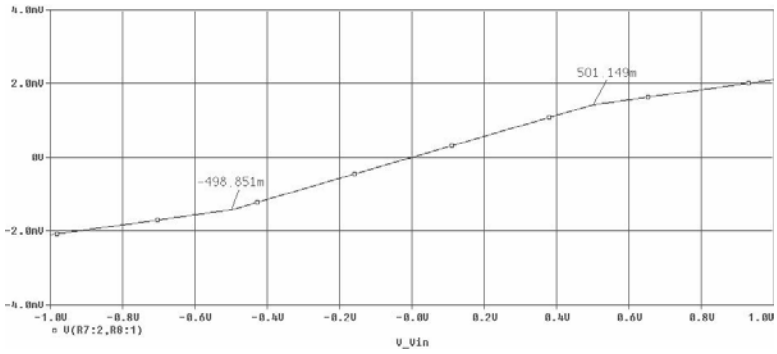


Figure 6.54 Input common-mode range plot

3. DC Transfer Characteristic

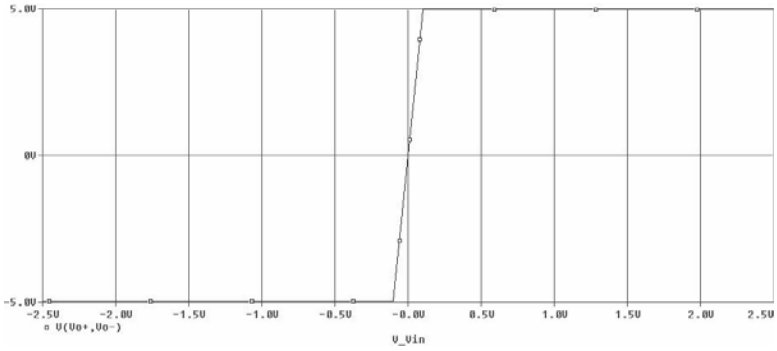


Figure 6.55 DC transfer characteristic for Telescopic FTFN

4. For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively

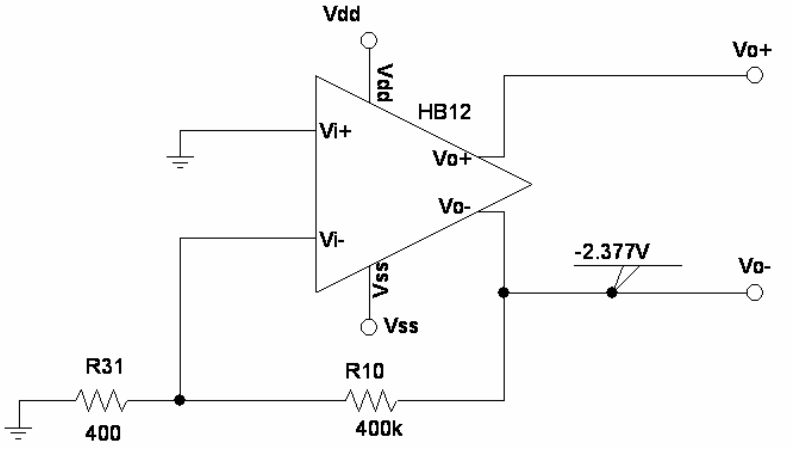


Figure 6.56 Offset-voltage calculation circuit

The offset voltage results in:

$$V_{off} = -\frac{1+\frac{4000}{35481.33}}{4000}(2)(-2.377V) = 1.32\,mV$$

5. Output Swing

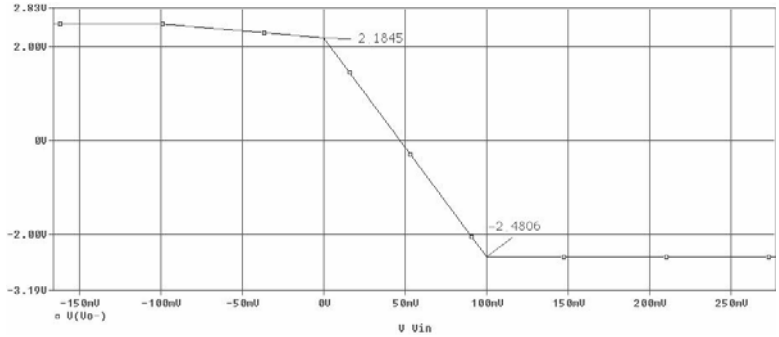


Figure 6.57 Output Swing for Telescopic FTFN test setup

6. Settling Time

A. Positive Settling Time

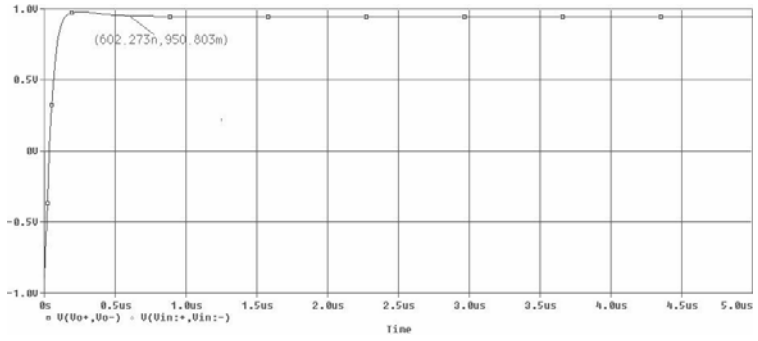


Figure 6.58 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling Time

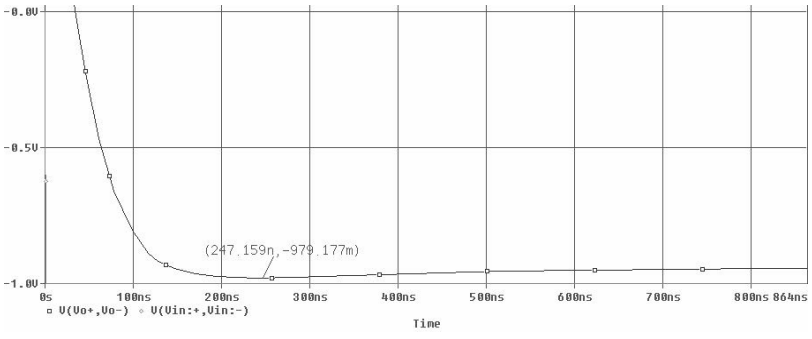


Figure 6.59 Negative slew-rate plot for the FTFA

7. Common-mode rejection ratio

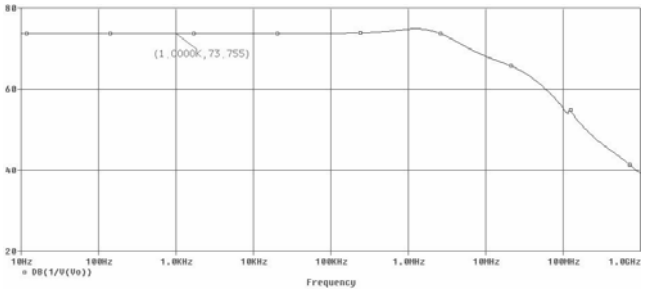


Figure 6.60 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE          =  2.080E-08 SQ V/HZ
                                    =  1.442E-04 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  2.013E+04
EQUIVALENT INPUT NOISE AT V_Vin =  7.163E-09 V/RT HZ
```

Figure 6.61 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = 1.819004E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.490E-01	1.000E+00	2.575E-02	0.000E+00
2	2.000E+03	1.977E-03	1.327E-02	8.945E+01	8.940E+01
3	3.000E+03	8.817E-05	5.917E-04	1.341E+02	1.340E+02
4	4.000E+03	5.875E-05	3.943E-04	7.873E+01	7.863E+01
5	5.000E+03	6.256E-05	4.199E-04	7.734E+01	7.721E+01
6	6.000E+03	6.174E-05	4.144E-04	7.553E+01	7.538E+01
7	7.000E+03	6.083E-05	4.083E-04	7.334E+01	7.316E+01
8	8.000E+03	5.981E-05	4.014E-04	7.113E+01	7.092E+01
9	9.000E+03	5.869E-05	3.939E-04	6.894E+01	6.871E+01

TOTAL HARMONIC DISTORTION = 1.332101E+00 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

DC COMPONENT = -2.163163E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	6.763E-02	1.000E+00	-1.800E+02	0.000E+00
2	2.000E+03	4.331E-04	6.404E-03	-9.117E+01	2.688E+02
3	3.000E+03	2.566E-05	3.794E-04	-9.466E+01	4.453E+02
4	4.000E+03	2.570E-05	3.801E-04	-1.006E+02	6.193E+02
5	5.000E+03	2.554E-05	3.776E-04	-1.025E+02	7.974E+02
6	6.000E+03	2.521E-05	3.728E-04	-1.045E+02	9.753E+02
7	7.000E+03	2.482E-05	3.670E-04	-1.067E+02	1.153E+03
8	8.000E+03	2.443E-05	3.613E-04	-1.089E+02	1.331E+03
9	9.000E+03	2.397E-05	3.545E-04	-1.111E+02	1.509E+03

TOTAL HARMONIC DISTORTION = 6.478528E-01 PERCENT

Figure 6.62 Fourier components of transient response

Simulation for FTFN Folded-Cascode using slow-fast models

1. Open-loop gain, 3dB frequency and phase margin

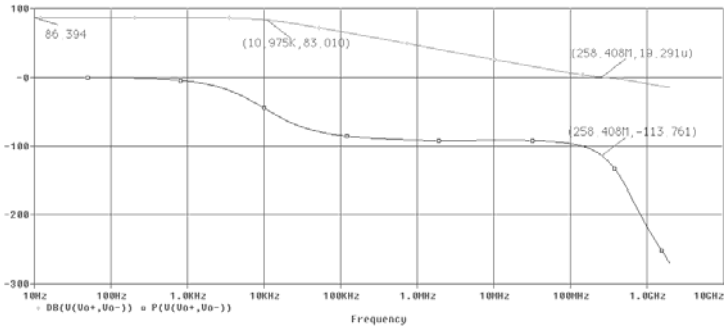


Figure 6.63 Gain and phase plots for Telescopic FTFN

2. Common-mode Input Range

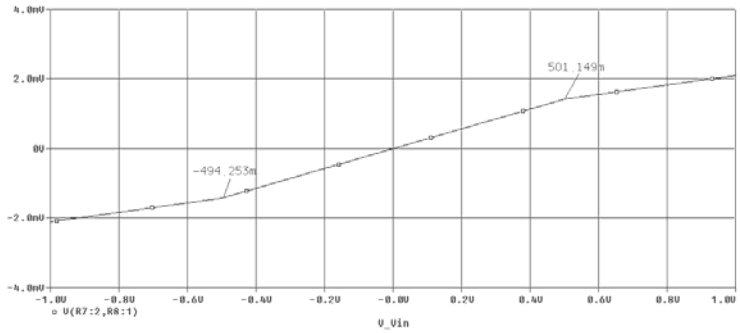


Figure 6.64 Input common-mode range plot

3. DC Transfer Characteristic

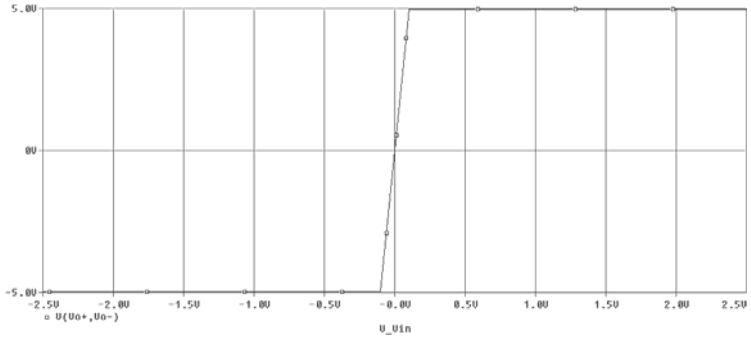


Figure 6.65 DC transfer characteristic for Telescopic FTFN

4. For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively

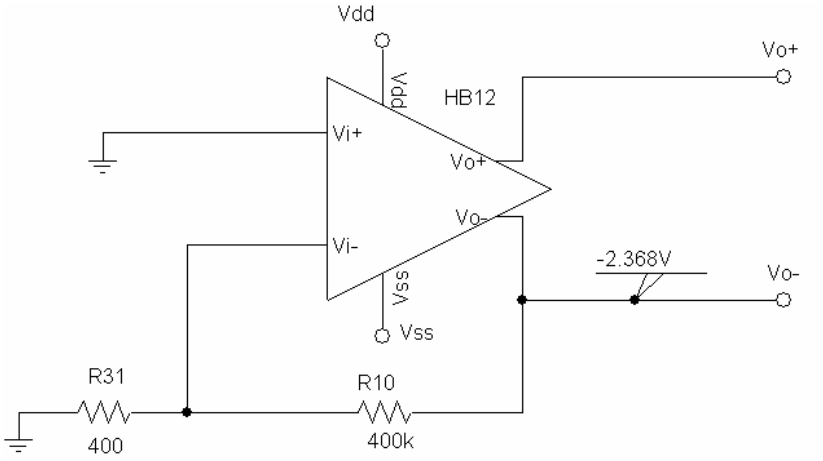


Figure 6.66 Offset-voltage calculation circuit

The offset voltage results in:

$$V_{off} = -\frac{1+\frac{4000}{35481.33}}{4000}(2)(-2.368V) = 1.31mV$$

5. Output Swing

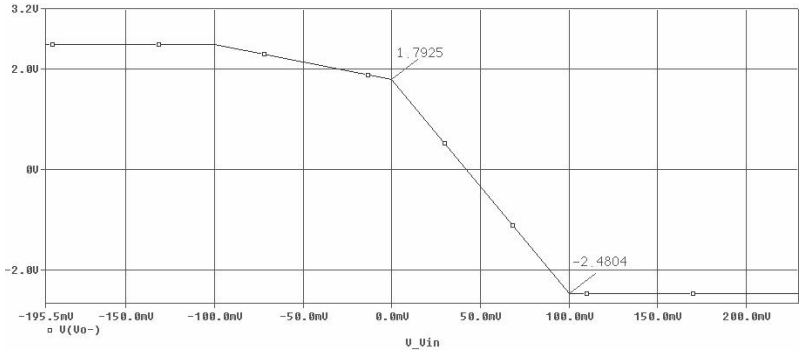


Figure 6.67 Output Swing for Telescopic FTFN test setup

6. Settling time

A. Positive Settling time

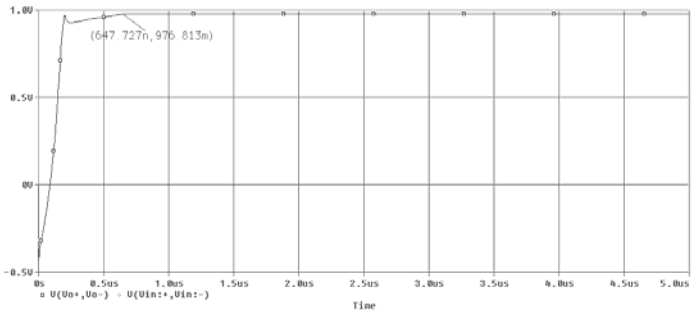


Figure 6.68 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling time

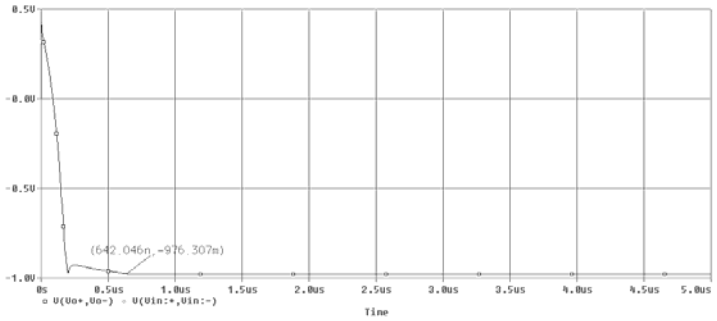


Figure 6.69 Negative slew-rate plot for the FTFA

7. Common-mode rejection Ratio

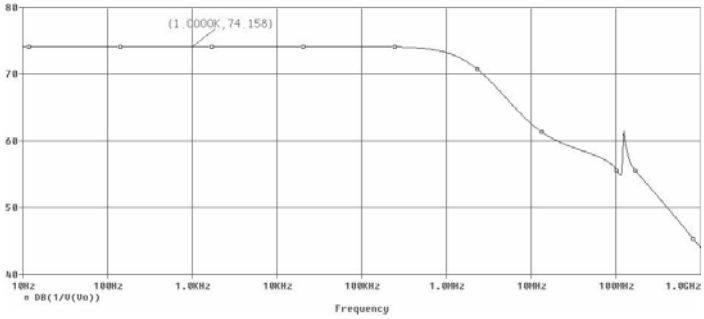


Figure 6.70 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE          =  5.402E-09 SQ V/HZ
                                    =  7.350E-05 V/RT HZ

TRANSFER FUNCTION VALUE:
  V(Vo+)/V_Vin                     =  1.044E+04
EQUIVALENT INPUT NOISE AT V_Vin =  7.041E-09 V/RT HZ
```

Figure 6.71 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = -2.288393E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.598E-02	1.000E+00	9.902E-03	0.000E+00
2	2.000E+03	3.546E-03	7.712E-02	-9.014E+01	-9.016E+01
3	3.000E+03	7.635E-04	1.660E-02	-5.386E-01	-5.683E-01
4	4.000E+03	4.073E-04	8.857E-03	-9.039E+01	-9.043E+01
5	5.000E+03	6.745E-04	1.467E-02	-1.598E+00	-1.648E+00
6	6.000E+03	3.192E-04	6.943E-03	-8.967E+01	-8.973E+01
7	7.000E+03	3.181E-04	6.918E-03	-3.029E+00	-3.098E+00
8	8.000E+03	2.044E-04	4.446E-03	-8.905E+01	-8.913E+01
9	9.000E+03	1.386E-04	3.015E-03	-2.821E+00	-2.910E+00

TOTAL HARMONIC DISTORTION = 8.149712E+00 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

DC COMPONENT = -2.288404E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.598E-02	1.000E+00	-1.799E+02	0.000E+00
2	2.000E+03	3.588E-03	7.803E-02	-8.969E+01	2.702E+02
3	3.000E+03	7.493E-04	1.630E-02	-1.784E+02	3.614E+02
4	4.000E+03	4.311E-04	9.376E-03	-8.664E+01	6.331E+02
5	5.000E+03	6.595E-04	1.434E-02	1.795E+02	1.079E+03
6	6.000E+03	3.185E-04	6.928E-03	-8.554E+01	9.941E+02
7	7.000E+03	3.078E-04	6.695E-03	1.762E+02	1.436E+03
8	8.000E+03	1.791E-04	3.896E-03	-8.402E+01	1.356E+03
9	9.000E+03	1.397E-04	3.039E-03	1.707E+02	1.790E+03

TOTAL HARMONIC DISTORTION = 8.225374E+00 PERCENT

Figure 6.72 Fourier components of transient response

Simulation for FTFN Folded-Cascode using fast-slow models

1. Open-loop gain, 3dB frequency and phase margin

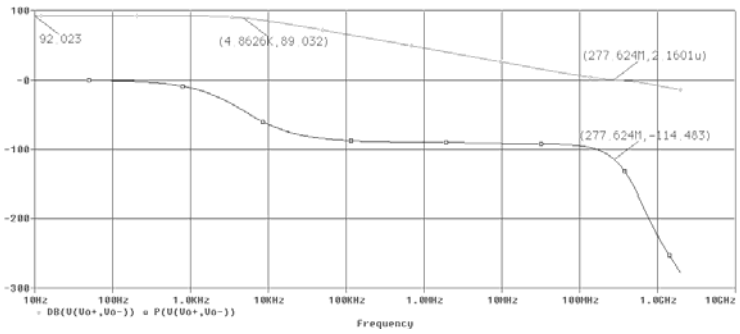


Figure 6.73 Gain and phase plots for Telescopic FTFN

2. Common-mode Input Range

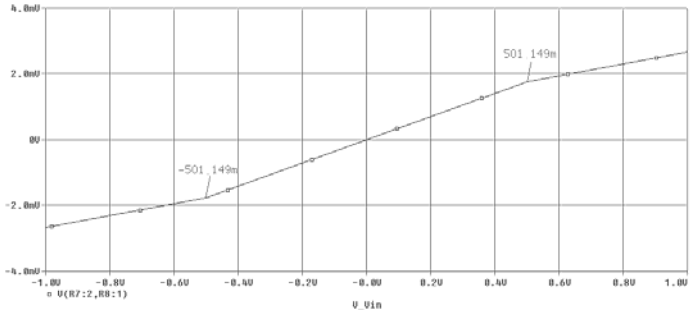


Figure 6.74 Input common-mode range plot

3. DC Transfer Characteristic

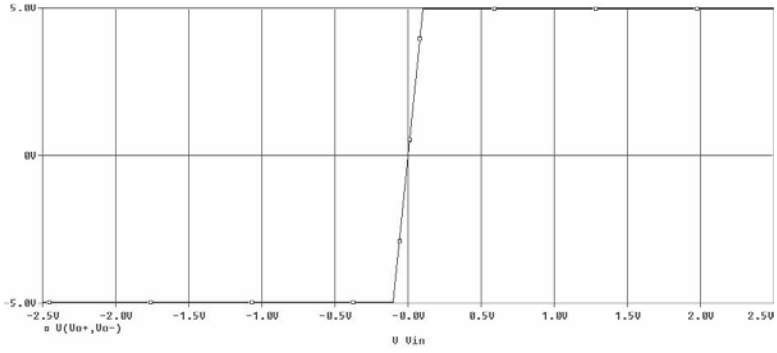


Figure 6.75 DC transfer characteristic for Telescopic FTFN

4. For the offset voltage measurement, a non-inverting configuration is used. In this case the offset voltage is calculated as follows:

$$V_{off} = -\frac{1+\frac{A_V}{a_{Vo}}}{A_V} 2V_o$$

$$A_V \approx 1+\frac{R_F}{R_2} \approx \frac{R_F}{R_2}$$

where A_V and a_{Vo} are the closed-loop and open loop gain respectively

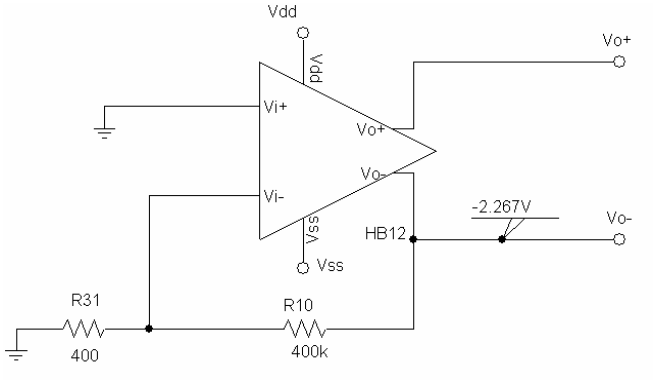


Figure 6.76 Offset-voltage calculation circuit

The offset results in:

$$V_{off} = -\frac{1+\frac{4000}{35481.33}}{4000}(2)(-2.267V) = 1.26\,mV$$

5. Output Swing

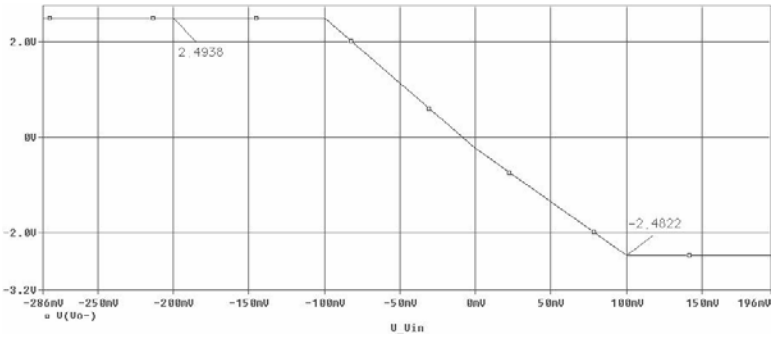


Figure 6.77 Output Swing for Telescopic FTFN

6. Settling time

A. Positive Settling time

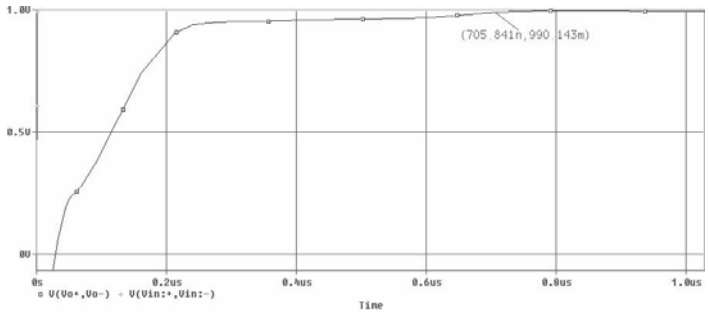


Figure 6.78 Positive slew-rate plot for the telescopic FTFA

B. Negative Settling time

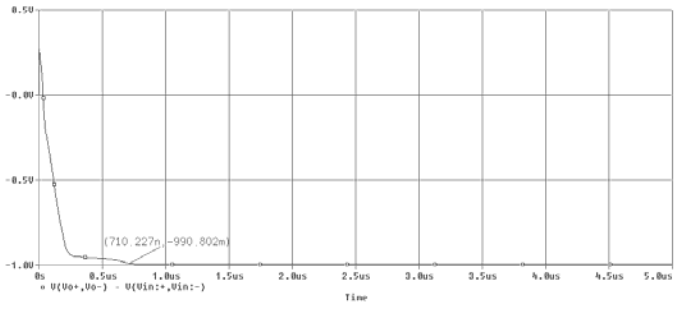


Figure 6.79 Negative slew-rate plot for the FTFA

7. Common-mode rejection ratio

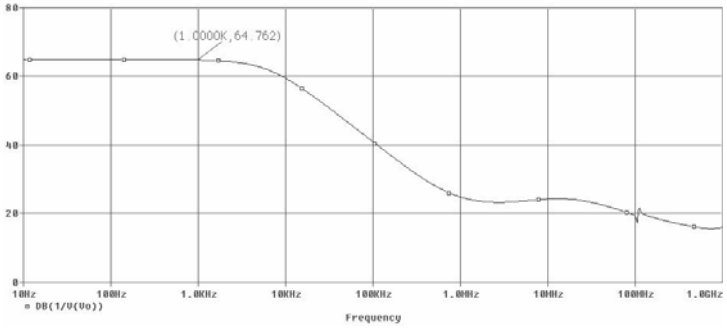


Figure 6.80 Common-mode rejection ratio plot

8. Input referred and total output noise

```
TOTAL OUTPUT NOISE VOLTAGE          =  2.271E-08 SQ V/HZ
                                    =  1.507E-04 V/RT HZ

TRANSFER FUNCTION VALUE:

  V(Vo+)/V_Vin                     =  1.996E+04

EQUIVALENT INPUT NOISE AT V_Vin =  7.551E-09 V/RT HZ
```

Figure 6.81 Output result for input-referred offset voltage and total output noise

9. Total Harmonic Distortion

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo+)

DC COMPONENT = -2.293172E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.978E-02	1.000E+00	7.537E-02	0.000E+00
2	2.000E+03	5.563E-03	1.118E-01	-9.003E+01	-9.018E+01
3	3.000E+03	1.769E-04	3.553E-03	1.610E+02	1.607E+02
4	4.000E+03	5.384E-04	1.082E-02	8.807E+01	8.777E+01
5	5.000E+03	1.204E-03	2.419E-02	6.242E-01	2.474E-01
6	6.000E+03	3.716E-04	7.464E-03	-8.758E+01	-8.803E+01
7	7.000E+03	2.479E-04	4.979E-03	-1.341E+00	-1.869E+00
8	8.000E+03	2.855E-05	5.735E-04	7.194E+00	6.591E+00
9	9.000E+03	2.587E-04	5.197E-03	-6.413E+00	-7.092E+00

TOTAL HARMONIC DISTORTION = 1.153770E+01 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(Vo-)

DC COMPONENT = -2.293182E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	4.978E-02	1.000E+00	-1.799E+02	0.000E+00
2	2.000E+03	5.550E-03	1.115E-01	-9.011E+01	2.697E+02
3	3.000E+03	1.660E-04	3.334E-03	-2.140E+01	5.184E+02
4	4.000E+03	5.236E-04	1.052E-02	8.919E+01	8.089E+02
5	5.000E+03	1.204E-03	2.419E-02	-1.791E+02	7.206E+02
6	6.000E+03	3.793E-04	7.619E-03	-8.952E+01	9.900E+02
7	7.000E+03	2.582E-04	5.188E-03	-1.780E+02	1.081E+03
8	8.000E+03	3.190E-05	6.408E-04	-4.207E+01	1.397E+03
9	9.000E+03	2.563E-04	5.149E-03	1.763E+02	1.796E+03

TOTAL HARMONIC DISTORTION = 1.151086E+01 PERCENT

Figure 6.82 Fourier components of transient response

Improved Telescopic FTFA

Parameter	Typical models	Slow-Slow models	Slow-Fast models	Fast-Slow models
Open-loop gain	113 dB	113 dB	113 dB	131 dB
Phase Margin	62°	58°	51°	66°
Unity-gain	294 MHz	320 MHz	355 MHz	276 MHz
3dB frequency	335 Hz	351 Hz	319 Hz	319 Hz
Input Common-Mode Range	$-502mV \le V_{CMR} \le 502mV$	$-497.7\,mV \le V_{CMR} \le 504.5\,mV$	$-504.5\,mV \le V_{CMR} \le 502.2\,mV$	$-504mV \le V_{CMR} \le 509.91mV$
Power Dissipation	88.25 mW	95.1 mW	95.75 mW	99 mW
Offset Voltage	1.22 mV	1.22 mV	1.22 mV	1.22 mV
Output Swing	$-2.426V \le V_{OS} \le 2.356V$	$-2.445V \le V_{OS} \le 2.358V$	$-2.433V \le V_{OS} \le 2.426V$	$-2.45V \le V_{OS} \le 1.37V$
Settling Time	$S^+ = 113ns\ S^- = 113ns$	$S^+ = 193ns\ S^- = 174ns$	$S^+ = 132ns\ S^- = 132ns$	$S^+ = 111.93ns\ S^- = 111.50ns$
Slew Rate	$SR^+ = 29.96\frac{V}{\mu s}$ $SR^- = 29.95\frac{V}{\mu s}$	$SR^+ = 29.96\frac{V}{\mu s}$ $SR^+ = 29.96\frac{V}{\mu s}$	$SR^+ = 24.33\frac{V}{\mu s}$ $SR^- = 24.34\frac{V}{\mu s}$	$SR^+ = 24.38\frac{V}{\mu s}$ $SR^- = 24.38\frac{V}{\mu s}$
Common-mode Rejection Ratio	80 dB	79 dB	80 dB	80 dB
Input-referred noise	$8.34\ \frac{nV}{\sqrt{Hz}}$	$8.19\ \frac{nV}{\sqrt{Hz}}$	$8.04\ \frac{nV}{\sqrt{Hz}}$	$9.64\ \frac{nV}{\sqrt{Hz}}$
THD@1KHz	$V_o^+ = 3.2610\%$ $V_o^- = 2.806\%$	$V_o^+ = 6.285\%$ $V_o^- = 6.294\%$	$V_o^+ = 4.991\%$ $V_o^- = 7.031\%$	$V_o^+ = 3.425x10^1\%$ $V_o^- = 3.414x10^1\%$

Table 6.1 Improved FTFA Telescopic results

Improved Folded Cascode FTFA

Parameter	Typical models	Slow-Slow models	Slow-Fast models	Fast-Slow models
Open-loop gain	91 dB	92 dB	86 dB	92 dB
Phase Margin	65°	63°	66°	65°
Unity-gain	269 MHz	302 MHz	258 MHz	277 MHz
3dB frequency	6.248 kHz	5.33 kHz	10.97 kHz	4.86 kHz
Input Common-Mode Range	$-501mV \le V_{CMR} \le 501mV$	$-498mV \le V_{CMR} \le 501mV$	$-494mV \le V_{CMR} \le 501mV$	$-501mV \le V_{CMR} \le 501mV$
Power Dissipation	76.2 mW	79.7 mW	76.4 mW	78.4 mW
Offset Voltage	1.32 mV	1.32 mV	1.31 mV	1.26 mV
Output Swing	$-2.48V \le V_{OS} \le 2.49V$	$-2.48V \le V_{OS}\ 2.184V$	$-2.48V \le V_{OS} \le 1.79V$	$-2.45V \le V_{OS} \le 1.37V$
Settling Time	$S^+ = 460ns\, S^- = 460ns$	$S^+ = 602ns\, S^- = 247ns$	$S^+ = 647ns\, S^- = 642ns$	$S^+ = 705.8ns\, S^- = 710ns$
Slew Rate	$SR^+ = 27.18\frac{V}{\mu s}$ $SR^- = 27.18\frac{V}{\mu s}$	$SR^+ = 12\frac{V}{\mu s}$ $SR^+ = 12\frac{V}{\mu s}$	$SR^+ = 10.31\frac{V}{\mu s}$ $SR^- = 10.31\frac{V}{\mu s}$	$SR^+ = 5\frac{V}{\mu s}$ $SR^- = 5\frac{V}{\mu s}$
Common-mode Rejection Ratio	75 dB	73 dB	74 dB	64 dB
Input-referred noise	$7.21\ \frac{nV}{\sqrt{Hz}}$	$7.16\ \frac{nV}{\sqrt{Hz}}$	$7\ \frac{nV}{\sqrt{Hz}}$	$7.55\ \frac{nV}{\sqrt{Hz}}$
THD@1KHz	$V_o^+ = 8.58\%$ $V_o^- = 8.59\%$	$V_o^+ = 1.332\%$ $V_o^- = 6.478\%$	$V_o^+ = 8.14\%$ $V_o^- = 8.22\%$	$V_o^+ = 1.1537x10^{l}\%$ $V_o^- = 1.1510x10^{l}\%$

Table 6.2 Improved FTFA Folded-Cascode results

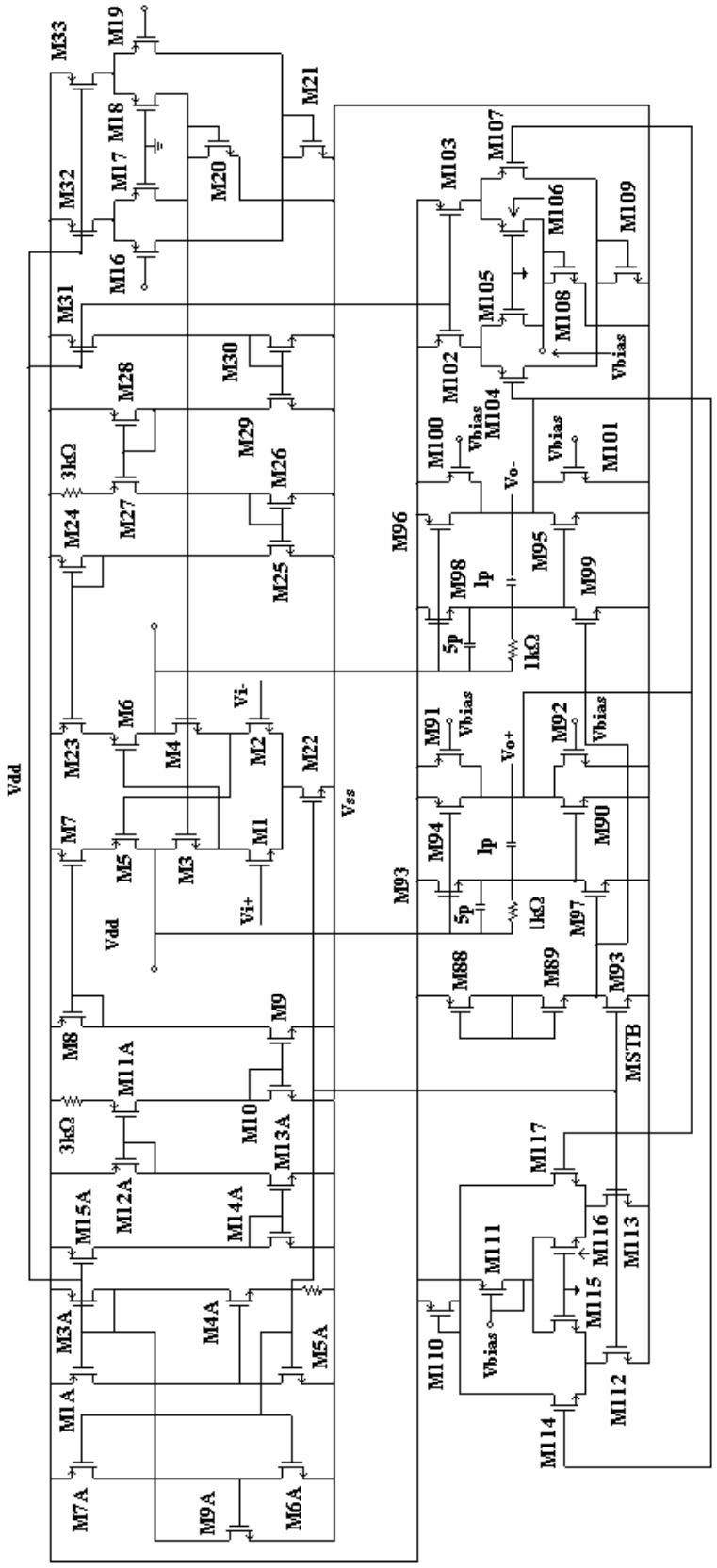


Figure 6.83 Telescopic FTFA with CCFMB

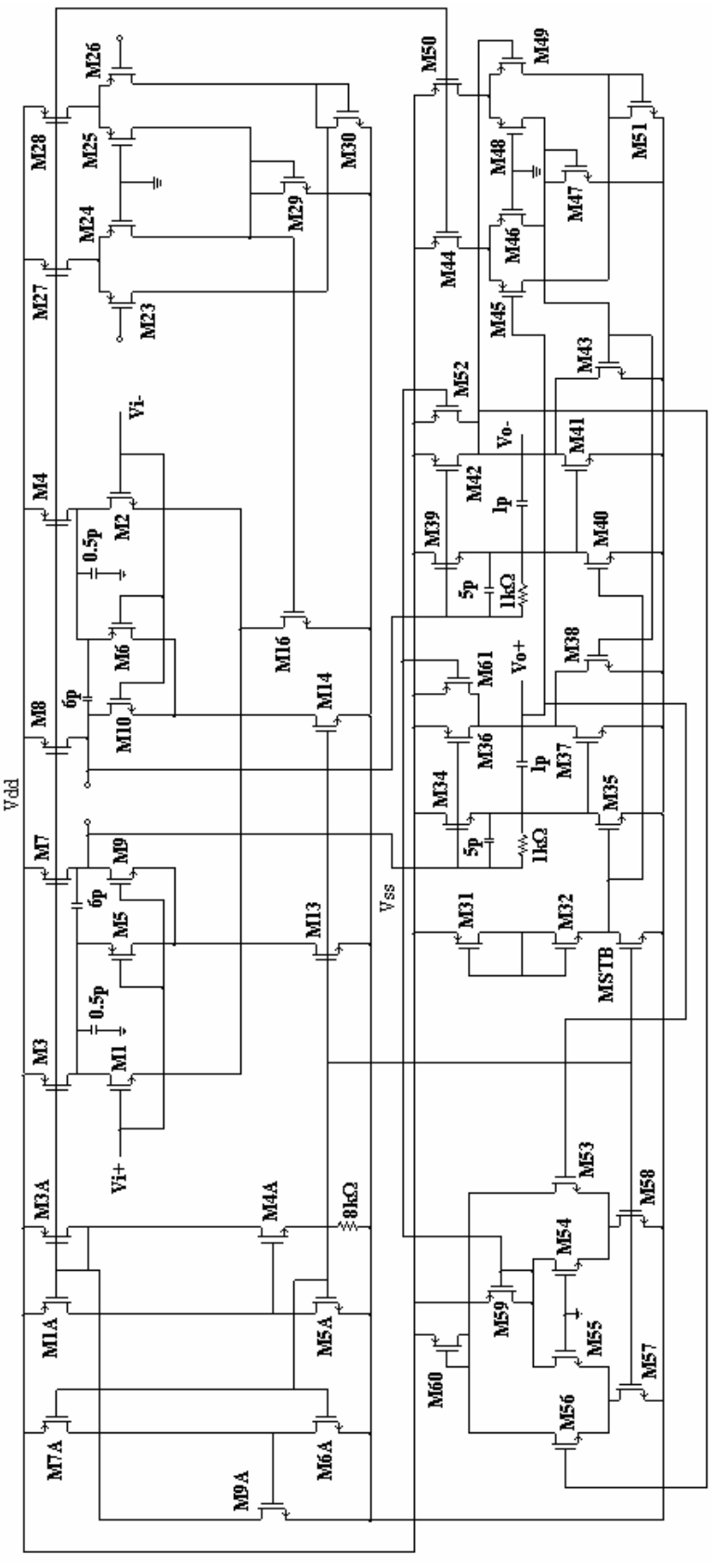


Figure 6.84 Folded-Cascode FTFA with CCMFB

Chapter 7 Applications in analog electronics using FTFN

This chapter presents simulations using the proposed designs in some applications. The objective is to validate the behavior of the proposed design.

7.1 Realization of inverse transfer functions

Electrical systems process a signal $u(t)$ is to produce an output $y = f(u(t))$. Given this result, a circuit realizing the inverse transfer functions and characteristics, that is, producing $y = f^{-1}(u(t))$ is sometimes desired.

Leuciuc [38], provided a general method to obtain the inverse transfer function for linear dynamic systems and the inverse transfer characteristic for nonlinear resistive circuits. Only an example of nonlinear resistive circuits will be illustrated here. Figure 7.1 shows the basic scheme for obtaining the inverse transfer function. More nullors may embedded in the circuit network.

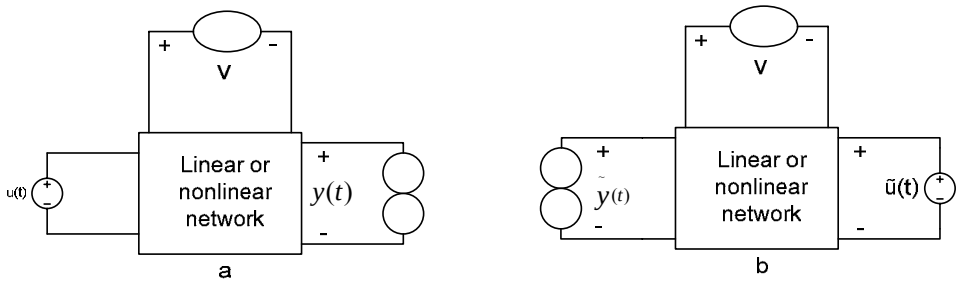


Figure 7.1 Basic schemes for inverse transformation with original circuit (a) and its inverse (b)

In figure 7.1a, $y(t) = f(u(t))$. Exchanging norator and input, the circuit of figure 7.1b realizes $\tilde{y}(t) = f^{-1}(\tilde{u}(t))$.

To illustrate the inverse concept with a non-resistive application, figure 7.2 shows a basic half-wave rectifier.

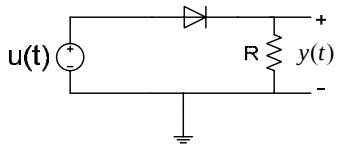


Figure 7.2 Basic half-wave rectifier

Figure 7.3 shows the circuit of Figure 7.2 with a nullor in unity-gain configuration in terms of norator and nullator models, and this would be the circuit corresponding to Figure 7.1a.

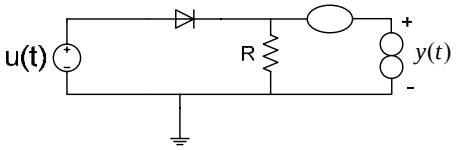


Figure 7.3 Basic half-wave augmented with unity gain

The inverse function circuit corresponding to Figure 7.1b is shown in Figure 7.4 for this example or, using an FTFN block as shown in Figure 7.5.

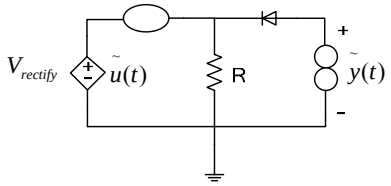


Figure 7.4 Inverse function circuit with nullators and norators

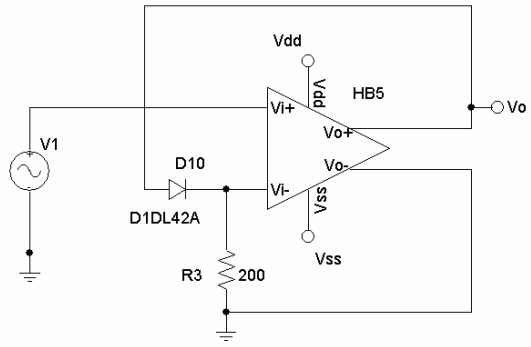


Figure 7.5 Inverse function circuit with FTFN

The circuit used for simulation is shown in Figure 7.6. The left hand side is the original circuit and the right half is the inverse circuit, which receives the rectified waveform as input. Theoretically, the same waveform as the one provided by the source should appear at the output of the right hand side.

The figure corresponds to the circuit for the telescopic FTFN. The folded-cascode amplifier is similarly used. Here, physical diodes models are used in the simulation.

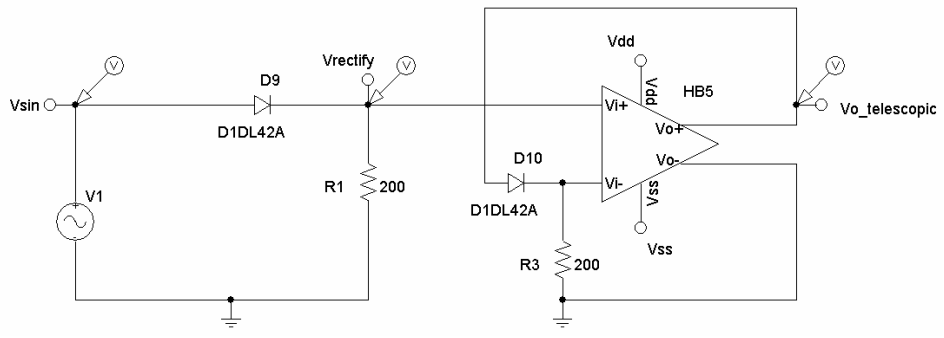


Figure 7.6 Half-wave rectifier and inverse circuit

The three curves in Figure 7.7 correspond to the sinusoidal source, the rectified voltage and the curve recovered through the inverse function circuit, respectively with the telescopic amplifier.

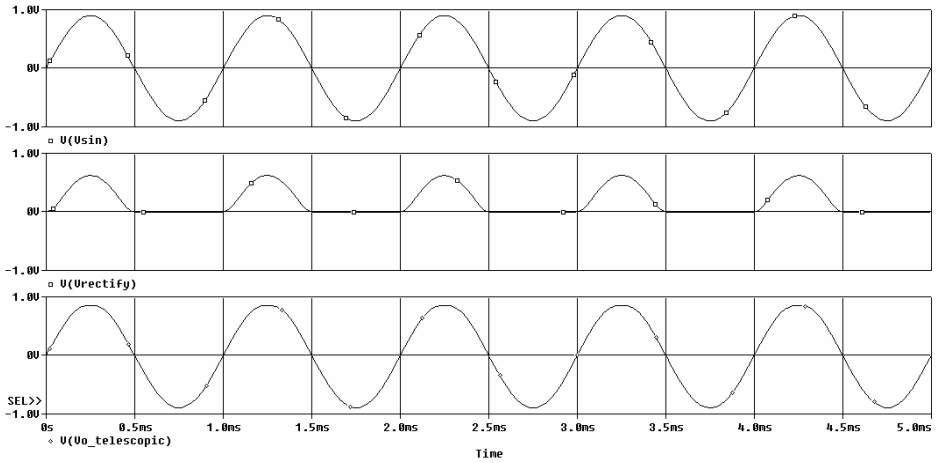


Figure 7.7 Sinusoidal, rectify and inverse function plot for telescopic FTFN

It can be seen that the inverse function operation is effectively realized with this circuit. Figure 7.8 shows the curves for the case of the folder-cascode FTFN.

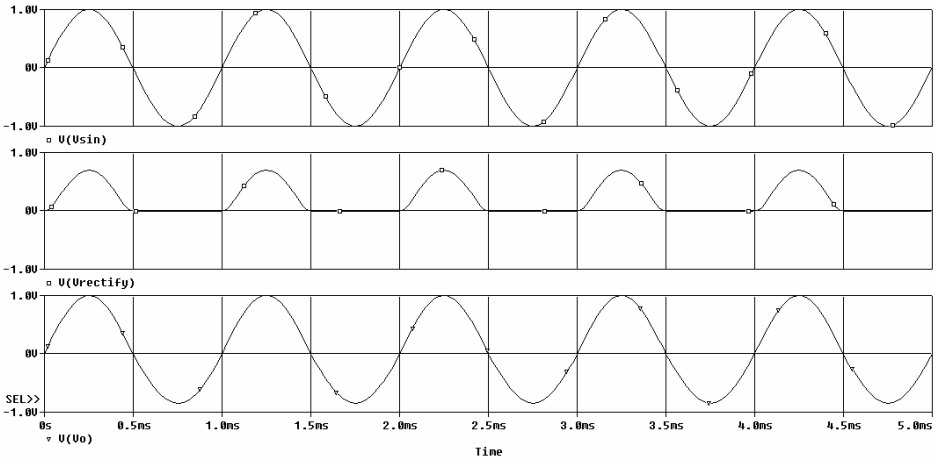


Figure 7.8 Sinusoidal, rectify and inverse function plot for folded-cascode FTFN

Saturation can be appreciated for one half of the recovered waveform. As a consequence, this amplifier's performance shows that compensation is needed in this case, or else that application falls outside the range of usefulness. Further study would be required to dilucidate the problem.

7.2 High-Pass Sallen-Key Filter

An interesting application arises when the output port of an active device is floating within a network. That is, none of the terminals is connected to ground. This is the case of the current mode high-pass Sallen-Key filter when it is derived from the voltage mode type [5]. Two examples of this filter will be shown. The first one is a voltage-mode high-pass Sallen-Key filter. This version is realizable with normal op-amp's and is tested here with the proposed designs too. The second is a current-mode high-pass Sallen-Key obtained by the transposition method. In this case, the use of common op-amp is not possible due to the floating requirement at the amplifier output.

Figure 7.9 shows the voltage mode high-pass Sallen-Key modelled with nullators and norators.

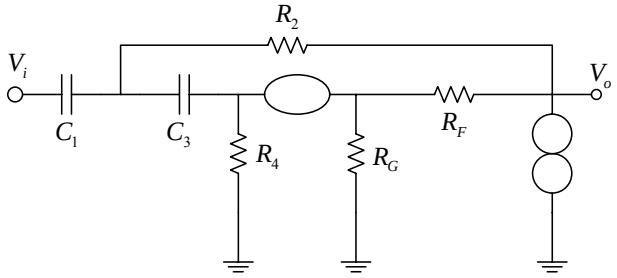


Figure 7.9 High-Pass Sallen-Key voltage-mode filter represented with nullators and norator

This circuit is used as departing point to obtain the current-mode filter equivalent by means of nullator and norator transposition [39]. This transformation is depicted in Figure 7.10.

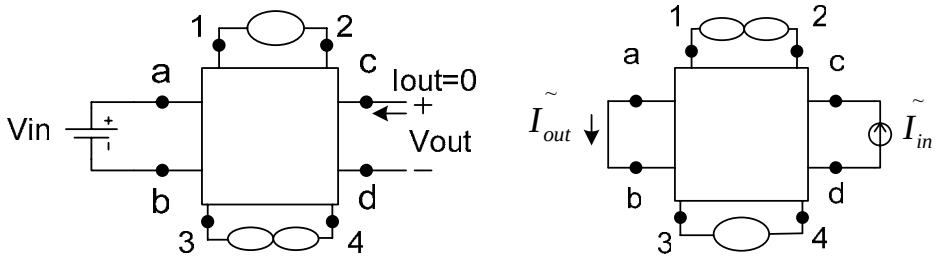


Figure 7.10 Transposed circuits with nullators and norators

The transfer functions for these two circuits are related as

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{\tilde{I}_{out}(s)}{\tilde{I}_{in}(s)} \tag{6.2.1}$$

As a consequence, the resultant nullator-norator based current-mode high-pass filter is shown in Figure 7.11, and realizes a current transfer function equivalent to the one obtained with the voltage mode circuit of Figure 7.10

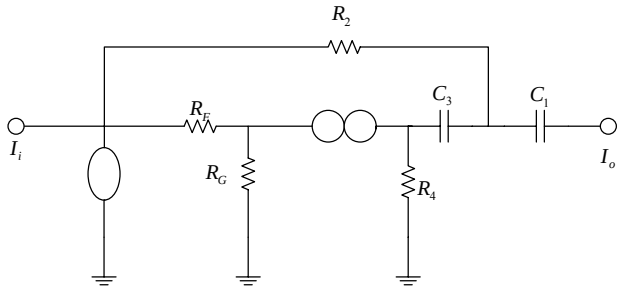


Figure 7.11 Nullator-norator high-pass sallen-key filter

FTFN's based implementations of both voltage-mode and current mode filters are shown in Figures 7.12 and 7.13 respectively. Owing to the presence of a floating output, the current-mode version cannot be implemented with any normal operational amplifiers.

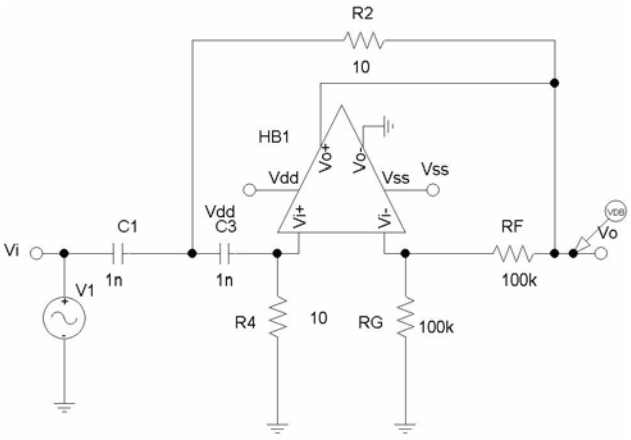


Figure 7.12 Voltage-mode High-pass Sallen-Key filter

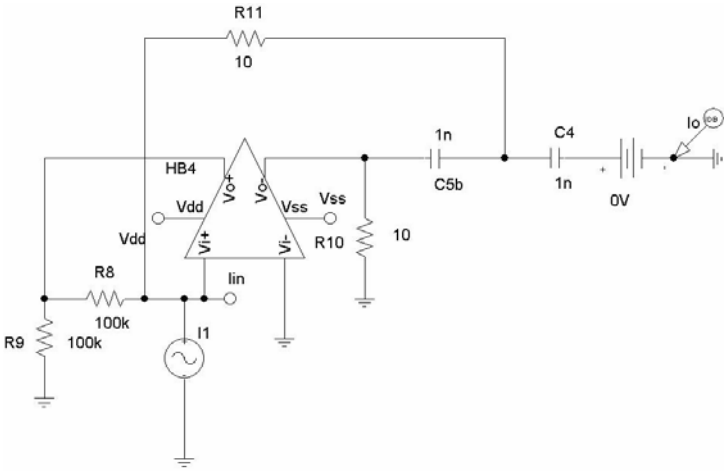


Figure 7.13 Current-mode High-Pass Sallen-Key filter

For simulation purposes, the values chosen for resistor and capacitors are $R_2 = R_4 = 100\,\Omega$, $R_F = R_G = 100k\,\Omega$ and $C_1 = C_2 = 0.1nF$. Both voltage-mode and current-mode ac circuit response are shown in Figure 7.14 for telescopic FTFN.

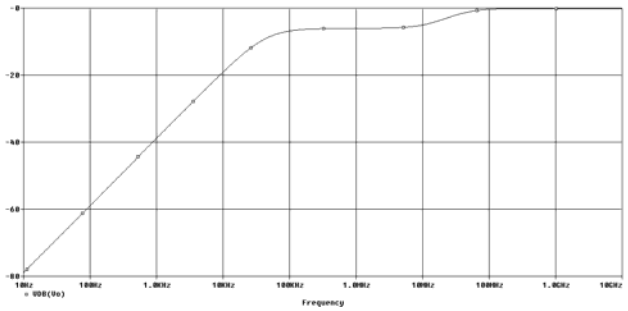


Figure 7.14a Voltage-mode Sallen-Key High Pass response for Telescopic FTFA

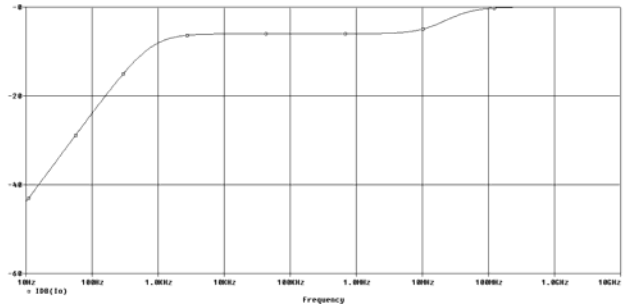


Figure 7.14b Current-mode High Pass Sallen-Key response for Telescopic FTFA

On the other hand, Figures 7.15a and Figure 7.15b show the response using the folded-cascode FTFN. Both voltage-mode and current-mode approaches show a similar response rejecting low-frequency signals which is not surprising because the transposition theorem applies also for non ideal amplifiers.

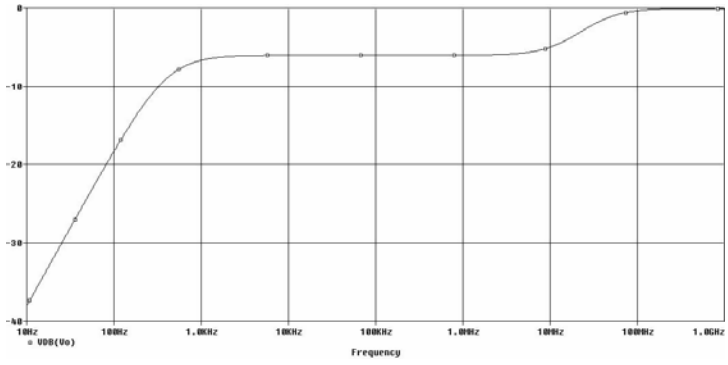


Figure 7.15a Voltage-mode Sallen Key High-Pass response with folded-cascode FTFA

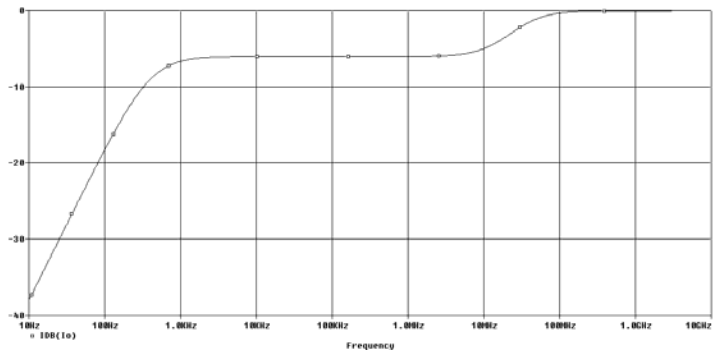


Figure 7.15b Current-mode Sallen-Key High Pass response with folded-cascode FTFA

7.3 FTFN realization of basic amplifiers

This section presents implementation of basic amplifiers with FTFN's. This is a common application type for operational amplifiers. Yet, unlike the case of common op-amps, we are now in position to realize basic amplifiers which require a floating output from the active device.

A common application common in analog electronics is the voltage follower. When the negative input terminal is connected with the output, an operational amplifier is transformed to a voltage follower. Figure 7.16 shows the DC simulation of the implementation, a) for the folded-cascode FTFN and figure 7.16b for the telescopic FTFN.

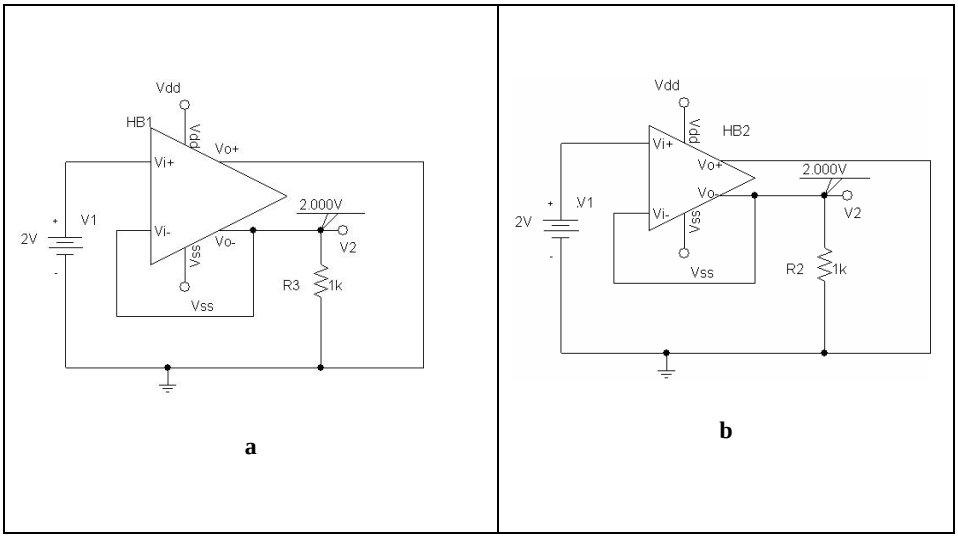


Figure 7.16 Voltage Follower realization with FTFN

7.3.1 FTFN realization of floating amplifiers

An application specific to the FTFN is the voltage-to-current converter or transadmittance amplifier. This realization is shown in Figure 7.17, where the spice schematic with a transadmittance amplifier is shown for comparison.

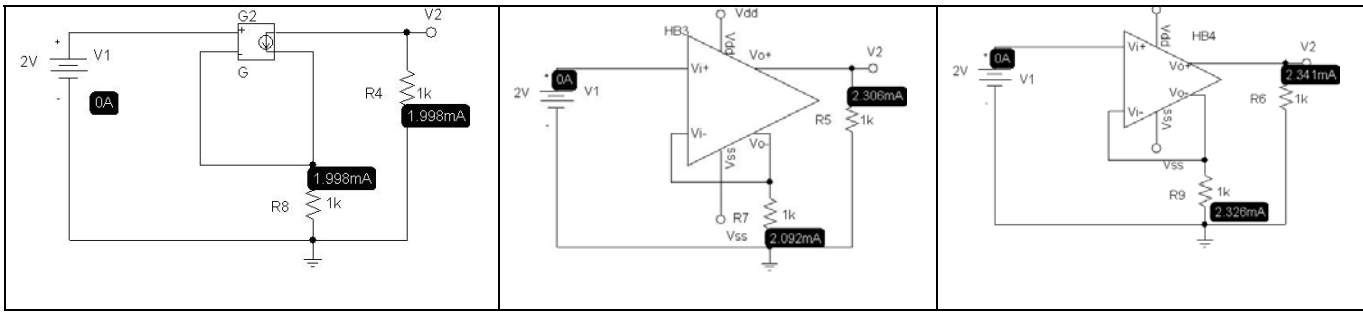


Figure 7.17 Voltage-to-Current converter with nullor and OFA symbols

The output current is calculated as:

$$I_{out} = \frac{V_1}{R_1} \tag{7.3.1}$$

with $V_{in} = 2V$ and $R_1 = 1k\Omega$.

Another application is the current amplifier which is shown in Figure 7.18. The current amplification for this application is:

$$A_I = \frac{-I_2}{I_1} = -(\frac{Y_1 + Y_2}{Y_2}), \text{ at } V_1 = 0 \tag{7.3.2}$$

An input current of $1mA$ with $R_1 = 5k$ and $R_2 = 5k$ was used for the simulation in the implementations of Figure 7.18.

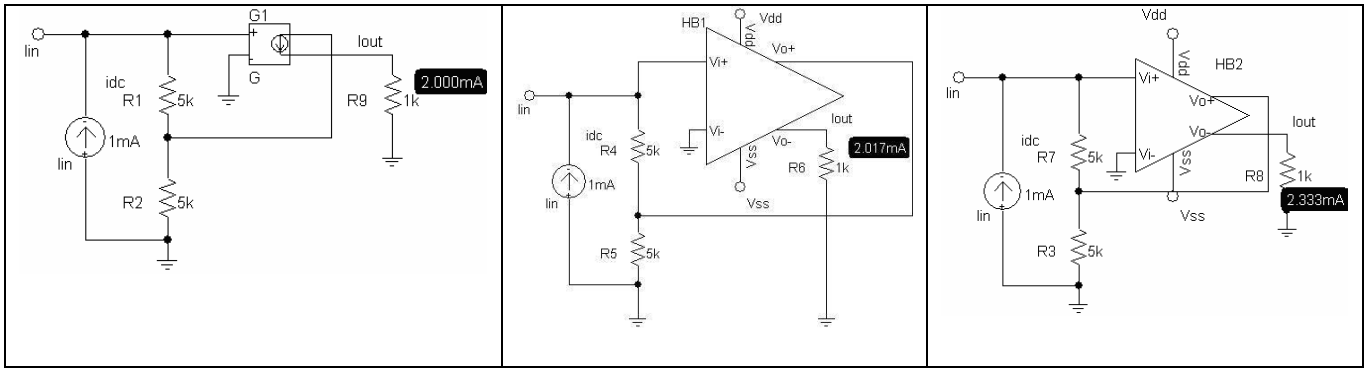


Figure 7.18 Current Amplifier based on FTFN

7.4 Simulation results with Improved Telescopic and Folded-Cascode FTFA

1. Inverse transfer function realization

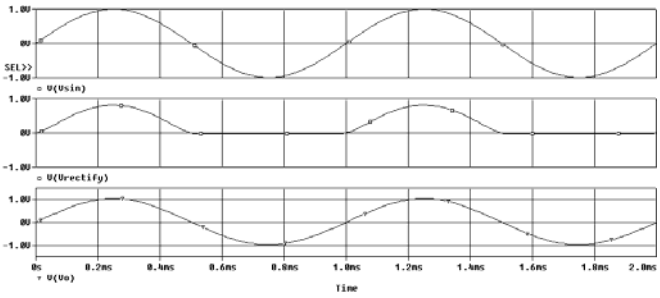


Figure 7.19 Inverse transfer realization using FTFA Telescopic

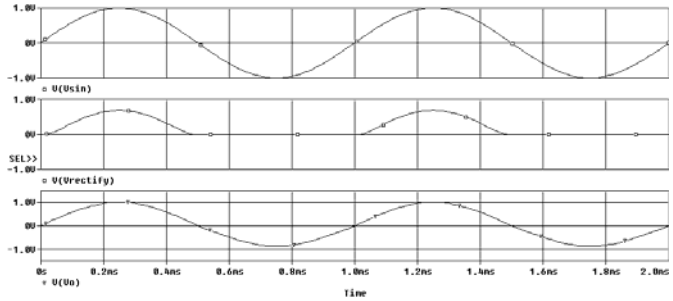


Figure 7.20 Inverse transfer realization using FTFA Folded-Cascode

2. Voltage-mode High-pass Sallen-Key Filter

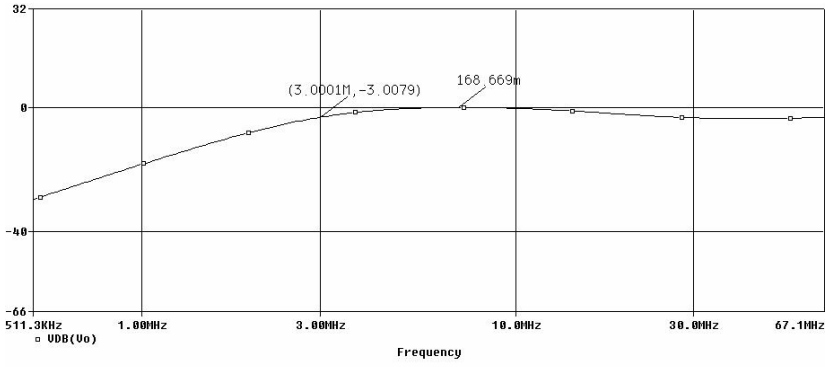


Figure 7.21 Voltage-mode High-pass Sallen-Key with Telescopic FTFA

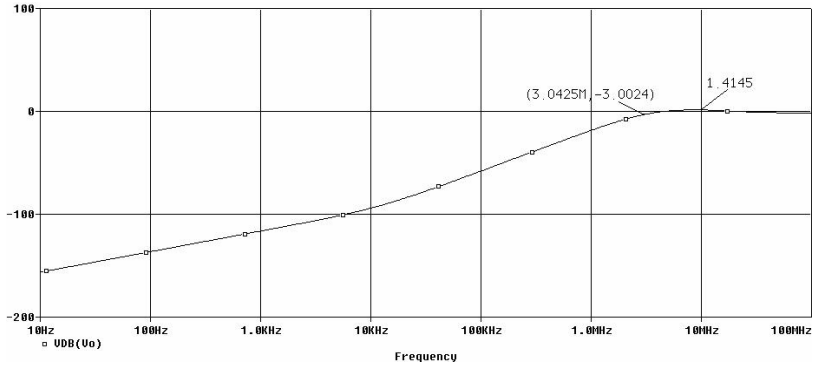


Figure 7.22 Voltage-mode High-pass Sallen-Key with Folded-Cascode FTFA

3. Current-mode High-pass Sallen-Key Filter

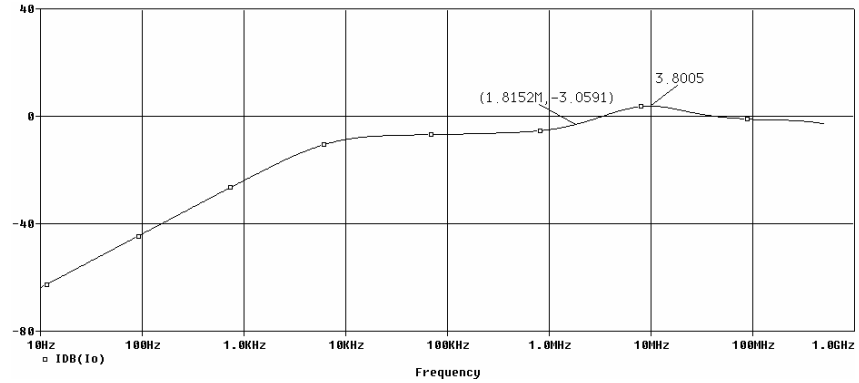


Figure 7.23 Current-mode High-pass Sallen-Key with Telescopic FTFA

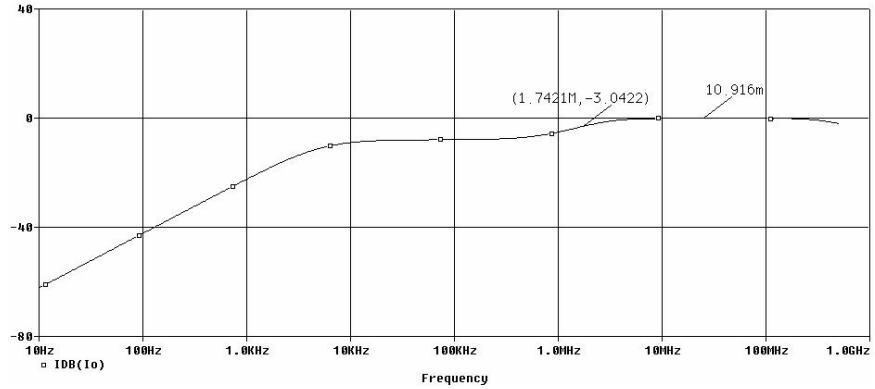


Figure 7.24 Current-mode High-pass Sallen-Key with Folded-Cascode FTFA

4. General Amplifiers

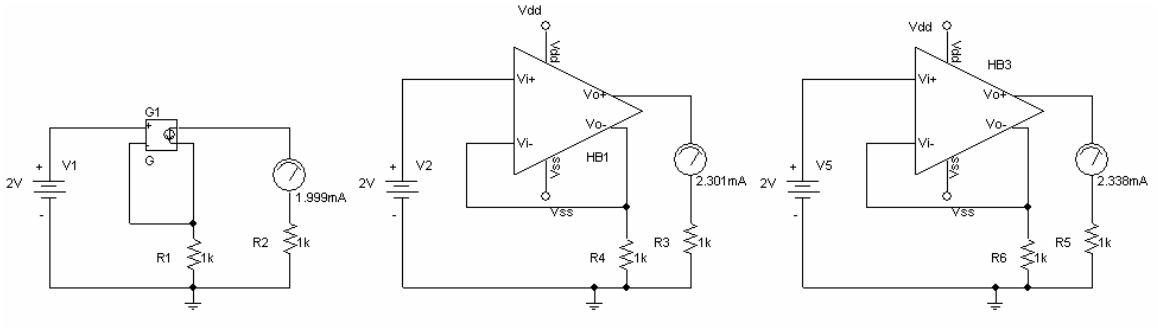


Figure 7.25 Voltage-to-current converter using a) Telescopic and b) Folded Cascode

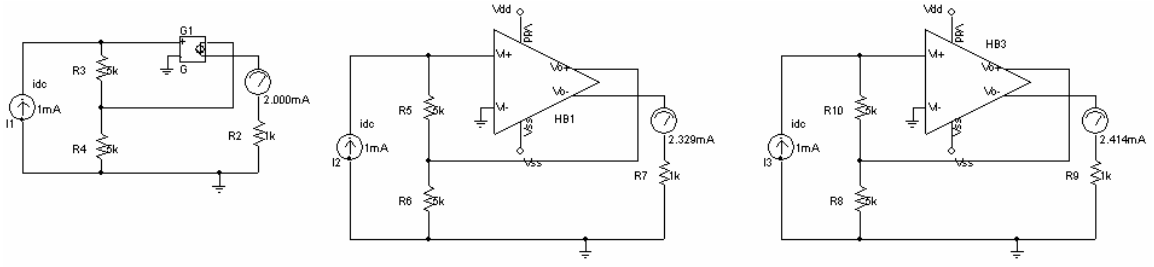


Figure 7.26 Current Amplifier with a) Telescopic and b) Folded-Cascode FTFA

Chapter 8 Conclusion

The use of FTFA for analysis and design circuits has been a valuable tool. That's one of the reasons for the emergence for a practical realization. This work presented a new approach to the design of a FTFA applying different techniques in other applications. The key parameters which guided the designs were open-loop gain, phase margin, unity-gain frequency and input-offset voltage.

Two implementations were proposed. The first one used a telescopic amplifier in combination with gain-enhanced negative conductance. The other implementation used a folded-cascode with a feedforward approach. The telescopic and folded-cascode were chosen as a departure because of the known increase in performance as previous circuits. Also, both of these implementations made use of common-mode feedback to guarantee proper operation.

The telescopic amplifier provided a higher gain and better frequency response. This is because the gain-enhancement technique does not introduce poles. Key parameters such as gain, phase margin and unity-gain frequency were at 115 db, 64º and 254 MHz, respectively. Also, acceptable values of input referred noise and offset voltages were obtained. These were $9.79\frac{nV}{\sqrt{Hz}}$ and $659.76\,\mu V$ respectively.

The Folded-cascode design approach was purposely designed also to obtain good high frequency operation. However, this design had a restriction; the output load at the input stage should be low to take advantage of such technique. This is reflected in the phase margin where a 58º was obtained. On the other hand, the folded-cascode didn't provide much advantage with input offset voltage, although it presented a high voltage

gain of 91 dB and good common-mode input range of $-1V \le V_{CMR} \le 1V$. These circuits prove to be good compared to recently implementations. Table 8.1 shows a comparison of key parameters of previous implementations against the two presented in this thesis.

Key parameter	U. Cam and H. Kuntman [22]	H. Alzaher and M. Ismail [23]	Folded Cascode FTFA	Telescopic FTFA
Open-loop gain	105 dB	75 dB	91 dB	115 dB
Phase Margin	71º	50º	58º	64º
Unity-gain	250 MHz	14 MHz	76 MHz	254 MHz
Input-offset voltage	1mV	N/A	6 mV	659 μV

Table 8.1 Key parameter comparison between previos implementations and proposed by this author

The proposed designs were simulated using Spice to verify the performance. These simulations were made using AMIC5N 0.6µ transistor level 49 models. Simulations on applications to validate the circuit design were presented. In particular, a nonlinear application proved versatility in the generation of inverse functions. Others, such as the current mode Sallen-Key High Pass filter were presented to demonstrating a key issue: single operational amplifiers and current conveyors can't be used as active devices in single active circuits.

Finally, some basic amplifiers were simulated resulting in neglible error percent compared to its ideal counterpart. This demonstrates that FTFA could be use as replacement of any type of the controlled sources previously presented in Chapter 2.

8.1 Future work

In addition to the work presented in this thesis, it is desired to complete the whole design process by implementing the proposed design in an integrated circuit. MOSIS, which allows circuit integration for educational purposes at no cost, is our choice for circuit implementation. Also, the chip will be tested using Texas Instruments VLCLT tester and testbenches using Labview.

Another proposed objective is the design of a family of FTFA. Also, low voltage versions of the FTFA should be designed with CMOS, but BiCMOS and bipolar implementations will be considered.

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Appendix "A" Linear System Theory

A.1 Linear System

Figure A.1 shows a symbolic representation of a system with input x(t) and output y(t).

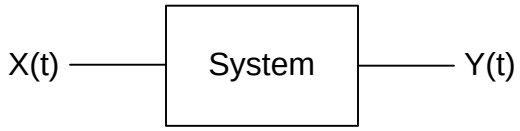

Figure A.1 General system representation

Let $y_1(t)$ be the output waveform for a specific input waveform $x_1(t)$, and $y_2(t)$ the output for an input $x_2(t)$. This is expressed as equation A.1.

$$x_1(t) \rightarrow y_1(t) \qquad \text{A.1}$$

$$x_2(t) \rightarrow y_2(t)$$

A system is said to be additive if, for all possible inputs $x_1(t)$ and $x_2(t)$ the corresponding input waveform $[x_1(t) + x_2(t)]$ results in the output $[y_1(t) + y_2(t)]$ [1]. This is expressed in equation A.2.

$$[x_1(t) + x_2(t)] \rightarrow [y_1(t) + y_2(t)] \qquad \text{A.2}$$

Equation A.2 is called additivity property of the system.

Another condition of interest for linear systems is the scalability or homogeneity property. The scaled input $\mathrm{k}\, x_1(t)$ has a corresponding scaled output [2]. That is,

$$\mathrm{k}\, x_1(t) \rightarrow \mathrm{k}\, y_1(t) \qquad \text{A.3}$$

A system is linear if it is additive and scalable. This is usually stated as follows: For the system of Figure. A.1, let $y_1(t)$ be the output waveform for a specific input waveform $x_1(t)$, and $y_2(t)$. the output for an input $x_2(t)$. Then the system is linear if and only if for any constants k_1 and k_2, the condition

$$[k_1 x_1(t) + k_2 x_2(t)] \rightarrow [k_1 y_1(t) + k_2 y_2(t)] \qquad \text{A.4}$$

The system is usually described mathematically by an equation, or an operator. If the system is linear, this should be reflected in the operator, and it is then said that the operator is linear. Conversely, if an operator satisfies A.4, then it is said to be linear, and the system in which the operator applies is also linear.

A.2. Linear Electrical elements and linear circuits

The linear resistor, capacitor and inductor are described by linear equations, or derivatives. For the capacitor and inductor, initial conditions are ignored. The respective equations are A.5, A.6 and A.7

$$v(t) = R\,i(t) \qquad \text{A.5}$$

$$i(t) = C\frac{dv(t)}{dt} \qquad \text{A.6}$$

$$v(t) = L\frac{di(t)}{dt} \qquad \text{A.7}$$

To verify the linearity characteristic of the resistor, we have

$$v(t) = R[k_1 i_1(t) + k_2 i_2(t)] = Rk_1 i_1(t) + Rk_2 i_2(t) = k_1 v_1(t) + k_2 v_2(t) \qquad \text{A.8}$$

With capacitors and inductors we can proceed similarly provided their initial condition is zero (for the integral expression). Other linear elements are linear dependent sources, coupled inductors, and so on. A circuit composed by linear elements can be described by a set of linear equations, or a set of linear differential equations, which when transformed by the Laplace Transform, itself a linear operator, yield a matrix equation of the form

$$Ax = b \qquad \text{A.9}$$

which describes a linear system $Ax = b$ [3].

The inclusion of nullators and norators does not alter the linearity property, since the corresponding equations for each pair do not affect the linearity of the system of equations.

A.3 AC linearity

A.3.1 AC device characteristic

Linearity is the behavior of a circuit, particularly an amplifier, in which the output signal amplitude varies in direct proportion to the input signal amplitude. When an amplifier's input level increases by a certain percentage, its output level must increase by the same percentage, otherwise distortion is produced, that is, it is expected that the output-to-input signal amplitude ratio remains always the same [1].

In an amplifier exhibiting linearity, the output-versus-input signal amplitude graph appears as a straight line. Two examples are shown below. The gain defines the slope of the line. The amplifier depicted by the line A has more gain than the one depicted by the line B. Both amplifiers are linear within the input-signal range shown, because both lines in the graph are straight.

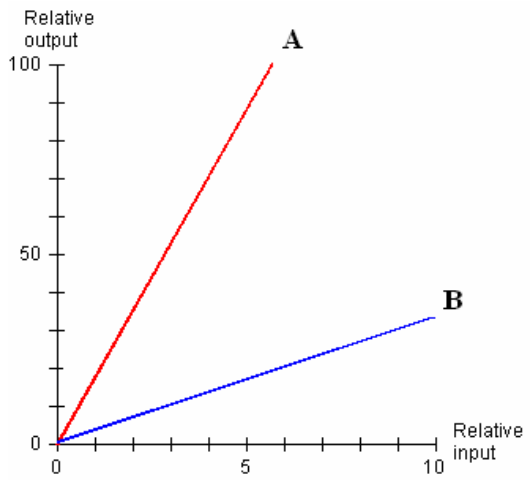

Figure A.2 Example of linearity

The deviation from a straight-line can be represented by a power series as shown below [3]:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \qquad \text{A.10}$$

Thus, for a sufficient small range of $x(t)$, equation A.10 may be approximated by $y(t) \approx \alpha_0 + \alpha_1 x(t)$ where α_0 and α_1 are the operating (quiescent) point and the small signal gain respectively. All higher terms are neglected to approximate a linear transfer.

When a single carrier $x(t) = A\cos\omega t$ input signal is substituted into the above expression, the output waveform will contain the original carrier and harmonic distortion products [2] in the form

$$y(t) \approx B_0 + B_1\cos\omega t + B_2\cos 2\omega t + B_3\cos 3\omega t + \ldots\ldots \qquad \text{A.11}$$

Thus, linearity is achieved if the higher order terms are neglected This is, possible for a sufficiently small input range of signal x(t).

Figure A.3 shows the transfer characteristic of a general amplifier [4]. Within a small or linear range the output signal is an amplified replica of the input (1). On the other hand, for larger input range, a distorted output results (2).

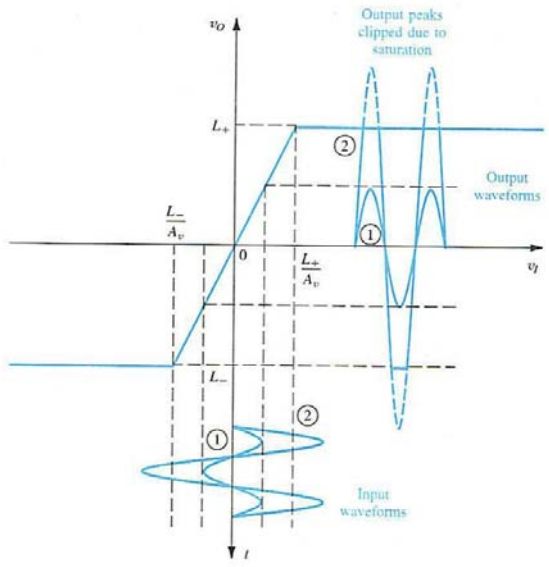

Figure A.3 Amplifier characteristic showing linear and nonlinear regions of operation (Reproduced from [4])

Thus, for a given gain A_V, the small-signal range is bounded to,

$$\frac{V_-}{A_V} \le V_I \le \frac{V_+}{A_V} \qquad \text{A.12}$$

Where V^- and V^+ are the negative and positive supply voltages respectively.

For a specific small range of operation, the small signal characteristic is typically obtained in two ways [5]:

1. Replacing all devices and elements with a linear small signal equivalent circuit in which the parameters in the small signal models are a function of the Q-point.
2. Directly upon the DC transfer characteristic using equation A.13,

$$\frac{x_o}{x_i} = \frac{\partial X_o}{\partial X_i} \qquad \text{A.13}$$

where x_i, x_o, X_i, X_o are the input and output small signal variables and input and output large signal variables respectively. However, there are some distinct advantages offered by obtaining the small signal transfer characteristic directly from the small signal model [5]. First, the analysis of the small signal circuit is linear and is typically less tedious than the dc. Second, more accuracy results with a direct small signal analysis.

A straightforward way to calculate the small signal characteristic is by using two-port analysis. Figure A.4 shows a two-port network with its corresponding small-signal input and output variables.

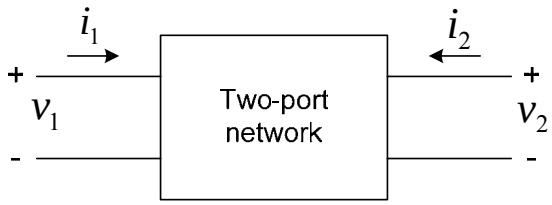

Figure A.4 Two-port network

Such network is described by two equations. The electrical behavior of linear two-port networks can be modeled in terms of one or more set of transfer function parameters such as h parameters, y parameters or g parameters. Using the admittance-parameters equations, the amplifier is described by [6],

$$i_1 = y_{11}v_1 + y_{12}v_2$$
$$i_2 = y_{21}v_1 + y_{22}v_2 \qquad \text{A.14}$$

where

$$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = \textit{Input admittance with the output short} - \textit{circuited}$$

$$y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} = \text{Re}\,\textit{verse transconductance with the input short} - \textit{circuited}$$

$$y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0} = \textit{Forward transconductance with the output short} - \textit{circuited}$$

$$y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} = \textit{Output admittance with the input short} - \textit{circuited}$$

To provide another view on linearity, a commonly known metric known as dynamic range is used. Most basically defined as the ratio of the maximum signal strength a circuit can handle to minimum input level at which it can generate an intelligible output [7] as shown in equation A.15 [8][9],

$$DR = \frac{\alpha_1 V_{IN}}{V_{NOUT}} = \frac{V_{IN}}{V_{NIN}} \qquad \text{A.15}$$

where V_{NIN} and V_{NOUT} are the input and output noise voltages (in RMS) respectively. Also, it can be expressed in decibel as:

$$DR_{dB} = V_{IN(dB)} - V_{NIN(dB)} \qquad \text{A.16}$$

Reference:

[A.1] Whatis.com Target Search, http://whatis.techtarget.com/definition/0,,sid9_gci529971,00.html

[A.2] A. Katz, R. Dorval, J. Dragoner "Ka-Band linearization", available at http://www.mpdigest.com/Articles/2004/Jan2004/Linearizer/Default.htm, Jan 2004.

[A.3] W. Sansen, "Distortion in Elementary Transistor Circuits", IEEE Trans. on Circuit and Systems II, vol. 46, No. 3, Mar 1996, pp.315-317.

[A.4] A.S. Sedra and K.C. Smith, Microelectronic Circuits, Oxford University Press, NY, 1998, p. 15.

[A.5] R.L. Geiger, P.E. Allen, N.R. Starder, VLSI Design techniques for analog and digital circuits, New York: McGraw Hill, 1990.

[A.6] P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, NY, 4^{th} ed., 2001, pp. 172-173.

[A.7] EE Times Online, Ultrawideband Technology Glossary available at www.eetimes.com/reshaping/wireless/OEG20020912S0034

[A.8] W. Sansen, "Distortion in Elementary Transistor Circuits", IEEE Trans. on Circuit and Systems II, vol. 46, No. 3, Mar 1996, pp.315-317.

[A.9] J. H. Huijsing, Operational Amplifiers: Theory and Design, Kluwer Academic Publishers, Boston, 2001, pp. 56-57.

Appendix "B": Nonlinearity

B.1 Nonlinearity general considerations

As stated in appendix A.3, electronic elements are non linear, affecting the performance of linear analog circuits. Of importance therefore, is the nonlinearity of the input/output characteristic of an amplifier. To gain insight of this phenomenon, the input/output characteristic is approximated by a power series expansion [1] as expressed in equation B.1.1.

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \qquad \text{B.1}$$

For a specific small range of $x(t)$, equation B.1 can be approximated as $y(t) \approx \alpha_0 + \alpha_1 x(t)$ where α_0 and α_1 are the operating (quiescent) point and the small signal gain respectively.

There are two ways to quantify the nonlinearity [2].

1. Identifying $\alpha_1, \alpha_2, \alpha_3, etc.$
2. Specifying the maximum deviation of the characteristic from an ideal one (a straight line).

However, a common, and usually more practical way to characterize the nonlinearity of a circuit is by measuring the harmonic content of the output when a sinusoid input is applied [1][2]. Letting $x(t) = A\cos(wt)$, equation B.1 becomes:

$$y(t) = \alpha_0 + \alpha_1 A\cos(wt) + \alpha_2 A^2 \cos^2(wt) + \alpha_3 A^3 \cos^3(wt) + \ldots \qquad \text{B.2}$$

Grouping odd and even terms and using trigonometric identities, equation B.2 is rewritten as:

$$y(t) = (\alpha_0 + \frac{\alpha_2}{2} A^2) + (\alpha_1 + \frac{3}{4}\alpha_3 A^2) A\cos(wt) + \frac{\alpha_2}{2} A^2 \cos(2wt) + \frac{\alpha_3}{4} A^3 \cos(3wt) + \ldots \quad \text{B.1.3}$$

$$y(t) = B_o + B_1 \cos(wt) + B_2 \cos(2wt) + B_3 \cos(3wt) + \ldots \quad \text{B1.4}$$

It is apparent that the harmonic content, that is, the presence of components of frequency *nw*, at the output increases with higher-order terms. Such effect is called harmonic distortion. It may be quantified by individual components, called n-th order harmonic distortion, or by summing the power of all the harmonics (excluding that of the fundamental) and normalizing the result to the power of the fundamental [2], a measurement called Total Harmonic Distortion.

The n-th order harmonic distortion H_n is defined as

$$HD_n = \left| \frac{B_n}{B_1} \right| \quad n > 1 \quad \text{B.1.5}$$

Thus, the second-order harmonic distortion yields,

$$HD_2 = \frac{1}{2} \frac{\alpha_2}{\alpha_1} A \quad \text{B.1.6}$$

In general, in measurements, Total Harmonic Distortion (THD) is defined as:

$$THD = \sqrt{HD_2^{\,2} + HD_3^{\,2} + \ldots} \quad \text{B.1.7}$$

Related measurements such as dynamic range has proved useful in quantifying distortion.

References

[B.1] W. Sansen, “Distortion in Elementary Transistor Circuits”, IEEE Trans. on Circuit and Systems II, vol. 46, No. 3, Mar 1996, pp.315-317.

[B.2] B. Razavi, Design of CMOS Integrated Circuits, Mc Graw-Hill, New York, NY, 2001, pp. 450-452.

[B.3] J. H. Huijsing, Operational Amplifiers: Theory and Design, Kluwer Academic Publishers, Boston, 2001, pp. 56-57.

Appendix "C": Noise

C. Input referred noise calculation

A limiting factor of the performance in analog circuits is electrical noise. It is defined as an unwanted voltage or current signal in electrical circuits. One way to measure noise is shown in figure C.1.

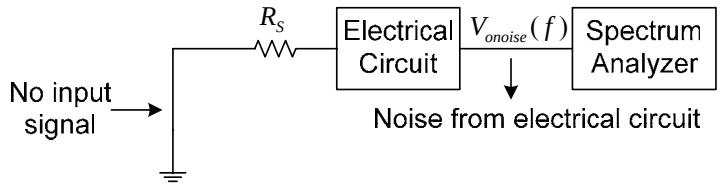

Figure C.1 Circuit setup for noise measurement

It is seen from figure C.1 that noise is measured at the output. However, the output referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain [1]. Instead, the noise voltage is referred to the input, defined as input referred noise. The idea is to combine all noise sources in the circuit in an equivalent voltage source $\overline{V_{n,in}^{\,2}}$ such that the output yield,

$$\overline{V_{n,out}^{\,2}} = A_v^{\,2}\overline{V_{n,in}^{\,2}} \qquad \text{C.1.1}$$

where $\overline{V_{n,in}^{\,2}}$ and $\overline{V_{n,out}^{\,2}}$ are the input and output referred noise voltages. Figure C.2 shows a general block diagram of the input referred noise representation [2].

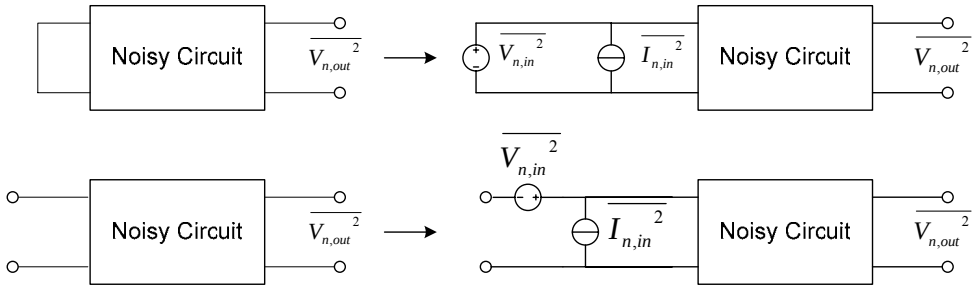

Figure C.2 Equivalent diagrams for voltage and current input-referred noise

References

[C.1] B. Razavi, Design of CMOS Integrated Circuits, Mc Graw-Hill, New York, NY, 2001, pp. 219-221.

[C.2] R.J. Baker, CMOS: Circuit Design, Layout, and Simulation, John Wiley and Sons Inc., Wiley Interscience, 2005, pp. 220,232.

Appendix "D" FTFA Telescopic and Folded-Cascode transistor sizes

Transistor ratios for Telescopic FTFA #1

Input Stage	Width (μm)	Length (μm)
$M_1,\ M_2$	80	1.95
M_3, M_4	17	1.95
M_5, M_6	18	1.95
M_7, M_8, M_{23}, M_{24}	40	1.95
M_{22}	12	1.95
$M_9, M_{10}, M_{25}, M_{26}$	10	1.95
$M_{11A}, M_{12A}, M_{27}, M_{28}$	20*(2)	1.95
$M_{13A}, M_{14A}, M_{29}, M_{30}$	3*(5)	1.95

Bias Circuit	Width (μm)	Length (μm)
M_{1A}, M_{3A}	10*(4)	1.95
M_{4A}	15*(2)	1.95
M_{5A}	12	1.95
M_{6A}	10*(10)	1.95
M_{7A}	10	1.95
M_{9A}	5	1.95
$M_{15A}, M_{31}, M_{32}, M_{33}$	10*(4)	1.95

Common-mode feedback	Width (μm)	Length (μm)
$M_{16}, M_{17}, M_{18}, M_{19}$	150	1.95
M_{20}	4	1.95
M_{21}	4	1.95

Output Stage	Width (μm)	Length (μm)
$M_{97}, M_{93}, M_{98}, M_{99}$	3	1.05
M_{94}, M_{96}	296	1.95
M_{90}, M_{95}	152	1.95
M_{88}, M_{89}	33	1.95
MSTB	12	1.95

Table D.1 Transistor sizes for Telescopic FTFA of figure 4.15

Transistor ratios for Telescopic FTFA #2 with CCMFB

Input Stage	Width (μm)	Length (μm)
$M_1,\ M_2$	80	1.95
M_3, M_4	50	1.95
M_5, M_6	30	1.95
M_7, M_8, M_{23}, M_{24}	40	1.95
M_{22}	11	1.95
$M_9, M_{10}, M_{25}, M_{26}$	5*(2)	1.95
$M_{11A}, M_{12A}, M_{27}, M_{28}$	9*(5)	1.95
$M_{13A}, M_{14A}, M_{29}, M_{30}$	10*(5)	1.95

Bias Circuit	Width (μm)	Length (μm)
M_{1A}, M_{3A}	10*(4)	1.95
M_{4A}	15*(2)	1.95
M_{5A}	11	1.95
M_{6A}	10*(10)	1.95
M_{7A}	10	1.95
M_{9A}	5	1.95
$M_{15A}, M_{31}, M_{32}, M_{33}$	10*(4)	1.95

Common-mode feedback #1	Width (μm)	Length (μm)
$M_{16}, M_{17}, M_{18}, M_{19}$	100	1.95
M_{20}	3	1.95
M_{21}	5	1.95

Output Stage	Width (μm)	Length (μm)
$M_{97}, M_{93}, M_{98}, M_{99}$	20	1.05
M_{94}, M_{96}	322	1.95
M_{90}, M_{95}	278	1.95
M_{88}, M_{89}	25	1.95
M_{93}	20	1.95
M_{91}, M_{100}	5*(24)	1.95
M_{92}, M_{101}	20	1.95

Common-mode feedback #2	Width (μm)	Length (μm)
$M_{104}, M_{105}, M_{106}, M_{107}$	100	1.95
M_{102}, M_{103}	5*(4)	1.95
M_{108}	10	1.95
M_{109}	10*(10)	1.95

Common-mode feedback #3	Width (μm)	Length (μm)
$M_{114}, M_{115}, M_{116}, M_{117}$	50	1.95
M_{112}, M_{113}	6*(2)	1.95
M_{110}	15	1.95
M_{111}	5	1.95

Table D.2 Transistor sizes for Telescopic FTFA of figure 8.3

Transistor ratios for Folded-Cascode FTFA #1

Input Stage	Width (μm)	Length (μm)
M_1, M_2	80	1.95
M_3, M_4	10*(4)	1.95
M_5, M_6	80	1.95
M_7, M_8	10*(2)	1.95
M_{11}, M_{12}	50	0.90
M_9, M_{10}	18	1.95
M_{13}, M_{14}	12	1.95
M_{16}	12	1.95

Bias Circuit	Width (μm)	Length (μm)
M_{15}, M_{22}	10*(4)	1.95
M_{17}	15*(2)	1.95
M_{18}	12	1.95
M_{19}	100	1.95
M_{20}	10	1.95
M_{21}	5	1.95

Common-mode feedback #1	Width (μm)	Length (μm)
$M_{23}, M_{24}, M_{25}, M_{26}$	70	1.95
M_{27}, M_{28}	10*(4)	1.95
M_{29}	12	1.95
M_{30}	4	1.95

Output Stage	Width (μm)	Length (μm)
$M_{34}, M_{35}, M_{39}, M_{40}$	10	1.05
M_{36}, M_{42}	349	1.95
M_{37}, M_{40}	260	1.95
M_{31}	29	1.95
M_{32}	18	1.95
M_{38}, M_{41}	16	1.95

Common-mode feedback #2	Width (μm)	Length (μm)
$M_{45}, M_{46}, M_{47}, M_{48}$	101	1.95
M_{44}, M_{50}	10*(4)	1.95
M_{47}	12	1.95
M_{51}	4	1.95

Table D.3 Transistor sizes for Folded-Cascode FTFA of figure 4.19

Transistor ratios for Folded-Cascode FTFA #2 CCMFB

Input Stage	Width (μm)	Length (μm)
M_1, M_2	80	1.95
M_3, M_4	10*(4)	1.95
M_5, M_6	80	1.95
M_7, M_8	10*(2)	1.95
M_{11}, M_{12}	50	0.90
M_9, M_{10}	18	1.95
M_{13}, M_{14}	12	1.95
M_{16}	12	1.95

Bias Circuit	Width (μm)	Length (μm)
M_{1A}, M_{3A}	10*(4)	1.95
M_{4A}	15*(2)	1.95
M_{5A}	12	1.95
M_{6A}	100	1.95
M_{7A}	10	1.95
M_{9A}	5	1.95
Common-mode feedback #1	Width (μm)	Length (μm)
$M_{23}, M_{24}, M_{25}, M_{26}$	70*(2)	1.95
M_{27}, M_{28}	10*(4)	1.95
M_{29}	12	1.95
M_{30}	4	1.95
Output Stage	Width (μm)	Length (μm)
$M_{34}, M_{35}, M_{39}, M_{40}$	10	1.05
M_{36}, M_{42}	330	1.95
M_{37}, M_{40}	260	1.95
M_{31}	29	1.95
M_{32}	12	1.95
M_{38}, M_{41}	10*(2)	1.95
M_{61}, M_{52}	25	1.95
MSTB	12*(2)	1.95
Common-mode feedback #2	Width (μm)	Length (μm)
$M_{45}, M_{46}, M_{47}, M_{48}$	100	1.95
M_{44}, M_{50}	9*(2)	1.95
M_{47}	18	1.95
M_{51}	4	1.95
Common-mode feedback #3	Width (μm)	Length (μm)
$M_{56}, M_{57}, M_{58}, M_{59}$	60	1.95
M_{57}, M_{58}	12*(2)	1.95
M_{59}	8*(2)	1.95
M_{60}	20	1.95

Table D.4 Transistor sizes for Folded-Cascode FTFA of figure 8.4

Appendix E. AMI 0.5 C5N transistor models

```
.MODEL AMI06N-Typ NMOS (                                LEVEL   = 7
+VERSION = 3.1           TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = 0.6696061
+K1      = 0.8351612     K2      = -0.0839158    K3      = 23.1023856
+K3B     = -7.6841108    W0      = 1E-8          NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 2.9047241     DVT1    = 0.4302695     DVT2    = -0.134857
+U0      = 458.439679    UA      = 1E-13         UB      = 1.485499E-
18
+UC      = 1.629939E-11  VSAT    = 1.643993E5    A0      = 0.6103537
+AGS     = 0.1194608     B0      = 2.674756E-6   B1      = 5E-6
+KETA    = -2.640681E-3  A1      = 8.219585E-5   A2      = 0.3564792
+RDSW    = 1.387108E3    PRWG    = 0.0299916     PRWB    = 0.0363981
+WR      = 1             WINT    = 2.472348E-7   LINT    = 3.597605E-
8
+XL      = 0             XW      = 0             DWG     = -
1.287163E-8
+DWB     = 5.306586E-8   VOFF    = 0             NFACTOR = 0.8365585
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0246738     ETAB    = -
1.406123E-3
+DSUB    = 0.2543458     PCLM    = 2.5945188     PDIBLC1 = -0.4282336
+PDIBLC2 = 2.311743E-3   PDIBLCB = -0.0272914    DROUT   = 0.7283566
+PSCBE1  = 5.598623E8    PSCBE2  = 5.461645E-5   PVAG    = 0
+DELTA   = 0.01          RSH     = 81.8          MOBMOD  = 1
+PRT     = 8.621         UTE     = -1            KT1     = -0.2501
+KT1L    = -2.58E-9      KT2     = 0             UA1     = 5.4E-10
+UB1     = -4.8E-19      UC1     = -7.5E-11      AT      = 1E5
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2E-10         CGSO    = 2E-10         CGBO    = 1E-9
+CJ      = 4.197772E-4   PB      = 0.99          MJ      = 0.4515044
+CJSW    = 3.242724E-10  PBSW    = 0.1           MJSW    = 0.1153991
+CJSWG   = 1.64E-10      PBSWG   = 0.1           MJSWG   = 0.1153991
+CF      = 0             PVTH0   = 0.0585501     PRDSW   = 133.285505
+PK2     = -0.0299638    WKETA   = -0.0248758    LKETA   = 1.173187E-
3
+AF      = 1             KF      = 0)
```

```
.MODEL AMI06P-Typ PMOS (                                LEVEL   = 7
+VERSION = 3.1            TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.9214347
+K1      = 0.5553722      K2      = 8.763328E-3    K3      = 6.3063558
+K3B     = -0.6487362     W0      = 1.280703E-8    NLX     = 2.593997E-
8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.5131165      DVT1    = 0.5480536      DVT2    = -0.1186489
+U0      = 212.0166131    UA      = 2.807115E-9    UB      = 1E-21
+UC      = -5.82128E-11   VSAT    = 1.713601E5     A0      = 0.8430019
+AGS     = 0.1328608      B0      = 7.117912E-7    B1      = 5E-6
+KETA    = -3.674859E-3   A1      = 4.77502E-5     A2      = 0.3
+RDSW    = 2.837206E3     PRWG    = -0.0363908     PRWB    = -
1.016722E-5
+WR      = 1              WINT    = 2.838038E-7    LINT    = 5.528807E-
8
+XL      = 0              XW      = 0              DWG     = -
1.606385E-8
+DWB     = 2.266386E-8    VOFF    = -0.0558512     NFACTOR = 0.9342488
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.3251882      ETAB    = -0.0580325
+DSUB    = 1              PCLM    = 2.2409567      PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3    PDIBLCB = -0.0551797     DROUT   = 0.2036901
+PSCBE1  = 6.44809E9      PSCBE2  = 6.300848E-10   PVAG    = 0
+DELTA   = 0.01           RSH     = 101.6          MOBMOD  = 1
+PRT     = 59.494         UTE     = -1             KT1     = -0.2942
+KT1L    = 1.68E-9        KT2     = 0              UA1     = 4.5E-9
+UB1     = -6.3E-18       UC1     = -1E-10         AT      = 1E3
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.9E-10        CGSO    = 2.9E-10        CGBO    = 1E-9
+CJ      = 7.235528E-4    PB      = 0.9527355      MJ      = 0.4955293
+CJSW    = 2.692786E-10   PBSW    = 0.99           MJSW    = 0.2958392
+CJSWG   = 6.4E-11        PBSWG   = 0.99           MJSWG   = 0.2958392
+CF      = 0              PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 5.292165E-3    LKETA   = -
4.205905E-3
+AF      = 1              KF      = 0)
```

```
.MODEL AMI06N-SS NMOS (                                LEVEL   = 7
+VERSION = 3.1           TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = 0.7087481
+K1      = 0.9382905     K2      = -0.1120562    K3      = 23.0789213
+K3B     = -7.3398981    W0      = 1E-8          NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 3.3388333     DVT1    = 0.4283914     DVT2    = -0.0952143
+U0      = 459.674806    UA      = 1E-13         UB      = 1.503507E-
18
+UC      = 1.325863E-11  VSAT    = 1.682969E5    A0      = 0.4784067
+AGS     = 0.0995613     B0      = 2.644452E-6   B1      = 5E-6
+KETA    = -5.808373E-3  A1      = 1.027068E-4   A2      = 0.3400289
+RDSW    = 1.329687E3    PRWG    = 0.0432392     PRWB    = 0.0149808
+WR      = 1             WINT    = 2.420178E-7   LINT    = 3.239617E-
8
+XL      = 0             XW      = 0             DWG     = -
1.396728E-8
+DWB     = 5.6316E-8     VOFF    = -2.57933E-3   NFACTOR = 0.8759425
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0152264     ETAB    = -
1.058244E-3
+DSUB    = 0.2005917     PCLM    = 2.6613926     PDIBLC1 = -0.7606454
+PDIBLC2 = 2.593415E-3   PDIBLCB = -0.0326937    DROUT   = 0.6688818
+PSCBE1  = 5.85807E8     PSCBE2  = 7.988657E-5   PVAG    = 0
+DELTA   = 0.01          RSH     = 81.9          MOBMOD  = 1
+PRT     = 8.621         UTE     = -1            KT1     = -0.2501
+KT1L    = -2.58E-9      KT2     = 0             UA1     = 5.4E-10
+UB1     = -4.8E-19      UC1     = -7.5E-11      AT      = 1E5
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.02E-10      CGSO    = 2.02E-10      CGBO    = 1E-9
+CJ      = 4.198358E-4   PB      = 0.99          MJ      = 0.4516115
+CJSW    = 3.241716E-10  PBSW    = 0.1000811     MJSW    = 0.1152935
+CJSWG   = 1.64E-10      PBSWG   = 0.1000811     MJSWG   = 0.1152935
+CF      = 0             PVTH0   = 0.0681426     PRDSW   =
188.2442761
+PK2     = -0.0295712    WKETA   = -0.0264969    LKETA   = -
2.950307E-5
+AF      = 1             KF      = 0)
*$
```

```
.MODEL AMI06P-SS PMOS (                                LEVEL   = 7
+VERSION = 3.1            TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.9223355
+K1      = 0.5769702      K2      = 9.039555E-3    K3      = 6.34861
+K3B     = -0.6383676     W0      = 1E-8           NLX     = 4.747861E-
8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.4578035      DVT1    = 0.576459       DVT2    = -0.1206691
+U0      = 211.8308394    UA      = 2.824327E-9    UB      = 1E-21
+UC      = -5.66493E-11   VSAT    = 1.622935E5     A0      = 0.8712138
+AGS     = 0.1383793      B0      = 7.726776E-7    B1      = 5E-6
+KETA    = -5.205201E-3   A1      = 2.378013E-5    A2      = 0.3
+RDSW    = 3E3            PRWG    = -0.0454944     PRWB    = -2.13823E-
4
+WR      = 1              WINT    = 2.849786E-7    LINT    = 5.529217E-
8
+XL      = 0              XW      = 0              DWG     = -
1.840088E-8
+DWB     = 2.185555E-8    VOFF    = -0.0684347     NFACTOR = 0.9119466
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.3751245      ETAB    = -0.0827039
+DSUB    = 1              PCLM    = 2.2966371      PDIBLC1 = 0.0365228
+PDIBLC2 = 3.733251E-3    PDIBLCB = -0.0621219     DROUT   = 0.2123397
+PSCBE1  = 7.499863E9     PSCBE2  = 7.328296E-10   PVAG    = 4.584372E-
6
+DELTA   = 0.01           RSH     = 101.9          MOBMOD  = 1
+PRT     = 59.494         UTE     = -1             KT1     = -0.2942
+KT1L    = 1.68E-9        KT2     = 0              UA1     = 4.5E-9
+UB1     = -6.3E-18       UC1     = -1E-10         AT      = 1E3
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.84E-10       CGSO    = 2.84E-10       CGBO    = 1E-9
+CJ      = 7.235521E-4    PB      = 0.9527404      MJ      = 0.4955303
+CJSW    = 2.692736E-10   PBSW    = 0.99           MJSW    = 0.295843
+CJSWG   = 6.4E-11        PBSWG   = 0.99           MJSWG   = 0.295843
+CF      = 0              PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 4.75772E-3     LKETA   = -
6.715425E-3
+AF      = 1              KF      = 0)
*$
```

```
.MODEL AMI06N-SF NMOS (                                LEVEL   = 7
+VERSION = 3.1           TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = 0.7149035
+K1      = 0.9483936     K2      = -0.1143426    K3      = 22.9362167
+K3B     = -7.5062363    W0      = 1E-8          NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 3.3919449     DVT1    = 0.4489453     DVT2    = -0.1041249
+U0      = 457.716722    UA      = 1E-13         UB      = 1.372758E-
18
+UC      = 9.187767E-12  VSAT    = 1.587379E5    A0      = 0.4423616
+AGS     = 0.074408      B0      = 2.495758E-6   B1      = 5E-6
+KETA    = -7.852725E-3  A1      = 0             A2      = 0.3722219
+RDSW    = 1.37701E3     PRWG    = 0.0473261     PRWB    = 0.0143246
+WR      = 1             WINT    = 2.276625E-7   LINT    = 3.643153E-
8
+XL      = 0             XW      = 0             DWG     = -
8.492651E-9
+DWB     = 5.745769E-8   VOFF    = -1.122941E-3  NFACTOR = 0.9488846
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0194621     ETAB    = -
1.316507E-3
+DSUB    = 0.2373912     PCLM    = 2.609637      PDIBLC1 = -0.2869359
+PDIBLC2 = 2.596336E-3   PDIBLCB = -9.96922E-3   DROUT   = 0.6175652
+PSCBE1  = 5.8967E8      PSCBE2  = 8.951955E-5   PVAG    = 0
+DELTA   = 0.01          RSH     = 81.7          MOBMOD  = 1
+PRT     = 8.621         UTE     = -1            KT1     = -0.2501
+KT1L    = -2.58E-9      KT2     = 0             UA1     = 5.4E-10
+UB1     = -4.8E-19      UC1     = -7.5E-11      AT      = 1E5
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.03E-10      CGSO    = 2.03E-10      CGBO    = 1E-9
+CJ      = 4.198358E-4   PB      = 0.99          MJ      = 0.4516115
+CJSW    = 3.241716E-10  PBSW    = 0.1000811     MJSW    = 0.1152935
+CJSWG   = 1.64E-10      PBSWG   = 0.1000811     MJSWG   = 0.1152935
+CF      = 0             PVTH0   = 0.0690695     PRDSW   =
181.3444668
+PK2     = -0.0304429    WKETA   = 0.0420944     LKETA   = -
3.044755E-3
+AF      = 1             KF      = 0)
```

```
.MODEL AMI06P-SF PMOS (                                LEVEL   = 7
+VERSION = 3.1           TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = -0.8558405
+K1      = 0.5644444     K2      = 6.387376E-3   K3      = 6.0462612
+K3B     = -0.5998096    W0      = 1E-8          NLX     = 3.340021E-
8
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 2.4979627     DVT1    = 0.5476217     DVT2    = -0.1143472
+U0      = 211.0603347   UA      = 2.770099E-9   UB      = 1.044234E-
21
+UC      = -5.9315E-11   VSAT    = 1.779657E5    A0      = 1.1297757
+AGS     = 0.172519      B0      = 6.127953E-7   B1      = 5E-6
+KETA    = -1.991554E-3  A1      = 0             A2      = 0.3
+RDSW    = 3E3           PRWG    = -0.0477698    PRWB    = -
1.197112E-4
+WR      = 1             WINT    = 2.778374E-7   LINT    = 5.81705E-8
+XL      = 0             XW      = 0             DWG     = -
1.563705E-8
+DWB     = 2.218513E-8   VOFF    = -0.0660365    NFACTOR = 0.9061795
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.1521419     ETAB    = -0.0473117
+DSUB    = 1             PCLM    = 2.3170883     PDIBLC1 = 0.0640318
+PDIBLC2 = 4.224165E-3   PDIBLCB = -0.0417139    DROUT   = 0.2703555
+PSCBE1  = 5.427801E9    PSCBE2  = 5.303858E-10  PVAG    = 0
+DELTA   = 0.01          RSH     = 102.2         MOBMOD  = 1
+PRT     = 59.494        UTE     = -1            KT1     = -0.2942
+KT1L    = 1.68E-9       KT2     = 0             UA1     = 4.5E-9
+UB1     = -6.3E-18      UC1     = -1E-10        AT      = 1E3
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.64E-10      CGSO    = 2.64E-10      CGBO    = 1E-9
+CJ      = 7.235521E-4   PB      = 0.9527404     MJ      = 0.4955303
+CJSW    = 2.692736E-10  PBSW    = 0.99          MJSW    = 0.295843
+CJSWG   = 6.4E-11       PBSWG   = 0.99          MJSWG   = 0.295843
+CF      = 0             PVTH0   = 5.98016E-3    PRDSW   = 14.8598424
+PK2     = 3.73981E-3    WKETA   = 3.730632E-3   LKETA   = -
4.016397E-3
+AF      = 1             KF      = 0)
*
```

```
.MODEL AMI06N-FS NMOS (                                LEVEL   = 7
+VERSION = 3.1           TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = 0.6406873
+K1      = 0.8993265     K2      = -0.1056377    K3      = 21.3163919
+K3B     = -7.1608652    W0      = 1E-8          NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 3.5203013     DVT1    = 0.4082348     DVT2    = -0.0884394
+U0      = 459.8817656   UA      = 1E-13         UB      = 1.519768E-
18
+UC      = 1.390305E-11  VSAT    = 1.618085E5    A0      = 0.6561988
+AGS     = 0.1483929     B0      = 2.633747E-6   B1      = 5E-6
+KETA    = 1.06352E-3    A1      = 7.568286E-5   A2      = 0.3677153
+RDSW    = 1.235008E3    PRWG    = 0.0513137     PRWB    = 0.0510984
+WR      = 1             WINT    = 2.396297E-7   LINT    = 3.585449E-
8
+XL      = 0             XW      = 0             DWG     = -
1.245253E-8
+DWB     = 5.532278E-8   VOFF    = 0             NFACTOR = 0.6559298
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0330898     ETAB    = -
1.406156E-3
+DSUB    = 0.2997589     PCLM    = 2.6313228     PDIBLC1 = -0.40275
+PDIBLC2 = 2.205592E-3   PDIBLCB = -0.0272899    DROUT   = 0.7201569
+PSCBE1  = 5.601647E8    PSCBE2  = 5.450628E-5   PVAG    = 7.40725E-3
+DELTA   = 0.01          RSH     = 81.2          MOBMOD  = 1
+PRT     = 8.621         UTE     = -1            KT1     = -0.2501
+KT1L    = -2.58E-9      KT2     = 0             UA1     = 5.4E-10
+UB1     = -4.8E-19      UC1     = -7.5E-11      AT      = 1E5
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.03E-10      CGSO    = 2.03E-10      CGBO    = 1E-9
+CJ      = 4.198358E-4   PB      = 0.99          MJ      = 0.4516115
+CJSW    = 3.241716E-10  PBSW    = 0.1000811     MJSW    = 0.1152935
+CJSWG   = 1.64E-10      PBSWG   = 0.1000811     MJSWG   = 0.1152935
+CF      = 0             PVTH0   = 0.0766435     PRDSW   =
163.0361088
+PK2     = -0.0297388    WKETA   = -0.0214699    LKETA   = -2.14921E-
5
+AF      = 1             KF      = 0)
```

```
.MODEL AMI06P-FS PMOS (                                LEVEL   = 7
+VERSION = 3.1            TNOM    = 27             TOX     = 1.39E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -1.0173478
+K1      = 0.5658287      K2      = 0.0116517      K3      = 10.5698978
+K3B     = -0.7608774     W0      = 1E-8           NLX     = 9.01509E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 3.3035484      DVT1    = 0.5614757      DVT2    = -0.0733879
+U0      = 213.2201651    UA      = 2.872001E-9    UB      = 1.05947E-
21
+UC      = -5.43332E-11   VSAT    = 1.545629E5     A0      = 0.4566597
+AGS     = 0              B0      = 6.789661E-7    B1      = 5E-6
+KETA    = -8.389653E-3   A1      = 4.693067E-8    A2      = 0.3
+RDSW    = 3E3            PRWG    = -0.046965      PRWB    = -
6.108168E-5
+WR      = 1              WINT    = 2.938786E-7    LINT    = 5.685662E-
8
+XL      = 0              XW      = 0              DWG     = -
1.995328E-8
+DWB     = 2.020066E-8    VOFF    = -0.0719834     NFACTOR = 0.7501867
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.1503769      ETAB    = -0.0623126
+DSUB    = 0.8623589      PCLM    = 2.2059151      PDIBLC1 = 0.0239419
+PDIBLC2 = 3.052934E-3    PDIBLCB = -0.0972847     DROUT   = 0.1509141
+PSCBE1  = 5.116843E9     PSCBE2  = 5E-10          PVAG    = 0
+DELTA   = 0.01           RSH     = 101.5          MOBMOD  = 1
+PRT     = 59.494         UTE     = -1             KT1     = -0.2942
+KT1L    = 1.68E-9        KT2     = 0              UA1     = 4.5E-9
+UB1     = -6.3E-18       UC1     = -1E-10         AT      = 1E3
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 3.18E-10       CGSO    = 3.18E-10       CGBO    = 1E-9
+CJ      = 7.235521E-4    PB      = 0.9527404      MJ      = 0.4955303
+CJSW    = 2.692736E-10   PBSW    = 0.99           MJSW    = 0.295843
+CJSWG   = 6.4E-11        PBSWG   = 0.99           MJSWG   = 0.295843
+CF      = 0              PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 2.574681E-3    LKETA   = -
7.296621E-3
+AF      = 1              KF      = 0)
```

Appendix E: Analysis and comparison results of Telescopic and Folded-cascode FTFA

In this section a comparison is established between previous and modified designs of the Telescopic and Folded-cascode FTFA. The improved versions were also simulated using AMI C5N 0.5 micron process. Process variations are modeled within each of the transistor models. For instance, the threshold voltage for NMOS changes from 0.64V to 0.71V which corresponds to a 3% to a 7% change respectively from the nominal value. On the other hand, PMOS threshold voltage changed from -0.85V to -1.01V corresponding to a 8% and 9% change respectively from the nominal value.

To evaluate the performance on process variations, Pspice simulations were performed. Table E.1 shows design parameters of previous and modified FTFA designs.

Parameter	Telescopic FTFA	Improved Telescopic FTFA
Open-loop gain	87 dB	113 dB
Phase Margin	79º	58°
Unity-gain	86 MHz	320 MHZ
3dB frequency	456 Hz	351 Hz
Input Common-Mode Range	$-422mV \le V_{CMIR} \le 422mV$	$-497.7\,mV \le V_{CMR} \le 504.5\,mV$
Power Dissipation	67mW	95.1 mW
Offset Voltage	1.46 mV	1.22 mV

Output Swing	$-2.48V \le V_{OSW} \le 2.02V$	$-2.445V \le V_{OS} \le 2.358V$
Settling Time	$S^+ = 457ns \; S^- = 457ns$	$S^+ = 193ns \, S^- = 174ns$
Slew Rate	$SR^+ = 27.70\frac{V}{\mu s}$ $SR^- = 27.67\frac{V}{\mu s}$	$SR^+ = 29.96\frac{V}{\mu s}$ $SR^+ = 29.96\frac{V}{\mu s}$
Common-mode Rejection Ratio	109 dB	79 dB
Input-referred noise	$8.19\frac{nV}{\sqrt{Hz}}$	$8.19\ \frac{nV}{\sqrt{Hz}}$
THD@1KHz	$V_o^+ = 3.90\%$ $V_o^- = 2.93\%$	$V_o^+ = 6.285\%$ $V_o^- = 6.294\%$

Table E.2 Previous and Modified worst-case results of Telescopic FTFA

From the table above, the modified telescopic present some improvements specifically in open-loop gain. Other improvements are seen on settling time, unity gain and input common-mode range.

A comparison is also established between the previous and modified Folded-cascode FTFA. Table E.2 shows design parameters for both circuit implementations.

Parameter	Improved Folded-cascode FTFA	Folded-cascode FTFA
Open-loop gain	92 dB	92 dB
Phase Margin	63°	77 º
Unity-gain	302 MHZ	125 MHz
3dB frequency	5.33 kHz	4.13 KHz

Input Common-Mode Range	$-498\ mV \le V_{CMR} \le 501\ mV$	$-498mV \le V_{CMIR} \le 498mV$
Power Dissipation	79.7 mW	77mW
Offset Voltage	1.32 mV	1.24 mV
Output Swing	$-2.48V \le V_{OS} \le 2.184V$	$-2..47V \le V_{OSW} \le 2.37V$
Settling Time	$S^+ = 602ns\, S^- = 247ns$	$S^+ = 312ns\ S^- = 312ns$
Slew Rate	$SR^+ = 12\frac{V}{\mu s}\ SR^+ = 12\frac{V}{\mu s}$	$SR^+ = 15.98\frac{V}{\mu s}$ $SR^+ = 14.75\frac{V}{\mu s}$
Common-mode Rejection Ratio	73 dB	65 dB
Input-referred noise	$7.16\ \frac{nV}{\sqrt{Hz}}$	$7.10\frac{nV}{\sqrt{Hz}}$
THD@1KHz	$V_o^+ = 1.332\%$ $V_o^- = 6.478\%$	$V_o^+ = 6.54E-1\%$ $V_o^- = 4.02E-1\%$

Table E.2 Previous and Modified worst-case results for Folded-cascode FTFA

In this case improvements are seen on unity-gain frequency, phase margin and Common-mode rejection ratio.