Development of an Electro-Thermal Model For a Multi-Chip IGBT Power Electronic Module

By

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Abstract

A lumped parameter thermal model for a multi-chip power module is presented based in the physical and geometrical characteristics of the module. The model is developed using the thermal component approach. The model is implemented in SABER and integrated with temperature dependent device models and other thermal component models to develop an electro-thermal model for a three-phase inverter. This report presents model development, implementation in SABER, simulation results, and calibration using experimental data. The model exhibit excellent matching of the temperature in the junction of the devices and good matching in the temperature in the heat sink which permits dynamic simulations of power electronic designs.

Resumen

Un modelo termal de parámetros conglomerados para un modulo de potencia múltiples chips es presentado basado en las características físicas y geométricas del modulo. Este modelo fue desarrollado usando el método de componentes termales. El modelo fue implementado en SABER e integrado con modelos de dispositivos dependientes de temperatura y otros modelos de componentes termales para desarrollar un modelo electro-termal para un invertidor trifásico. Este reporte presenta el desarrollo, implementación del modelo en SABER, resultados de simulaciones y calibración usando información experimental. El modelo presenta excelente concordancia con la temperatura de junta de los dispositivos además de buena concordancia en la temperatura del disipador de calor lo que permite simulaciones de diseños de electrónica de potencia.

Dedicatory

I dedicate this work to my family, especially to my mother Juana E. Rodríguez Feliciano and my father José Ángel Rodríguez Irizarry who pass away during this work and didn't reach to see the rewards of his insightful advices. Also, I wish dedicate this work to my fiancée Miriam Romero, this is the reward after all your support, you are always in my heart. And over all things, I dedicate this work to God who gives me the direction and courage to finish this work.

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Chapter 1

Introduction

1.1. Problem Statement and Justification

Power electronic systems are used widely to convert electric energy from one form to other using electronic devices. Four basic power electronics functions are AC to DC conversion, DC to AC conversion, DC to DC conversion and AC-AC conversion. These basic functions are used to build power supplies, DC transmission systems, electric drives, etc. Since the conversion process is not 100% efficient, power electronic systems loose energy that is released as heat affecting system's temperature. Changes in the temperature and its spatial distribution can significantly influence the electrical and mechanical behavior of power electronics systems. Electro-thermal and thermo mechanical issues in power electronics systems are becoming more important as industry seeks to increase packaging and power densities for power electronic systems

A key concept in this effort is the use of the power electronic module (PEM) where elementary building blocks or power modules are used to design power electronic systems. In this concept, it is required that PEM structures should be common in a sense

that all or most of the power conversion functions share the same building blocks so that the system could be configured and reconfigured easily, acquisition cost could be reduced, and reliability and maintainability could be improved [1].

The electrical characteristics and reliability of PEM (Power Electronic Module) can be greatly influenced by the temperature distribution inside the module, it is important to be able to simulate the coupled electrical and thermal system for design and analysis of PELS (Power Electronic Systems). In a PEM electro-thermal model, an electrical model of the PEM is coupled with a thermal model of the PEM package. The thermal model uses electrical power losses as input to compute the temperature distribution of the package. The temperature distribution is then used in conjunction with temperature dependent models of power semiconductor devices to study the effects of heating in the electrical performance of the PEM. This is illustrated in Figure 1.1.

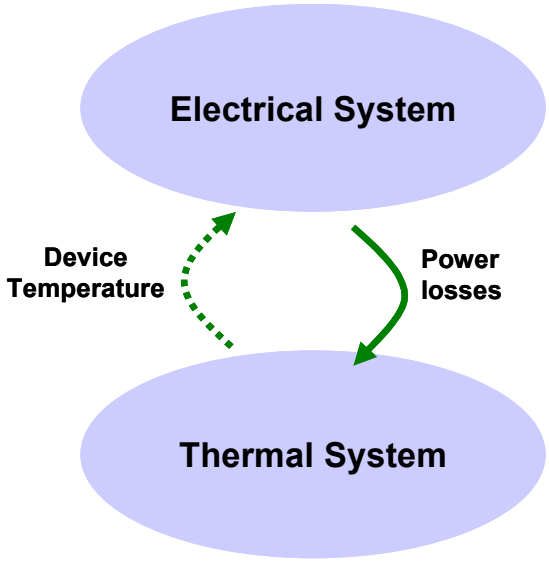

Figure 1.1 Diagram of Electro-thermal modeling.

The IGBT has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET. IGBTs have been the preferred device under these conditions:

- Low duty cycle
- Low frequency (<20kHz)
- Narrow or small line or load variations
- High-voltage applications (>1000V)
- Operation at high junction temperature is allowed (>100°C)
- >5kW output power

Because of their versatility for high frequency switching, high voltage and high power application, there has been a significant growth in the use of IGBTs. Sample IGBT applications include [2]:

- Motor control: Frequency < 20kHz, short circuit/in-rush limit protection
- Uninterruptible power supply (UPS): Constant load, typically low frequency
- Welding: High average current, low frequency (< 50 kHz), ZVS circuitry
- Low-power lighting: Low frequency (< 100 kHz)

IGBTs can be found in applications from Kilo to Megawatts operating at switching frequencies of the order of kilohertz. These posses a challenge in terms of handling power losses and the effect on system performance. Electro-thermal models for a single chip IGBT have been developed in [3]. Our work focused on extending this

approach to multi-chip PEM used in high power applications and its implementation in the SABER simulation environment.

1.2. Literature Review

To describe the thermal behavior of power semiconductor devices, several methods have been used for solving the heat diffusion equation to describe their surface temperature. These methods include steady-state Fourier series solution [4], convolution of the thermal step response with analytical power dissipation functions [5], empirical extraction of thermal network element values from the measured thermal step response [6], physics-based thermal resistance and thermal capacitance network element analysis [7], three-dimensional finite difference and finite element simulation [8], and lumped thermal capacitance method [9]. However each of these methods has limitations that prevent efficient dynamic electro-thermal simulation. The first method is very efficient for three-dimensional steady-state thermal analysis, but is not applicable to dynamic thermal conditions. The second is useful for analytical calculations of the dynamic temperature distribution from predetermined power dissipation functions, but is only valid for linear materials and would require the evaluation of a convolution integral by the circuit simulator which is inefficient. All these methods require a very exhaustive and complex mathematical analysis, because are based on three-dimensional heat diffusion equation, that's why they represent a computational straightjacket, since they do not allow an easy addition of new elements. It is to say, if it is wanted to consider new forms of heat dissipation in the thermal analysis of an electronic package, the

mathematical model must be modified significantly; this means that these methods have limited practical use in iterative design processes for module optimization.

The Lumped Thermal Capacitance Method (LTCM) [9] allows an unsteady heat transfer analysis, dependent only on the time variable, representing spatial thermal distribution by the physical and thermal characteristics of the PEM. This method requires that heat conduction effects are dominant over convective and radiation effects [9]. This method, in order to obtain the temperature profile of a PEM each material is treated as a control volume or lumped assumes that inside the PEM the conduction is negligible.

Analysis of PEMs for modeling the thermal and electrical behavior using several software's: I-DEAS, Maxwell, Flotherm and SABER was studied by Chen in [10]. The models are three-dimensional for the thermal analysis, also using Kirchhoff's current law to determine the power dissipated and doing an electro-magnetic analysis.

The complex thermal interactions between the heat sources, substrate, and enclosing walls as affected by the thermal conductance of the walls and substrate was studied by Tummala in [11]. They tried to determine which physical effects and level of detail are necessary to accurately predict thermal behavior of discretely heated enclosures. Their analysis was based on the 3D equations of continuity, momentum, and energy.

In typical analysis of electronic circuits, the changes in temperature and its spatial distribution in the device during operation are neglected assuming no significant influence in the electrical device behavior but actually the behavior is greatly affected. Particularly, two effects usually have to be considered. First, thermal runaway where the

dissipated electrical energy causes a temperature rise over an extended area of a device that result in an increase in power dissipation. The second is self-heating where the device temperature increases leading to an irrecoverable device failure burn out, unless a safe equilibrium situation can occur with a cooling system removing all of the dissipated energy [12].

Most electrical and electronic systems need some form of thermal management due to elevated temperatures that can adversely affect electronic device operation, reliability, power-handling capability, and achievable packing density [13]. Computer-based analysis of the thermal behavior in electronic packages can be based on discretizations of the heat transfer equation using tools like FLOTHERM [14] and IDEAS [15]. These software tools are used by the electronics industry, for cooling design, thermal design, thermal management, and thermal simulation of electronics packages. However these models are not suitable for dynamic electro-thermal simulation due to their high dimensionality and computational requirements.

We need to look at transient electro-thermal behavior since dynamic thermal and electrical variables may have strong and nonlinear dynamic interaction generating "unexpected" oscillations of electrical and thermal variables with devices working in forward bias safe operating area (FBSOA) and at low temperatures [16]. These fluctuations correspond to stable limit cycles of the electro-thermal model. While the system evolves along a limit cycle or during the transient to reach it, device temperatures might have values greater than the maximum allowable, i.e., operating points outside the FBSOA that may result in device destruction. This effect is well known by designers

jointly to the knowledge that static thermal model are inadequate to study this aspect and to predict a possible failures.

Electro-thermal device models are currently implemented in circuit simulators such as SABER [17]. This suggest to integrate lumped parameter thermal models with electric circuit models, and temperature dependent device models to simulate transient electro-thermal behavior of power electronics systems using circuit simulators.

An electro-thermal simulation methodology using the SABER simulator has previously been introduced for discrete power devices and packages [18], [19]. In this methodology, the simulator solves for the temperature distribution within the semiconductor devices, packages and heat sinks (thermal network) as well as current and voltages within the electrical network. The interface between the thermal and electrical networks is thought the temperature dependent device models [20]. The device model has terminals that are connected to the electrical network and a terminal connected to the thermal network. The thermal network is the interconnection of compact thermal component model that aims to accurately predict the temperature of the package only in a few critical points like junction, case, and leads [3]. Each model represents an indivisible building block used by the designer to form the thermal network. The modular structure of the models allows the designer to interchange different thermal components, examine different configurations of the thermal network easily, and the development of standard component libraries for simulation software such as SABER. Furthermore, the output of the thermal model can be used to predict thermal stresses, evaluate operation within maximum ratings, and analyze PEM long-term reliability. In this thesis work, we used

the thermal component network approach to build a thermal model for a high power multi-chip IGBT PEM.

The previously developed thermal network component models for single chip IGBT PEM [3] don't apply to high power modules because these modules contain multiple chips within the same package, requiring complex dissipation systems. The objective of this research was to develop the models required to extend single chip IGBT SABER electro-thermal modeling methodology to multi-chip high power IGBT module.

Modeling of PEM thermal interactions is achieved by application of the 1-D heat transfer equation to model heat flow through complex geometries. The numerical solution of the heat flow equation is achieved by finite difference (FDM) methods implemented through SABER system variables. The implemented thermal component models are parameterized in terms of structural and material parameters to facilitate parametric generation of thermal component network libraries for PEM and parametric analysis of PEM.

The developed thermal component model for the multi-chip IGBT PEM is used to simulate the electro-thermal aspects of a high-power three-phase inverter.

1.3. Thesis outline

Chapter 2 presents the basic methodology used to derive and implement the thermal models for the multi-chip IGBT PEM. Chapter 3 presents an overview of the considerations needed to take care to develop an electro-thermal model for a multi-chip PEM. In Chapter 4, the development of the thermal modeling of a PEM-based system is presented. In Chapter 5 and 6, results and conclusions of this thesis are presented.

Chapter 2

Electro-Thermal Modeling Basics

In this chapter, we present the basic concept of thermal component network modeling. This is a key concept in the development of our model.

2.1. Basic concepts in thermal modeling

Heat transfer is the energy transferred between an object and its environment due to a temperature difference between the two. There are three basic mechanisms for heat transfer: convection, conduction, and radiation. They are described individually for simplicity however, a system will typically exhibit all three processes simultaneously.

Conduction is the mechanism described by heat transfer through a medium in direct contact with surfaces of different temperatures. The first requirement for conduction is that the medium is static. Thus the medium must be a rigid solid, or if fluid, it must have no circulating currents. The law that governs this heat flow is the Fourier's law of heat conduction equation (2.1), which states that the heat flux is proportional to the negative of the local temperature gradient. Where q is the heat flux, or heat flow per unit area perpendicular to the flow direction (W/m^2), T is the local temperature (K or ˚C), x is the coordinate in the flow direction (m) and k is the thermal conductivity of the material.

$$q = -k\frac{dT}{dx} \tag{2.1}$$

A fluid (e.g., water, air), by virtue of its temperature, can transport energy. Strictly speaking, convection is the transport of energy by bulk motion of a medium from a surface to a moving fluid. There are essentially two types of convection: forced and natural convection.

$$q_s = h_c(T_s - T_e) \tag{2.2}$$

where q_s is the heat flux by convection in equation (2.2), T_s is the surface temperature, T_e is the fluid temperature and h_c is the convective heat transfer coefficient, this value varies for forced and natural convection.

Radiation is the mechanism of heat transfer where energy is emitted due to an object's temperature. Therefore any object at a temperature above absolute zero will radiate energy. We are not interested in radiation since, in our case the dominant effects at the range of operation of power electronic equipment are conduction and convection. For more in depth details refer to any heat and mass transfer book like [21].

2.2. Thermal modeling of PEM's

In the case of vertical power devices [22], where the thickness L_O is small compared to other dimensions, it is commonly considered that heat is generated at the top surface of silicon and flows uniformly along the x-axis (perpendicular to the silicon surface). So, the top surface is considered to be a geometrical boundary of the device at x=0, where the input power $P_{in}(t)$ is assumed to be uniformly dissipated. The lower surface (at $x = L_O$) is considered to be the cooling boundary, where the temperature is assumed to be equal to the input temperature T_{in} as show in Figure 2.1 [22]. Convection and radiation are assumed to be negligible. So a one-dimensional (1-D) heat-flow may be considered so that the thermal system is governed by the 1D heat transfer equation [23]:

$$\frac{\partial}{\partial x}\left[K(T)\frac{\partial T}{\partial x}(t,x)\right]+\dot{q}=\rho c\frac{\partial T}{\partial t}(t,x) \tag{2.3}$$

with boundary conditions

$$SK\frac{\partial T}{\partial x}\bigg|_{X=0}=-P_{in}(t) \tag{2.4}$$

$$T(t,x=L_o)=T_{in}(t) \tag{2.5}$$

where L (cm), S (cm2)is the effective length and area of the semiconductor device, c is the silicon-specific heat (J/g/K), ρ is the silicon mass density (g/cm3), T is the absolute temperature (K), T_{in} is the input temperature (K), P_{in} is the input dissipated power(W), and K is the thermal conductivity (W/cm/K).

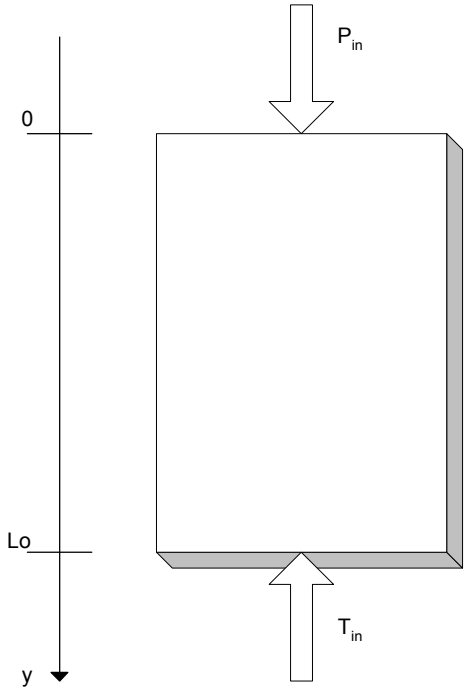

Figure 2.1 Semiconductor die Diagram.

Next the FDM, FEM and the Analytical method are introduced based on the study developed in [22]:

a. Finite Difference Method

In the finite difference method, the 1-D structure is discretized using *n* constant steps of value *h* at node number *i* the discretization of (2.3) with a constant step value *h* give the classical relation [3]:

$$\frac{T_{i+1}(t)+T_{i-1}(t)-2T_i(t)}{h^2}=\frac{\rho c}{K}\frac{\partial T_i(t)}{\partial t}, \qquad i=1,n-1 \tag{2.6}$$

where is the temperature at the node number i and $h=L/n$.

The first order discretization of the boundary condition at x = 0 gives

$$\frac{T_0(t) - T_1(t)}{h} = \frac{P_{in}(t)}{KS} \tag{2.7}$$

Taking into account (2.6) and (2.7), the equivalent RC circuit of the 1-D thermal model can be derived and is shown in the Figure 2.2.

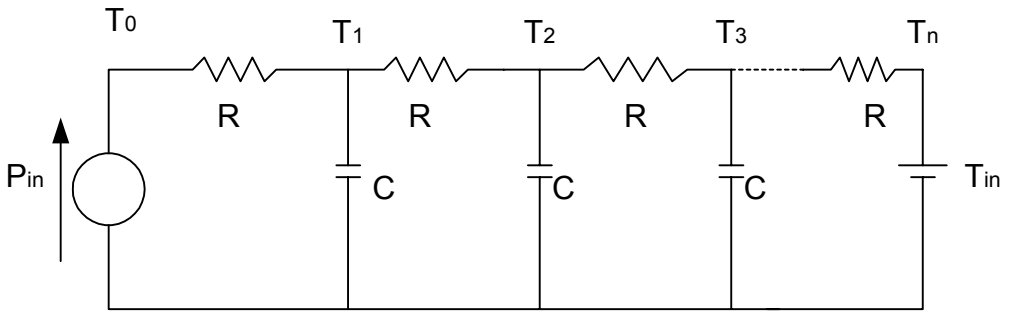

Figure 2.2 RC thermal network obtained by the FDM.

where, $R = (h/KS)\cdot(K/W)$ and $C = h\rho cS\cdot(J/K)$ are the element thermal resistance and capacitance, respectively.

b. Finite Element Method

The finite element method is based on a variational equation of the heat equation [24], so the approximated solution of (2.3) is given by:

$$T(x,t) = \sum_{i=1}^{m} \xi_i(t) W_i(x) \tag{2.8}$$

where $W_i(x)$ are base functions and $\xi_i(t)$ are the coordinates of the temperature approximation in the space basis formed by the base functions. A trial function $S_i(x)$ is considered, and using (2.4) the integration of (2.3) multiplied by a function $S_i(x)$ over [0, L] yields the following variational equation [23].

$$\frac{d}{dt}\int_0^L T(x,t)S_i(x)dx + \frac{K}{\rho c}\int_0^L \frac{\partial T(x,t)}{\partial x}\frac{dS_i}{dx} - \frac{K}{\rho c}S_i(L)\frac{\partial T}{\partial x}(L,t) = \frac{P(t)}{\rho cS}S_i(0) \tag{2.9}$$

where $S_i(x)$ are the trial functions. The boundary condition (2.4) is taken into account in (2.9). Equation (2.9) applied for m trial function $S_i(x)$ may be written in a matrix form as follows

$$\frac{dX}{dt} = AX + Bu \tag{2.10}$$

where

$$X = M\xi \ , \ A = -RM^{-1}, \ u = P_{in}$$

$$M_{ij} = \int_0^L W_j(x)S_i(x)dx$$

$$R_{ij} = \frac{K}{\rho c}\int_0^L \frac{dW_j}{dx}\frac{dS_i}{dx}dx - \frac{K}{\rho c}\frac{dW_i(L)}{dx}S_i(L)$$

$$B_i = \frac{S_i(0)}{\rho cS}.$$

and the obtained model is a state-space model, where $X_i(t)$ are the state variables. An example of this may be that the output value $y(t)$ of the model can be the temperature at x = 0

$$y(t) = T(0,t) = W(0)M^{-1}X(t)$$

The temperature at abscissa x is given by

$$T(x,t) = W(x)M^{-1}X(t) \tag{2.11}$$

where $W(x)$ is the row vector formed by the decomposition functions $W_i(x)$.

The equivalent circuit of the obtained 1-D thermal model is shown in Figure 2.3 [25] where:

$C_1 = (\rho cSh/2)$, $C_2 = (\rho cSh/6)$ and $R_1 = (h/KS)$

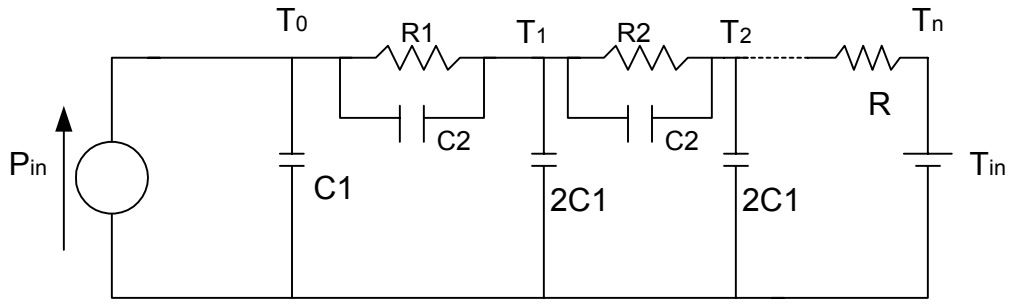

Figure 2.3 Equivalent thermal circuit networks obtained by the FEM.

c. Analytical Model and Internal Approximation

In this approach, the idea is to develop an analytical and efficient model based on an internal approximation where the decomposition functions have a support equal to the complete domain ($W_i(x)$ defined for $0 < x < L$) instead of a restriction to a neighborhood segment of a given node as in the FEM. Therefore, the approximate solution of equation (2.3) can be written as follows

$$T_{IA}(x,t) = T_{in}(t) + \sum_{i=1}^{m} \xi_i(t) W_i(x) \tag{2.12}$$

here $\zeta_i(t)$ does not correspond to the node temperature value. The variational equation associated with the boundary value problem equations (2.3)-(2.5) is given by equation (2.9).

Taking into account equation (2.12), the following differential equations represent the system dynamics are:

$$M\xi + R\xi = BP_{in} + C\frac{dT_{in}}{dt} \tag{2.13}$$

C is a vector defined by

$$C_i = \int_0^L S_i(x)dx$$

The state variable vector is defined by

$$X = -M\xi + CT_{in}$$

and the state equation of the internal approximation of the boundary value problem can be written as

$$\frac{dX}{dt} = AX + B_1 u_1 \tag{2.14}$$

where $A = -RM^{-1}$, B_1 is a two-column/m-vector matrix including the vector (-B) and (-AC), $B_1 = (-B, -AC)$ and $u_1 = \begin{pmatrix} P_{in}(t) \\ T_{in}(t) \end{pmatrix}$. Finally the output relations are defined as

$$\begin{aligned} T_{out}(t) &= T_{in}(t) + W(x=L)M^{-1}(CT_{in} - X(t))P_{out}(t) \\ P_{out}(t) &= -SK\sum_{i=1}^{m}\xi_i(t)\frac{\partial W}{\partial x}(x=L) \\ &= SKM^{-1}\frac{dW}{dx}(x=L)(X(t) - CT_{in}). \end{aligned} \tag{2.15}$$

Studies in [23] have shown the advantage of the finite element method compared to the finite difference element method especially in the case of large power surge of short time duration.

2.3. Electro-Thermal Modeling of the IGBT

In an IGBT PEM, the power semiconductor die is the primary source of heat and its properties are temperature dependent. To implement a dynamic electro-thermal model, the use of an electrical model capable of dynamically changing its properties with changes in temperature is needed. These models are already implemented in the SABER simulator environment for devices like the IGBT, BJT and power diodes. The work presented here focuses in the IGBT. The IGBT functions as a bipolar transistor with the base current supplied by a voltage controlled MOSFET as illustrated in Figure 2.4. The bipolar transistor of the IGBT consists of a low-doped wide base with the base virtual contact at the collector end of the base [25]. This bipolar transistor has a low gain and is in the high-level injection condition for the practical current density range of the device. Consequently, the IGBT bipolar transistor cannot be described in traditional ways.

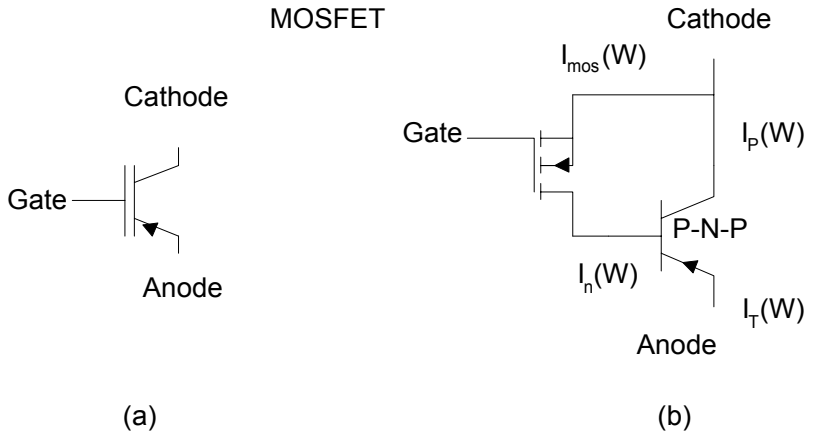

Figure 2.4 Basic equivalent circuit model of IGBT: a) symbol b) equivalent model.

Most semiconductors devices like the IGBT's are made of silicon. An important characteristic of silicon semiconductors is its thermal conductivity [12] whish is equal to:

$$K(T) = 1.5486\left(\frac{300K}{T}\right)^{4/3} \tag{2.16}$$

This thermal conductivity varies with temperature from 1.56W/cm at 25ºC to 1.16W/cm at 100ºC a 26 percent difference. This is used to develop the temperature dependent model of the device.

Hefner developed a methodology to implement the IGBT analytical model, described in [25] - [28], into the SABER circuit simulator. This model describes accurately the on-state *v*-*i* characteristics and transient current and voltage waveforms of the IGBT for general loading conditions. These equations are presented in Table 1. Device parameters and physical constants at 25ºC are presented in [25]. Hefner developed a physics-based electro-thermal dynamic model for the IGBT by coupling a temperature-dependent IGBT electrical model with dynamic thermal models for the IGBT silicon chips in the device [20]. The device temperature depends upon the circuit operation and does not remain constant for dynamic operating conditions.

Table 2.1 IGBT Electrical Model System Equations [27].

$$V_{dg} = V(drain) - V(gate)$$
$$V_{gs} = V(gate) - V(cathode)$$
$$V_{ds} = V(drain) - V(cathode)$$
$$V_{eb} = V(emitter) - V(drain)$$
$$V_{ae} = V(anode) - V(emitter)$$
$$V_{ec} = V(emitter) - V(cathode)$$
$$V_{bc} = V_{ds}$$
$$N_{scl} = N_B + N_{sat}$$
$$W_{gdj} = \sqrt{2\varepsilon_{si}(V_{dg} + V_{Td})/qN_{scl}}$$
$$W_{dsj} = \sqrt{2\varepsilon_{si}(V_{ds} + 0.6)/qN_{scl}}$$
$$W_{bcj} = \sqrt{2\varepsilon_{si}(V_{bc} + 0.6)/qN_{scl}}$$
$$W = W_B - W_{bcj}$$
$$Q_{gs} = C_{gs}V_{gs}$$
$$Q_{ds} = A_{ds}\sqrt{2\varepsilon_{si}(V_{bc} + 0.6)qN_{scl}}$$
$$Q_{ds} = AWqN_{scl}$$
$$Q_{bi} = A\sqrt{2\varepsilon_{si}qN_B 0.6}$$
$$C_{bcj} \equiv A\varepsilon_{si}/W_{bcj}$$
$$C_{cej} = QC_{bcj}/3Q_B$$
$$C_{dsj} = (A - A_{gd})\varepsilon_{si}/W_{dsj}$$
$$C_{gdj} = A_{gd}\varepsilon_{si}/W_{gdj}$$
$$C_{gd} = \begin{cases} C_{oxd} & \rightarrow \text{ for } \ V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd} + C_{gdj}) & \rightarrow \text{ for } \ V_{ds} > V_{gs} - V_{Td} \end{cases}$$
$$\mu_{nc} = 1/(1/\mu_n + 1/\mu_c)$$
$$\mu_{pc} = 1/(1/\mu_p + 1/\mu_c)$$
$$\mu_{eff} = \mu_{nc} + \mu_{pc}Q/(Q + Q_B)$$
$$D_c = 2(kT/q)\mu_{nc}\mu_{pc}/(\mu_{nc} + \mu_{pc})$$
$$L = \sqrt{D_c\tau_{HL}}$$

$$P_0 = Q/qAL\tanh(W/2L)$$
$$\overline{\delta_p} \equiv P_0\sinh(W/2L)/\sinh(W/L)$$
$$\eta_{eff} \equiv \frac{W/2L\sqrt{N_B^2 + P_0^2\csc h^2(W/L)}}{\arctan h\left[\dfrac{\sqrt{N_B^2 + P_0^2\csc h^2(W/L)\tanh(W/2L)}}{N_B + P_0\csc h^2(W/L)\tanh(W/2L)}\right]}$$
$$R_b = \begin{cases} W/(q\mu_{nc}AN_B) & \text{for} \quad Q < 0 \\ W/(q\mu_{eff}A\eta_{eff}) & \text{for} \quad Q \ge 0 \end{cases}$$
$$V_{ebj} = 0.6 - (Q - Q_{bi})^2/(2qN_B\varepsilon_{si}A^2)$$
$$V_{ebd} = \frac{kT}{q}\ln\left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B}\right)(N_B + P_0)\right] - \frac{D_c}{\mu_{nc}}\ln\frac{P_0 + N_B}{N_B}$$
$$V_{ebq} = \begin{cases} V_{ebj} & \text{for } Q < 0 \\ \min(V_{ebj}, V_{ebd} & \text{for } Q_{bi} > Q \ge 0 \\ V_{ebd} & \text{for } Q \ge Q_{bi} \end{cases}$$
$$BV_{cbo} = BV_f \cdot 5.34 \times 10^{13} \cdot N_{scl}^{-0.75}$$
$$M = 1/\left[1 - (V_{cb}/BV_{cbo})^{BV_n}\right]$$
$$I_T = V_{ae}/R_b$$
$$I_{css} = (1/(1+b)I_T) + (1/(1+b)) \cdot 4D_pQ/W^2$$
$$I_c = I_{css} + C_{cer} \cdot dV_{ec}/dt$$
$$I_{bss} = \frac{Q}{\tau_{HL}} + \frac{Q^2}{Q_B^2} \cdot \frac{4N_{scl}^2}{n_i^2} \cdot I_{sne}$$
$$I_{mos} = \begin{cases} 0 & \text{for } V_{gs} < V_T \\ \dfrac{K_{plin}\left[(V_{gs} - V_T)V_{ds} - \dfrac{K_{Plin}V_{ds}^2}{2K_{Psat}}\right]}{1 + \theta(V_{gs} - V_T)} & \text{for } V_{ds} \le (V_{gs} - V_T)\dfrac{K_{Psat}}{K_{Plin}} \\ \dfrac{K_{Psat}(V_{gs} - V_T)^2}{2\left[1 + \theta(V_{gs} - V_T)\right]} & \text{for } V_{ds} > (V_{gs} - V_T)\dfrac{K_{Psat}}{K_{Plin}} \end{cases}$$
$$I_{gen} = qn_iA\sqrt{2\varepsilon_{si}V_{bc}/qN_{scl}/\tau_{HL}}$$
$$I_{mult} = (M - 1)(I_{mos} + I_c) + M \cdot I_{gen}$$

To incorporate the electro thermal effects into the SABER IGBT model described in Table 2.1 [27], the expressions in Tables 2.2 and 2.3 are added to the IGBT model. The device parameter and physical thermal dependency properties are included and the corresponding expressions are presented in Tables 2.2 and 2.3 [18].

Table 2.2 Temperature Dependent IGBT Parameter [18].

$$\tau_{HL}(T_j) = \tau_{HL0} \cdot (T_j / T_0)^{\tau_{HL1}}$$

$$I_{sne}(T_j) = \frac{I_{sne0} \cdot (T_j / T_0)^{I_{sne0}}}{\exp[14000 \cdot (1/T_j - 1/T_0)]}$$

$$V_T(T_j) = V_{T0} + V_{T1} \cdot (T_j - T_0)$$

$$K_p(T_j) = K_{p0} \cdot (T_0 / T_j)^{K_{p0}}$$

Table 2.3 Temperature Dependent Properties of Silicon [18].

$$\mu_n(T_j) = 1500 \cdot (300/T_j)^{2.5}$$

$$\mu_p(T_j) = 450 \cdot (300/T_j)^{2.5}$$

$$D_n(T_j) = \mu_n \cdot kT_j/q)$$

$$D_p(T_j) = \mu_p \cdot kT_j/q)$$

$$n_i(T_j) = 3.88 \times 10^{16} \cdot (T_j)^{1.5} / \exp(7000/T_j)$$

$$v_{nsat}(T_j) = 10^7 \cdot (300/T_j)^{0.87}$$

$$v_{psat}(T_j) = 8.37 \times 10^6 \cdot (300/T_j)^{0.52}$$

$$\alpha_1(T_j) = 1.04 \times 10^{21} \cdot (T_j/300)^{1.5}$$

$$\alpha_2(T_j) = 7.45 \times 10^{13} \cdot (T_j/300)^2$$

The IGBT electro-thermal model is implemented in the SABER circuit simulator and is used in electrical circuit simulation in the same way as the temperature independent IGBT model. The main difference is that it has an additional terminal that is connected to the thermal component model for the package and cooling system.

The thermal nodes in the thermal network have units of temperature across the nodes and units of power (W) flowing through the nodes, whereas the through and across variables for electrical networks are current and voltage.

2.4. Thermal Component network modeling

The thermal network is represented as an interconnection of compact thermal components so the system designer can readily interchange different thermal components and examine different configurations of the thermal network. The thermal component models are parameterized in terms of their structure and material properties so the details of the heat transfer physics are transparent to the user.

A compact model is a simplification of a detailed model of a device. It is a simple network comprising a limited number of thermal resistances and capacitance, connecting the critical part of the device (usually the junction) to the outer parts of the device, and is capable of accurately represents the full model. This method of thermal characterization is suited for embedding in the electronics, and the compact models can be incorporated into the component libraries of simulator analysis software packages like SABER [29]. Thermal compact models enable the prediction of junction temperatures of complicated components in a system level numerical simulation with a minimum of computational effort [30].

2.5. Implementing the model in SABER

First, we want to explain how the thermal characteristics can be simplified by considering the thermal properties analogous to electrical properties. The temperature

drop ΔT is analogous to the voltage drop V. The rate of heat flow P (or Q) is analogous to current flow. Thermal resistance θ is analogous to electrical resistance R. Thermal conductivity K is analogous to electrical conductivity σ.

When several materials are stacked in series, such as die is attached with epoxy to a substrate which is solder to a package base, the equivalent become the sum of the individual resistances. This is analogous to several resistors in series. Also the storage of energy in form of heat by the material is analogous to a capacitor in each node.

To implement the model, we select SABER a software package capable of simulating electric, electronic, and mechanical systems around others [33]. SABER software is used in the automotive, aerospace, power, and IC industry to simulate and analyze systems, sub-systems and components to reduce the need for physical prototypes. A large model library, advanced analyses, and support for standard hardware description languages such as MAST help designers and engineers to create more robust and cost efficient designs faster. The MAST is a hardware description language (HDL) very similar to C, is an advanced modeling language available for analog, mixed-signal and mixed-technology applications. We take advantage of these features to develop our model.

A basic example of that can be the source code for Figure 2.5 is show in Figure 2.6. First, the external nodes are defined in this case as header and case then the thermal properties of the material. The parameters are of the material and the positions of the internal nodes are calculated. Then the areas for each of the nodes and the volumes for each element are calculated using these values the thermal capacitance and thermal

resistance are calculated in source code presented in Figure 2.7. Finally, the code that connects the thermal resistance and thermal capacitance that made the thermal network. This point is the point in which SABER iterates until find a solution for the system of equations presented.

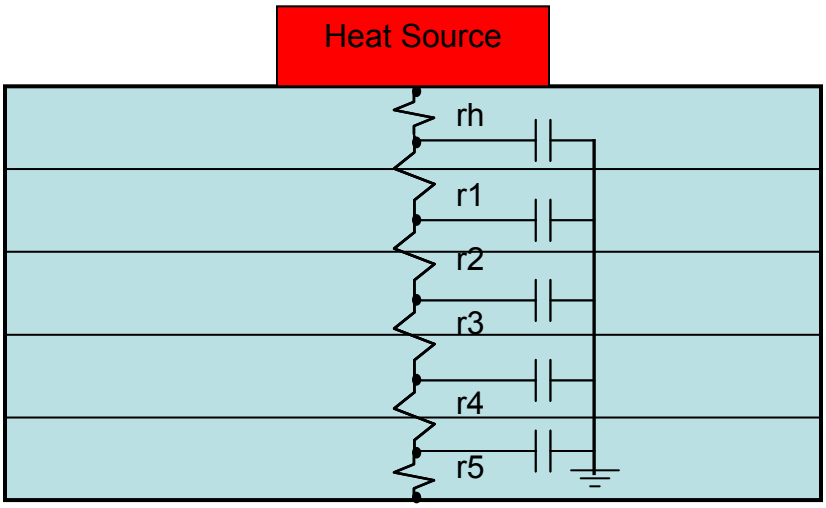

Figure 2.5 Thermal network for a simple body.

```
#----------------------Template Header----------------------#

#node type
thermal_c header, case

# model parameter default values
number thick=0.05       #(cm)         thickness of copper
etc...

#Values of Thermal constants of the different layers materials
number row=8.9          #(g/cm**3)    density of copper
etc...
number c=0.39           #(J/g/K)      specific heat of copper
etc...

#Values of Thermal constants of Layers
number k=2              #(W/cm/K)     thermal conductivity of copper 2
etc...
{
###Template Body ###
parameters {
        #calculated material parameter
        hc=row*c
        etc...

        #calculated chip Boundaries
        ...
        #calculated node positions
        s1=thick*1/10
        s2=thick*3/10
        etc...

        #calculated area for header

        #calculated area at node 1
        #calculated area at node 2
        etc...

        #calculate elements volume

        v1=a1*thick/5
        v2=a2*thick/5
        etc...
```

Figure 2.6 Example of source code in SABER.

```
#########################################################
        #calculate volume thermal capacitance
        ca1=v1*hc
        etc...
#########################################################

        calculate inter-node thermal resistances
        rh1 = (thick/5)/k/(ah+a1)
        etc...
        }
        values  {
        th=tc(header)+math_ctok
        t1=tc(node1)+math_ctok
        etc...
        h1=t1*c1
        h2=t2*c2
        etc...
        }
equations {
        p(header -> node1)+= (th-t1)/rh1
        p(node1 -> node2)+= (t1-t2)/r12
        etc...
        p(node1)+= d_by_dt(h1)
        p(node2)+= d_by_dt(h2)
        etc...
        }
}
```

Figure 2.7 Continuation of source code in SABER.

2.6. PEM Electro-thermal Model Development

The concept of electro-thermal model consists in the interconnection of an electrical network and thermal network thought thermal terminals as show in Figure 2.8. In the development of the electro-thermal model, we use thermal network component models derived from the heat diffusion equation using the component geometry, the nonlinear thermal properties of the materials, and other nonlinear heat transport mechanisms such as convection. The three-dimensional heat flow is accounted for using appropriate symmetry in the discretization of the heat equation for each region of the component. The silicon chip thermal model is based upon the one-dimensional rect-angular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The package models describe the two-dimensional lateral heat spreading and the heat capacity of the periphery of the package. The heat sink models describe the heat spreading beneath the package-heat sink interface; check the semi cylindrical heat flow from the package toward the heat sink fins, and the nonlinear forced and natural convection heat transfer at the heat sink fins.

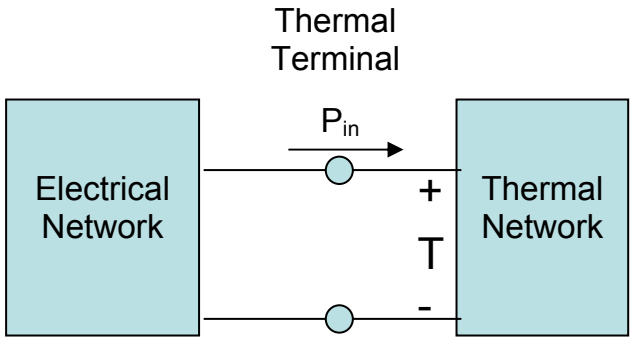

Figure 2.8 Interconnection of electrical network and thermal network.

The three-dimensional heat diffusion equation for isotropic materials (thermal conductivity is independent of direction) can be written as:

$$\nabla \cdot (k(T)\nabla T) = \rho c \frac{\partial T}{\partial t} \tag{2.17}$$

For various symmetry conditions, this partial differential equation can be discretized into a finite number of first-order ordinary time-dependent differential equations of the form

$$\frac{T_{i+1} - T_i}{R_{i,i+1}} - \frac{T_i - T_{i-1}}{R_{i-1,i}} = \frac{dH_i}{dt} \tag{2.18}$$

where

$$H_i = C_i \cdot T$$

is the heat energy stored at thermal node *i.* The heat equation and the discretization coefficients ($R_{i,i+1}$, and C_i) are explained in more detail in Chapter 4.

In the discretization process of equation (2.17), it is assumed that the temperature gradient and thermal conductivity do not vary substantially between adjacent grid points. Therefore, the accuracy of the thermal component model is determined by the number and locations of the thermal nodes within the component. For high power dissipation levels during short periods of time (e.g., for switching transients), the silicon chip surface temperature rises faster than the heat diffuses into the chip (nonquasistatic heating), and a high density of thermal nodes is required at the silicon chip surface. However, the thermal gradients disperse as the heat diffuses through the chip, so a grid spacing that increases logarithmically with distance from the heat source (silicon chip surface) results in the minimum number of thermal nodes required to describe the temperature distribution for the range of applicable power dissipation levels (heating rates).

The methods used in this work to develop the temperature dependent models for power semiconductor devices are described in the literature, see for example [3][4][12][18][27]. These techniques are used to develop and to implement the thermal network component models in SABER for PEM's that includes paralleled silicon chips, electrical insulating layer structure (DBC), and base-plate. To develop the model, we need to take in to consideration all the differences between a single ship module and a multi-chip module.

A detailed explanation of the development of the model done in this thesis is presented in the next two chapters.

2.7. Summary

This chapter presents the basic concepts of thermal modeling, and different approach to resolve the thermal problem for PEM which includes finite difference, finite elements, analytical model and internal approximation, and thermal component network methods. An overview of thermal component network modeling, development, and implementation in SABER is presented.

Chapter 3

Electro-thermal Modeling of a Multi-Chip PEM

Chapters 1 and 2 have introduced the basic methodology that is used to derive and implement the thermal models for the multi-chip IGBT PEM. In this chapter, we discuss the differences between a single chip and multi-chip PEM in developing a thermal model. The next chapter explains the use of the model in a system.

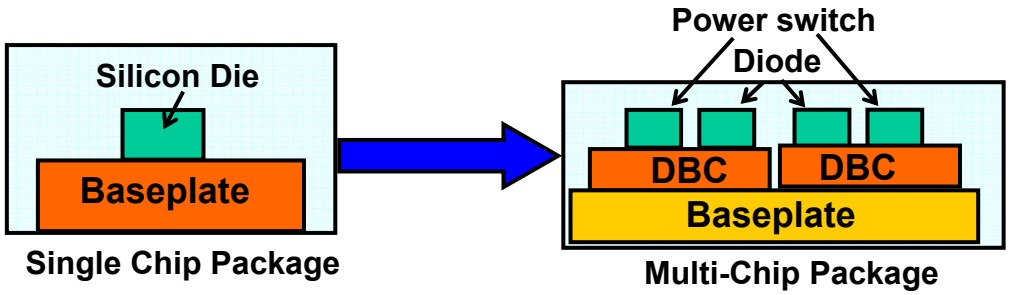

Figure 3.1 The single chip and multi-chip packages.

3.1. Description of Packages

Figure 3.1 shows the basic structure of a single chip and a multi-chip PEM. The single chip package is a simple structure composed only of a silicon die over a copper base. The multi-chip package is a more complex structure because it includes several semiconductors thermally coupled. A direct bonded copper (DBC) layer structure is used to isolate and attach the silicon chips to the solid structure of the module and also work as a heat spreader. The DBC is composed of layers of different materials as show in Figure 3.2.

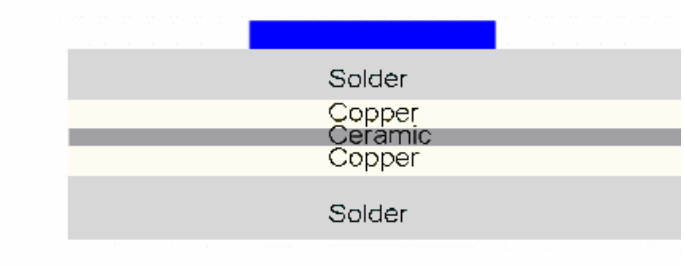

Figure 3.2 Direct Bonded Copper (DBC) layer structure.

In Figure 3.3, we see the top view of the inside of the high power IGBT Module studied in this research and we can see the composition of the package, which includes parallel devices (IGBT's and Diode's) to be able to manage the amount of power delivered to the device.

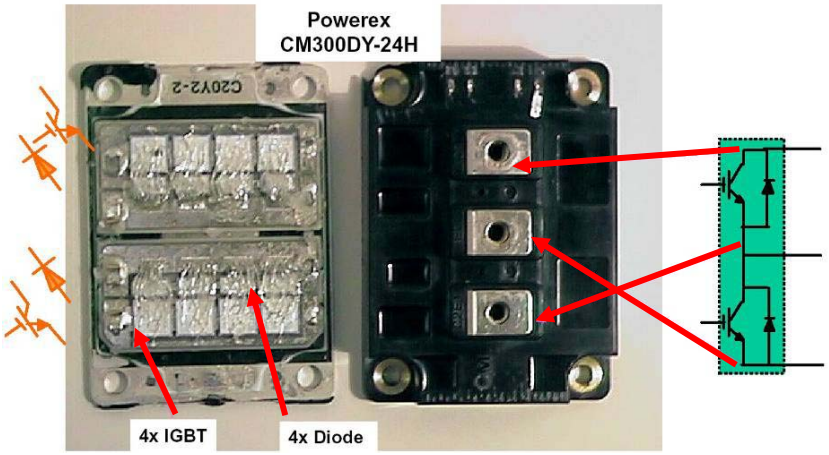

Figure 3.3 Layout of a high power IGBT module.

Figure 3.4 shows a top view of the physical layout of the high power multi-chip module. Several silicon chips are connected in parallel to construct a single high power device and two high-power IGBTs connected in SPDT (single-pole double-throw) configuration, one of the most common building cells in power electronic circuits.

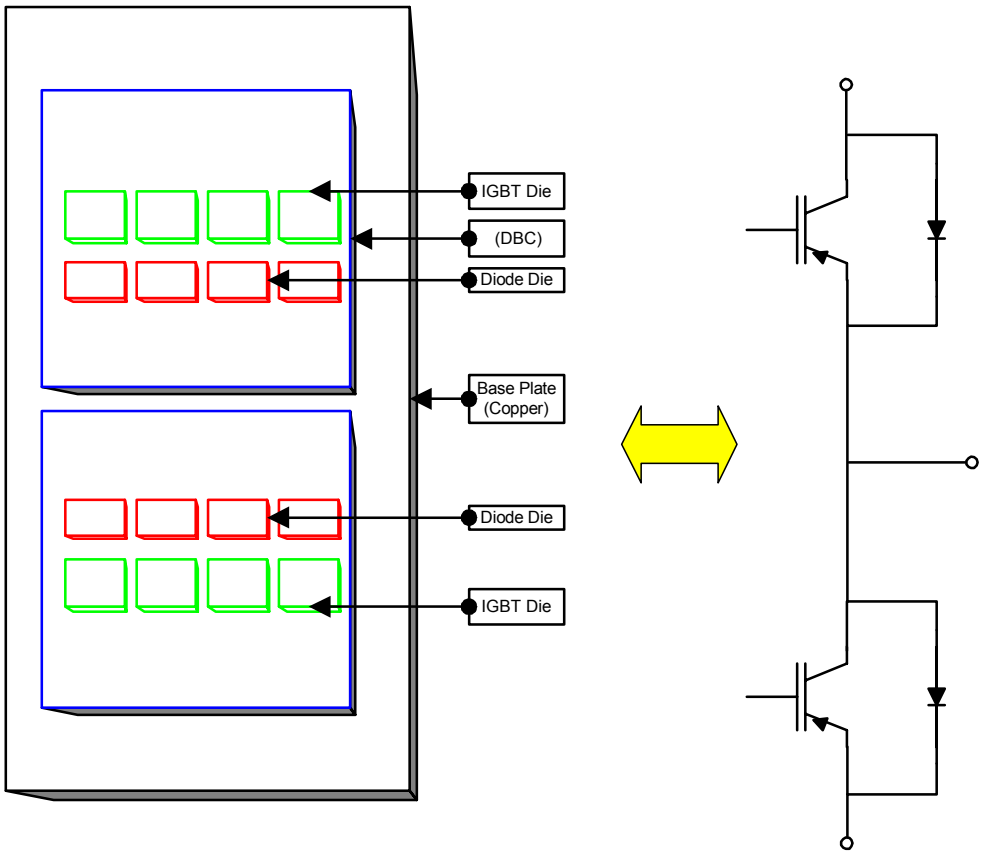

Figure 3.4 Internal Layout of a commercial PEM.

3.2. Development of the Thermal model

In the development of the thermal model for the power module, the module is divided into different regions that form thermal component building blocks. The thermal blocks are interconnected to form the thermal network that will be the thermal model of the module. For the half bridge module structure of Figure 3.4, the vertical heat flow is divided into four basic paths; one for each set of paralleled chips. Each of the heat flow paths contains a silicone chip, DBC, and baseplate. Figure 3.5 shows the heat thermal paths in which the lateral thermal coupling within the module takes place in the DBC for each pair of silicon die and in the baseplate for all the dies in the module.

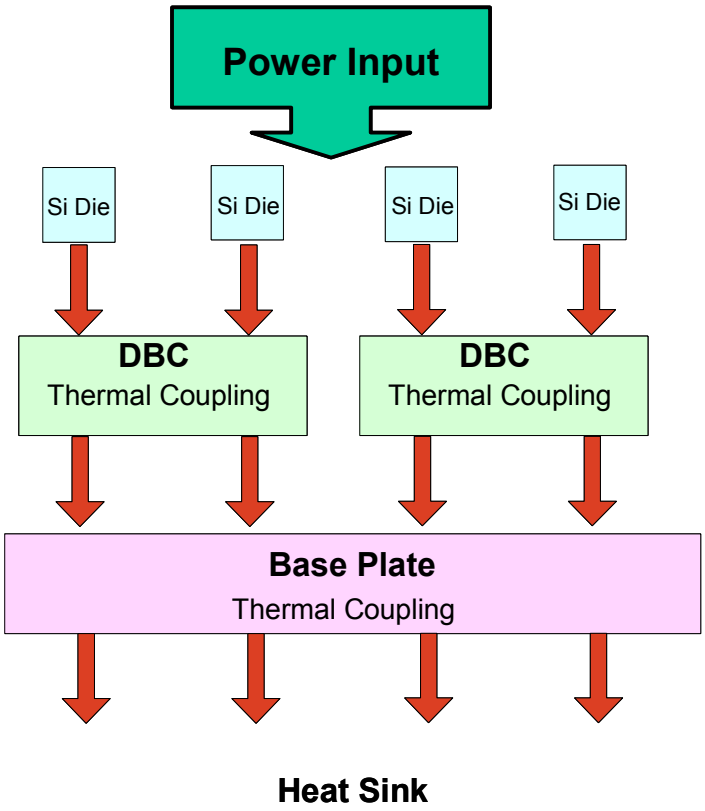

Figure 3.5 Heat flow paths in a PEM package.

3.3. Thermal modeling of a PEM-Based System

In the SABER circuit simulator, the model that describes each of the components of the system is accessed from the SABER libraries of standard component models or from user-defined SABER templates where the equations that describe the physical behavior of the new component types are implemented. SABER templates are written in the MAST® modeling language, which is similar to the C programming language with the addition of specially designed modeling constructs [35-36]. For example, Figure 3.6 is an abbreviated outline of the SABER template for the silicon chip thermal model. The

first statement in the template header defines the name of the model template, the names of the terminal connection points, and the names of the model parameters. The next statement defines the terminal types of the junction and header to be thermal_c type. The thermal_c type terminals have units of temperature (ºC) across the terminals and units of power *(W)* flowing through the terminals. The number statements in the header section define the default values of the model parameters. The equations that describe the behavior of the thermal component are defined in the body of the template.

```
#########################Template Header#########################
template chip_therm_src2 junct header  =   a ,thick, list, zoffset, wp,
                                           lambda, unif
thermal_c junct, header    # thermal type terminal

# default model parameters
number a = 0.1              #(cm**2)        #active area of chip
number thick = 0.05         #(cm)           #thickness of chip
number list = 1             #(0,1)          #flag for parameter output
number zoffset = 0.0        #(cm)           #depth of junct terminal for output
number wp = 0.005           #(cm)           #thickness of heat source
number lambda = 1           #               #source shape (wp/wj)
number unif = 100           #               #heat uniformity in element1
{ ###################Template Body ###################

## local declarations
parameters { # parameters calculated prior to simulation}
values { # nonlinear functions of system variables}
equations { # equations for system variables}
}
```

Figure 3.6 Abbreviated outline of SABER template for silicon chip thermal model.

To implement thermal component models into SABER templates, the models are formulated such that the components of power flow between the thermal nodes are expressed in terms of nonlinear functions of the system variables and in terms of the time

rate of change of these functions of the system variables. System variables for thermal models are the temperatures at the thermal nodes (thermal terminals and internal thermal nodes) and explicitly defined system variables that account for implicit model equations. The local declarations section of the template is used to define constants, designate internal nodes, and explicitly define the additional system variables (in addition to the node temperatures) needed to describe the state of the component. The parameters section of the template is used to calculate quantities that do not change during simulation, such as the node positions and heat capacitance. The functions of the system variables such as the nonlinear thermal conductivity of silicon for each node are implemented in the values section of the template. The equations section is then used to describe the components of power flow between the internal thermal nodes in terms of the quantities calculated in the values and parameters sections.

3.4. Silicon Chip thermal model

The basic chip_therm_src2 model has an internal thermal node for each discretization indices *i* at position *z,* and the terminal nodes are at the silicon chip surface junction and the chip-package interface header. Figure 3.7 shows an abbreviated form of the equation section of the chip_therm_src2 SABER template where only five internal nodes are indicated for simplicity (the actual model consists of a 10-node quasilogarithmically spaced grid). The first six statements of Figure 3.7 describe the heat conduction between the adjacent nodes using the thermal resistances (left-hand side of 2.18). The next five statements describe the components of power that are stored as heat energy in the thermal capacitance at each thermal node (right-hand side of 2.18). The last

four statements describe the dissipated power at each node due to the distributed heat source (described below). The equations section for the discretized heat diffusion equation has a similar form for all of the thermal component models except that each model uses a different method to calculate the discretization coefficients ($R_{i,i+1}$, and C_i) in the parameters and values sections of the template.

The silicon chip thermal model is a standard library component in the SABER software and it is based upon the rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The details of the model are given in [3].

```
#--------------------------------- Template Header ---------------------------------#

                                ###Template Body###

                                  ### Parameters###
values  {
          th = tc(header)+math_ctok
          t1 = tc(node1)+math_ctok
          etc…

          h1 = t1*c1
          h2 = t2*c2
          etc…

        }
equations {
           p(header -> node1)+= (th-t1)/rh1
           p(node1  -> node2)+= (t1-t2)/r12
           p(node2  -> node3)+= (t2-t3)/r23
           p(node3  -> node4)+= (t3-t4)/r34
           p(node4  -> node5)+= (t4-t5)/r45
           p(node5  -> case) += (t5-tc)/r5c
           p(case -> nodep)  += (tc-tp)/rp

           p(node1)+= d_by_dt(h1)
           p(node2)+= d_by_dt(h2)
           p(node3)+= d_by_dt(h3)
           p(node4)+= d_by_dt(h4)
           p(node5)+= d_by_dt(h5)
           p(nodep)+= d_by_dt(hp)

            }}
```

Figure 3.7 Values and equation sections for discretized form of heat diffusion equation.

The silicon chip thermal model is based upon the rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The chip thermal model also includes a distributed heat source option if the parameter $w_p > 0$, where the power dissipation density as a function of depth into the chip z is given by:

$$P(z,t) = \begin{cases} P_T(t) \cdot \dfrac{1-\lambda z/w_p}{1-\lambda/2} & \text{for } z \le w_p \\ 0 & \text{for } z > w_p \end{cases} \qquad (3.1)$$

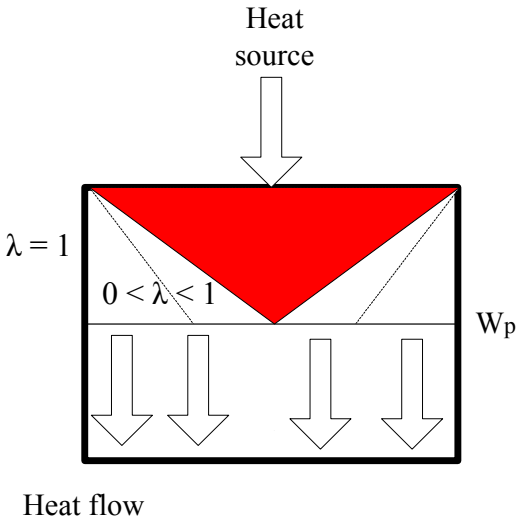

Figure 3.8 Heat flow in the silicon chip.

The heat source of equation (3.1) is triangular if the model parameter λ = 1 corresponding to a depletion region that extends from the surface into the chip, or trapezoidal if 0 < λ < 1 corresponding to a depletion region that is terminated by a high doped layer at w_p as show in Figure 3.8. For λ = 0 the power density is constant between 0 and w_p. Based upon equation (3.1) and the model parameters in the parameter list, the silicon chip thermal model calculates the fraction of heat source power that is dissipated

in each thermal element within the heat source f_i (i.e., fraction of power dissipated between $(z_{i-1} + z_i)/2$ and $(z_i + z_{i+1})/2$. The heat source power into each node during simulation is then calculated using $P_{di} = P_{d1} \cdot f_i / f_1$, where the power from the heat source into node 1 is given by $P_{d1} = (T_j - T_1)/R_{j1}$.

A logarithmically spaced grid is used by the chip thermal model to minimize the number of nodes required to accurately represent the dynamic temperature distribution for the full range of applicable power dissipation levels. To aid in the visualization of the transient temperature distribution, a quasi-logarithmically spaced grid is used which consists of an evenly spaced grid within segments where the segment size increases logarithmically with distance from the heat source. For improved modularity, the quasi-logarithmic grid spacing of the chip thermal model is implemented using a hierarchical approach. Figure 3.9 is an abbreviated outline of the 10 node, quasi-logarithmically spaced grid, chip thermal model *chip_therm_scr_10*. The parameters section of the template calculates the thickness of each segment and the z-axis offset from the silicon chip surface to the top of each segment. Each segment is then implemented by netlisting an instance of the five-node, evenly spaced grid, subchip thermal model. The offset parameter is used so that the output list of node positions for each segment is specified relative to the location of the chip surface.

```
#----------------------Template Header-----------------------#
template chip_therm_src_10_2 junct header  =         a,thick,list,wp,lambda,unif
#Template Body

parameters {

thick2 = 4/5*thick
thick1 = thick -thick2

zoffset1 = 0
zoffset2 = thick1


}
chip_therm_src2.top  junct  level1  =  a,thick1,list,zoffset1,wp,lambda,unif
chip_therm2.bot      level1 header  =   a,thick2,list,zoffset2

}
```

Figure 3.9 Abbreviated outline of the SABER template for 10-node, quasi-logarithmically spaced grid, silicon chip thermal model.

Using the values of the model parameters specified in the netlist, the silicon chip thermal model calculates the positions of the internal nodes z_i to form the logarithmic grid spacing. The node positions, the chip area, and the instantaneous node temperatures, are used to evaluate the model functions $R_{i,i+1}$, H_i and P_{di} that are used by the equations section in Figure 3.7. The node positions, heat capacitance and fraction of power dissipated within each element are calculated in the parameters section of the SABER template prior to simulation time because they do no depend on simulator systems variables. These calculated parameters can be listed when the templates are loaded by setting the parameter list > 0. The thermal conductivities, thermal resistances, heat energies, and the dissipated heat source power for each node are calculated in the values section because they depend upon the instantaneous temperatures of the thermal nodes,

which are simulator system variable. Because the expression for the thermal conductivity of silicon in equation (2.16) is not defined for $T \leq 0$ K, the calculations of thermal conductivity must be bounded to prevent numerical computation errors.

In Figure 3.10, we can see the quasilogarithmic distribution of the nodes used to place the thermal resistance in the silicon die. It is divided in to main sections one of 1/5 and the other 4/5 of the total length of the die. This follow the logarithmic grid spacing principle, the silicon die model includes 10 thermal nodes in the heat conduction path from the die header toward the DBC. Each one of the section was sectionalized with five internal nodes. Notice that the top and bottom nodes of each section have only a length of 1/10, the others have 1/5 of the corresponding section. Between nodes a thermal resistance was placed using the nonlinear thermal conductivity of the silicon that varies with temperature as show in equation (2.16).

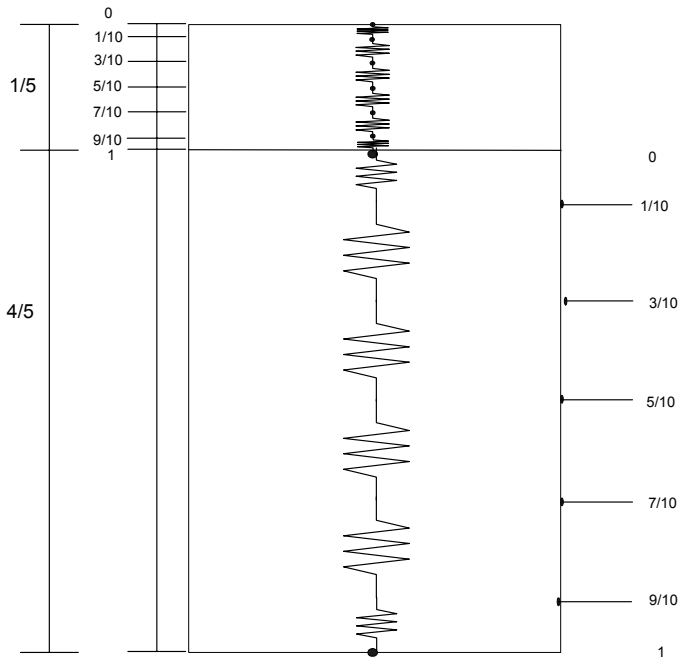

Figure 3.10 Quasilogarithmic distribution of the nodes.

3.5. Package Thermal Model

The package in a power electronic module PEM is composed of a DBC and a baseplate. The key of its design relies is optimizing the dimension of the package for thermal management and minimizing the physical stresses. Here the SABER implementation of the DBC and baseplate is presented.

The discretized heat equation of the package thermal model is formulated similarly to the silicon chip thermal model except that the expressions used to calculate the thermal resistances, thermal capacitances, and the heat energies are different. The package model describes the two-dimensional lateral heat spreading, the die attachment thermal resistance, and the heat capacity of the package periphery. In accordance with the logarithmic grid spacing principle, the DBC model of the package includes five thermal nodes in the heat conduction path from the package header toward the baseplate, and two nodes in the baseplate toward the heat sink. The package periphery is modeled as an additional thermal node that is not in the direct heat conduction path and accounts for the remainder of the heat capacitance outside of the main heat conduction path. The parameters for the generic package thermal model include the chip area, the location of the chip on the package header, the width of the header, the length of the header, and the thickness of the header. Based upon these parameters, the discretization coefficients are calculated in the parameters section of the template and can be listed when the templates are loaded by setting appropriate options in the program.

Thus, various package thermal component models can be generated from the generic package template by specifying structural and material parameters, and the user does not need to calculate the internal thermal resistances and thermal capacitances.

The lateral heat spreading in the package results in an effective heat flow area that increases with depth into the package [3]. In the model, the effective heat flow area at each depth into the package is obtained by combining the components of heat flow area due to the cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip. For $r_{i+1} - r_i \ll r_i$, one can find from Taylor series expansions that the spherical (r, θ, ϕ) and cylindrical (r, z, θ) components of thermal capacitance and thermal resistance are given approximately by equations (3.3) and (3.4) given in Table 3.1 for the rectangular coordinate system with y- and x-axis symmetry [3]. The expression for the area A is replaced by equation (3.6) given in Table 3.2 for the cylindrical coordinate system with z- and θ-symmetry and equation (3.10) given in Table 3.3 for the spherical coordinate system with θ- and ϕ- symmetry, respectively. This is a reasonable approximation because the heat flow area is dominated by the area of the chip for small distances into the package and the cylindrical and spherical components of heat flow area are important only for larger distance into the package where $r_{i+1} - r_i \ll r_i$, is satisfied.

Table 3.1 Rectangular coordinate y- and x- Axis symmetry.

$$A\frac{\partial}{\partial z}\left(k(T)\frac{\partial T}{\partial z}\right)=A\rho c\frac{\partial T}{\partial t} \tag{3.2}$$

$$C_i = A\rho c\left(z_{i+1}-z_{i-1}\right)/2 \tag{3.3}$$

$$R_{i,i+1}=(z_{i+1}-z_i)/(A\cdot k_{i,i+1}) \tag{3.4}$$

Table 3.2 Cylindrical coordinate z- and θ- Axis symmetry.

$$A\frac{1}{r}\frac{\partial}{\partial r}\left(k(T)r\frac{\partial T}{\partial r}\right)=A\rho c\frac{\partial T}{\partial t} \tag{3.5}$$

$$A = 2\pi r\gamma z \tag{3.6}$$

$$C_i=\pi\gamma z\rho c\left(\left(\frac{r_{i+1}+r_i}{2}\right)^2-\left(\frac{r_i+r_{i-1}}{2}\right)^2\right) \tag{3.7}$$

$$R_{i,i+1}=\frac{1}{2\pi\gamma z k_{i,i+1}}\ln\left(\frac{r_{i+1}}{r_i}\right) \tag{3.8}$$

Table 3.3 Spherical coordinate θ- and ϕ- Axis symmetry.

$$A\frac{1}{r^2}\frac{\partial}{\partial r}\left(k(T)r^2\frac{\partial T}{\partial r}\right)=A\rho c\frac{\partial T}{\partial t} \tag{3.9}$$

$$A = 4\pi r^2\gamma \tag{3.10}$$

$$C_i=\frac{4}{3}\pi\gamma\rho c\left(\left(\frac{r_{i+1}+r_i}{2}\right)^3-\left(\frac{r_i+r_{i-1}}{2}\right)^3\right) \tag{3.11}$$

$$R_{i,i+1}=\frac{1}{4\pi\gamma k_{i,i+1}}\left(\frac{1}{r_i}-\frac{1}{r_{i+1}}\right) \tag{3.12}$$

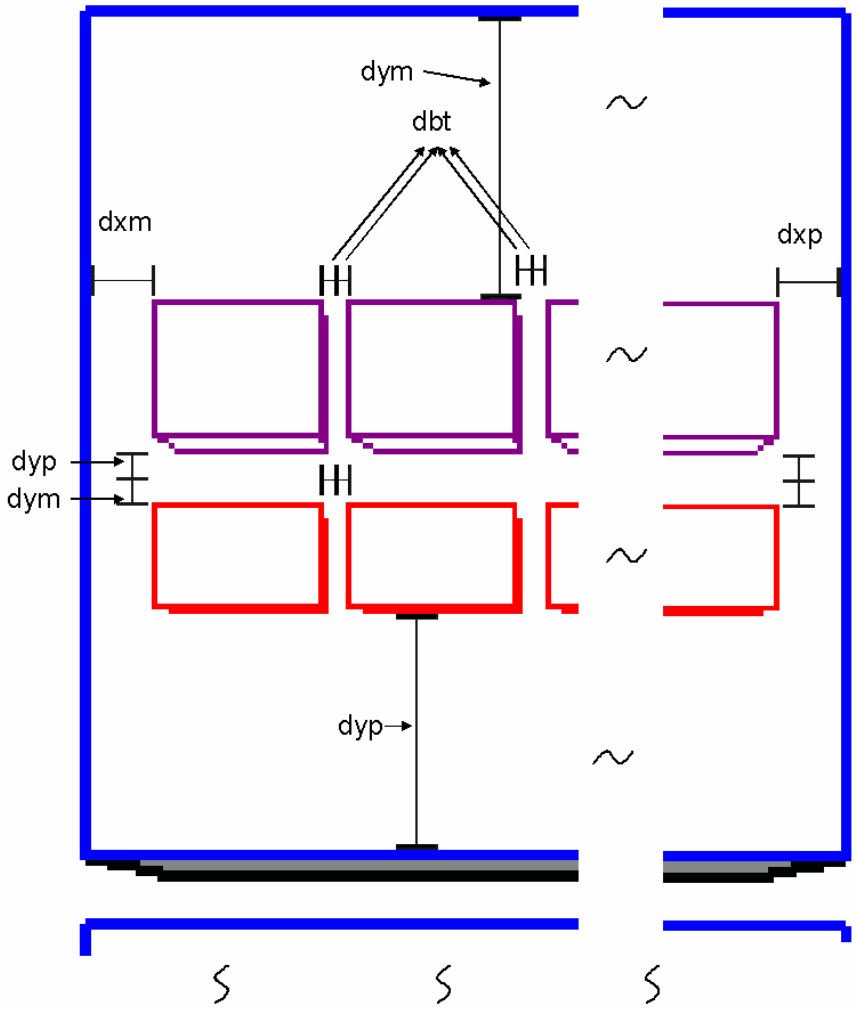

Figure 3.11 Definition of boundary variables.

Since the heat does not spread laterally beyond the edges of the package, the radius that the heat spreads beyond each edge of the chip (rxp_i, rxm_i, ryp_i, rym_i, rbt_i) is limited in the model for each node at depth z_i by the distance from each edge of the chip to the edges of the package and an invisible boundary in equation (3.13). Where rxp_i is the radius in the positive x direction, rxm_i is the radius in the negative x direction, ryp_i is the radius in the positive y direction, rym_i is the radius in the negative y direction, and rbt_i is the radius between chips. The boundary between the parallel chips exits because each

one generates the same amount of heat (dbt_i) where dbt_i is the boundary between chips that is equal to half the distance between chips. In similar way dxp_i is the distance from the edge of the positive extreme chip to the edge of the package in the x direction, dyp_i is the distance from the edge of the positive extreme chip to the edge of the package in the y direction, dxm_i is the distance from the edge of the negative extreme chip to the edge of the package in the x direction, and dym_i is the distance from the edge of the negative extreme chip to the edge of the package in the y direction at depth z_i. Figure 3.11 shows the location of the boundaries in a section of the multi-chip package module, the location of the radius of the heat spreads (rxp_i, rxm_i, ryp_i, rym_i, rbt_i) are in the same direction of the corresponding boundary, for example rxp_i is in the same direction as dxp_i.

$$rxp_i = \begin{cases} z_i & \text{for } z_i \le dxp \\ dxp & \text{for } z_i > dxp \end{cases} \tag{3.13}$$

We assume that the boundary is located right in the middle between chips. We consider cylindrical and spherical components when quantifying the heat flow area. The cylindrical component of the heat flow area is given by the areas of the one-quarter cylinders at each edge of the chip by equation (3.14):

$$\begin{aligned} Acyl_i = {} & \frac{\pi}{4} W_{ch}(rym_i + ryp_i) + n\frac{\pi}{4} L_{ch}(rxm_i + rxp_i) + \\ & (n-1)\frac{\pi}{4} W_{ch}(rbt_i^2) \end{aligned} \tag{3.14}$$

where one-half of the lateral heat spreading has been assumed to be towards the package periphery and the other half towards the package case. The spherical component of heat flow area is then given by the area of the one-eighth spheres at each corner of the chip by equation (3.15):

$$Asph_i = \frac{\pi}{4} W_{ch} (rym_i + ryp_i) \cdot (rxm_i + rxp_i) + (n-1) \frac{\pi}{4} W_{ch} (2 \cdot rbt_i) \cdot (rxm_i + rxp_i) \quad (3.15)$$

These expressions for the cylindrical and spherical components of heat flow area at the i^{th} node are a modified version of those developed in [3] to be able to characterize the geometry of a power module as presented in Figure 3.12.

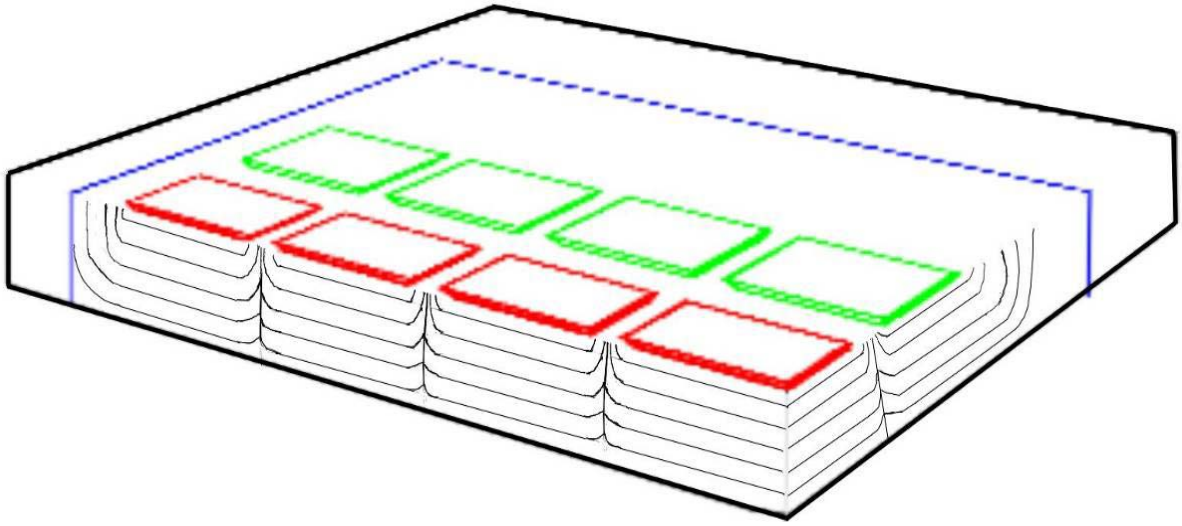

Figure 3.12 Heat flow paths inside the PEM.

The value of the effective heat flow area used to calculate the thermal resistance and capacitance at each node is then given by Aeff = Acyli + Asphi + Achip. The value of the effective heat flow area at the package case is also used as a parameter for the heat sink thermal model *area_heat*.

The effective areas for each of the nodes are calculated in the parameter section of the SABER model and take in to consideration the boundaries of the package. The area

changes with depth, also temperature conductivity changes with the materials involved between each pair of nodes. These values are used to calculate the thermal resistance between nodes using equation (3.16):

$$R_{i,i+1} = \frac{thick_{i,i+1}}{\sum_{m=a}^{n}\left(\frac{k_m}{f_{m,(i,i+1)}}\right)\cdot\left(\frac{A_i + A_{i+1}}{2}\right)} \tag{3.16}$$

where $R_{i,i+1}$ is the thermal resistance between node i and node $i+1$, k_m is the thermal conductivity of material m, $f_{m,(i,i+1)}$ is the fraction of material m in between node i and $i+1$ and A_i is the area of node i. Also the average of the effective area between nodes is used to calculate the volume between nodes. The thermal capacitance is given by equation (3.17):

$$C_i = v_i \sum_{m=a}^{n}\left(f_{m,i}\rho_m c_m\right) \tag{3.17}$$

where C_i is the thermal capacitance in layer i, v_i is the volume of layer i, ρ_m is the material density of material i and c is the specific heat of material i and implemented in template show in Figure 3.13.

```
#------------------------------ Template Header --------------------------------#

                                ###Template Body###

                                ### Parameters###
values  {
          th = tc(header)+math_ctok
          t1 = tc(node1)+math_ctok
          etc…

          h1 = t1*c1
          h2 = t2*c2
          etc…

        }
equations {
           p(header -> node1)+= (th-t1)/rh1
           p(node1  -> node2)+= (t1-t2)/r12
           p(node2  -> node3)+= (t2-t3)/r23
           p(node3  -> node4)+= (t3-t4)/r34
           p(node4  -> node5)+= (t4-t5)/r45
           p(node5  -> case) += (t5-tc)/r5c
           p(case -> nodep)  += (tc-tp)/rp

           p(node1)+= d_by_dt(h1)
           p(node2)+= d_by_dt(h2)
           p(node3)+= d_by_dt(h3)
           p(node4)+= d_by_dt(h4)
           p(node5)+= d_by_dt(h5)
           p(nodep)+= d_by_dt(hp)

            }}
```

Figure 3.13 Values and equation sections for discretized form of heat diffusion equation.

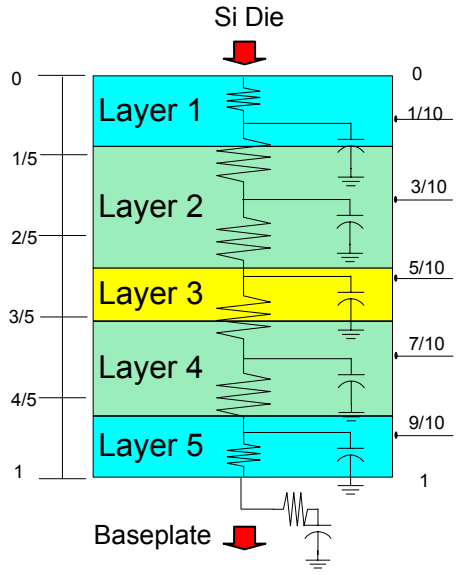

Figure 3.14 Distribution for the vertical nodes for the DBC.

The distribution for the vertical nodes for the DBC is similar to the silicon die previously explained as show in Figure 3.14 where the arrow represent the direction of the heat flow. The difference consist that only one section was use and the material in the DBC is composed of five layers of different material in this case. It is divided following the logarithmic grid spacing principle, the DBC model includes five thermal nodes in the heat conduction path from the DBC header toward the baseplate. As show previously in equations (3.16) and (3.17), the amount of each material between node for the thermal resistance and in the Layers for the thermal capacitance is taken in consideration. Notice again that the top and bottom nodes of each section have only a length of 1/10, the others have 1/5 of the corresponding section. Between nodes, a thermal resistance was placed using the thermal conductivity properties of the composed material. The variation in temperature of this material neglected due to the range of operations. To calculate the thermal capacitance the volume affected due to the heat spreading and the DBC is divided in five equally spaced regions.

The power electronic module is composed of two DBC, where an IGBT and a power diode are placed. Each IGBT is composed of four devices in parallel working as one. So each DBC thermal model is composed of the vertical nodes previously explained and a thermal coupling resistance is placed between the last nodes corresponding to each chip as show in Figure 3.15.

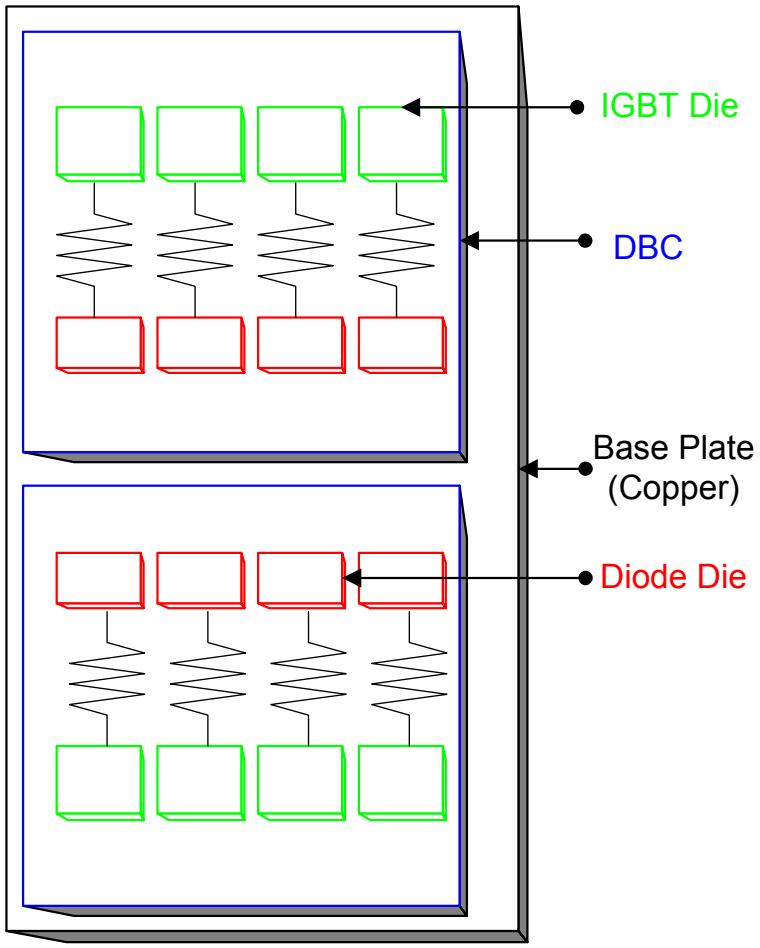

Figure 3.15 Thermal coupling resistance placed between the last node for each DBC.

In the baseplate, the node and layer distribution are made in the same way as in the DBC with the advantage that is composed only of copper. All the heat loss in the power electronic module flows from the two DBC through the baseplate to a heat dissipation mechanism, like a heat sink. So the two nodes of each DBC are connected to the baseplate having it four input and four outputs made out of the vertical nodes previously described. In addition, a thermal coupling resistance is placed between the last nodes of each terminal as show in Figure 3.16.

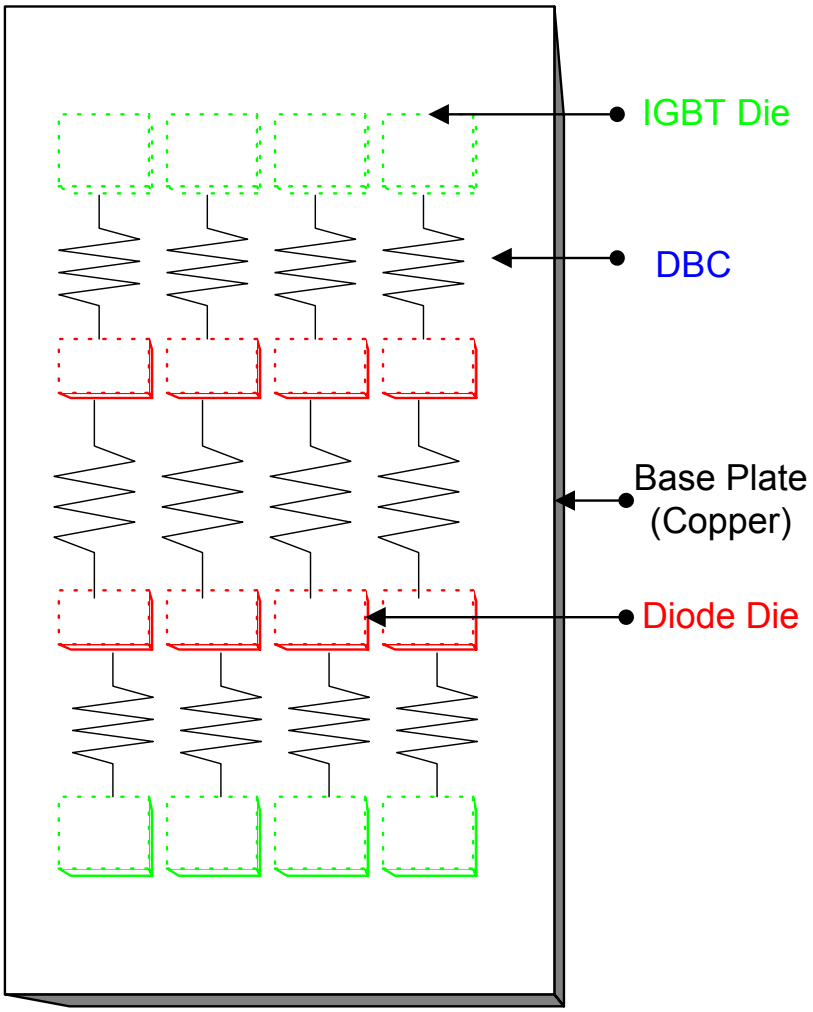

Figure 3.16 Thermal coupling resistance placed between the last nodes in the baseplate.

3.6. Summary

In this chapter, the differences between a single chip and multi-chip PEM in developing a thermal model are discussed. Also a detailed description of the implementation of the thermal component network for the silicon chip and package thermal models is presented.

Chapter 4

Thermal modeling of a PEM-Based Three Phase Inverter

In this chapter, we describe the three phase inverter system which is used to validate the multi-chip PEM thermal model. We also discuss the development of the heat sink thermal model and its use to couple the multi-chip PEM thermal model to obtain a thermal model for a three-phase inverter.

4.1. PEM-Based Three Phase Inverter Thermal Model

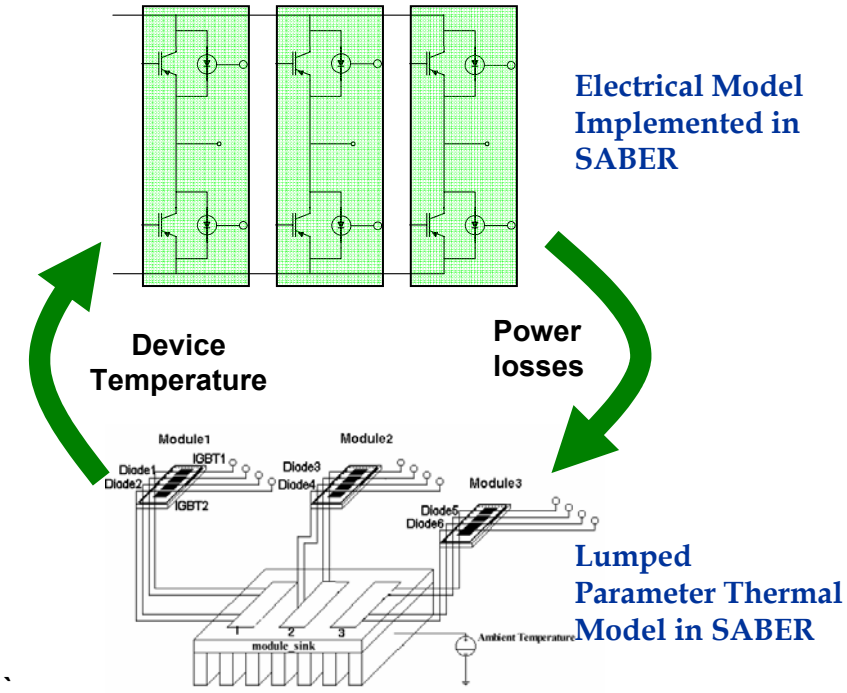

Figure 4.1 SABER electrical and thermal network model interconnection of the experimental system.

The inverter uses three half-bridge IGBT modules mounted on a common heat sink. Figure 4.1 shows the schematic of a three phase inverter and the SABER schematic of its thermal model developed in this work to demonstrate and validate the multi-chip power module package and multi-module heat sink thermal models.

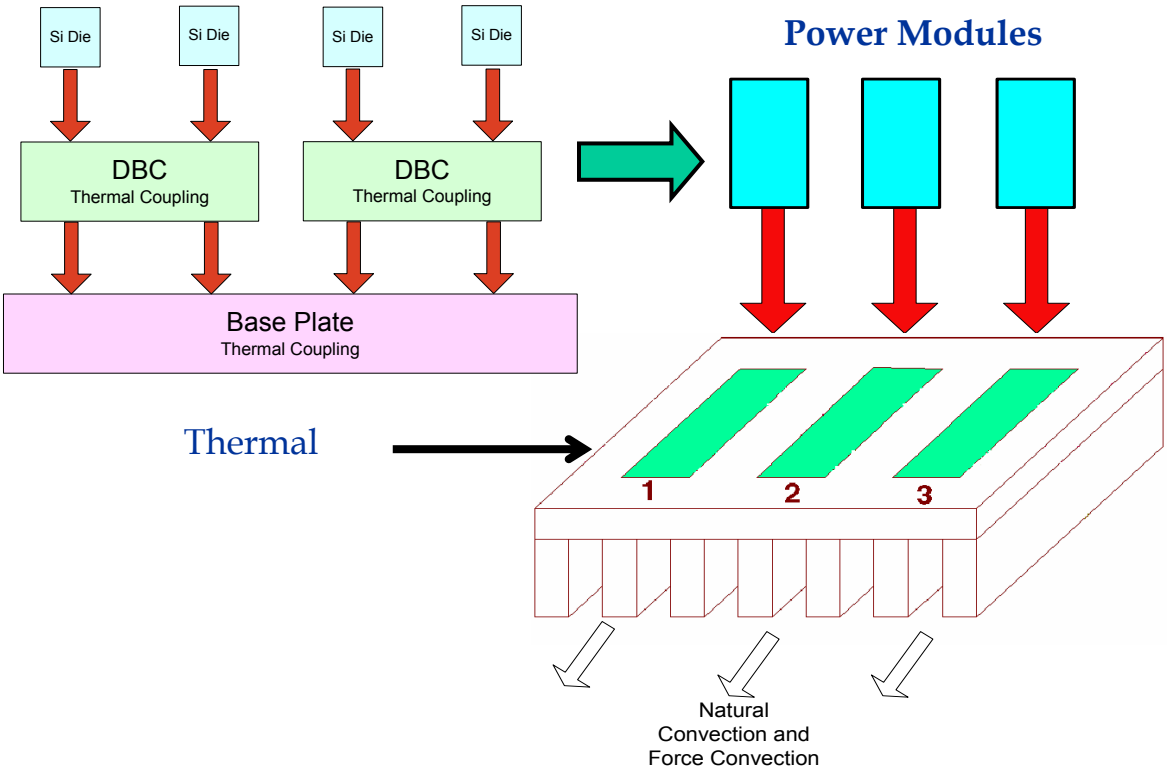

Figure 4.2 Representation of the heat flow across the thermal network.

The thermal model for the three phase inverted is obtained by combining the three PEM thermal model and the heat sink thermal model as show in Figures 4.1 and 4.2. A portion of the electrical power delivered to the PEM electrical terminals is dissipated as heat in the silicon dies. The thermal resistance and capacitance in the baseplate, DBC, and silicon dies are calculated as explained in Chapter 3. The four heat flow paths originated in the silicon dies pass through the DBC and baseplate thermal network and

continue their way to the heat sink. Where the thermal resistance and capacitances are calculated and the heat flows through this network until reach the fins that dissipated the heat by natural and forced convection.

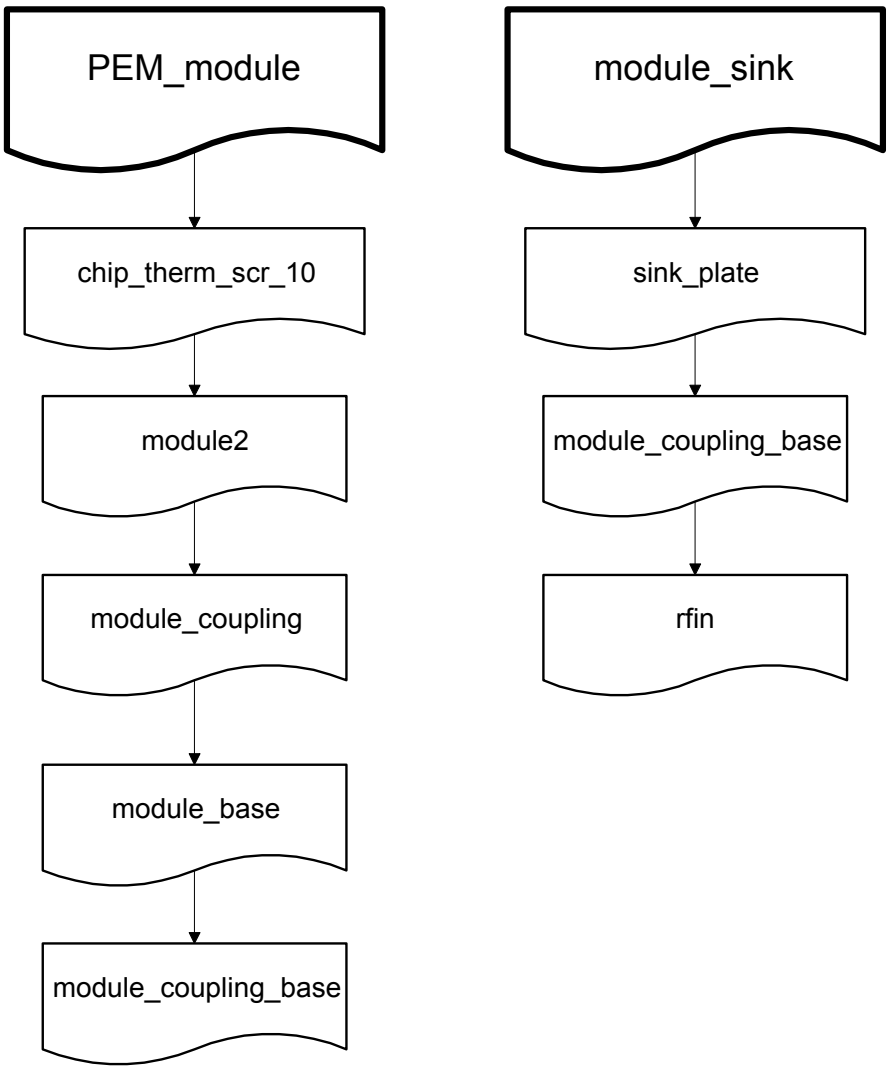

Figure 4.3 Hierarchical representation of package module and heat sink module templates.

Figure 4.3 presents a hierarchical representation of the subtemplates of which the package module and heat sink module templates were developed in SABER. This hierarchical representation shows the subtemplates that together form the PEM and heat

sink thermal models. In the PEM model the *chip_therm_src_10*, receive the heat dissipated in the electrical network through an external terminal, where the quasilogarithmically spaced nodes and their corresponding resistances for the silicon die are calculated. Its final node is connected to *module2*, where quasilogarithmically spaced nodes and their corresponding resistances and capacitances for the DBC are calculated. In *module_coupling* template the heat flow paths in the DBC are couple through a thermal resistance connected in the last node of *module2*. Them the last node of module2 is connected to *baseplate*, where quasilogarithmically spaced nodes and their corresponding resistances and capacitances for the baseplate are calculated. In *module_coupling* template the heat flow paths in the baseplate are couple through a thermal resistance connected in the last terminal of *baseplate*. The final node corresponding to each of the devices in the *PEMmodule* template finish with and external node which can be connected to an additional heat dissipation device like a heat sink.

In the heat sink model *sink_plate*, receive the input of the heat flow from the PEM baseplate external terminal, here the quasilogarithmically spaced nodes and their corresponding resistances for the heat sink base are calculated. Its final node is connected to *module_coupling_base* template to couple the heat flow paths in the heat sink through a thermal resistance connected in the last terminal of *sink_plate*. Finally the last *sink_plate* terminal is connected to *rfin* where the nonlinear equation for natural and forced convection are calculated and the heat is dissipated thought the ambient which temperature is set through an external terminal in *sink_plate*.

4.2. Heat sink Thermal Model

The heat sink thermal component model includes a discretized heat equation similar to the chip and package thermal models where the discretization coefficients are determined by the structural and material parameters of the heat sink as well as the value of *area_heat* determined by the package models. The heat sink model describes: the lateral thermal coupling between IPEM over the heat sink, the semi-cylindrical heat diffusion from the area beneath the package toward the heat sink fins, and the nonlinear forced and natural convection heat transfer from the heat sink fins to the ambient terminal. The parameters for the heat sink template include the package heat source area for each of the regions of each device, the thickness of the heat sink base, and the location of the package on the heat sink. It also needs the fin area, the fin height, and the air velocity for forced convection.

In the vicinity of the heat source (location of package), the heat diffuses vertically toward the back of the heat sink body and also spreads laterally, as described for the package models. After the heat has diffused to the back of the heat sink body beneath the heat source, the heat flow continues diffused vertically and also spreads laterally beyond the location of the heat source. The same happen in each of the four connection of each module. After that the heat is transferred laterally around the heat sink by thermal resistance between adjacent nodes in the x and y direction.

In accordance with the logarithmic grid spacing principle, three thermal nodes are required to describe the vertical heat flow through the base region. At the heat sink fins, the heat is transferred to the ambient terminal by forced and natural convection. The

natural convection thermal resistance is given in [34], where R_{nat} is the thermal resistance due to natural convection and given by equation (4.1) and (4.2), where T_f is the fin temperature, T_a is the ambient temperature, h'_{nat} is the natural convection, and A_{fin} is the fin area.

$$h'_{nat} = 4.84 \cdot 10^{-4} \frac{A_{fin}}{P_{fin}^{0.35}} \tag{4.1}$$

$$R_{nat} = \frac{1}{h'_{nat} \cdot (T_f - T_a)^{0.35}} \tag{4.2}$$

The forced convection thermal resistance is given by equations (4.3)-(4.5) [34], where R_{for} is the thermal resistance due by forced convection, h'_{for} is the forced convection and v_{air} is the air velocity.

$$f = \begin{cases} 1.7 + 0.148 \cdot \ln(v_{air}/508) & \text{for } v_{air} \le 508\, cm/s \\ 1.7 + 0.433 \cdot \ln(v_{air}/508) & \text{for } v_{air} \le 508\, cm/s \end{cases} \tag{4.3}$$

$$h'_{for} = f \cdot 4.88 \cdot 10^{-4} \frac{A_{fin}}{\sqrt{Z_{fin}}}, \tag{4.4}$$

$$R_{for} = \frac{1}{h'_{for} \cdot \sqrt{v_{air}}} \tag{4.5}$$

```
#---------------------------------- Template Header----------------------------------------------
template module_sink module connections ambient = Parameters
thermal_c  module connections

#default model parameters
{
###Template Body ###
# local declarations

sink_plate.module1q1 case1q1 fin1q1                    =          Parameters
# SAME FOR EACH NODE

# Coupling between components in each module

module_coupling_base.1 fin1q1 fin1d1                   =          Parameters

module_coupling_base.6 fin2d2 fin2q2                   =          Parameters

module_coupling_base.8 fin3d1 fin3d2                   =          Parameters

# Coupling between components in each module

module_coupling_base.10 fin1q1 fin2q1                  =          Parameters
module_coupling_base.14 fin2q1 fin3q1                  =          Parameters

rfin.1q1      fin1q1 ambient                           =          Parameters
rfin.1d1
# SAME FOR EACH TERMINAL
}
```

Figure 4.4 Overview of the heat sink implemented in MAST.

where the fin-to-ambient thermal resistance is the parallel combination of the forced convection thermal resistance, the natural convection thermal resistance, and the shunt chases mounting thermal resistance. Because h'_{nat} and h'_{for} do not depend upon the simulator system variables, they are calculated in the parameters section of the SABER template and can be listed when the templates are loaded. Figure 4.4 shows and illustrative part of the heat sink template developed as part of this work. Figure 4.4 present the path of the heat thought the thermal network.

4.3. Summary

In this chapter, the thermal model for a three phase inverter system which is used to validate the multi-chip PEM thermal model is described. Also a detailed description of the implementation of the thermal component network for the heat sink thermal models is given.

Chapter 5

Experimental Model Calibration and Validation

In this chapter, we describe the experimental data acquisition and calibration temperature sensitive parameters. And the results of calibration and validation are presented.

5.1. Experimental Data acquisition and calibration temperature-sensitive electrical parameters

The thermal model for the PEM and the three phase inverter developed in Chapters 3 and 4 was calibrated and validated using an experimental setup shown in Figure 5.1. The System was first built at the National Institute of Standards and Technology (NIST) and reproduced at the University of Puerto Rico in Mayagüez. The testbed consisted of a computer-based data acquisition system based on Lab Windows-CVI from National Instruments with digital multimeters and recorders as shown in Figure 5.1. and 5.2

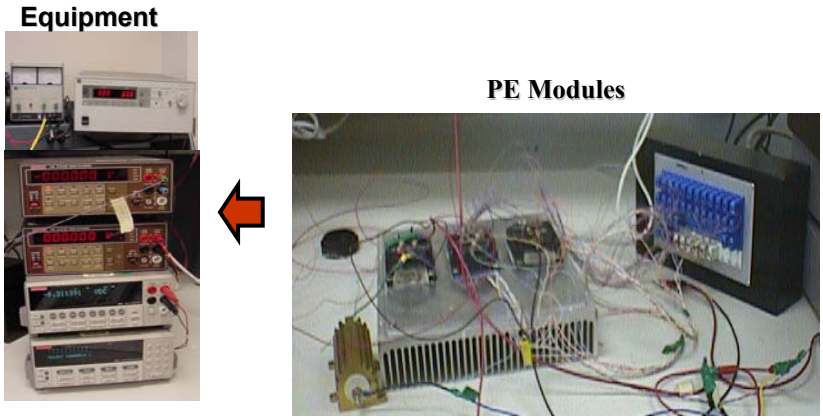

Figure 5.1 Experimental Setup used for the validation and calibration.

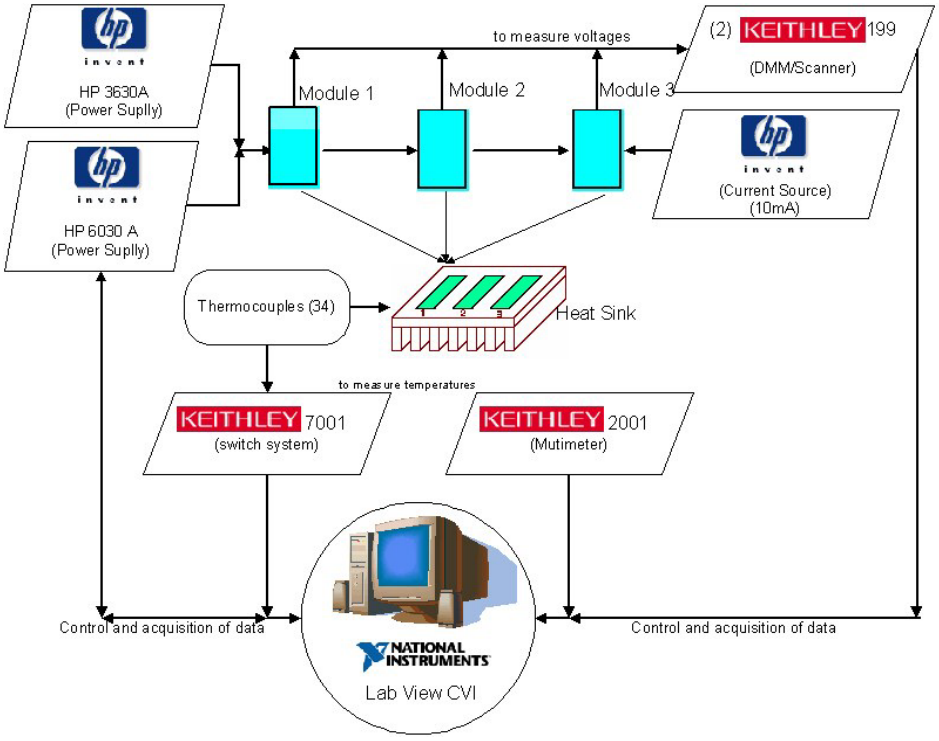

Figure 5.2 Schematic of the data acquisition system used for the validation and calibration.

The system acquires temperature at different points in the three-phase inverter and voltages at the module inputs. Communication between instruments and the computer is

based on the GPIB protocol. Two programs were developed: one for calibration and one for data acquisition and junction temperature estimation.

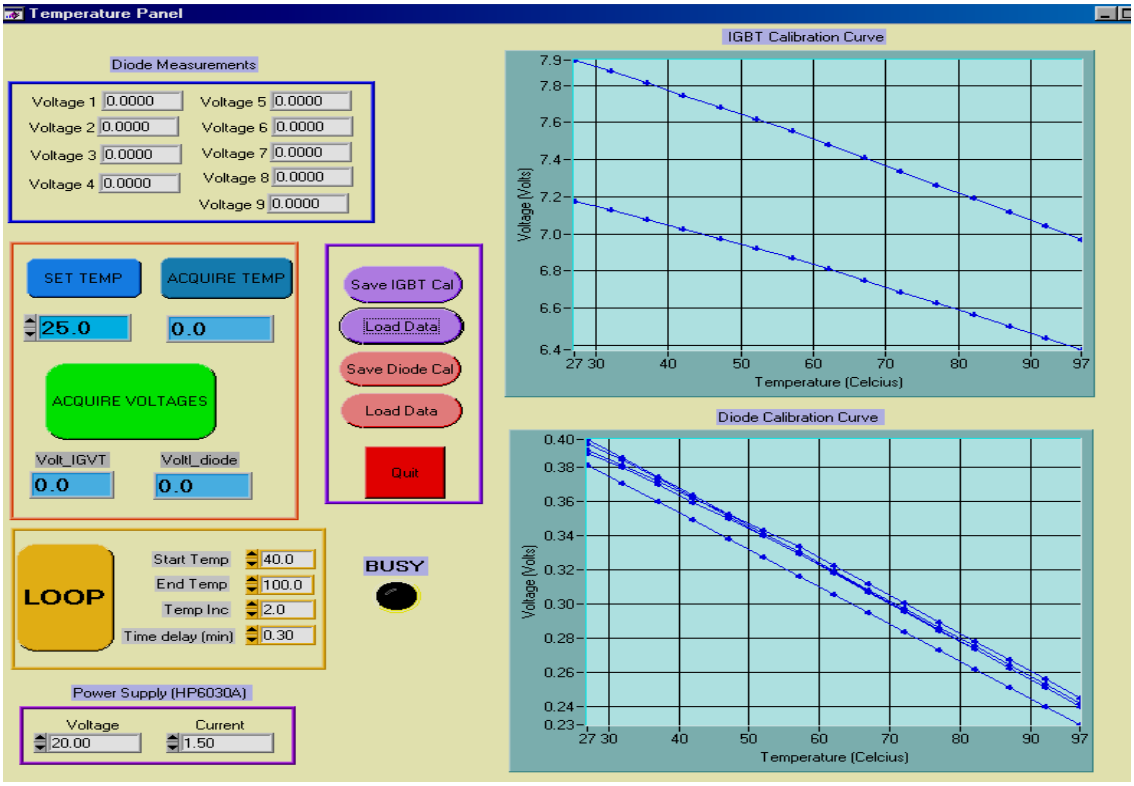

Figure 5.3 Lab Windows CVI Calibration Panel.

The calibration program panel is shown in Figure 5.3. The diodes are calibrated for their temperature-forward voltage characteristics, and the IGBT are calibrated for their temperature-threshold voltage characteristic using a temperature controlled heat sink. This enables the semiconductor devices to be used as sensors of the device junction temperatures using temperature-sensitive electrical parameters TSEP [35], since the junction temperature of a device is not directly measurable. Pressing "LOOP" initiates the calibration cycle where temperature is changing and voltage is measured until the

final temperature is reached. During that time the measured data is displayed graphically for the diodes and the IGBT. The text boxes in the right of the "LOOP" button are for setting the temperature controller. The collected data is used later by the transient panel to estimate the device junction temperature from terminal voltage measurements.

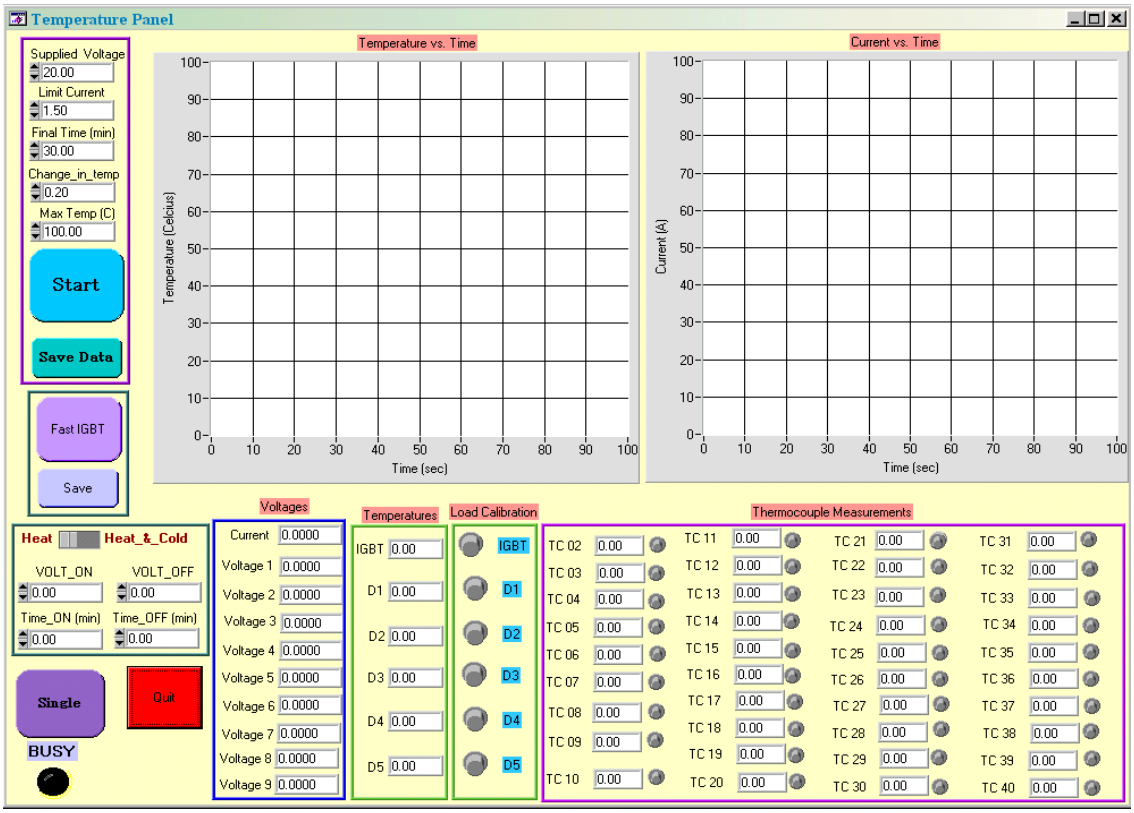

Figure 5.4 Lab Windows CVI Transient Panel.

The transient program panel is show in Figure 5.4. This is the program used to collect the data measured at the places where the thermocouples are located in the heat sink and estimates the transient junction temperatures from the measured gate to drain voltage using the calibration curves determined with the calibration program [36]. The collected data will be used to validate and calibrate the model. The voltages are

measured at some points in the modules in order to calculate the voltage at the IGBT and the diodes. As can be seen in Figure 5.4, the panel obtained by this program allows the user to select the thermocouple and the diodes that are desired to examine. The user set the voltage that the HP 6030A will supply. This program has three main buttons; the simplest is the "Single" button. By Pressing "Single" the user gets the voltage and the temperature of the diodes, IGBT, and thermocouples at a particular instant of time. Using the "Start" button, the user gets the temperature of the diodes, IGBT, and selected thermocouples for the amount of time selected. The "Fast IGBT" button just gets the temperature of the IGBT for the amount of time selected, and since is one measurement the data resolution is higher.

5.2. Model Calibration

The test circuit built for the model calibration and validation experiments is presented in Figure 5.5 indicating the interconnection of the top IGBT of the first module, and the interconnection of the free wheeling diodes of the remaining IGBT in the first module and the other two modules of the inverter.

The IGBT is biased to act as a 150 watts constant-power source, and the diodes are biased with a constant-power dissipation of 10 watts and are used as temperature indicators. The electrical circuit of the three phase inverter system was implemented so the power dissipation in the active IGBT (IGBT1) is achieved by operating the IGBT in the active region, and a high power 10Ω resistor is used for feedback stabilization, and the diodes 2-5 are biased with a constant power dissipation of 10 watts to be used as

temperature indicators. A one ampere current is applied to the active IGBT. The one ampere current is achieved by controlling the gate voltage until reach one ampere at about 18 volts. With this configuration the power dissipation through the IGBT is approximately equal to the magnitude to the voltage of the drain since the source voltage is small and the current through the IGBT is one ampere.

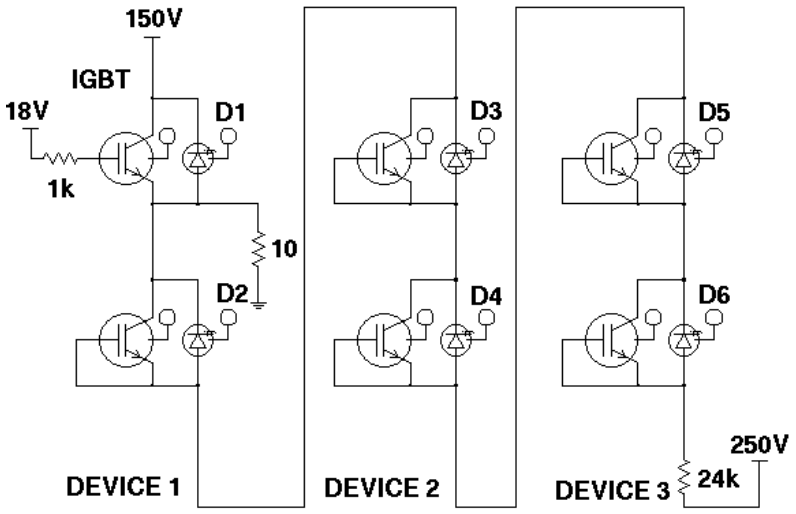

Figure 5.5 Schematic for the experimental circuit.

The 10 watts power dissipation in diodes 2-5 is achieve by connecting them in series with a current of 10 miliamperes. This was done by connecting the diodes in series with a 24kΩ resistance and a voltage source of 250 volts.

The experimental data collection began when power is applied to the IGBT. The temperature of the heat sink and heat sink fins are measured at thirty different points using thermocouples, and all voltage nodes are monitored as the heating progresses and all voltage points are monitored by an automated data-collection system.

Using the measured data, the model is calibrated modifying the *"fin_area_per_area"* and the *"thick_base"*. The *"fin_area_per_area"* parameter relates the fin area to surface area of the heat sink, in this case this parameter was changed from 10.67 to 8.13. The main effect from changing this parameter is the maximum temperature achived since this parameter control the dissipation of heat to the ambient. The *"thick_base"* parameter is the thickness of the baseplate of the module and was change from 0.3cm to 0.25cm. The main effect from changing this parameter is the thermal mass in the module which control how fast the module can change in temperature.

The model was calibrated using a 150 watts step that change to 75 watts dissipation through the IGBT and them was changed to 75 watts at around 15000 seconds. A constant dissipation of 10 watts through the diodes was maintained through the entire experiment. Figure 5.6 shows the calibrated model response while Figure 5.7 shows the experimental response.

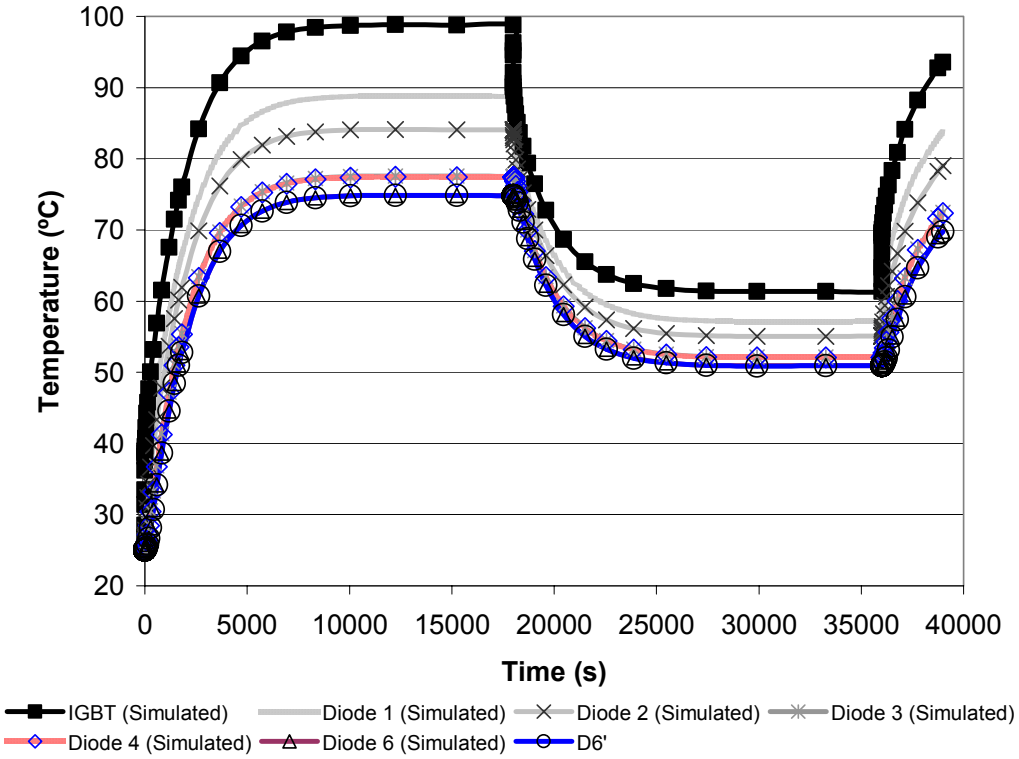

Figure 5.6 Simulations for 300 minutes at 150v and 300 minutes at 75v.

The Figures 5.8 – 5.13 compare the experimental junction temperatures for each of the device in the modules the model response. The results in Figure 5.8 and 5.9 present that at this point the error is about 2 ˚C degrees between simulated and experimental results of the IGBT and the diode D2. In Figures 5.10-5.13 show that the error in diodes D3 to D6 is between 5 to 10˚C. In Table 5.1 we can appreciate the error in percent between simulated and measured for the calibration. The error for the calibration varies from 1.42 % in the IGBT to 14.5% in the diode 6. It is important to note that the error in the current gain due to the temperature is 0.01%.

The behavior of the experiment and the simulation are similar but with slight differences in the transient behavior and steady temperatures. We can notice that the percentage of error increases with the distance from IGBT, the main source of heat. Figure 5.14 compares the experimental and simulated behavior of the current of the IGBT, as expected the simulated match the experimental result and probing that the interaction between the electrical and thermal network is working

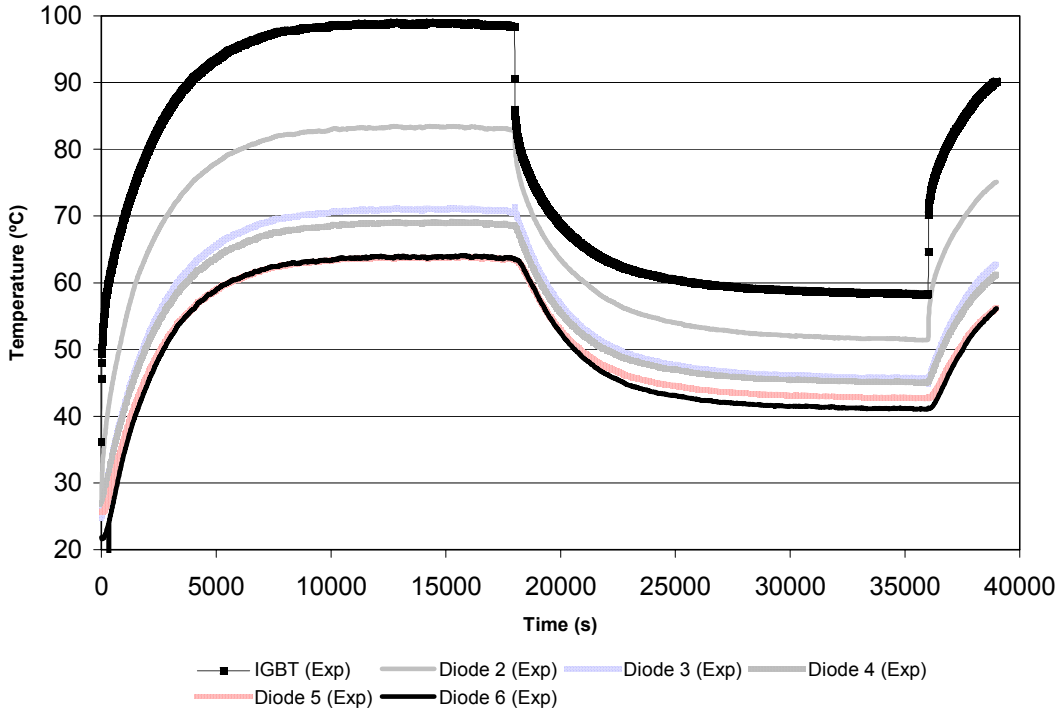

Figure 5.7 Experimental data for 300 minutes at 150v and 300 minutes at 75v.

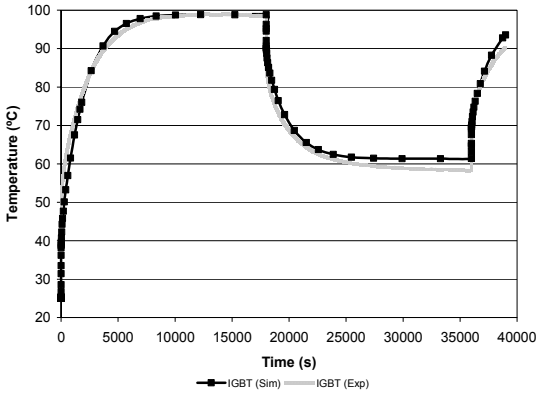

Figure 5.8 Comparison of experimental and simulation temperature of the IGBT junction for 300 minutes at 150v and 300 minutes at 75v.

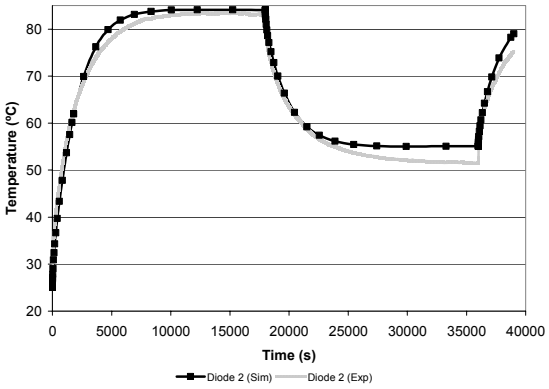

Figure 5.9 Comparison of experimental and simulation temperature of the Diode 2 junction for 300 minutes at 150v and 300 minutes at 75v.

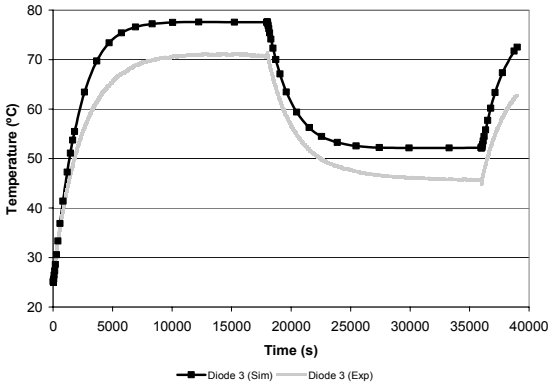

Figure 5.10 Comparison of experimental and simulation temperature of the Diode 3 junction for 300 minutes at 150v and 300 minutes at 75v.

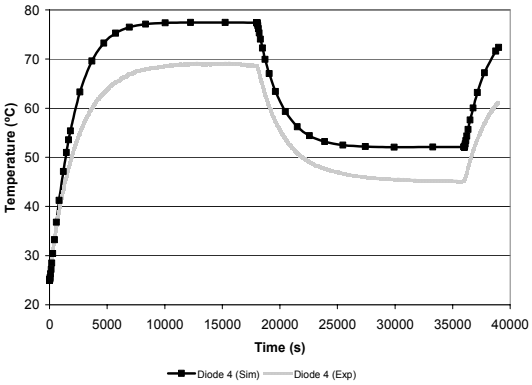

Figure 5.11 Comparison of experimental and simulation temperature of the Diode 4 junction for 300 minutes at 150v and 300 minutes at 75v.

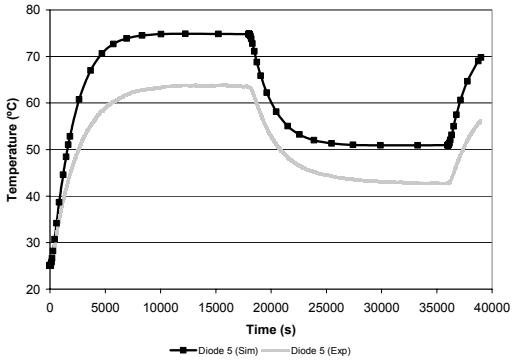

Figure 5.12 Comparison of experimental and simulation temperature of the Diode 5 junction for 300 minutes at 150v and 300 minutes at 75v.

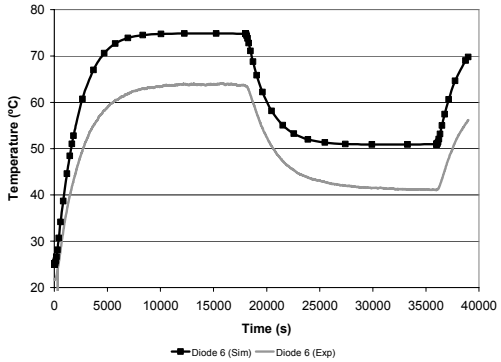

Figure 5.13 Comparison of experimental and simulation temperature of the Diode 6 junction for 300 minutes at 150v and 300 minutes at 75v.

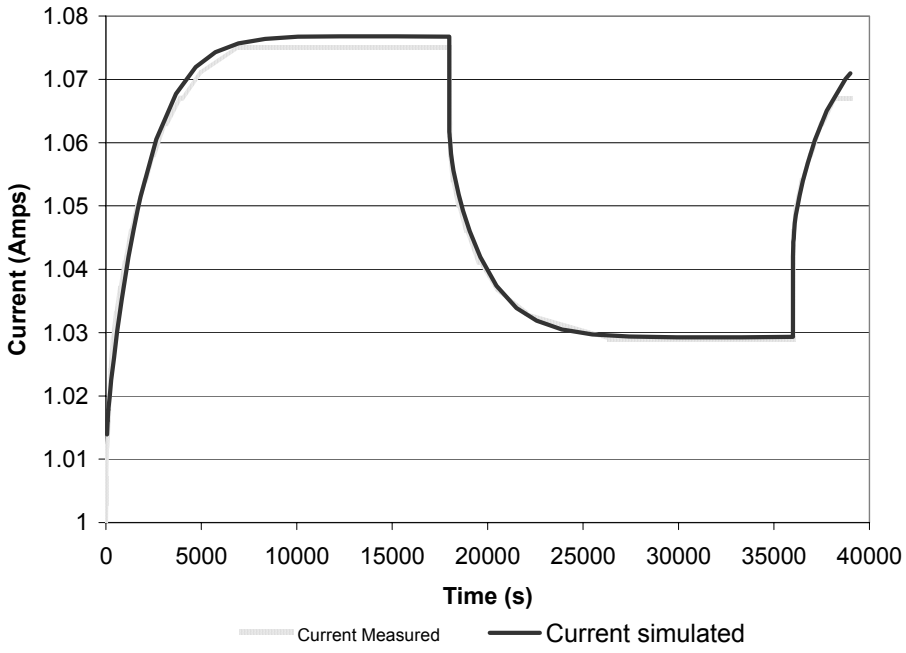

Figure 5.14 Comparison of experimental and simulation Current for 300 minutes at 150v and 300 minutes at 75v.

Table 5.1 Percent of error of calibration.

	Percent of Error
Current	0.09
IGBT	1.42
Diode 2	2.68
Diode 3	8.34
Diode 4	10.90
Diode 5	14.50
Diode 6	14.50

5.3. Electro-Thermal Model Validation

Now we present the validation of the developed model at different power levels.

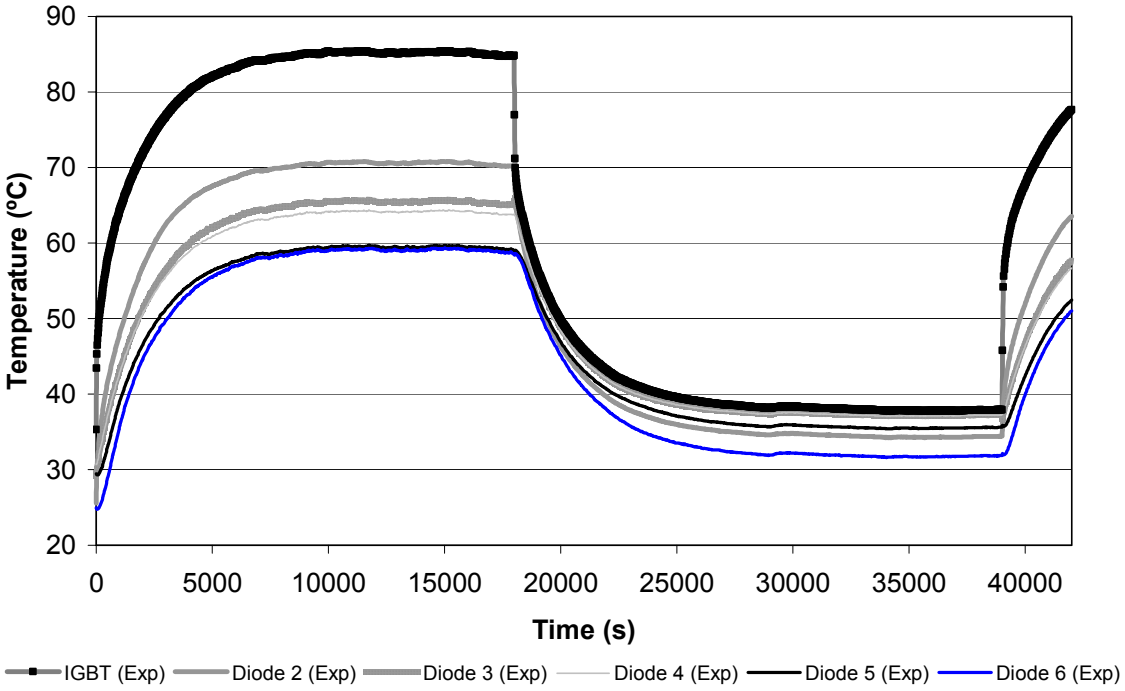

Figure 5.15 Experimental data for 300 minutes at 120v and 300 minutes at 40v.

Figures 5.15 – 5.20 show other test performed to validate the developed model. An input of 120 watts for 300 minutes and them 40 watts for 300 minutes was used. The

percentages of error in temperature are presented in Table 5.2. The error in this validation varies from 1.33% in the IGBT to 11% in diode 6. Again is important to notice that the error in the current is 0.73%.

Table 5.2 Percent of error of Validation for 300 minutes at 120v and 300 minutes at 40v.

	Percent of Error
Current	0.73
IGBT	1.33
Diode 2	2.97
Diode 3	3.30
Diode 4	5.49
Diode 5	9.95
Diode 6	11.05

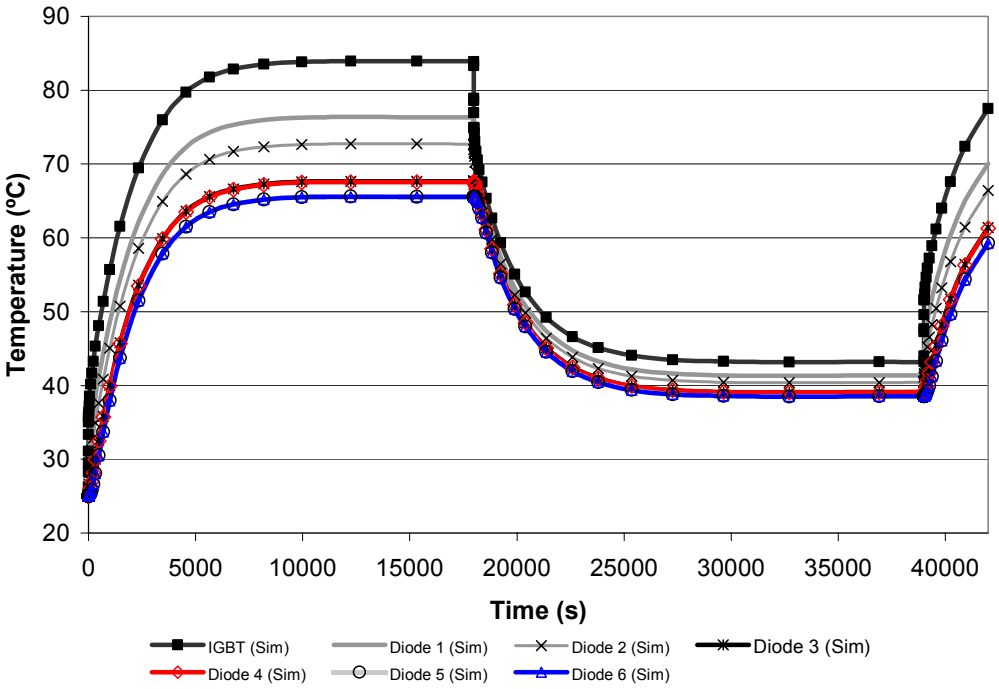

Figure 5.16 Simulation data for 300 minutes at 120v and 300 minutes at 40v.

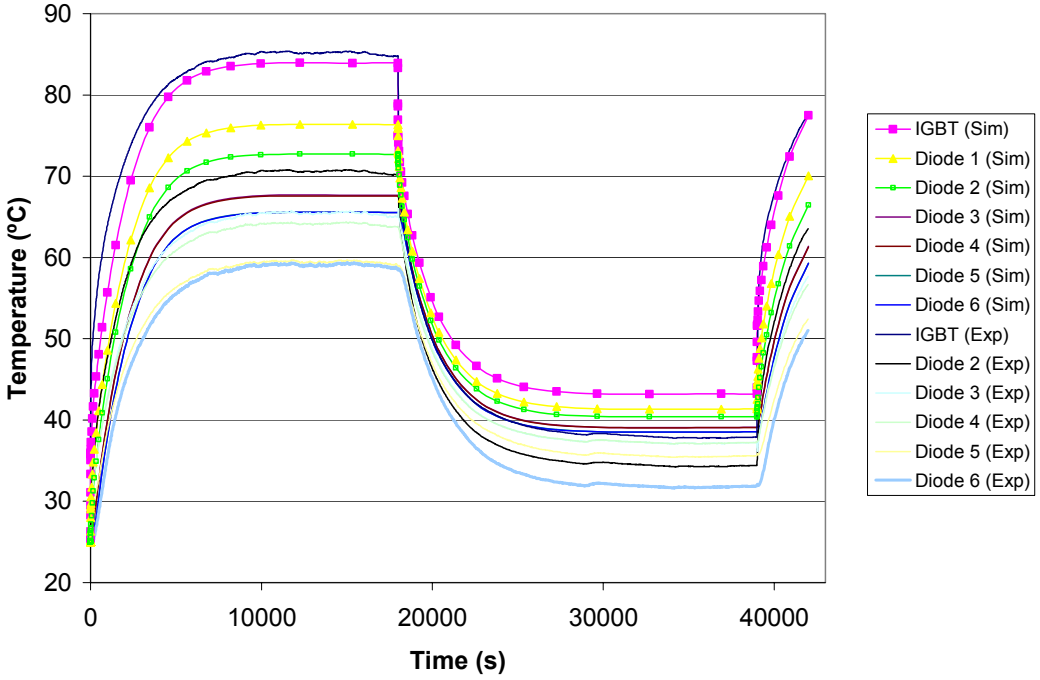

Figure 5.17 Comparison of experimental and simulation temperature for 300 minutes at 120v and 300 minutes at 40v.

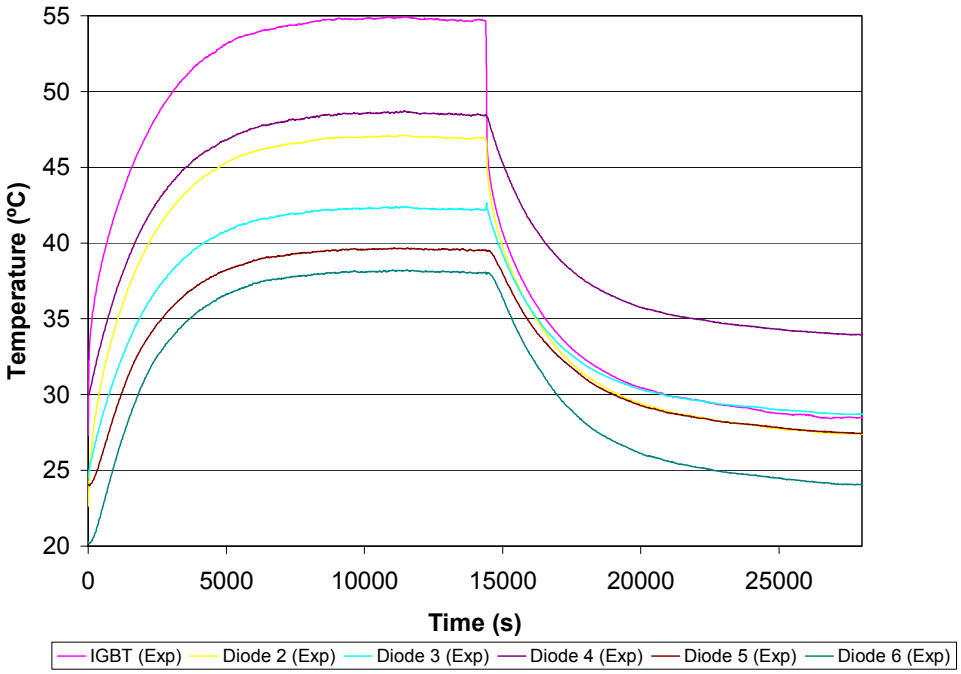

Figure 5.18 Experimental data for 240 minutes at 75v and 240 minutes at 30v.

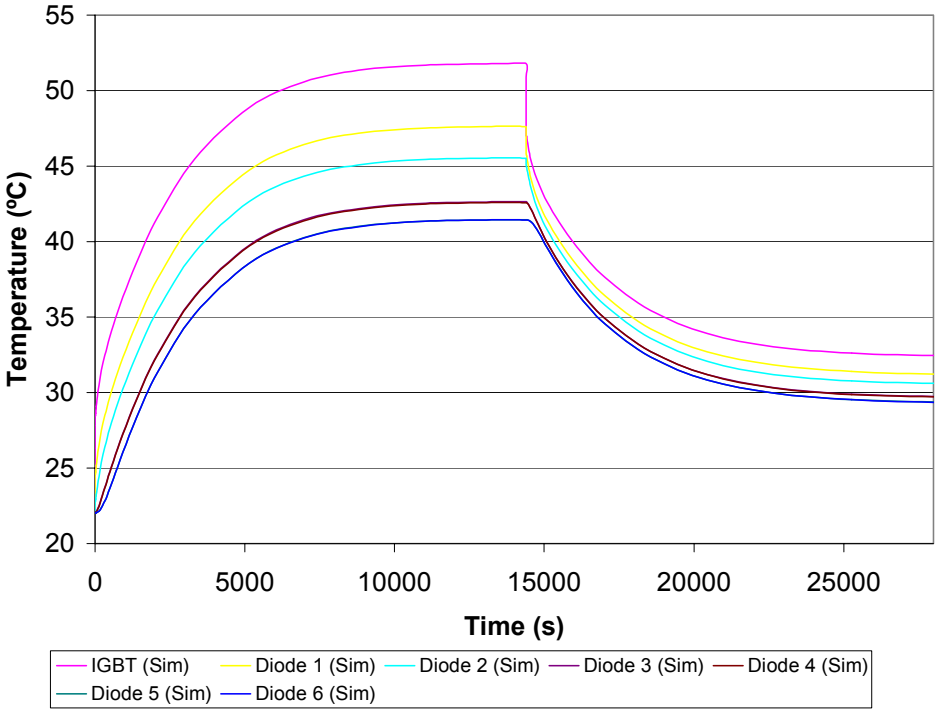

Figure 5.19 Simulation data for 240 minutes at 75v and 240 minutes at 30v.

A second input for validation was 75 watts for 240 minutes and them 30 watts for 240 minutes. The percentages of error for this case are presented in Table 5.3. The errors in this validation vary from 0.43% in the diode 3 to 8.3% in diode 6. Again it important to note that the error in the current that changes due to the temperature is 0.3%. The behavior of the experiment and the simulation are similar but with slight differences in the transient behavior and steady temperatures.

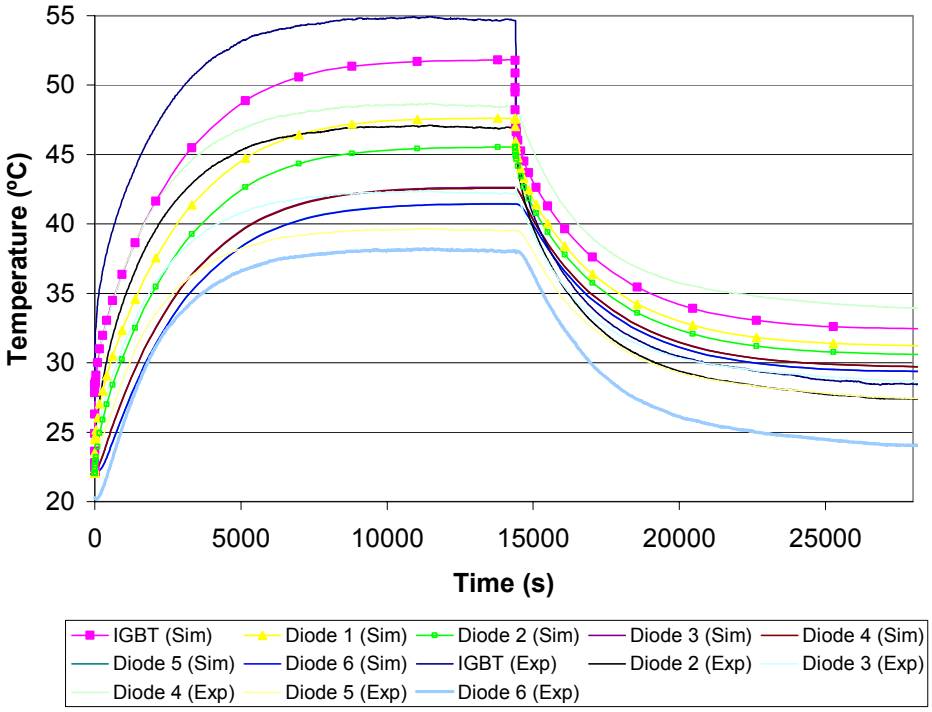

Figure 5.20 Comparison of experimental and simulation temperature for 240 minutes at 75v and 240 minutes at 30v.

Table 5.3 Percent of error of Validation for 240 minutes at 75v and 240 minutes at 30v

	Percent of Error
Current	0.29
IGBT	5.77
Diode 2	3.54
Diode 3	0.43
Diode 4	14.21
Diode 5	4.29
Diode 6	8.30

The experimental results show good fitting of the junction temperature response of the devices by the model. Figure 5.20 shows simulated results for the temperatures at different positions in the heat sink under the IGBT. The modeled heat sink surface

temperature is about 5°C higher than the measured temperature. This is due to the fact that the modeled temperature was on the top of the heat sink next to the baseplate, while the measured heat sink temperature is in a hole drilled slightly below the surface. The fin temperatures are predicted to within approximately 2°C of the measured temperature. These results show good agreement considering that the model represents a local spatial average compared to single point measurements.

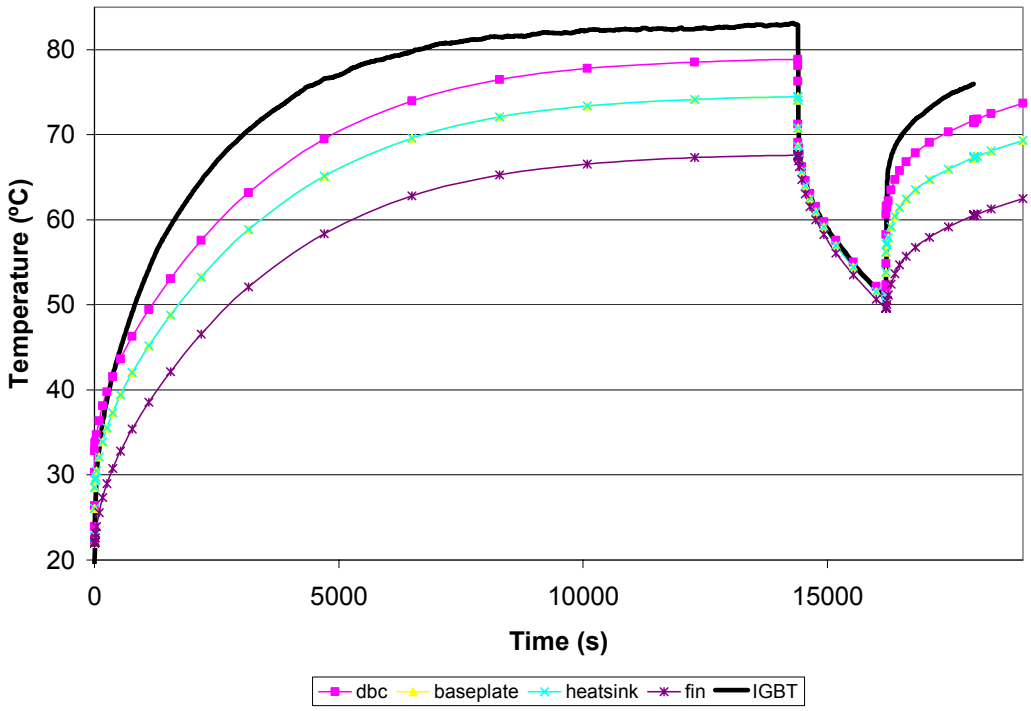

Figure 5.21 Temperature at different positions under the IGBT.

5.4. Summary

This chapter describes the experimental data acquisition and calibration temperature sensitive parameters. The calibrated model and validated model results are presented. The results from the calibration and validation show that the error in the IGBT junction varies from 1.33% to 5.77% showing an excellent agreement with measured data in the testbed.

Chapter 6

Conclusions and Future Work

6.1. Conclusions

This work presents the development, validation and calibration of an electro-thermal model for a multi-chip PEM. The model permits the calculation of temperature for the silicon die chips in transient and steady state conditions. The temperature calculation is performed using compact models derived from the thermal properties of the materials of the packages and the spatial distribution of the components within the package. The model was calibrated and validated in a three phase inverter system connected to a computer that controls its operation and acquired the temperature and electrical variables of the system. The results from the calibration and validation show that the error in the IGBT junction varies from 1.33% to 5.77% showing an excellent agreement with measured data in the testbed. The result for the farthest diode varies from 8.3% to 14.5% demonstrating that we still have issues with the thermal coupling in the heat sink. One of the main results that we achieved using this model was the current gain dependence from temperature in which the error varies from 0.09% to 0.73%. The current gain can be used as a parameter of the effectiveness of the electro-thermal model by whish we can said that the simulated system characterized the electro-thermal behavior in the system.

The thermal network methodology developed by Hefner was adapted to develop the complete thermal network of the multi-chip PEM in this case a half bridge package

and a model for the heat sink. A reduced-order electro-thermal model of a PEM and heat sink cooling system are developed and is used to develop an electro-thermal model for a three-phase inverter system. The models are developed from a finite difference discretization of the heat transfer equation using the thermal network component modeling methodology. The resulting models are implemented in SABER and allow parametric analysis for the PEM electro-thermal performance within the inverter.

To calibrate the PEM and the heat sink model developed in SABER, the *"thick_base"* parameter in the PEM module and the *"fin_area_per_area"* parameter in the heat sink were adjusted at 150 watts constant power dissipation with me measure data. These parameters were modified base in experience and trial and error. Calibration results show good agreement between experimental data and model output with less than 2% of error in the IGBT junction and 14.5% of error in the farthest diode from the main heat source.

After the calibration process more data was collected and the model was validated. The model was validated under different operating modes including switching operation. The results presented in this thesis show good agreement with measured data for the testbed system with less than 5.8% of error in the IGBT junction and less than 11.1% of error in the farthest diode from the main heat source. The model developed here allows considerable insight about the thermal behavior inside a PEM.

From the error in the results we can notice that the error in the temperature in the diodes have a tendency to increase with the amount of power of the principal heat source

the IGBT. And the farthest the higher the error, this behavior let us to think that the thermal coupling in the heat sink is not accurate.

It should be emphasized that the simulated data is predicted on the basis of the geometrical dimensions and physical properties of the PEM and is calibrated using the data and is not a "fitted" model. Consequently quantitative predictions of the performance of the devices with various alterations to the structure could be obtained without the need to build prototypes. The combination of the physical properties and geometrical dimensions with the calibration data provides a fully physical electro-thermal model which is capable of describing the mutual thermal interaction at the die level and above.

6.2. Limitation and Future Work

The model developed has the limitation that the user needs to have precise geometry and materials data for the PEM. Usually the manufacturers don't give away this kind of information.

- In this thesis, we showed the development of a multi-chip PEM electro-thermal model in SABER. The developed model resulted in a good emulation of the thermal behavior of the temperatures thought the thermal network. We think that this is a considerable contribution to the thermal design of PEM's in the area of power electronics. However the thermal model for the heat sink is a simple solution to use in our problem, but a more detailed model of the heat sink can

improve the results. Also the validation of the system for a rectifier in power conversion operation needs to be performed.

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