High Frequency Behavioral Modeling of Second-Order Sigma Delta Modulators

By

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ABSTRACT

Sigma delta modulators ($\Sigma\Delta$Ms) form part of the core of today's mixed-signal designs. They are cornerstone components of oversampled data converters. Such data converters take advantage of digital signal processing techniques and VLSI technology to provide high performance with low sensitivity to analog component imperfections and noisy conditions. The ongoing research on these devices shows the potential of $\Sigma\Delta$ data converters as a promising candidate for high-speed, high-resolution, and low-power mixed-signal interfaces. As for any electronic system, efficient modeling and simulation tools are essential in the design cycle of oversampled converters, particularly for their embedded $\Sigma\Delta$Ms. Although transistor-level simulation is the most accurate approach known for these components, this method becomes impractical for complex systems due to the long computational time required. This situation has led circuit designers to consider alternate modeling techniques. Among these, the simulation of $\Sigma\Delta$Ms using behavioral models has become the focus of attention for a large portion of the design community. This thesis presents an accurate behavioral model of a high speed, second-order, multi-bit $\Sigma\Delta$M using VHDL-AMS as the modeling language. The model addresses several nonidealities such as the integrator dynamics, thermal noise, jitter noise, and capacitance mismatch. The proposed model provides a reliable tool for the design of low-power, high-speed $\Sigma\Delta$Ms. Results from simulations of a second-order multi-bit $\Sigma\Delta$M demonstrate the model to be valid and accurate when compared to SPICE and experimental data.

RESUMEN

Los moduladores sigma delta ($\Sigma\Delta$Ms) forman una parte básica en muchos diseños contemporáneos de circuitos de señal mixta, como componentes fundamentales de los convertidores de data sobre-muestreados. Estos convertidores aprovechan técnicas de procesamiento digital de señales y de tecnología VLSI para proveer alto funcionamiento con baja sensibilidad a ruido y a imperfecciones de componentes analógicos. La investigación en curso sobre estos dispositivos muestra el potencial de los convertidores $\Sigma\Delta$ como un candidato prometedor para interfaces de señales-mixtas de alta velocidad, alta resolución y baja potencia. Como para cualquier sistema electrónico, el modelaje eficiente y la simulación son herramientas esenciales en el ciclo del diseño de los convertidores sobre-muestreados, particularmente para sus $\Sigma\Delta$Ms. La simulación a nivel de transistores es la técnica conocida más exacta para estos componentes, pero resulta impráctica para diseños complejos por el largo tiempo que requiere la simulación. Esta situación ha movido a los diseñadores a considerar técnicas alternas de modelaje. Entre estas, el modelaje de comportamiento se ha convertido en un foco de atención para gran parte de la comunidad científica. Esta tesis presenta un modelo comprensivo del comportamiento de un $\Sigma\Delta$M de segundo-orden de múltiples bits y de alta-velocidad usando VHDL-AMS como el lenguaje de modelaje. El modelo trata varias no-idealidades tales como la dinámica del integrador, el ruido termal, el ruido jitter y las desviaciones en los valores de capacitancia. Los modelos propuestos proporcionan una herramienta confiable en el diseño de los $\Sigma\Delta$Ms de alta velocidad y baja potencia. Resultados de simulaciones para un $\Sigma\Delta$M de segundo-orden de múltiples bits demuestran que el modelo es válido y exacto en comparación con simulaciones en SPICE y con datos experimentales.

DEDICATION

To God, without him nothing is possible.

To my wife Adelis, my parents George and Judith, family and friends.

For their guidance, support, love and enthusiasm.

Without these things this thesis could not have been possible.

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LIST OF ABBREVIATIONS

Δ**M**	Delta Modulator
$\Sigma\Delta$	Sigma Delta
$\Sigma\Delta$M	Sigma Delta Modulator
A/D	Analog to Digital
ADC	A/D Converter
CAD	Computer Aided Design
CT	Continuous Time
D/A	Digital to Analog
DAC	D/A Converter
DEM	Dynamic Element Matching
DT	Discrete Time
ENOB	Effective Number of Bits
GBW	Gain Bandwidth
GSM	Global System for Mobile Communications
ILA	Individual Level Averaging
LSB	Least Significant Bit
MSB	Most Significant Bit
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PDF	Probability Density Function
PSD	Power Spectral Density
SC	Switched Capacitor

SNR	Signal to Noise Ratio
SNDR	Signal to Noise plus Distortion Ratio
SQNR	Signal to Quantization Noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
WCDMA	Wideband Code Division Multiple Access

CHAPTER 1

Introduction

Sigma Delta Modulators ($\Sigma\Delta$Ms) form part of the core of today's mixed-signal designs as the cornerstone elements of oversampled analog-to-digital (A/D) and digital-to-analog (D/A) converters. Such types of converters are essential in applications where signals with low to medium bandwidth need to be converted with a high resolution and low dependency on the factors that typically affect the analog front end. $\Sigma\Delta$ data converters take advantage of digital signal processing techniques and VLSI technology to provide high performance with low sensitivity to analog component imperfections and noisy conditions. Recently, $\Sigma\Delta$Ms have been receiving much attention in mixed-signal integrated circuits (ICs) for radio frequency (RF) designs. The ongoing research on these devices shows the potential of $\Sigma\Delta$ converters as a promising candidate for high-speed, high-resolution, and low-power mixed-signal interfaces.

Modeling and simulation are fundamental steps in the design cycle of mixed-signal systems. In the design of $\Sigma\Delta$Ms these steps become of critical importance. Despite this importance only a few modulator architectures have been fully analyzed, mainly because analytical expressions for the modulator's behavior and performance are generally unavailable. Even when an analytical model of the desired topology becomes available, simulation might still be necessary to obtain accurate results [41].

A reason for this is that analytical models often, although relatively fast, do not provide the effects of analog nonidealities on system performance. Evidently, the ΣΔM design process needs rapid evaluation to be feasible in today's fast paced digital designs. The use of approximate models can help reduce the number of iterations in the ΣΔM design cycle. These models must provide the designer good estimates for stability, SNDR, and distortion.

Many simulation approaches exist for evaluating the performance of ΣΔMs. Although device-level simulation is the most accurate approach known for these components, this method becomes impractical for complex systems due to the long computational time required. For this reason device-level simulation, normally, is left to the final design verification. This situation has led circuit designers to consider alternate modeling techniques. Among these, the simulation of ΣΔMs using behavioral models has become the focus of attention for a large portion of the design community. Behavioral models offer the designer a set of reusable building blocks that represent components and nonidealities. Furthermore, this approach brings the simulation of mixed-signal circuits closer to logic simulation, which is a more time-efficient and practical solution.

The previous discussion evidences the need for accurate behavioral models in the design of ΣΔMs. Since ΣΔMs are mixed-signal circuits, the use of a language like VHDL-AMS, which provides ways of using both event-driven and normal circuit simulation methods, becomes a natural choice. Nevertheless, VHDL-AMS models for ΣΔMs are rare in literature because of the recent standardization of the language. The few ones published concentrate mainly on the behavioral aspects of these circuits, leaving aside details that become important at high speeds. Despite these, high speeds data converters are becoming increasingly prevalent in all types of communication applications.

Most of today's oversampled data conversion applications use second-order ΣΔMs since higher order modulators become unstable and difficult to implement [41]. Therefore, efficient modeling techniques for second-order ΣΔMs at high frequencies are becoming an essential part of the design cycle of contemporary high speed data converters. The main objective of this research is to develop an accurate behavioral model of a high speed, second-order, multibit ΣΔM using VHDL-AMS as the modeling language. To make the model as accurate as possible, it addresses the main noise sources and nonidealities including: thermal noise, sampling jitter, capacitance mismatch, and integrator defective settling.

ΣΔMs exhibit thermal and jitter noise. Thermal noise in ΣΔMs is associated with the amplifier and the finite switch resistance of the switched-capacitor integrator. Moreover, the sampling period of switched-capacitor circuits is not constant. This shift in the sampling period introduces a noise source known as jitter.

The gain factors in switched-capacitor integrators are implemented using capacitor ratios. The accuracy of these ratios is restricted by the matching accuracy of fabrication processes. Consequently, the capacitance mismatch turns in gain variations which affect the transfer functions of the integrator, and potentially the system's stability. A second effect of mismatch becomes critical in multi-bit designs. Mismatch in the internal D/A converter causes inaccurate output levels such that the output contains harmonic distortion. This harmonic distortion makes the system integral linearity no better than that of the internal D/A converter. Dynamic element matching techniques are used to reduce the effects of component mismatch inside the D/A converter. In this research the individual level averaging technique is employed.

The incomplete settling of switched-capacitor integrators has become one of the most limiting factors in the performance of ΣΔMs. The integrator defective settling is mostly due to the operational transconductance amplifier characteristics such as

the finite and nonlinear DC gain, the finite gain-bandwidth, and the slew-rate limitations. This research presents a behavioral transient model of a switched-capacitor integrator that includes the effects of the amplifier transconductance and output conductance relation, and the dynamic capacitive loading effect on the settling time. Unlike traditional behavioral models where this level of detail is usually omitted, the proposed model provides a convenient tool to aid in the design of low-power high-speed switched-capacitor $\Sigma\Delta$Ms.

This thesis is organized as follows: A review of previous works, and the objectives and methodology for this research are presented in Chapter 2 and 3, respectively. Chapter 4 presents the theoretical background for the A/D conversion process including Nyquist, oversampled and $\Sigma\Delta$ converters evidencing the advantage of $\Sigma\Delta$ converters. Also, the characteristics of some of the $\Sigma\Delta$Ms topologies such as first-order, second-order, and multi-bit are addressed. Chapters 5 and 6 present the considerations that affect the performance of a $\Sigma\Delta$M, and the behavioral modeling blocks, respectively. In Chapter 7 results are presented for simulations of a VHDL-AMS second-order multi-bit $\Sigma\Delta$M model. Finally some remarks are made at the conclusion in Chapter 8.

CHAPTER 2

Literature Review

In the design of ΣΔMs, modeling and simulation plays a central role. Although, analytical models can provide a good starting point in the design of ΣΔMs, modeling and simulation is still needed to predict the effects of analog nonidealities on system performance [41]. Moreover, performance measures such as the signal-to-noise ratio (SNR) and SNR-versus-input amplitude require extensive simulations. The idea behind modeling and simulation is the adoption of a proper technique to efficiently analyze the performance of ΣΔMs.

Modeling and simulation of ΣΔMs is not a straightforward task. Some difficulties arise from the mixed-signal nature of the circuit, including its nonlinearity, dual-time domains, performance expectations on long transient simulations, and the required high simulation accuracy. Several modeling methods exist for the simulation of electronic circuits. In general, these methods can be classified in one of the following categories:

- ***Device Models***: Are based on low level descriptions of active and passive devices. Simulations are performed using a circuit simulator such as SPICE [38]. SPICE is a conventional and accurate circuit simulator but as circuit complexity grows it requires increasingly large amounts of time. Several device-

level models for ΣΔMs can be found in the literature, evidencing the advantages and limitations of this approach [27][33][50].

- ***Circuit Macromodels***: Represent equivalent circuits using a minimum set of passive and active devices available in the circuit simulator. They allow the introduction of nonidealities. This approach provides good accuracy but improvement of simulation speed is limited. Multiple examples of operational transconductance amplifier macromodels have been reported which have found applications in the modeling of ΣΔMs [24][32] [41][45][65][68].

- ***Time-Domain Macromodels***: Rely on a set of equations describing the transient behavior of the circuit. They allow to introduce dynamic behavior and nonidealities. Although limited in number, a few examples of time-domain macromodels for ΣΔMs can be found in literature [13][34][46][72].

- ***Finite-Difference Equations***: Exploit the z-domain descriptions of the system. They provide fast simulation but the introduction of nonidealities is limited. Some examples of ΣΔM models have been documented based on finite-difference equations [42][43][71].

- ***Table-Lookup Models***: Consist of a dual step approach. First, a table is generated with the output data obtained by simulating the original circuit with a circuit simulator such as SPICE. Next, the generated table data is used instead of the circuit for transient simulations. Examples of table-lookup modeling for ΣΔMs can be found in [4][6][69].

- ***Behavioral Models***: Attempt to bring the simulation of mixed-signal circuits closer to logic simulation. They take advantage of some of the mentioned methods. This method requires a complete knowledge of the system functionality

and behavior. Behavioral models offer the designer a set of building blocks that represent components and nonidealities. Recent behavioral models for ΣΔMs have been reported in literature [2][7][20].

The simultaneous need of fast and accurate transient estimates when simulating ΣΔMs reaches the limit of a SPICE type conventional simulator, resulting in extremely long simulation time. The simulation time reduction of behavioral modeling and other approaches, has promoted the development of multiple tools in recent years. A representation set of the most salient of these tools is outlined below:

- **ASIDES**: Behavioral simulation tool for switched capacitor ΣΔMs. Includes analog circuits nonidealities that affect the performance of the modulator [36].
- **AWEswit**: A mixed signal simulator for switched-capacitor SC circuits that allows partitions of the circuit to be modeled with digital blocks controlled by an event queue and analog circuits [62][63][64].
- **DAISY**: Delta-Sigma Analysis and Synthesis (DAISY) is a high-level synthesis tool for ΣΔ modulators. The approach determines the modulator topology and the required building block specifications to meet specified requirements [23].
- **DAISY-CT**: High-level synthesis software for continuous-time ΣΔMs. The approach is the same as DAISY but extended to continuous-time ΣΔMs [24].
- **Delsig**: The Delta-Sigma is a MATLAB toolbox that provides all the major functions needed to begin the design of a delta-sigma (sigma-delta) A/D or D/A converter [52].
- **DelSi**: Is a MATLAB toolbox used for the design and simulation of delta-sigma modulators. It exploits an analytical a-priori approach of the error source inside the ADC to phase-plane modeling [2].

- **SCAPN**: Switched-Capacitor Analysis Program for N phases (SCAPN) is a program which embodies features for the evaluation of SC circuit designs. The formulation is based on modified nodal analysis and equation ordering [30].

- **SCLNAP**: Is a MATLAB program based on the adjoint network theory to perform noise analysis of periodically switched linear circuits [70].

- **SCNAP4**: Simulation software for the analysis of general linear networks, especially ideal and nonideal switched capacitor and switched-current circuits based on discrete solutions [54][55][56][70].

- **SDnoise**: A macromodel simulator for ΣΔMs that emphasize the simulation of the dither effect of thermal noise and clock jitter in discrete and continuous-time ΣΔMs [17][18].

- **SD Toolbox**: This toolbox includes set of blocks implemented in the Simulink environment, which allows designers to perform time-domain behavioral simulations of switched-capacitor sigma-delta modulators. The proposed set of blocks takes into account most of the SC sigma-delta modulator nonidealities [7].

- **SIGGEN**: CAD tool dedicated to find a design solution for a ΣΔMDAC, based on a high level specification using a mixture of design equations and behavioral simulation [47].

- **SIMSIDES**: SIMulink-based SIgma-DElta Simulator (SIMSIDES) is a toolbox in the MATLAB/SIMULINK platform. The tool is able to simulate arbitrary ΣΔ topologies implemented by using discrete-time - switched-capacitor and switched-current and continuous- time circuit techniques, considering the most important circuit parasitics [49][48].

- **SWITCAP2**: Is a general simulation program for analyzing linear switched-capacitor (SC) networks and mixed switched-capacitor digital networks. High levels of abstraction including parasitics and nonidealities can be simulated, however is computationally time consuming [60].

- **TOSCA**: A netlist-based SC $\Sigma\Delta$ A/D converter simulator based on descriptions at building block level. It is based on the partitioning of switched capacitor circuits modulators into blocks creating a block level network [16].

- **VSIDES**: A simulation tool based on ASIDES using VHDL and VHDL-AMS with a commercial simulator. It provides the same analysis of ASIDES but allows a similar VHDL-based input description of the $\Sigma\Delta$ [10].

- **SDSIM**: A $\Sigma\Delta$ data converter simulator based on finite difference equations in the time domain. Makes use of the clocked operations of these circuits to formulate a set of finite difference equations in the time domain [43][71].

- **ZSIM**: The Z-domain SIMulator (ZSIM) is a tool based on a table-based approach for the simulation of $\Sigma\Delta$Ms and switched capacitor integrators [4][9][41].

- **GNSCODER**: A simulation software for conventional multi-loop and cascade noise-shaping coders and $\Sigma\Delta$Ms. It performs time-domain simulation and provides time or frequency results [9].

- **MIDAS**: High level functional simulator for sampled-data digital and analog systems. It is often used for the simulation of SC networks of $\Sigma\Delta$M [29].

The main differences between these behavioral tools are the implementation platform (i.e. C++, MATLAB), the number of included basic blocks and the precision of the models. Some drawbacks of these behavioral tools include accessibility to the tool,

their difficult user interface, limitation to incorporate new topologies, incorporation with CAD tools and accuracy. These drawbacks have led designers to consider other options for the simulation of ΣΔMs. Among these options, custom reusable models implemented in languages such as MATLAB and VHDL have become quite popular.

Recently, MATLAB Simulink has been widely accepted to model and simulate ΣΔMs. Some of the most recent works are [20], [35] and [48]. Previous models [20] based on the symbolic admittance matrix were successful at lower frequencies but failed to provide the required accuracy at higher frequencies. Moreover, Simulink models exhibit some limitations. The main limitation is that CPU time requirements increase as the model complexity increases. Also, due to the non-circuit type environment, system descriptions need to be strictly behavioral, not allowing hybrid models. In addition, MATLAB models cannot be fully incorporated as part of the design in most CAD tools.

In addition to MATLAB, VHDL behavioral models have been used to simulate ΣΔMs. These models for ΣΔMs such as [47], [53] and [58] are limited in literature due the nature of the language. VHDL was primarily designed for digital modeling, making difficult its use for behavioral modeling of analog components. In the early 1990s, the need for a hardware description language supporting analog and mixed-signal modeling became apparent. VHDL-AMS was developed and approved in 1999 under the IEEE Standard 1076.1 *Definition of Analog and Mixed Signal Extensions to IEEE Standard VHDL*. This language fills a number of needs in the design process, including the integration of analog and digital simulation [3].

Despite of the language advantages, VHDL-AMS behavioral models are rare in the literature. Published VHDL-AMS ΣΔM models provide a system level description based on macromodels [66][65]. These publications only present models for continuous-time modulators leaving aside the widely used discrete-time or SC ΣΔMs.

Additional published VHDL-AMS behavioral models lack of a full set of considerations for high speed designs [61]. VSIDES is the only ΣΔ Modulator simulation tool that makes use of VHDL-AMS, although is based on ASIDES but using VHDL-AMS. In a similar way as the other behavioral tools for the simulation of ΣΔMs, it exhibits some of the mentioned drawbacks.

VHDL-AMS is suitable for the analysis of noise and harmonic contributions to the system performance. It also allows to perform high-level analysis of the system nonidealities and dynamics, such as thermal noise, jitter, amplifier slewing and components mismatch. An important fact is that many VHDL-AMS compiler-simulators tools provide the option to include SPICE code to simulate at the device level. This permits hybrid models containing behavioral and device level description, allowing to improve accuracy where it is extremely needed. Since VHDL-AMS is an extension of VHDL, it provides an advantage when modeling and simulating digital circuits. In addition, recent CAD tools allow the use of VHDL-AMS model as part of the design modeling and simulation providing full design integration tools. Evidently, there is a necessity for alternate ways of modeling and simulating ΣΔMs. The main reasons are the lack of detailed ΣΔM models, frequency considerations, a complete set of noise sources and nonidealities, and the integration with contemporary CAD tools.

CHAPTER 3

Objectives and Methodology

3.1 Objectives

The main objective for this research is to develop and simulate an accurate, high frequency model of a second-order multi-bit ΣΔM using VHDL-AMS. Moreover, to carry this goal the following objectives must be accomplished:

- Develop an accurate behavioral model of a second-order multi-bit ΣΔM.
- Make use of VHDL-AMS as the modeling language.
- Model nonidealities and noise sources such as thermal noise, sampling jitter, integrator dynamics such as slew rate limitations, finite DC gain and gain bandwidth.
- Develop a modular reusable model for other ΣΔM topologies.
- Obtain the power spectral density (PSD) of the ΣΔM and extract the Signal-to-Noise and Distortion Ratio (SNDR) as a performance measure.

- Validate the model with available experimental data for the global system mobile (GSM) communications and wideband code division multiple access system (WCDMA) bandwidths of 200kHz and 2.0MHz, respectively.

- Validate the model at target bandwidths of 135kHz, 270kHz and 615kHz using SPICE as the reference.

3.2 Methodology

A cognitive map for the research methodology is illustrated in Figure 3.1. The methodology can be divided into four major parts: Study of Related Areas, Models of Errors in ΣΔ Modulators, Behavioral Modeling Blocks in VHDL-AMS and Modeling Outcomes.

3.2.1 Study of Related Areas

The study of related areas provides the necessary background to address the research needs. The main studied areas are: Analog electronics with emphasis on switched-capacitor circuits, noise and operational transconductance amplifiers, Data converters including Nyquist converters and Oversampled ΣΔ data converters, and signal processing including sampling, oversampling and noise shaping theory. In addition to these areas, a comprehensive analysis of published conferences articles, journal articles and specialized books is also included.

3.2.2 Model of Errors Sources in ΣΔ Modulators

Behavioral modeling is the adopted modeling approach for this research. The performance of a ΣΔM is significantly affected by circuit nonidealities. Therefore,

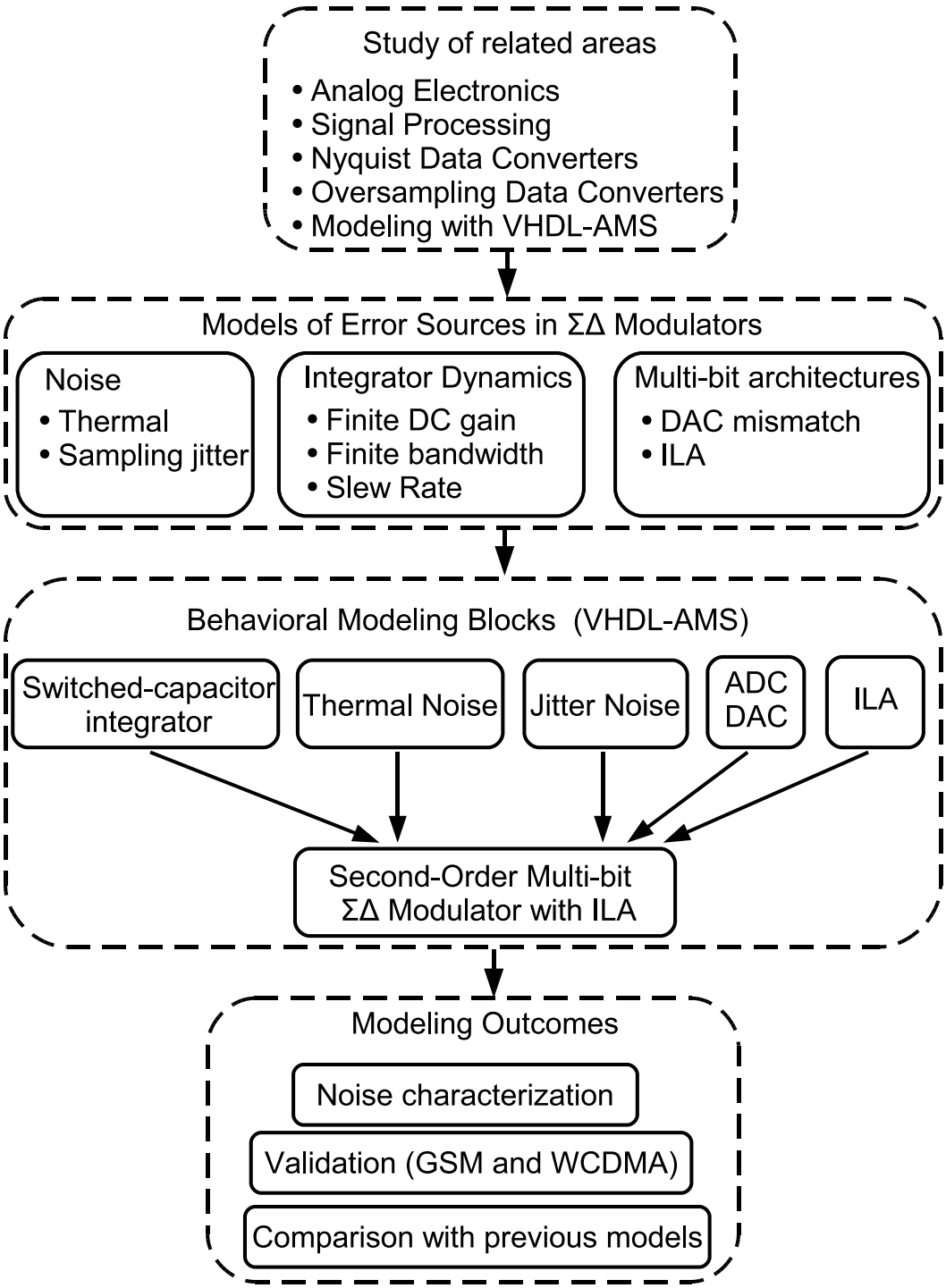


Figure 3.1. Cognitive map for research methodology.

their analysis becomes mandatory to obtain behavioral models for fast and precise time-domain simulations. The main nonidealities addressed in this work are the SC integrator defective settling, thermal noise, sampling jitter, and capacitance mismatch in the D/A converter for multi-bit ΣΔMs. This analysis will emphasize high frequency behavior and other corresponding issues.

3.2.3 Behavioral Modeling Blocks in VHDL-AMS

The mentioned nonidealities are contained into the behavioral modeling blocks in VHDL-AMS. This approach allows a modular analysis of the ΣΔM, allowing to concentrate at one submodel at a time without loosing perspective of the whole system. Each major component of the ΣΔM will be modeled individually thus providing flexible, modular and reusable models.

3.2.4 Modeling Outcomes

Simulations are carried and validated with SPICE results for target bandwidths of 135kHz, 270kHz and 615kHz. Additional validation is carried for the GSM and WCDMA bandwidths of 200kHz and 2.0MHz, respectively, using reported experimental data. The SNDR will be used as a measure of performance of the modulator but the PSD is also used as a correctness measure. Characterization of the main noise sources such as sampling jitter, thermal noise and D/A converter mismatch is also carried. Finally, simulations are performed to compare results between established models presented in [14] and [20], and the model presented in this research.

CHAPTER 4

Theoretical Background

4.1 Analog-to-Digital Conversion

The analog-to-digital (A/D) process converts a continuous in time and amplitude signal into a discrete-amplitude and discrete-time signal. A more detailed diagram of this process is shown in Figure 4.1. According to Figure 4.1 an analog anti-aliasing filter limits the input signal bandwidth so that subsequent sampling does not alias any unwanted noise or signal components into the actual signal band. Next, the input signal $x_a(t)$ is sampled at uniform intervals $f_s = 1/T_s$ and quantized into its digital representation $x_d[n]$. The process is discussed in the following sections.

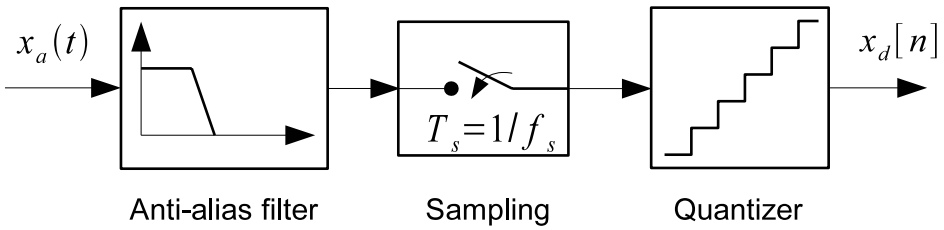


Figure 4.1. Conventional analog-to-digital conversion process.

4.1.1 Sampling Process

In general, signals can be divided into two categories: analog signals, which can be defined in a continuous-time domain, and digital signals, which can be represented as a sequence of numbers in a discrete-time domain. The sampling process transforms a continuous-time signal $x_a(t)$ into a discrete-time signal $x(n) = x_a(nT_s)$, where T_s is the sampling period and n is an integer. Thus, a discrete-time signal $x(n)$ can be represented by a sampled continuous-time signal $x_a(t)$ as

$$\begin{aligned} & x\left(n\right) = \sum_{n=-\infty}^{\infty} x_a\left(t\right)\delta\left(t - nT_s\right) \\ & where, \\ & \delta\left(t\right) = \begin{cases} 1, & t = 0 \\ 0, & elsewhere \end{cases} \end{aligned} \tag{4.1}$$

Since $\delta\left(t - nT_s\right)$ is a periodic function with period $T_s = 1/f_s$ where f_s is the sampling frequency, it can be represented by a Fourier series

$$x\left(n\right) = \sum_{n=-\infty}^{\infty} x_a\left(t\right)\delta\left(t - nT_s\right) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} x_a\left(t\right)e^{(j2\pi nt)/T_s} = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} x_a\left(t\right)e^{j2\pi ntf_s} \tag{4.2}$$

Equation 4.2 states that the act of sampling is equivalent to modulating the input signal by carrier signals at multiples of f_s (e.g. f_s, $2f_s$, $3f_s$ ...). Moreover, the sampling process creates repeated versions of the signal spectrum at multiples of f_s as shown in Figure 4.2. Consequently, signals above the Nyquist criteria, which is half the sampling frequency, cannot be properly converted since they create new signals in the base-band that do not represent the original signal. This effect is known as aliasing. An anti-aliasing filter preceding the sampling circuit is therefore required to ensure that the signal is band-limited to half the sampling frequency.

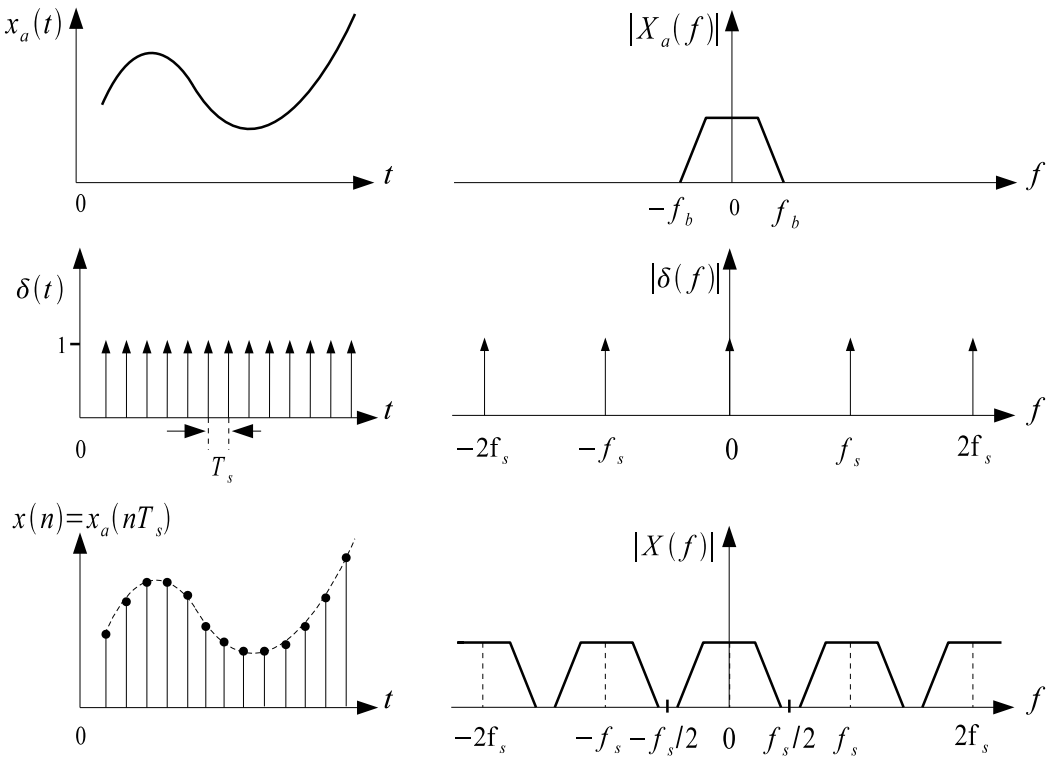


Figure 4.2. Sampling process of a continuous-time signal.

The ratio of the sampling rate f_s to the signal bandwidth differentiates two types of converters: Nyquist-rate and oversampled data converters. In Nyquist-rate data converters, the sampling frequency is twice the analog signal bandwidth, $f_s = 2f_b$, to allow accurate reproduction of the original data. In oversampling converters the signal is sampled at a greater rate than that of the Nyquist. Oversampling data converters offer several advantages over Nyquist-rate converters including the relaxation of the anti-alias filter requirements and quantization noise shaping.

4.1.2 Quantization Noise

Quantization noise is the inherent uncertainty when digitizing a continuous value sample into one of a finite set of discrete values. In general, quantization error is on the order of one least-significant-bit (LSB) in amplitude, and it is relatively small

when compared to the signal amplitude. After the input signal is sampled to obtain the sequence $x(n)$, each value is encoded using finite words of B-bits allowing 2^B quantization levels. Assuming that $|x(n)| \leq 1$ the interval between adjacent levels known as the quantization step is given by

$$\Delta = \frac{2}{2^{B-1}} \tag{4.3}$$

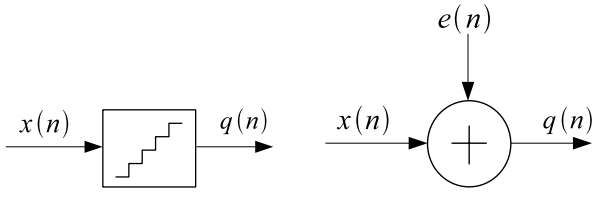
Moreover, the sample $x(n)$ is rounded to the nearest level. Given Equation 4.3, the difference between the input sample $x(n)$ and its quantized value $q(n)$ or better known as the quantization error can be expressed as

$$e(n) = q(n) - x(n) \tag{4.4}$$

Rearranging Eqn 4.4 the quantized error is given by

$$q(n) = x(n) + e(n) \tag{4.5}$$

In the case that the quantization levels are large and equally probable, $e(n)$ is assumed to be uncorrelated with the input signal. Under this assumption $e(n)$ exhibits a white spectrum and its probability density function (PDF) is uniform in the range $[-\Delta/2, \Delta/2]$. Therefore, in a linear model the quantization error can be considered as an independent additive white noise source as shown in Figure 4.3. In addition for an



(a) Quantizer (b) Quantizer linear model

Figure 4.3. Quantizer block diagram and its linear model.

input signal which is large compared to Δ, the error term $e(n)$, the quantization power is given by

$$\sigma^2(e) = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} = \frac{2^{-2B}}{3} \tag{4.6}$$

For the discussion of spectral densities of the noise, we assumed that all the power is in the positive range of frequencies. When a quantized signal is sampled at $f_s = 1/T_s$, all its power folds into the band $0 \leq f < f_s/2$ [41]. If the quantization noise is white, the power spectral density of the sampled noise if given by

$$S_E(f) = \frac{\sigma^2(e)}{f_s/2} = \frac{\Delta^2}{12 f_s/2} \tag{4.7}$$

Moreover, if the dither is sufficiently large and busy to decorrelate the quantization error, the noise power that falls into the signal band f_b is given by

$$P_Q = \int_0^{f_b} S_E(f) df = \frac{\Delta^2}{12} \tag{4.8}$$

Being an error source, the quantization noise affects the quality of the signal. This is expressed using the signal-to-noise ratio (SNR) or often called signal-to-quantization noise ratio ($SQNR$), expressed as

$$SNR = \frac{Signal\ \ Power}{Quantization\ \ Noise\ \ Power} \tag{4.9}$$

For a sine wave input signal with amplitude variation $2A = (2^B - 1)\Delta$, its power is given by $A^2/2$ and the SNR is expressed as

$$SNR = 10log\left(\frac{A^2/2}{\Delta^2/12}\right) \cong 10log\left(\frac{3 \cdot 2^{2B}}{2}\right) = 6.02{\cdot}B + 1.76\ \ dB \tag{4.10}$$

It is clear that the SNR determines the effective number of bits ($ENOB$) that the converter can resolve, given by

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} \tag{4.11}$$

4.2 Nyquist-Rate A/D Converters

A Nyquist-rate A/D converter (ADC) generates a series of output levels where each of these levels has a one-to-one correspondence to a particular input value. The operation of a Nyquist ADC is illustrated in Figure 4.1. The sampling frequency is twice the analog signal bandwidth, $f_s = 2f_b$. Nyquist-rate converters are usually classified depending on the number of clock cycles they required to complete a single conversion. Some of these converters include flash, sub-ranging, successive approximation and pipelined.

Flash ADCs, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. They only need one clock cycle to perform the conversion and make use of 2^N comparators, where N is the number of bits. They are suitable for applications requiring very large bandwidths. However, because of the matching and accuracy requirements of its analog components (resistors, capacitors) they are limited in resolution. Furthermore, the complexity of the implementation grows exponentially with the number of bits making the flash ADC practical in high-speed applications with a relatively small resolution, typically of 10-bit or less.

To overcome some of the limitations of flash ADCs several architectures have been proposed. The basic idea of these architectures is to divide the quantization process over several cycles. For example, in a sub-ranging ADC two cycles are required to perform the conversion. In the first step, $N/2$ bits are resolved using a $N/2$ flash

ADC. To resolve the remaining $N/2$ bits, the digital signal obtained in the first step is converted back to the analog domain, subtracted from the input signal and then converted. With this kind of architecture only $2^{(N/2)+1}$ comparators are needed, but the latency time is increased by two. This means that two cycles are necessary to perform a single conversion. In addition, the accuracy of these converters would still need to match the overall resolution [28].

Other architectures such as the pipelined use the same technique of dividing the quantization process over several cycles. The major difference is the latency time to perform a single conversion and the number of bits that are resolved by several stages. In addition, some of these architectures require digital correction and calibration techniques to improve the resolution. In other methods such as the successive approximation a single comparator is used and one-bit is resolved per clock cycle. The successive approximation converter applies a binary search algorithm to determine the closest digital representation of the input signal. Therefore, these architectures are called algorithmic converters. From the most significant bit (MSB) to the LSB, each bit is determined by making a comparison with the previous cycle analog result. Consequently, a successive approximation converter needs N clock cycles to complete an N-bit conversion.

4.2.1 Limitations of Nyquist-Rate A/D Converters

Nyquist-rate converters exhibit two major significant limitations: the anti-alias filter and the quantization noise. At first glance, the requirements of an anti-alias filter are fairly straightforward: the passband must accurately pass the desired input signals. The stop-band must attenuate any interferer outside the passband. This attenuation must be sufficient so the residue (remnant after the filter) will not hurt the system performance when aliased into the passband after sampling by the ADC.

Actual design of anti-alias filters can be very challenging. If out-of-band interferers are both very strong and very near the pass frequency of the desired signal, the requirements for filter stop-band and narrowness of the transition band can be quite severe. Severe filter requirements call for high-order filters. Unfortunately, topologies of filters having such characteristics (e.g. Chebychev) typically place costly requirements on component match and tend to introduce phase distortion at the edge of the passband, threatening signal recovery. In addition the pass-band distortion of the analog anti-alias filters should be at least as good as the ADC since any out-of-band harmonics introduced will be aliased.

The second limitation of Nyquist-rate converters is the quantization noise. Nyquist-rate data converters use the minimal required sampling frequency, determined by the Nyquist criteria allowing a maximal quantization error as stated by Equation 4.8. This error has a direct effect on the signal quality as stated by the SNR in Equation 4.9. Moreover, in real designs, quantization is done by comparing the sampled signal values with generated reference voltages. Reference voltages are generated using passive elements such as resistors and capacitors. For high resolution designs, typically greater than 12-bit, the reference voltages are in the order of microvolts. With today's VLSI technology it is difficult to implement such matching and tolerance in the components, limiting the resolution of Nyquist converters.

4.3 Oversampled A/D Converters

Oversampling data converters offer several advantages over Nyquist-rate converters including the anti-alias filter requirements and quantization noise [44]. These advantages are achieved by sampling the input signal at a higher frequency than that of the Nyquist rate. Consequently, a decimation filter is needed at the output to filter

and downsample the digital stream as shown in Figure 4.4. For instance, consider a signal that is sampled at the Nyquist-rate $f_N = 2f_b$ and a signal that is sampled with a sampling frequency of N times the Nyquist frequency $f_s = Nf_N$. The ratio between the sampling rate and the Nyquist frequency is defined as the oversampling ratio (OSR)

$$OSR = \frac{f_s}{f_N} \tag{4.12}$$

Moreover, consider the OSR equal to 2. The spectrum of Nyquist-rate and oversampling-rate sampled signals is illustrated in Figures 4.5(a) and 4.5(c), respectively. The required response for the anti-alias filter of the Nyquist-rate sampled, and oversampled signals is illustrated in Figures 4.5(b) and 4.5(d), in that order. It is evident that the images of the oversampled signal band are not so close to one another and, consequently, specifications of the anti-alias filter can be relaxed as shown in Figure 4.5(d). In addition to the relaxed requirements for the anti-alias filter, the quality of the signal stated by the SNR is improved when oversampling is employed. Assuming that the quantization error is uncorrelated and uniformly distributed, the quantization noise is considered to be white and its power spread over the entire frequency range. Following Equation 4.8 the quantization noise is spread along the entire frequency range, but for the oversampling case the sampling frequency has been increased by a

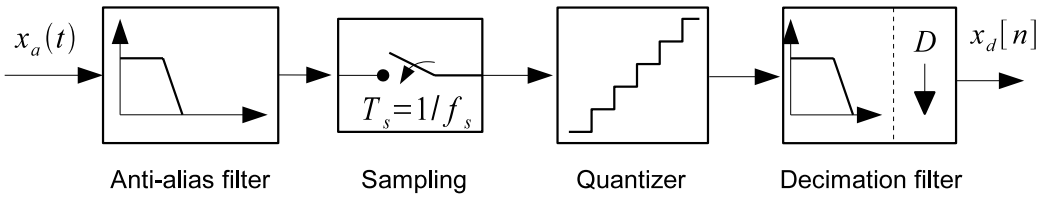
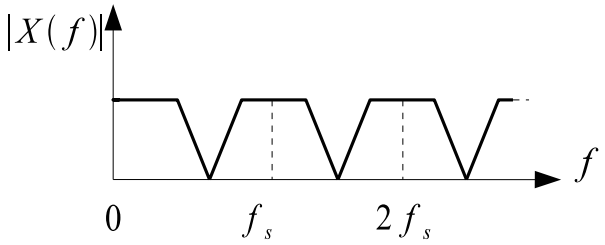
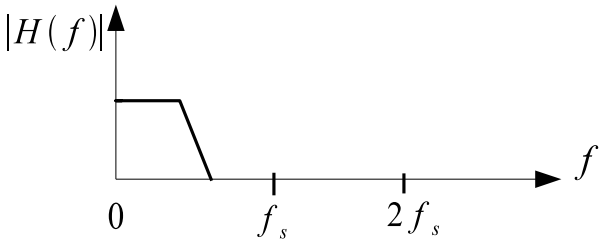


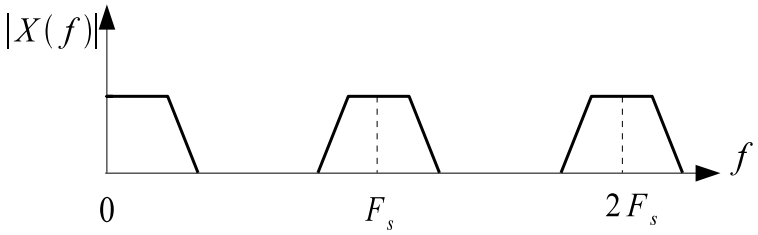
Figure 4.4. Conventional oversampled A/D converter.



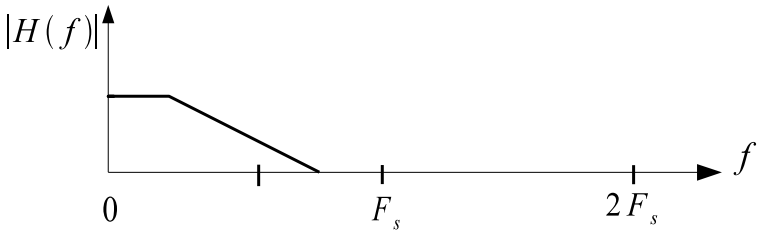
(a) Nyquist-rate sampled signal spectrum



(b) Anti-alias filter response for Nyquist-rate ADC



(c) Oversampled signal spectrum



(d) Anti-alias filter response for Oversampled ADC

Figure 4.5. Anti-alias filter response for Nyquist-rate and oversampled ADC.

factor OSR. Consequently, the in-band quantization power can be expressed as

$$P_Q = \int_0^{f_b} S_E(f)df = \frac{\Delta^2}{12}\frac{2f_b}{F_s} = \frac{\Delta^2}{12OSR} \tag{4.13}$$

The power part of the quantization noise lying outside the signal band can be eliminated by means of a digital filter. Accordingly, the SNR for a sine wave is given by

$$SNR = 10log\left(\frac{A^2/2}{(\Delta^2/2)/OSR}\right) = 6.02{\cdot}B + 1.76 + 10log(OSR)\ \ dB \tag{4.14}$$

Equation 4.14 shows that the SNR is improved by 3dB every time the sampling frequency is doubled. Moreover, this improvement in the SNR is equivalent to adding half a bit in the resolution of the quantizer.

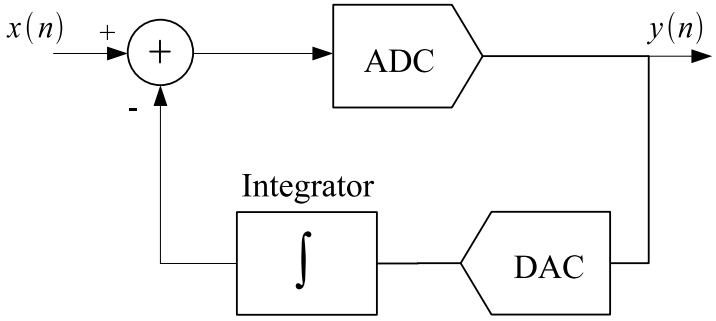
4.3.1 Error Mechanisms in Oversampled A/D Converters

In oversampled converters, quantization noise can be further reduced or shaped by adding a feedback loop. A much greater improvement in resolution with increasing OSR can be obtained by embedding a quantizer in the feedback loop. Feedback can be use for prediction or noise shaping, which is implemented by Δ modulation and $\Sigma\Delta$ modulation, respectively.

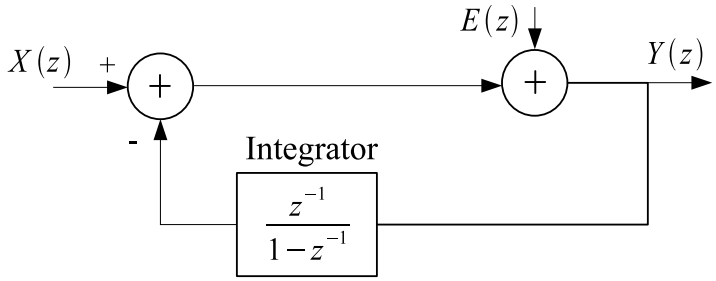
Δ Modulator

The predictive delta modulator (ΔM) reduces the quantization noise by only detecting the change of the signal rather than the absolute signal value. When a signal is oversampled, successive samples do not change significantly in the interval. This can lead to a reduction in the number of quantization levels if the difference of two consecutive samples is quantized. Since the values of these samples are very close,

they are highly correlated and therefore future samples could be predicted from the past ones. Therefore, a modulator whose operation is based on this prediction principle is called a predictive modulator. Figures 4.6(a) and 4.6(b) illustrate the ΔM block diagram and its corresponding z-domain model, respectively. In general, the ΔM is formed by a differential loop where the difference $x(n) - x(n-1)$ is quantized to give the output sequence $y(n)$ so that the signal $x(n-1)$ should track the input signal $x(n)$ all the time. The advantage of this structure is that for oversampled signals the



(a) ΔM block digram



(b) ΔM linear z-domain model

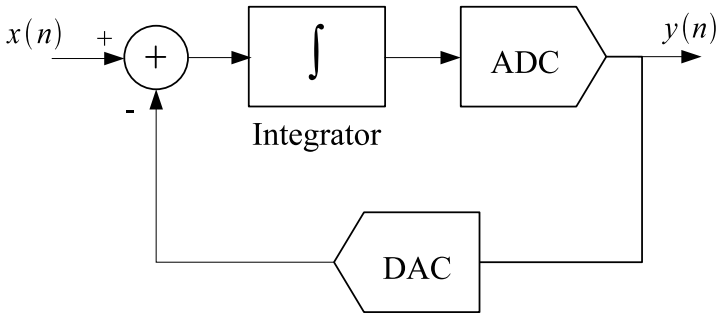
Figure 4.6. ΔM block diagram and linear model.

difference $x(n) - x(n-1)$ is much smaller that $x(n)$ itself, on average, and hence the larger input signals can be allowed. There are, however, several disadvantages. The main drawback of a predictive modulator is the slope overload for rapidly changing input signals $x(n)$. When the input signal changes faster than $\Delta/(2T_s)$, where Δ is the quantization step, the modulator starts losing track of the input and slope overload occurs. In addition, the integrator is in the feedback path, and hence its

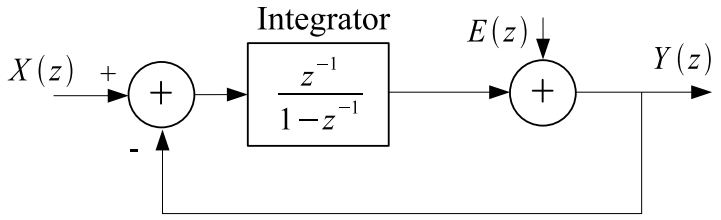
nonidealities limit the achievable linearity and accuracy.

ΣΔ Modulator

A ΣΔM is an alternative oversampling architecture which avoids the drawbacks of the ΔM. Figure 4.7(a) illustrates the block diagram while Figure 4.7(b) the corresponding linear model for a first-order ΣΔM. The noise-shaping ΣΔM is derived from the ΔM with an additional integrator in front of the quantizer. A ΣΔM also performs a coarse quantization of the input signal, but it employs filtering and negative feedback to shift a large amount of the quantization noise to higher frequencies, out of the signal band. Thereby, the in-band quantization noise is reduced and high resolutions can be achieved. Out-of-band noise, including quantization noise, is suppressed by a subsequent digital low-pass filter (decimation filter).



(a) First-order ΣΔM block digram



(b) First-order ΣΔM linear z-domain model

Figure 4.7. First-order ΣΔM block and linear model.

The main advantage of the ΣΔM in comparison with the ΔM is the shaping of the quantization noise toward high frequencies. Noise shaping in combination with

oversampling is the key to improve the SNR and consequently achieve high resolution.

4.4 ΣΔ Modulator Architectures

A conventional ΣΔ A/D converter is shown in Figure 4.8. Oversampling converters reduce the in-band quantization noise by spreading it uniformly across the frequency band. Moreover, oversampling ΣΔ ADCs reduce the quantization noise power inside the signal band by pushing most of the in-band noise outside the signal band. The output of the ΣΔM is then low-pass filtered and finally down sampled to or near to the Nyquist rate like conventional oversampled converters as shown in Figure 4.8.

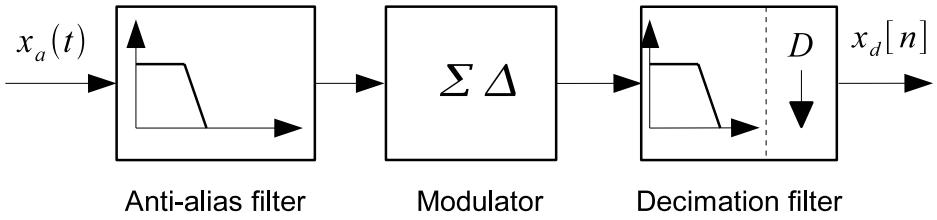


Figure 4.8. Conventional oversampled ΣΔ A/D converter.

The quantization noise spreading and shaping characteristics are present in various types of ΣΔMs. The noise shaping properties of the modulator define its order and properties. The following sections introduce the fundamental ΣΔM topologies and their base analysis.

4.4.1 First-Order ΣΔ Modulator

A block diagram and linear model of a First-order ΣΔM are shown in Figures 4.7(a) and 4.7(b), respectively. The main components are: a summing node at the input, an integrator, an ADC and a DAC inside the feedback loop. Since the integrator has infinite DC gain, the loop has infinite DC gain and therefore the DC

component average is zero. Therefore the DC component at the output of the feedback DAC will be identical to the DC component of the input signal. From the previous it is reasonable to think that even for a single-bit ADC where the quantization error is considerable, the averaged quantized signal tracks the analog input signal.

As an example consider a single-bit ADC with a DC input of 0.28V. Assuming the initial condition of the integrator feedback reference to be a negative reference voltage, the output of the first 20 cycles is: 0, 1, 0, 1, 0, 0, 0, 1, 0, 1, 0, 0, 1, 0, 0, 0, 0, 0, 0, and 0. Furthermore, the average of this stream is 0.25V. The past example shows that the resolution of the modulator will increase as the number of samples included in the average is increased [20]. The increase in the number of samples is achieved by an increase in the OSR. On the other hand an increase in the OSR decreases the bandwidth.

Modulation Noise for Busy Signals

Consider the first-order ΣΔM linear model shown in Figure 4.7(b). Analyzing the linear system, using the z-transform, the output $Y(z)$ yields

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right) E(z) \tag{4.15}$$

From this equation we can obtain the signal transfer function (STF) is and the noise transfer function (NTF)

$$STF(z) = z^{-1} \tag{4.16}$$

$$NTF(z) = 1 - z^{-1} \tag{4.17}$$

Equations 4.16 and 4.17 state that the STF delays the signal, not altering its content, while the NTF suppress the quantization error at low frequencies (high-pass filter). Since the signal is oversampled by OSR, the quantization noise is further reduced inside the signal band $[0, f_s/2OSR]$. Assuming that the quantization noise is uncorrelated and uniformly spread in the signal band, the power spectral density (PSD) of the modulation noise is

$$S_Q(f) = S_E(f)\left(1 - \exp^{-j2\pi f T_s}\right)^2 = 4S_E(f)sin^2\left(\frac{2\pi f}{2f_s}\right) \tag{4.18}$$

In comparison with Equation 4.13, feedback around the quantizer reduces the noise at low frequencies, but increases it at high frequencies as shown in Figure 4.9. The total noise power in the signal band is

$$P_Q = \int_0^{f_b} S_Q(f)df \approx \frac{\Delta^2}{12}\frac{\pi^2}{3OSR^3} \;\; f_s^2 >> f_b^2 \tag{4.19}$$

Moreover, each doubling of the OSR reduces the noise by 9dB and provides 1.5 bits of extra resolution. A digital filter is required at the output of the modulator, so the modulated signal can be decimated to the Nyquist rate. Otherwise, the pushed noise toward high-frequencies will degrade the resolution when it is sampled at the Nyquist rate [41].

Pattern Noise

When the input to the first-order modulator is a DC signal, the quantized signal bounces between two levels keeping its mean value close to the input signal. The frequency of repetition depends on the input level affecting the modulator performance. When this frequency lies in the signal band the modulation is said to be noisy, other-

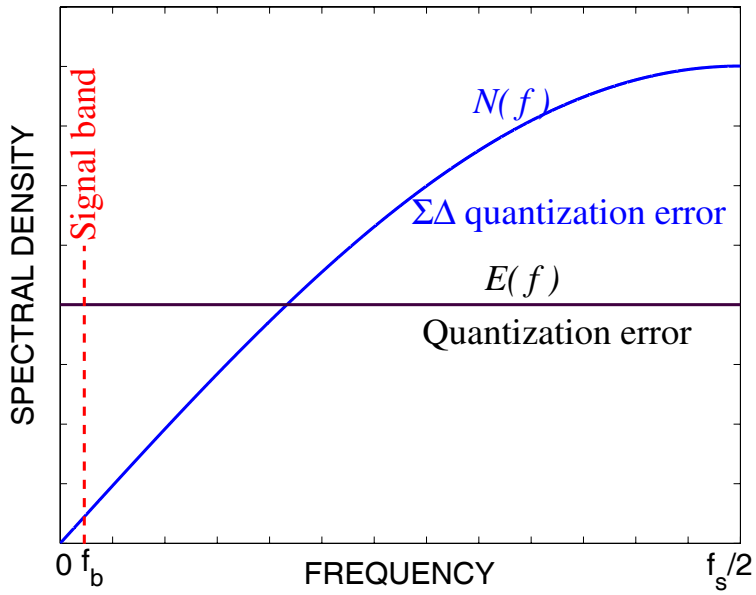


Figure 4.9. PSD for ΣΔM quantization and ordinary noise.

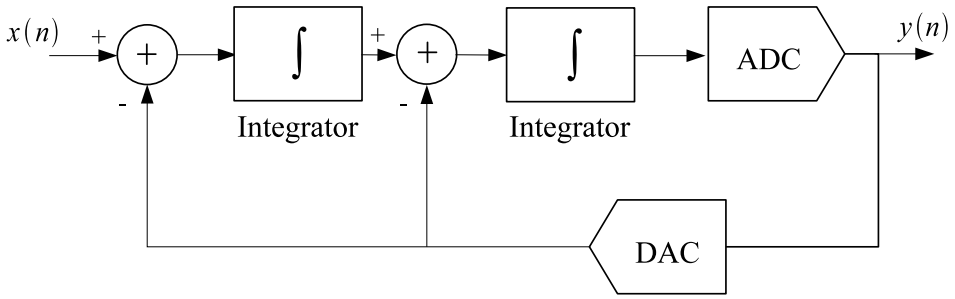
wise is said to be quiet. The structure of the quantization noise developed by noisy modulation is called pattern noise [41].

Dead Zones

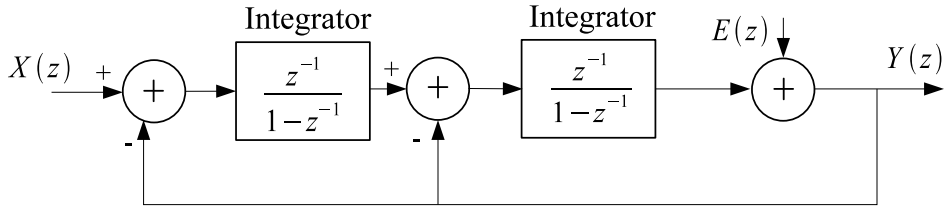
If small, fast changes appear at the modulator input they might be ignored under certain conditions. It can be shown that the location and extension of such transient dead zones corresponds to the position and size with the peaks of the pattern noise. In most applications the pattern noise is more noticeable than the dead zones. This may not be true when the integrator is leaky, having low DC gain. In this case the dead zones might be significant [41].

4.4.2 Second-Order ΣΔ Modulator

For a second-order ΣΔM the NTF is $N(z) = (1 - z^{-1})^2$. Figures 4.10(a) and 4.10(b) show the block diagram and its linear model for this modulator architecture.



(a) Second-order ΣΔM block digram



(b) Second-order ΣΔM linear z-domain model

Figure 4.10. Second-order ΣΔM block and linear model.

The spectral density of this noise is

$$S_Q(f) = S_E(f)\left(1 - \exp^{-j2\pi f T_s}\right)^4 = 16 S_E(f) sin^4\left(\frac{2\pi f}{2f_s}\right) \tag{4.20}$$

Moreover, for busy signals the noise is given by

$$P_Q = \int_0^{f_b} S_Q(f)df \approx \frac{\Delta^2}{12}\frac{\pi^4}{5OSR^5} \quad f_s^2 >> f_b^2 \tag{4.21}$$

For this architecture the noise falls by 15dB for each doubling of the OSR, giving 2.5 extra bits of resolution [41].

4.4.3 Higher-Order ΣΔ Modulators

Higher order modulators are obtained by adding more feedback loops to the system. In general, an L-order modulator contains L feedback loops. When the modu-

lator is not overloaded, the noise spectral density is given by

$$S_Q(f) = S_E(f)\left(1 - \exp^{-j2\pi f T_s}\right)^{2L} = 2^{2L} S_E(f) sin^{2L}\left(\frac{2\pi f}{2f_s}\right) \tag{4.22}$$

Similarly, for $f_s^2 >> f_b^2$ the rms noise in the signal band can be approximated by

$$P_Q = \int_0^{f_b} S_Q(f)df \approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}} \tag{4.23}$$

Figure 4.11 shows the spectral densities for $L = 1, 2$ and 3. In accordance with the analysis, the quantization noise falls $[3\,(2L+1)]$ dB for every doubling of the OSR, providing $(L + 0.5)$ extra bits of resolution. A drawback of ΣΔMs with $L > 2$ is their high tendency to instability [37].

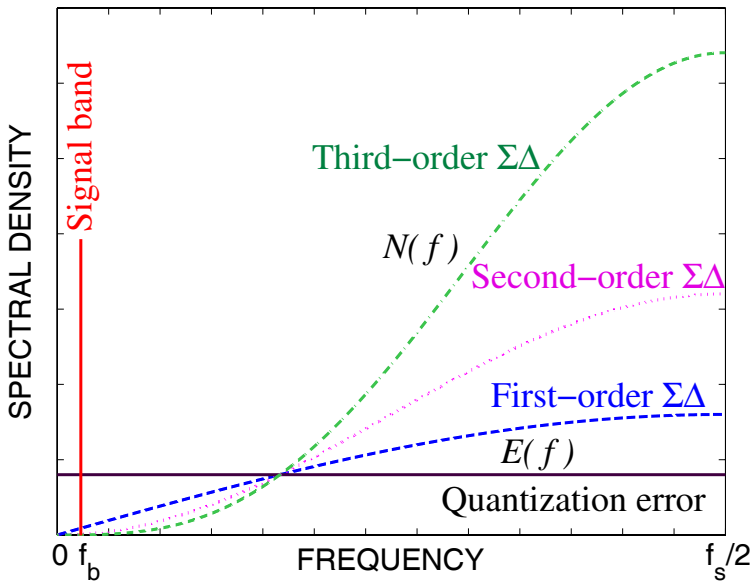


Figure 4.11. PSD for different order ΣΔM quantization and ordinary noise.

4.4.4 Multi-bit ΣΔ Modulators

Multi-bit ΣΔ Modulators offer several advantages over single-bit implementations. The main difference between a multi-bit and a single-bit architecture is that single-bit architectures have a 2-level quantizer, while multi-bit architectures have a quantizer with M-levels where $M > 2$. The main quality of ΣΔMs employing multi-bit quantizers is that the SNR is dramatically improved. In comparison with a single-bit modulator, a multi-bit structure typically provides an increase of 6 dB per additional bit. Therefore, it is possible to increase the overall resolution of any ΣΔ ADC without increasing the OSR by simply increasing the number of levels in the internal quantizers. Equivalently, architectures with multi-bit quantizers can achieve resolutions comparable to those of architectures with single-bit quantizers at lower OSR. Furthermore the use of multi-bit quantization improves stability in high-order modulators [37].

There are some drawbacks with the use of multi-bit quantizer in ΣΔMs. Adding a multi-bit quantizer requires a multi-bit D/A converter (DAC) in the feedback loop increasing the complexity of the analog and digital circuitry. The most significant problem with multi-bit designs is the local DAC linearity and mismatch which degrades the performance. These nonidealities require additional digital circuitry, such as dynamic element matching techniques (DEM) to reduce the error. Consequently, more area and power are needed to support the design.

4.5 ΣΔ Converters for Wideband Applications

Mobile telecommunications have experienced tremendous growth since the progressive development of wireless communication systems. Today, several different mobile telecommunication standards are used worldwide in the transition from the

second generation (2G) digital system into the third generation (3G) system, which include global system mobile (GSM) communications, general packet radio service (GPRS), and a wideband code division multiple access system (WCDMA) [12]. The main applications of mobile telecommunications are to provide high quality voice communications, high-speed data transmissions, real-time dynamic images, and multimedia services. Consequently, digital communications require high speed and high resolution A/D converters.

Figure 4.12 shows a block diagram of a receiver suitable for GSM/WCDMA wideband communications, where the $\Sigma\Delta$ data converter is at the right end [57]. In this multi-standard wideband receiver, two sets of band filters and low noise amplifiers (LNA) are required for GSM/WCDMA selection. The RF signal is directly down converted using a tunable frequency synthesizer. The subsequent filtering and gain amplification are all to be done in baseband at low frequencies followed by the high-resolution high-speed $\Sigma\Delta$ A/D converter. High-speed digital signal processing (DSP) techniques can then be used to demodulate the digital signals.

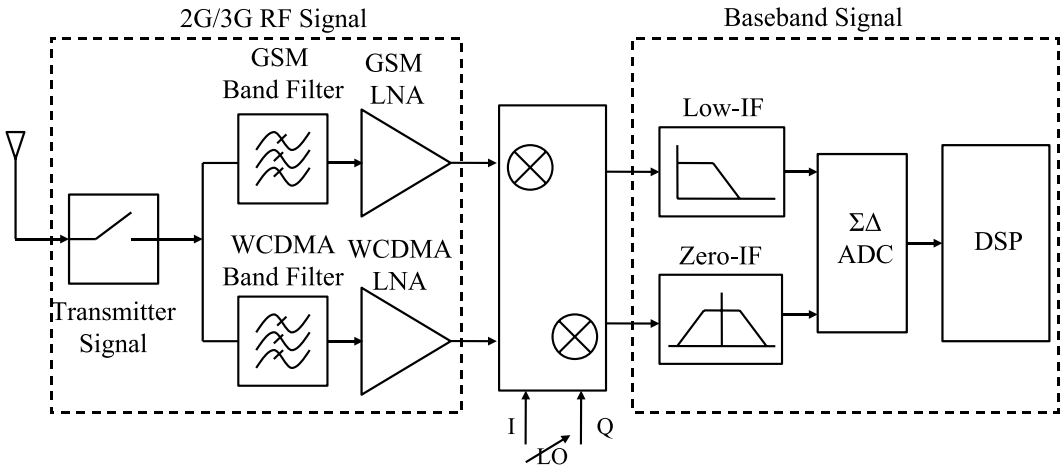


Figure 4.12. Zero-IF Receiver Architecture.

Oversampling $\Sigma\Delta$ converters have become a top choice solution for mobile telecommunications. This is mainly due the high-resolution, and low sensitivity to analog

component imperfections and noisy conditions characteristics. Several designs of $\Sigma\Delta$ A/D converters for wideband communications have been reported evidencing the advantages of $\Sigma\Delta$ converters for high-speed and high resolution applications. For detailed information on $\Sigma\Delta$ converters for wideband applications the reader is referred to the works of Gomez and Haroung [26], Altun, Koh and Allen [1], Chiang, Chou and Chang [12], Burger and Huang [8], Dezzani and Andre [15], and Farahani and Ismail [19].

CHAPTER 5

Modeling of Error Sources in $\Sigma\Delta$ Modulators

The equations presented in Chapter 4 assumed the use of ideal components and only consider the quantization noise. Nevertheless, this is not the case in practice. Although, $\Sigma\Delta$Ms are intrinsically less sensitive to noise sources and components nonidealities, it is necessary to analyze its effect on the $\Sigma\Delta$M performance. The importance of these becomes crucial when design specifications can bring out significant performance degradation [5][37]. Consequently, their analysis becomes mandatory to obtain behavioral models for accurate time-domain simulations. The main nonidealities are the switched-capacitor (SC) integrator defective settling, thermal noise, jitter, capacitance mismatch, and DAC mismatch.

5.1 Integrator Dynamics

The integrator is the fundamental block of a $\Sigma\Delta$M and therefore its nonidealities largely affect the $\Sigma\Delta$M performance. Figure 5.1 shows a typical double branch SC integrator. Nonidealities such as the defective settling become one of the domina-

ting limiting factors in SC ΣΔMs, especially for those performing at high sampling frequencies. The defective settling is defined as an incomplete charge transfer inside the SC integrator, mostly due to the operational transconductance amplifier (OTA) characteristics. The finite and nonlinear DC gain, the finite gain-bandwidth (GBW), and the slew-rate (SR) limitation are among the most common. Moreover, these characteristics introduce unwanted harmonic components affecting the performance of the ΣΔM. The third harmonic in the spectral density plot is the most common component.

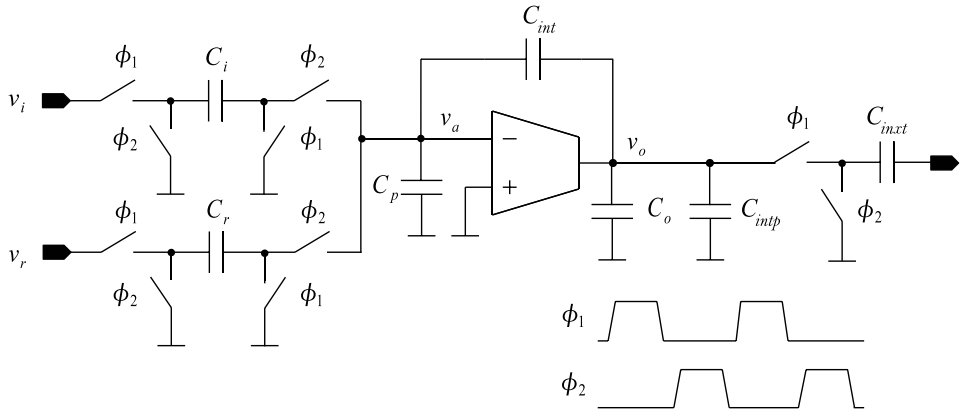


Figure 5.1. Typical double branch SC integrator.

5.1.1 Traditional Transient Response

The effects of the defective settling are better described by an integrator transient model such as the one presented in [37]. To describe the transient behavior, consider the SC integrator of Figure 5.1, where C_i and C_r are the input and reference capacitors respectively, C_p corresponds to the sum of OTA input and summing node bottom plate parasitic capacitance, C_o the OTA output, C_{intp} the integrating bottom plate parasitic capacitance and C_{inxt} the next stage capacitance. The corresponding amplifier is modeled with a single-pole, dynamic non-linear current function with

maximum output current I_o, transconductance g_m, output conductance g_o, and output capacitance C_o as shown in Figure 5.2.

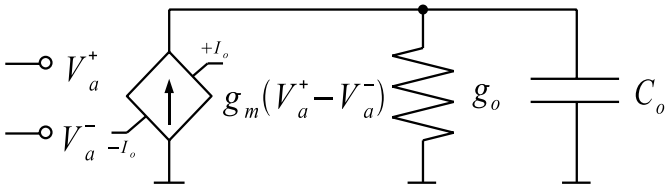


Figure 5.2. OTA model.

Integration Phase (ϕ_2)

To describe the transient response during integration (ϕ_2), consider the SC integrator shown in Figure 5.3. Assuming that the output resistance of the amplifier is large, the integrator output voltage v_o changes abruptly in the opposite direction to that of the final increase [51]. Similarly, v_a exhibits a jump from zero toward the opposite sign of to that of the final v_o. The charge conservation theorem states that the initial voltage at v_a will be given by

$$v_{ai,i} = \frac{1}{C_{int,eq}} \left(1 + \frac{C_{o,eq}}{C_{int}}\right) (-v_i C_i - v_r C_r) + \frac{C_p + C_{o,eq}\,(1 + C_p/C_{int})}{C_{int,eq}} v_{a,n-1} \qquad (5.1)$$

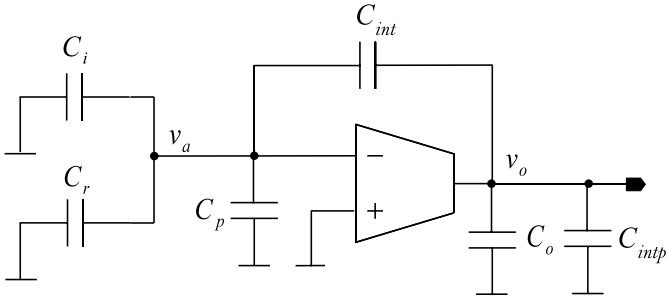


Figure 5.3. SC Integrator during integration.

Using $v_{a,n-1} \neq 0$ reflects a possible defective settling at the previous sampling phase. In addition, $C_{int,eq}$, $C_{o,eq}$ and $C_{i,eq}$ are the lumped capacitances for the integration phase given by

$$C_{i,eq} = C_i + C_r + C_p \tag{5.2}$$

$$C_{o,eq} = C_o + C_{intp} \tag{5.3}$$

$$C_{int,eq} = C_{i,eq} + \frac{C_{i,eq}}{C_{int}} \tag{5.4}$$

Using the amplifier dynamic model, assuming that $g_m >> g_o$, and depending on $v_{ai,i}$ and the slewing time (t_o) three scenarios are possible for the amplifier operation: linear, slewing, and partial slewing.

- Linear $|v_{ai,i}| \leq I_o/g_m$

$$v_a(\phi_2) = v_{ai,i} \exp\left(-\frac{g_m}{C_{int,eq}} t\right) \tag{5.5}$$

- Slewing $|v_{ai,i}| > I_o/g_m$ and $t < t_{o,i}$

$$v_a(\phi_2) = v_{ai,i} - \frac{I_o}{C_{int,eq}} sgn\left(v_{ai,i}\right) t \tag{5.6}$$

- Partial Slewing $|v_{ai,i}| > I_o/g_m$ and $t \geq t_{o,i}$

$$v_a(\phi_2) = -sgn\left(v_{ai,i}\right) \frac{I_o}{g_m} \exp\left\{-\frac{g_m}{C_{int,eq}} \left(t - t_{o,i}\right)\right\} \tag{5.7}$$

where t is the integration time. Moreover, the slewing time $t_{o,i}$ is given by

$$t_{o,i} = \frac{|v_{ai,i}|}{SR} - \tau_{int} = \frac{C_{int,eq}}{I_o} |v_{ai,i}| - \frac{C_{int,eq}}{g_m} \tag{5.8}$$

$$\tau_{int} = \frac{C_{int,eq}}{g_m} \tag{5.9}$$

$$SR = \frac{I_o}{C_{int,eq}} \tag{5.10}$$

where τ_{int} is the settling time constant during integration and SR the amplifier slew rate. Finally, during the integration phase the amplifier output is given by

$$v_o(\phi_2) = v_{o,n-1} - \left(1 + \frac{C_p}{C_{int}}\right) v_{a,n-1} - \left[\frac{C_i}{Cint}(-v_i) + \frac{C_r}{Cint}(-v_r)\right] + \left(1 + \frac{C_p + C_i + C_r}{C_{int}}\right) v_a(\phi_2) \tag{5.11}$$

Sampling Phase (ϕ_1)

During the next sampling phase, the voltage across C_{int} is constant while v_a drops exponentially to zero. Figure 5.4 shows the SC integrator configuration during the sampling phase. The charge conservation states that the initial voltage at v_a during the sampling phase (ϕ_1) will be given by

$$v_{ai,s} = v_a(\phi_2) - \frac{C_{inxt}}{C_{samp,eq}} v_o(\phi_2), \tag{5.12}$$

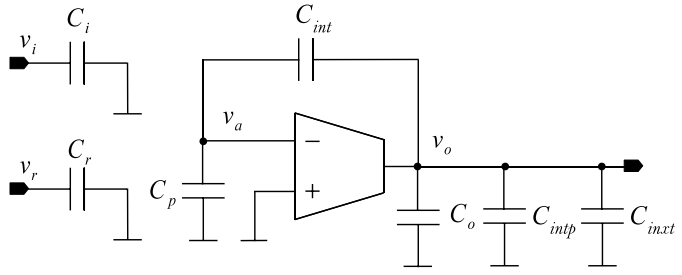


Figure 5.4. SC Integrator during sampling.

where the lumped capacitance $C_{samp,eq}$ during the sampling phase results to be

$$C_{samp,eq} = C_p + (C_o + C_{intp} + C_{inxt}) \left(1 + \frac{C_p}{C_{int}}\right) \tag{5.13}$$

Applying a similar analysis, the sampling phase can be described with three possible scenarios: linear, slewing and partial-slewing. Assuming that $g_m >> g_o$, the final voltages at node v_a are given by

- Linear $|v_{ai,i}| \leq I_o/g_m$

$$v_a(\phi_1) = v_{ai,s} \exp\left(-\frac{g_m}{C_{samp,eq}} t\right) \tag{5.14}$$

- Slewing $|v_{ai,i}| > I_o/g_m$ and $t < t_{o,s}$

$$v_a(\phi_1) = v_{ai,s} - \frac{I_o}{C_{samp,eq}} sgn\left(v_{ai,s}\right) t \tag{5.15}$$

- Partial Slewing $|v_{ai,i}| > I_o/g_m$ and $t \geq t_{o,s}$

$$v_a(\phi_1) = sgn\left(v_{ai,s}\right) \frac{I_o}{g_m} \exp\left\{-\frac{g_m}{C_{int,eq}} \left(t - t_{o,s}\right)\right\}, \tag{5.16}$$

where t is the sampling phase duration time. In this case the slewing time during the sampling phase is given by

$$t_{o,s} = \frac{|v_{ai,s}|}{SR} - \tau_{samp} = \frac{C_{samp,eq}}{I_o} |v_{ai,s}| - \frac{C_{samp,eq}}{g_m} \tag{5.17}$$

$$\tau_{samp} = \frac{C_{samp,eq}}{g_m} \tag{5.18}$$

$$SR = \frac{I_o}{C_{samp,eq}} \tag{5.19}$$

where τ_{samp} is the settling time constant during the sampling phase and SR the slew rate. At the end of the sampling phase, the output voltage is expressed by

$$v_o(\phi_1) = v_o(\phi_2) + \left(1 + \frac{C_p}{C_{int}}\right)[v_a(\phi_1) - v_a(\phi_2)] \tag{5.20}$$

5.1.2 Proposed Transient Response

The increase in frequency on high-resolution, high-speed discrete-time (DT) ΣΔMs, has made the incomplete settling of SC integrators one of the most limiting factors in the performance of ΣΔMs. Although a detailed settling of the integrator is not strictly necessary for the modeling of ΣΔMs, a robust model is convenient and becomes crucial in high frequency applications [39]. The need for such a model arises from the relationship between the degrading effects of harmonic distortion and their power consumption. Although traditional transient models consider the amplifier transconductance g_m and output conductance g_o relation in the analysis of the SC integrator, they neglect g_o due its small value in comparison with g_m. Although this is a valid approximation for designs where $g_m >> g_o$, it ceases to hold in low-power designs, leading to modeling errors in ΣΔMs. Neglecting g_o when modeling deep sub-micron type of designs introduce errors in the integrator model and consequently in the ΣΔM. What is more, traditional models do not consider the ratio between slewing and non-slewing amplifier loads and its effect when modeling the settling time as proposed in [21]. All this may lead to under or over estimation of the SC integrator incomplete settling behavior, a factor of great importance for high speed and low power applications.

Previously modified SC integrator models including all these effects, namely the symbolic node admittance matrix [20] exhibited accuracy limitations in modeling ΣΔMs at high frequencies (e.g. WCDMA). The proposed model is intended to include

all these effects but providing high accuracy at high frequencies [59]. Accordingly, this model will provide a convenient tool to aid in the design of low-power high-speed SC ΣΔMs. The proposed SC integrator transient model is presented in the following subsections.

Integration Phase (ϕ_2)

A similar analysis applies to that of the traditional SC integrator behavioral model but including the amplifier output conductance g_o. Let $v_{a,n-1}$ and $v_{o,n-1}$ be the amplifier input and output voltages from the previous sampling phase, respectively. The charge conservation law at the beginning of the integration phase states that the initial voltage at node v_a is given by

$$v_{ai,i} = \frac{1}{C_{int,eq}}\left(1+\frac{C_{o,eq}}{C_{int}}\right)\left(-v_i C_i - v_r C_r\right) + \frac{C_p + C_{o,eq}\left(1+C_p/C_{int}\right)}{C_{int,eq}} v_{a,n-1} \quad (5.21)$$

The amplifier response relies on the relation between $v_{ai,i}$, I_o/g_m and the slewing time $t_{o,i}$. Depending on the initial voltage $v_{ai,i}$ three cases are described: linear, slewing and partial slewing evolutions.

- Linear $|v_{ai,i}| \leq I_o/g_m$

$$v_a\left(\phi_2\right) = \left(v_{ai,i} + \frac{v_{o,n-1} + v_i' C_i + v_r' C_r}{A_i}\right) \exp\left\{-\frac{g_m + g_o\left(1+C_{i,eq}/C_{int}\right)}{C_{int,eq}} t\right\} - \frac{v_{o,n-1} + v_i' C_i + v_r' C_r}{A_i} \quad (5.22)$$

- Slewing $|v_{ai,i}| > I_o/g_m$ and $t < t_{o,s}$

$$v_a\left(\phi_2\right) = \left[v_{ai,i} + \frac{v_{o,n-1} + v_i' C_i + v_r' C_r}{1+C_{i,eq}/C_{int}} - \frac{I_o \mathrm{sgn}\left(v_{ai,i}\right)}{g_o\left(1+C_{i,eq}/C_{int}\right)}\right]$$

$$\cdot \exp\left\{-\frac{g_o\left(1+C_{i,eq}/C_{int}\right)}{C_{int,eq}}t\right\} - \frac{v_{o,n-1}+v_i'C_i+v_r'C_r}{1+C_{i,eq}/C_{int}} + \frac{I_o \mathrm{sgn}\left(v_{ai,i}\right)}{g_o\left(1+C_{i,eq}/C_{int}\right)} \tag{5.23}$$

- Partial Slewing $|v_{ai,i}| > I_o/g_m$ and $t \geq t_{o,s}$

$$v_a\left(\phi_2\right) = \left[-\frac{I_o}{g_m}\mathrm{sgn}\left(v_{ai,i}\right) + \frac{v_{o,n-1}+v_i'C_i+v_r'C_r}{A_i}\right] \cdot \exp\left\{-\frac{g_m+g_o\left(1+C_{i,eq}/C_{int}\right)}{C_{int,eq}}\left(t-t_{o,i}\right)\right\} - \frac{v_{o,n-1}+v_i'C_i+v_r'C_r}{A_i} \tag{5.24}$$

where $C_{i,eq}$ and $C_{int,eq}$ are the same as in Equation 5.2 and Equation 5.4, respectively. Moreover, A_i, $t_{o,i}$, and $C_{int,slew}$ are given by

$$A_i = 1 + \frac{g_m}{g_o} + \frac{C_i + C_r + C_p}{C_{int}} \tag{5.25}$$

$$t_{o,i} = |v_{ai,i}|\frac{C_{int,slew}}{I_o} - \frac{C_{int,eq}}{g_m} \tag{5.26}$$

$$C_{int,slew} = C_{o,eq} + \frac{C_{i,eq}C_{int}}{C_{i,eq}+C_{int}} \tag{5.27}$$

The new equivalent load $C_{int,slew}$, is used to calculate a more accurate SR and settling time. It can be noticed that Equation 5.4 is highly dependent on C_i while Equation 5.27 is dependent on C_o. This modification may have a great impact on the settling effects of the model [21]. Finally, the amplifier output voltage v_o is the same as for the traditional model given by

$$v_o(\phi_2) = v_{o,n-1} - \left(1 + \frac{C_p}{C_{int}}\right) v_{a,n-1} - \left[\frac{C_i}{Cint}(-v_i) + \frac{C_r}{Cint}(-v_r)\right] + \left(1 + \frac{C_p + C_i + C_r}{C_{int}}\right) v_a(\phi_2) \tag{5.28}$$

Sampling Phase (ϕ_1)

The same analysis is applied for the sampling phase. Let $v_{o,n-1}$ be the voltage from the previous integration phase. The charge conservation states that the initial voltages of the sampling phase will be given by

$$v_{ai,s} = v_a(\phi_2) - \frac{C_{inxt}}{C_{samp,eq}} v_o(\phi_2) \tag{5.29}$$

where $C_{samp,eq}$ is the same given by Equation 5.13. Depending on $v_{ai,s}$ and the slewing time $t_{o,s}$ for the sampling phase, the same three scenarios are possible: linear, slewing and partial slewing.

- Linear $|v_{ai,i}| \leq I_o/g_m$

$$v_a(\phi_1) = \left(v_{ai,i} + \frac{v_{o,n-1}}{A_i}\right) \cdot \exp\left\{-\frac{g_m + g_o(1 + C_p/C_{int})}{C_{samp,eq}} t\right\} - \frac{v_{o,n-1}}{A_i} \tag{5.30}$$

- Slewing $|v_{ai,i}| > I_o/g_m$ and $t < t_{o,s}$

$$v_a(\phi_1) = \left[v_{ai,i} + \frac{v_{o,n-1}}{1 + C_p/C_{int}} - \frac{I_o \text{sgn}(v_{ai,i})}{g_o(1 + C_p/C_{int})}\right] \cdot \exp\left\{-\frac{g_o(1 + C_p/C_{int})}{C_{samp,eq}} t\right\} - \frac{v_{o,n-1}}{1 + C_p/C_{int}} + \frac{I_o \text{sgn}(v_{ai,i})}{g_o(1 + C_p/C_{int})} \tag{5.31}$$

- Partial Slewing $|v_{ai,i}| > I_o/g_m$ and $t \geq t_{o,s}$

$$v_a(\phi_2) = \left[-\frac{I_o}{g_m} \mathrm{sgn}(v_{ai,i}) + \frac{v_{o,n-1}}{A_s} \right]$$

$$\cdot \exp\left\{ -\frac{g_m + g_o(1 + C_p/C_{int})}{C_{samp,eq}} (t - t_{o,s}) \right\} - \frac{v_{o,n-1}}{A_s} \tag{5.32}$$

where the slewing time during the sampling phase $t_{o,s}$, $C_{samp,slew}$ and A_s are given by

$$t_{o,s} = |v_{ai,s}| \frac{C_{samp,slew}}{I_o} - \frac{C_{samp,eq}}{g_m} \tag{5.33}$$

$$C_{samp,slew} = C_o + C_{intp} + C_{inxt} + \frac{C_p C_{int}}{C_p + C_{int}} \tag{5.34}$$

$$A_s = \frac{g_m}{g_o} + \left(1 + \frac{C_p}{C_{int}}\right) \tag{5.35}$$

At the end of the sampling phase, the output voltage, expressed by equation (5.36), is the same as the voltage across C_{int} at the integration

$$v_o(\phi_1) = v_o(\phi_2) + \left(1 + \frac{C_p}{C_{int}}\right) (v_a(\phi_1) - v_a(\phi_2)) \tag{5.36}$$

Unlike the traditional model, the ratio between the slewing and non-slewing amplifier loads is considered when modeling the settling time t_o, as proposed in [21]. This is noticeable in the settling time t_o expression for both integration and sampling phases in Equations 5.26 and 5.33 where the $C_{int,slew}$ and $C_{samp,slew}$ are used. Taking in account this effect in addition to the g_m/g_o relationship, the proposed model is expected to provide a more reliable behavioral model of the degrading effects of settling errors on high-speed $\Sigma\Delta$Ms.

5.2 Thermal Noise

Thermal noise in integrated circuits is caused by the random fluctuation of carriers due to thermal energy. ΣΔMs exhibit thermal noise from the OTA and the finite switch resistance of the SC integrator during the sampling and integration phases. Thermal noise has a white spectrum and a wide band, limited only by the time constants of the switched capacitors or the bandwidths of the amplifiers. Since aliasing needs to be taken into account, calculations involving thermal noise are complicated. For a detailed analysis and calculations of the thermal noise the reader is referred to the works of Fisher and Medeiro [22], [37].

The thermal noise power spectral density (PSD) during sampling is given by equation (5.37),

$$S_{eq,samp}(f) = \left(1 + \frac{C_r^2}{C_i^2}\right) \frac{4kT}{3f_s\left(C_i + C_r + C_p\right)} \left(\frac{\tau_{samp}}{T_s}\right)^2 + \left(1 + \frac{C_r}{C_i}\right) \frac{2kT}{f_s C_i} \left(\frac{\tau_{samp}}{T_s}\right)^2 \tag{5.37}$$

where C_i and C_r are the input and reference sampling capacitors, C_p is the OTA parasitic input capacitance, k is the Boltzman constant, T the temperature, t_{samp} is the duty cycle of the sampling phase, f_s is the sampling frequency, and $T_s = 1/f_s$.

Moreover, the PSD for the thermal noise during the integration phase is given by equation (5.38),

$$S_{eq,int}(f) = \left(1 + \frac{C_r^2}{C_i^2}\right) \frac{4kTg_mR_{on}}{3f_s\left(C_i + C_r + C_p\right)} \left(\frac{\tau_{int}}{T_s}\right)^2 \tag{5.38}$$

where all the parameters are the same as equation (5.37), g_m is the OTA transconductance, R_{on} is the switch on-resistance and t_{int} is the duty cycle of the integration

phase. Assuming that noise sources are uncorrelated, the spectral noise density of all components becomes the sum of equations (5.37) and (5.38).

5.3 Jitter Noise

The term clock jitter refers to the uncertainty of the time characteristics of the clock source. The cause of jitter is the intrinsic noise generated by components of the clock generating circuit such as crystals, transistors, resistors, etc. The effect of clock jitter on SC circuits is completely determined by computing the effects of sampling the input signal. Any deviation of the sampling period from its ideal value results in an error voltage in the sampled signal. This error is equal to the signal change between these two moments. The magnitude of this error is a function of the statistical properties of the jitter and the input signal to the system [5]. When a sinusoidal input is taken, the error introduced by jitter can be modeled by

$$x(t+\delta) - x(t) \approx 2\pi f_{in}\delta A cos(2\pi f_{in}t) = \delta\frac{d}{dt}x(t), \tag{5.39}$$

where A is the input signal amplitude, f_{in} is the input signal frequency and δ is the sampling uncertainty. Assuming that δ exhibits a Gaussian distribution with zero mean and standard deviation σ_δ, the resulting error has a white noise power spectral density from 0 to $f_s/2$. The jitter noise PSD can be approximated by

$$S_\delta(f) = \frac{A^2}{2}\frac{(2\pi f_{in}\sigma_\delta)^2}{f_s} \tag{5.40}$$

Since jitter is assumed to be white, the total in-band power in the ΣΔM can be expressed as

$$P_{\Delta t} \leq \frac{A^2}{2}\frac{(2\pi f_{in}\delta)^2}{OSR}, \tag{5.41}$$

where $\pm\Delta/2$ is the worst case amplitude. Equation 5.41 shows the inverse relationship of the total in-band power and the oversampling ratio. The jitter noise has a direct relationship with the input signal, which implies that at higher frequencies the jitter noise may become a significant component [20].

5.4 Capacitor Mismatching

In SC integrators the gain factors are implemented using capacitor ratios. Figure 5.5 illustrates the linear model of a second-order ΣΔM including the gains of the integrator. Although today's fabrication processes can produce matching with an error as low as 0.1%, still the gains differ from their nominal values affecting the performance of the integrator. Moreover, this capacitance mismatch alters the transfer function of the integrator, consequently affecting the signal and quantization noise. For instance, consider the ΣΔM shown in Figure 5.5. Assuming that the gain error in each integrator is given by

$$g_k = g_{k,ideal}\left(1-\varepsilon_{g_k}\right) \;\; k=1,2 \tag{5.42}$$

Then, the STF and NTF of the second-order modulator are given by

$$|SFT\left(z\right)| = \frac{\left(1-\varepsilon_{g_1}\right)}{\left(1-\varepsilon_{g_1'}\right)} \tag{5.43}$$

$$|NFT\left(z\right)| = \frac{\left(1-z^{-1}\right)^2}{\left(1-\varepsilon_{g_1'}\right)\left(1-\epsilon_{g_2}\right)}, \tag{5.44}$$

where it has been assumed that $g_1' = g_1$ and $g_2' = 2g_1g_2$ [37]. As expressed by equations (5.43) and (5.44), the effect of mismatch consists of an error in the modulator gain

and an increase in the quantization noise. Nevertheless, the zeros of the transfer function are not altered.

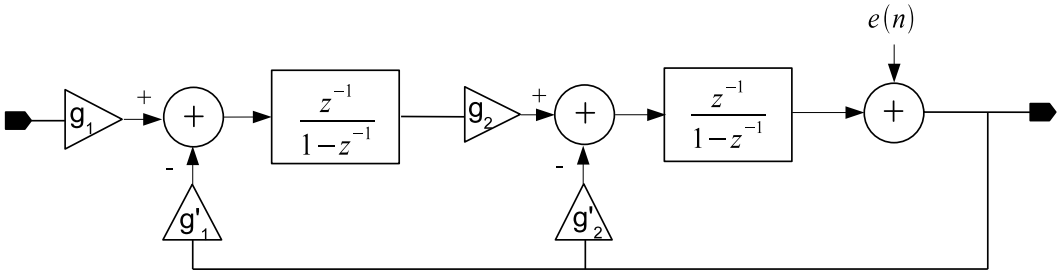


Figure 5.5. ΣΔM multibit linear model.

A second effect of the gain error is related to the system's stability, which could be affected by variations in the modulator's internal gains. Published results of simulations and experimental ΣΔM designs have demonstrated that small gains lead to a slow response to changing inputs. Furthermore, gains greater that 1.3 have been found to lead to system instability [41]. It has been reported that gain deviations as large as 1% do not produce a perceivable degradation in the performance of ΣΔMs [37], although. For most applications the degradation in SNR produced by a 10% of gain error is still considered tolerable [41].

5.5 Errors in Multi-bit ΣΔ Modulators

As it was explained in Section 4.4.4, multi-bit ΣΔM architectures provide some advantages over single-bit configurations. The most attractive advantage is the increase in the overall resolution of any ΣΔ ADC by increasing the number of levels in the internal quantizers without increasing the OSR. In general, the quantization noise is reduced by 6 dB with every bit increased in the quantizer resolution. Further-

more the use of multi-bit quantization improves stability in high-order modulators [37]. Figure 5.6 shows a multi-bit second order ΣΔM.

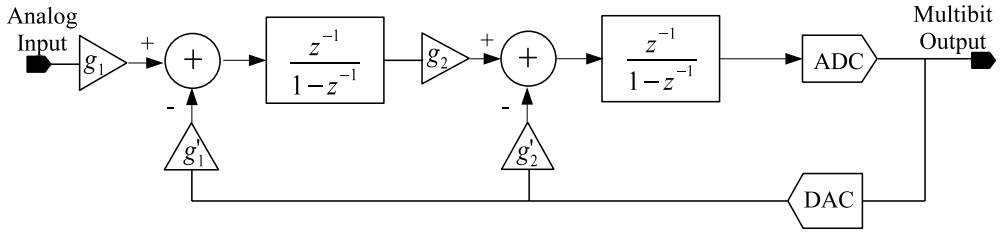


Figure 5.6. Second order multi-bit ΣΔM.

There are some drawbacks associated to the use of multi-bit quantizers in ΣΔMs. The main issue of multi-bit designs is the component mismatch in the DAC. References in a DAC are typically voltages or currents generated by matched components, such as resistors, transistors, and capacitors. Fabrication process variations, temperature gradients across the circuit, component aging, and component noise cause circuit component values to differ from their design values. These variations, or mismatch errors, cause inaccurate output levels such that the DACs output contains harmonic distortion. This mismatch affects the integral linearity of the DAC, making the system integral linearity no better than that of the internal DAC.

Figure 5.7 shows a linear model of a second-order multi-bit ΣΔM. Noise sources from the quantization noise, ADC threshold errors in the comparators and the DAC mismatch are represented by $e(n)$, $c(n)$ and $d(n)$, respectively. It can be observed that unlike $e(n)$ and $c(n)$, the error $d(n)$ lies inside the feedback path. Hence, it is not shaped by the NTF in the feedback of the modulator. Consequently, the linearity of the modulator is no better than the linearity of the N-bit internal DAC.

Several methods, such as the use of special VLSI layout techniques, element-trimming, digital correction, self-calibration, and dynamic element matching (DEM),

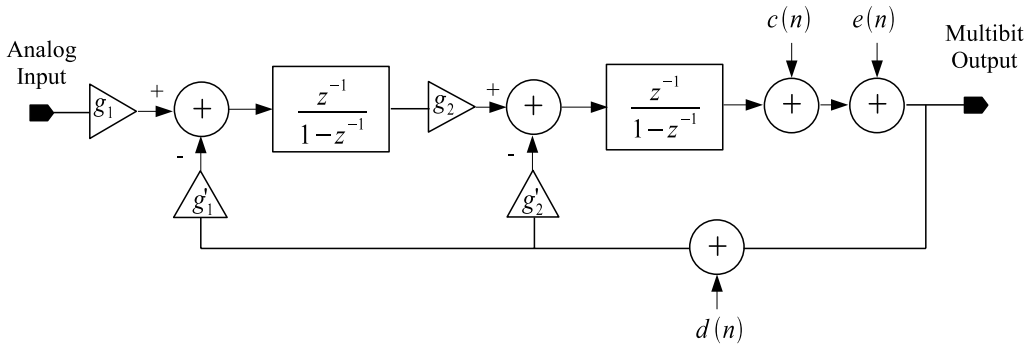


Figure 5.7. Multi-bit ΣΔM linear model with noise from elements mismatch.

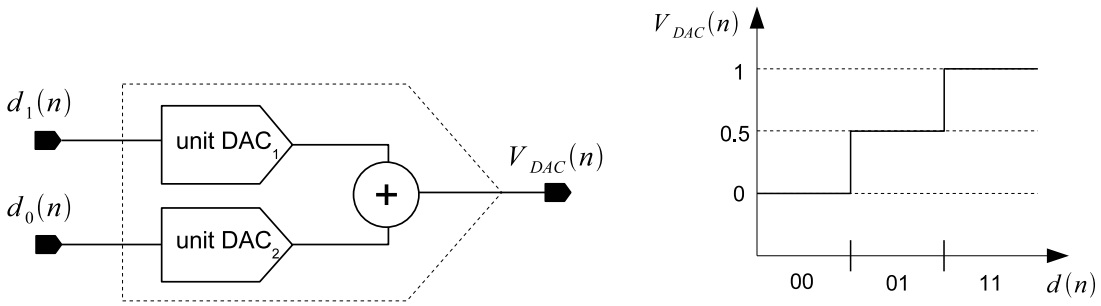
have been proposed to reduce the effects of component mismatch errors. DEM techniques are among the most commonly used. DEM is a process that reduces the effects of component mismatches in electronic circuits by dynamically rearranging the interconnections of mismatched components. By appropriately varying the virtual positions of mismatched components, the effects of mismatched components can be reduced, eliminated, or frequency shifted. In this work the individual level averaging (ILA) DEM technique proposed by Leung and Surtaja in [31] is considered.

5.6 Individual Level Averaging

The ILA DEM algorithm is essentially a clocked level averaging performed on a per-level basis [67]. ILA rotates or flips circuit elements in a periodic fashion, but a separate rotation state is maintained for each digital level. The advantage of the ILA is that distortion is moved into higher frequency bands while preserving the noise shaping characteristics of the ΣΔM modulator. To introduce the ILA algorithm consider the case of a DAC with two unit elements as illustrated in Figure 5.8(a). These units represent the passive components networks such as resistors and capacitors typically used in DAC implementations. The ideal DAC transfer curve is shown in Figure

5.8(b). As shown, the DAC will have three levels "0", "0.5" and "1". The input to the DAC is the output of the ΣΔM $d(n)$, where n is the sample number. If there is a mismatch between the two units such that their values are $1 + \varepsilon_1$ and $1 + \varepsilon_2$ for unit 1 and 2, respectively, then the DAC will have three levels corresponding to "0", "$(1 + \varepsilon_1)/(2 + \varepsilon_1 + \varepsilon_2)$" and "1". The DAC output waveform for the mismatch in units 1 and 2 are shown in Figures 5.9(a) and 5.9(b), in that order.

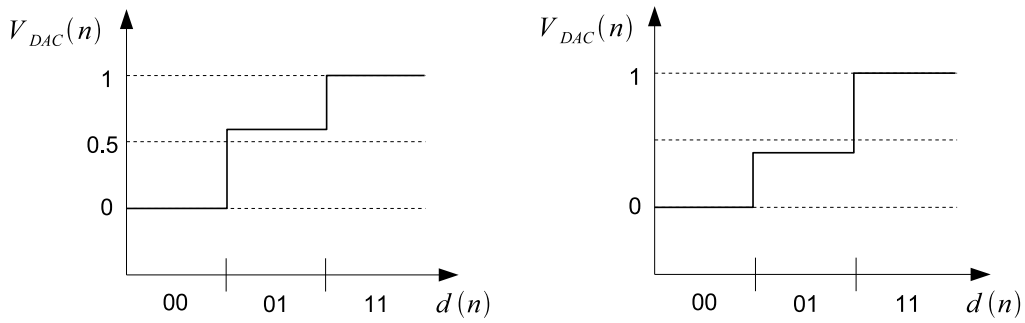
If for example, a dc input of "0.25" is applied to a first-order multi-bit ΣΔM with an ideal DAC, the output for the first four sample will consist of a periodic digital sequence $d(n)$: "00", "01", "00", "01". This sequence results in a periodic DAC output sequence $V_{DAC}(n)$: "0", "0.5", "0", "0.5" as shown in Figure 5.10(a). Furthermore, analyzing the first four cycles of the feedback signal $V_{DAC}(n)$ it turns out that it is not longer periodic. If the initial voltage of the ΣΔM is zero then the digital output is "00", "01", "00", "01" for the first four cycles. Therefore, the DAC output voltage will consist of "0", "$(1+\varepsilon_1)/(2+\varepsilon_1+\varepsilon_2)$", "0", "$(1+\varepsilon_1)/(2+\varepsilon_1+\varepsilon_2)$" as shown in Figure 5.10(b). Although, the feedback signal $V_{DAC}(n)$ is interpolating between the input signal of "0.25" the average value differs from this value and an error is made. This conversion error is fed back to the input of the ΣΔM and stored



(a) DAC with unitary elements

(b) Ideal DAC transfer curve

Figure 5.8. Unitary DAC model and transfer curve.



(a) Error ε_1 (b) Error ε_2

Figure 5.9. Transfer curve for DAC with mismatched units.

in the integrator. When a positive conversion error is made, it will be stored in the integrator and when its absolute value is larger than 1 LSB of the internal ADC, an extra "01" will be generated. In the same manner when a negative conversion error is made and its absolute value is larger than 1 LSB of the internal ADC, an extra "00" will be generated. Since the average value of the feedback signal $V_{DAC}(n)$ is forced to follow the input voltage because of the negative feedback scheme and the value "$(1+\varepsilon_1)/(2+\varepsilon_1+\varepsilon_2)$" is less than "0.5" then it is going to appear more than supposed to compensate the error. This leads to a no longer periodic output digital sequence $d(n)$ containing some extra "01" or "00" depending on the sign of the error.

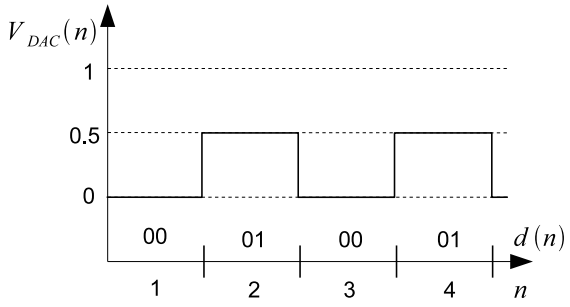
The problem of the error in the feedback signal $V_{DAC}(n)$ and consequently in the $\Sigma\Delta$M output $d(n)$ is solved by the use of ILA. Again, for the ideal case assuming that for an input signal of "0.25", the output $d(n)$ for the first four cycles is: "00", "01", "00", "01". At $n = 1$, $d(1) =$"00" and the transfer curve of Figure 5.9(a) is selected. The fact that the curve for ε_1 was selected for the code "00" is remembered. At $n = 2$, $d(2) =$"01" and the curve ε_1 is selected making $V_{DAC}(2) =$"$(1+\varepsilon_1)/(2+\varepsilon_1+\varepsilon_2)$". Again, the use of curve ε_1 for "01" is remembered. Now at $n = 3$, $d(3) =$"00" the fact that for $n = 1$ the curve ε_1 was used now the curve ε_2 is selected. Finally, at

$n = 4$, $d(4)$ ="01". Since for $n = 2$ curve ε_1 was used, this time ε_2 is selected making $V_{DAC}(4)$ ="$(1+\varepsilon_2)/(2+\varepsilon_1+\varepsilon_2)$". The DAC waveform for the conversion using ILA is shown in Figure 5.10(c). Accordingly, the average value of $V_{DAC}(n)$ is "0.25" as given by

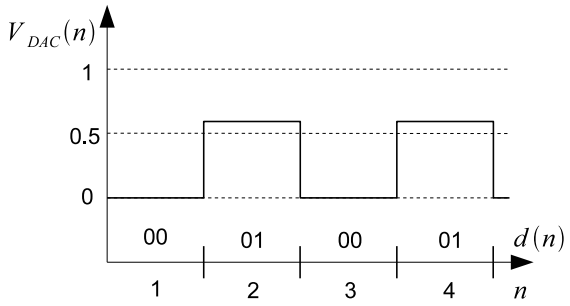
$$\bar{V}_{DAC} = \frac{1}{4}\sum_{n=1}^{4} V_{DAC}\,(n) = \frac{1}{4}\left(0 + \frac{1+\varepsilon_1}{2+\varepsilon_1+\varepsilon_2} + 0 + \frac{1+\varepsilon_2}{2+\varepsilon_1+\varepsilon_2}\right) = 0.25 \qquad (5.45)$$

It can be seen that the ILA algorithm applied to the DAC does not interfere with the averaging activity given by the negative feedback of the ΣΔM. This ensures that the cancellation of the DAC error can be achieved independently of the modulated signal.

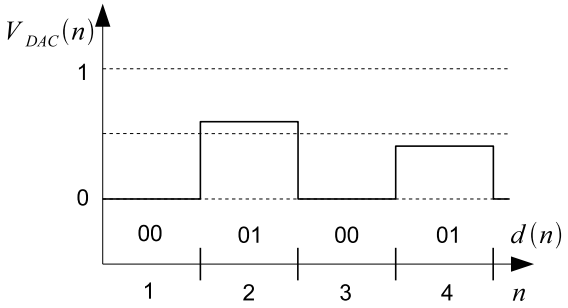
The ILA can be implemented in two ways: rotation and addition. In the rotation implementation a register R_K of $log_2(M)$ bits is required for each of the M possible digital input codes. The elements to be used at time i are selected by the indexes $R_K(i)$ through $R_K(i) + K - 1$. If an index is greater than M, then a wrap around is used and the first elements are chosen. Then, $R_K(i+1)$ is updated to $R_K(i) + 1$ for the use of the next time code K is required. To rotate through all the possible combinations of the DAC, M cycles are needed. Since K elements are used per cycle, each element is picked K times. For perfect cancellation a total of M cycles are needed. Moreover, in the addition method the indexes of the elements to be used at time i, are the same as for the rotational style: $R_K(i)$ through $R_K(i) + K - 1$ and if $R_K(i) + K - 1 > M$, then wrap around would occur. This algorithm uses a different update method: $R_K(i+1)$ to $R_K(i) + K$ is used for the next time code K is needed. If M is an integer multiple of K, then each element is picked once in M/K cycles. The cancellation cycle is reduced to M/K cycles. If M is not a integer multiple of K, the worst case cancellation cycle is M.



(a) DAC ideal output waveform



(b) DAC output waveform without ILA



(c) DAC output waveform with ILA

Figure 5.10. DAC transfer curve ideal, with and without ILA.

CHAPTER 6

Behavioral Models for the Simulation of $\Sigma\Delta$ Modulators

The fundamental blocks for the behavioral simulation of SC $\Sigma\Delta$Ms are SC integrators, ADCs, DACs and noise sources such as sampling jitter, and thermal noise. Additional blocks representing digital circuits such as DEM algorithms and decoders are also necessary and useful to increase the level of abstraction. Since the nonideal analog behavior of the blocks is the dominating limiting factor in the performance of a $\Sigma\Delta$M, the digital part is assumed to be mostly ideal. The following sections present the behavioral models for the SC integrator, sampling jitter, thermal noise, ADC, DAC, and ILA algorithm.

6.1 SC Integrator

The behavioral model for the SC integrator is based on equations (5.21) to (5.36). Using a system clock, an output sample is calculated for each clock phase, namely sampling and integration. This approach provides the advantage that computations are only made at the points of interest, thus reducing the simulation time. Figure 6.1

shows the general SC integrator behavioral model flowchart.

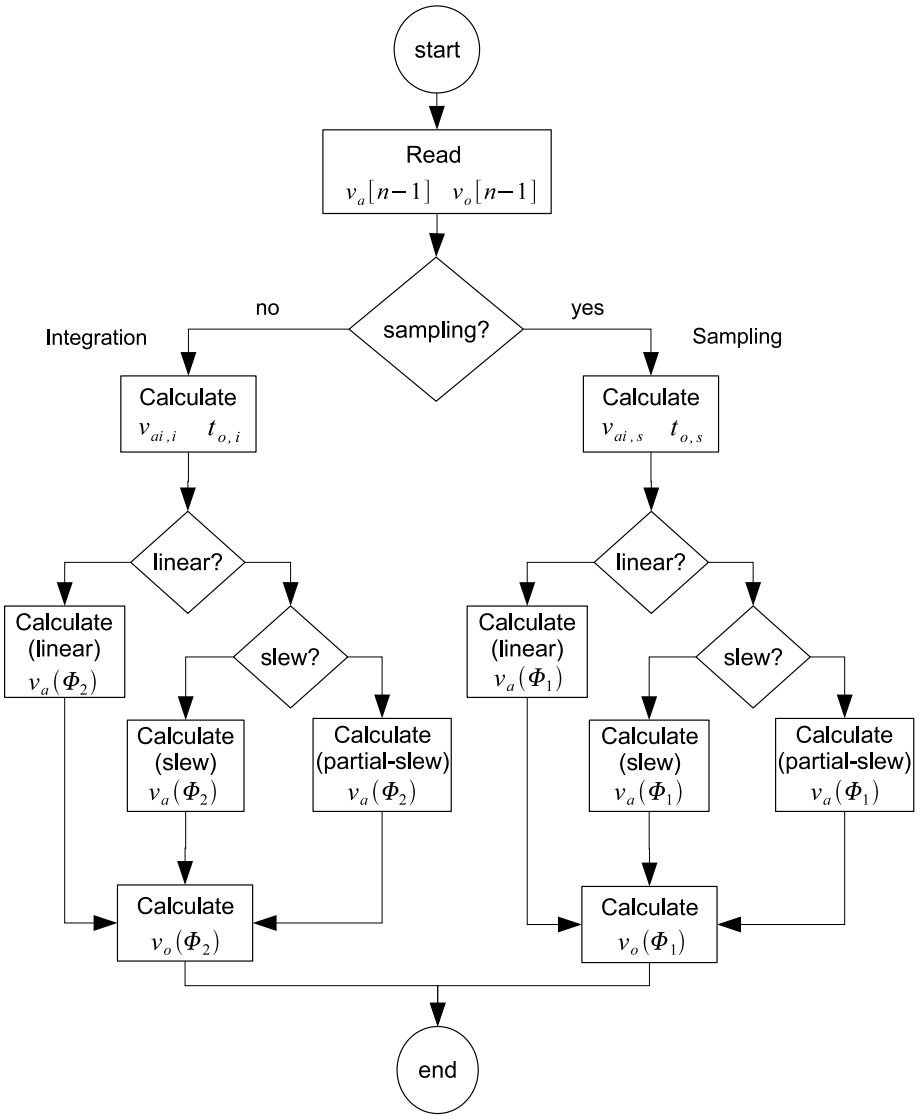


Figure 6.1. Flowchart for the SC integrator behavioral model.

6.2 Thermal Noise

Assuming that noise sources are uncorrelated, the spectral noise density for the total noise is the sum of Equations (5.37) and (5.38). The model for thermal noise pre-calculates a noise term for each system clock phase. This noise term is added

to the input of the ΣΔM using a uniformly distributed random number generator. Thus, the added voltage at the input sampling capacitor that represents the thermal noise of the modulator is

$$v_{Th} = rand\left(\sqrt{12 f_s (S_{eq,samp} + S_{eq,int})}\right) \tag{6.1}$$

where $rand(v)$ represents a uniformly distributed random number in the interval $[-v/2, v/2]$, [37].

6.3 Jitter Noise

Jitter noise can be modeled using two approaches. The first approach pre-contaminates the input signal with white jitter noise as stated by the right end of equation (5.39). The expression for this approach is

$$v_{in}(nT_s) = A\sin(2\pi f nT_s) + \delta\frac{d}{dt}A\sin(2\pi f nT_s), \tag{6.2}$$

where δ is a Gaussian (normal) distribution. Moreover, the second approach consists of sampling the input signal in a non-uniform way. This is done by adding a deviation δ in the sampling period at the input expressed as

$$v_{in}(nT_s) = A\sin\left(2\pi f(nT_s + \delta)\right), \tag{6.3}$$

where $T_s + \delta$ is the non-uniform sampling period. Both approaches satisfy equation (5.41) [37]. From the above discussion, modeling the jitter noise requires the generation of normal distributed random numbers. The Box-Muller method is used to generate such numbers using a uniformly distributed random number generator [40].

6.4 A/D Converter

The nonidealities in the ADC are less important than those of the feedback DAC due the location in the modulator. Since the ADC lies in the noise-shaped loop, the nonidealities of the quantizer are suppressed by the gain of the preceding integrators. Therefore, in many cases for simulation purposes their nonidealities such as gain and offset errors can be neglected [25]. Multi-bit quantizers are often implemented using flash topologies. To explain the behavioral implementation for the ADC consider a 5-level 3-bit flash ADC as shown in Figure 6.2. It is formed by a bank of comparators and an encoder. The output from the comparators is known as thermometer code, and is encoded to the final binary code.

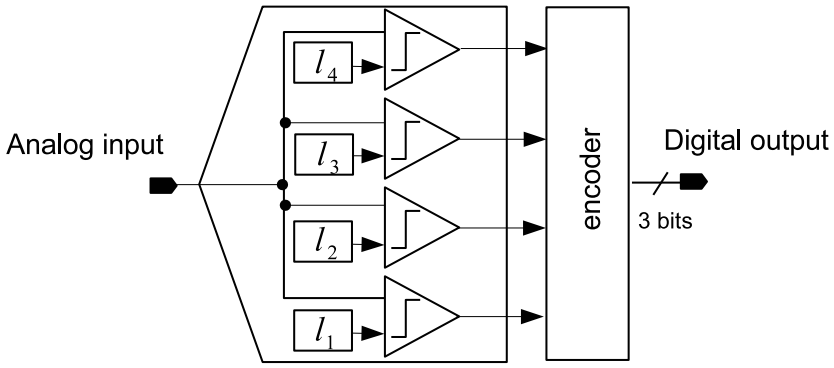


Figure 6.2. 5-level A/D Converter model.

In order to quantize the signal, the input signal is compared with multiple levels l_k, set within the input range. Assuming a reference voltage of 1, arbitrary levels for the flash ADC shown in Figure 6.2 are: -0.75, -0.25, 0.25 and 0.75, for l_1, l_2, l_3 and l_4 in that order. Usually, these levels are implemented using passive elements such as resistors and capacitors and exhibit some mismatch due fabrication processes. Mismatch in the components produce gain and offset errors. These can be modeled by adding a gain and offset error to the input signal.

6.5 D/A Converter

The most frequently used structure for the implementation of a DAC with increased linearity is based on the used of unit elements [41]. These elements may be current sources, resistors, capacitors, etc. In a similar way, the behavioral implementation of the DAC is based on unitary D/A converters. To explain the behavioral implementation consider a 5-level D/A converter using 4 unit elements as shown in Figure 6.3. For simplicity it is assumed that the converter reference voltage is 1. Moreover, the unit elements exhibit the following values: $(\pm 1+\varepsilon_1)/4$, $(\pm 1+\varepsilon_2)/4$, $(\pm 1+\varepsilon_3)/4$, and $(\pm 1+\varepsilon_4)/4$, where ε_k represent the mismatch error in the k-th unit element.

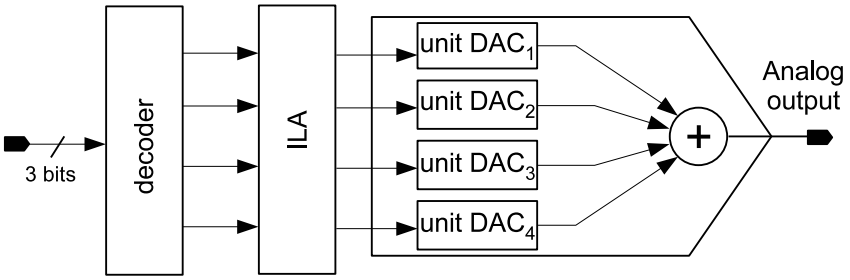


Figure 6.3. Modeling blocks for ILA and 5-level D/A Converter.

The fact that $\varepsilon_k \neq 0$, makes the elements no longer unitary introducing errors in the D/A converter transfer curve. If a one-to-one mapping between the digital input and the used D/A converter units exists, then the output voltage for each digital code is given in Table 6.1.

Table 6.1. D/A converter input/output map including mismatched units.

Digital input	Thermometer code	Ideal output	Output with mismatch
"000"	"0000"	-1	$-1+\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4$
"001"	"0001"	-0.5	$-0.5+\varepsilon_1$
"010"	"0011"	0	$0+\varepsilon_1+\varepsilon_2$
"011"	"0111"	0.5	$0.5+\varepsilon_1+\varepsilon_2+\varepsilon_3$
"100"	"1111"	1	$1+\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4$

It can be seen how the mismatch in the converter unit elements affects the output voltage. Moreover, this mismatch cause deterministic conversion errors that cause harmonic distortion and reduce the D/A converter performance [67].

6.6 Individual Level Averaging

The main idea of the ILA algorithm is to guarantee that every element is used with equal probability for each digital input code [11]. It decides which elements are used for a specific digital code each time it occurs. By doing this, it equalizes the number of times each element has been used to generate that specific digital code. The ILA behavioral model is based on the rotational algorithm since it provides a simpler concept than that of the addition algorithm. A rotational approach allows an implementation based on the *modulo* operator, which provides a method to ensure that for each digital code the units are used uniformly. To explain the behavioral implementation of the ILA consider the same D/A converter shown in Figure 6.3, where the elements have the following values: $\pm 1+\varepsilon_1/4$, $\pm 1+\varepsilon_2/4$, $\pm 1+\varepsilon_3/4$, and $\pm 1+\varepsilon_4/4$.

For this D/A converter the ILA model contains 3 variables, 1 for each digital code except the upper and lower codes, used as counters to keep track of the units rotations. Table 6.2 shows the possible rotations of the DAC units for each code. As shown in Table 6.1, the upper and lower limits of the DAC are fixed so no rotation is necessary. Moreover, the DAC mid values between limits and the center value, are ± 0.5. For -0.5 only one unit is required, but four rotations are needed in order to use all the units uniformly. Three units are necessary to produce the +0.5 output voltage. In a similar manner, four rotations are needed to equalize the number of times that each code was used. Since four rotations are needed for ± 0.5 a modulus

4 counter is implemented. For the center voltage at 0, two units are needed. In this case a modulus 2 counter is used since 2 rotations are sufficient for its representation.

Table 6.2. D/A converter input/output map with ILA rotations.

Digital input	Thermometer code	Ideal output	Output with mismatch
"000"	"0000"	-1	$-1+\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4$
"001"	"0001"	-0.5	$-0.5+\varepsilon_1$
	"0010"		$-0.5+\varepsilon_2$
	"0100"		$-0.5+\varepsilon_3$
	"1000"		$-0.5+\varepsilon_4$
"010"	"0011"	0	$0+\varepsilon_1+\varepsilon_2$
	"1100"		$0+\varepsilon_3+\varepsilon_4$
"011"	"0111"	0.5	$0.5+\varepsilon_1+\varepsilon_2+\varepsilon_3$
	"1110"		$0.5+\varepsilon_2+\varepsilon_3+\varepsilon_4$
	"1101"		$0.5+\varepsilon_1+\varepsilon_3+\varepsilon_4$
	"1011"		$0.5+\varepsilon_1+\varepsilon_2+\varepsilon_4$
"100"	"1111"	1	$1+\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4$

CHAPTER 7

Results

A second-order, multi-bit ΣΔM model with ILA has been built using VHDL-AMS as the modeling language. The model includes nonidealities such as sampling jitter, thermal noise, capacitance mismatch, and integrator dynamics. To asses the model correctness and validate its results several simulations were carried. The results are presented in the next sections.

7.1 Validation

As part of the validation process, simulations were carried for the GSM and WCDMA bandwidths at 200kHz and 2.0MHz, respectively. Results for simulations at GSM bandwidths were compared against SPICE simulations. Moreover, simulation results for both GSM and WCDMA are compared against experimental data. For simplicity, Table 7.1 shows the description of the integrators parameters. The nominal values for the parameters are contained in Table 7.2.

Table 7.1. Description of Integrator Parameters.

Parameter	**Description**
Cin	Input signal sampling capacitor
Cr	Reference signal sampling capacitor
$Cinp$	OTA parasitic input capacitance
$Cint$	Integrating capacitor
$Cintp$	C_{int} bottom plate capacitance
$Cinxt$	Next stage input capacitance
Co	OTA output capacitance
go	OTA output conductance
gm	OTA transconductance
Io	OTA maximum output current
Ron	Switch resistance
fs	Sampling frequency

Table 7.2. Nominal Values for Integrator Parameters.

Parameter	**First Integrator**	**Second Integrator**
C_i	0.4pF	0.3pF
C_r	0.4pF	0.3pF
C_{inp}	0.5pF	0.7pF
C_{int}	0.8pF	0.3pF
C_{intp}	0.08pF	0.03pF
C_{inxt}	0.3pF	0.8pF
C_o	0.7p	0.35pF
g_o	1e-8Ω^{-1}	1e-8Ω^{-1}
g_m	1.9mA/V	1.9mA/V
I_o	64μA	64μA
R_{on}	200Ω	200Ω
fs	19.2MHz	19.2MHz

7.1.1 Validation with SPICE

Simulations were carried for the GSM mode at target bandwidths of 135kHz, 270kHz and 615kHz and compared with SPICE simulations. An input signal of 33kHz and amplitude of -6dB was used where 0dB corresponds to the ADC reference voltage. Variations in transconductance and temperature were introduced. A change in transconductance has a significant impact on the integrator dynamics which can lead to an increase in the harmonic distortion, thus degrading the SNDR. Moreover, a change in temperature affects the noise floor on the PSD as discussed in Section 5.2 and consequently affects the SNDR. The values for the parameters of the integrators are those in Table 7.2 except for the changes in temperature and transconductance specified for each case.

Tables 7.3 and 7.4 show the SNDR results for a temperature of 27^oC and transconductance of 1.16mA/V and 1.75mA/V, respectively. Moreover, Tables 7.3 and 7.4 summarize the SNDR results for a transconductance of 1.9mA/V and temperatures of -30^oC and 27^oC, respectively. Effectively, the VHDL-AMS model provides results with less than 7% of error when compared with SPICE simulations. These results improve over previous models [20] showing an error reduction of about 36% when compared to SPICE simulations.

Table 7.3. VHDL-AMS Model vs SPICE for g_m=1.16 mA/V and T=27^oC.

Bandwidth	SPICE SNDR	VHDL-AMS Model SNDR	Error
135kHz	86.56dB	85.43dB	1.31%
270kHz	74.65dB	70.35dB	5.76%
615kHz	54.99dB	51.42dB	6.50%

Table 7.4. VHDL-AMS Model vs SPICE for g_m=1.75 mA/V and T=27^{o}C.

Bandwidth	SPICE SNDR	VHDL-AMS Model SNDR	Error
135kHz	86.10dB	84.63dB	1.71%
270kHz	72.45dB	70.30dB	2.96%
615kHz	53.62dB	51.34dB	4.25%

Table 7.5. VHDL-AMS Model vs SPICE for g_m=1.9 mA/V and T=-30^oC.

Bandwidth	SPICE SNDR	VHDL-AMS Model SNDR	Error
135kHz	89.90dB	84.07dB	6.48%
270kHz	71.08dB	71.04dB	0.06%
615kHz	53.53dB	51.93dB	2.99%

7.1.2 Validation with Experimental Data

This section presents the results for the ΣΔM model operating at GSM and WCMDA bandwidths, and compared with experimental data reported by Gomez and Haroun [26]. For the GSM mode at a target bandwidth of 200kHz, an input signal of 33kHz and -6dB amplitude was used. Figure 7.1 shows the PSD obtained for the VHDL-AMS model simulation. An SNDR of 76.57dB was obtained turning out into a 2.78% of error when compared to the experimental data SNDR of 74.5dB. In addition, the third harmonic around 100kHz evidences the presence of the amplifier nonidealities.

Simulations for the WCDMA bandwidth of 2.0Mhz were carried with an input signal of 300kHz and -1dB amplitude. The PSD obtained for the VHDL-AMS model is shown in Figure 7.2. Similar to the plot for the GSM mode, the third harmonic can

Table 7.6. VHDL-AMS Model vs SPICE for g_m=1.9 mA/V and T=27^{o}C.

Bandwidth	SPICE SNDR	VHDL-AMS Model SNDR	Error
135kHz	87.57dB	84.98dB	2.95%
270kHz	72.73dB	70.54dB	3.01%
615kHz	53.37dB	51.89dB	2.78%

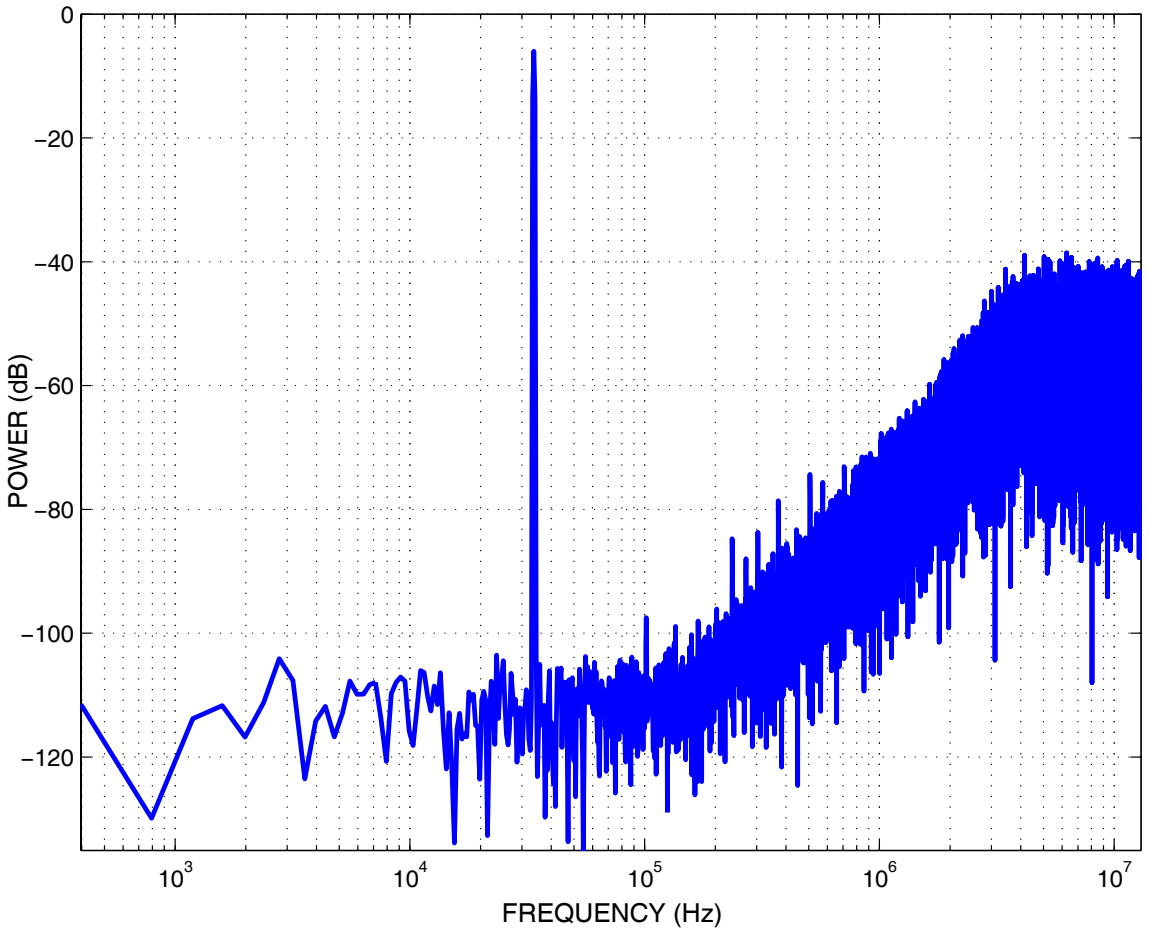


Figure 7.1. Power spectrum density for VHDL-AMS model validation in GSM mode at a target bandwidth of 200kHz.

be distinguished in the plot around 300kHz. A peak SNDR of 47.82dB was obtained resulting in 2.41% of error when compared to the experimental data peak SNDR of 49dB. Table 7.7 summarizes the results for the validations with experimental data for the VHDL-AMS model. It provides an error of less than 3% when compared to experimental data.

Table 7.7. VHDL-AMS Model vs Experimental data.

Bandwidth	Experimental Data SNDR	VHDL-AMS Model SNDR	Error
200kHz	74.5dB	76.57dB	2.78%
2.0MHz	49.0dB	47.82dB	2.41%

7.2 Noise Sources Characterization

7.2.1 Jitter Noise

Section 6.3 described two behavioral models for the jitter noise were presented, namely, the derivative approximation, and sampling deviation models. Simulations to compare both models were carried using an input signal of 62kHz and -8dB amplitude, and jitter with a standard deviation of 5ns. In addition, the D/A converter mismatch is omitted and the parameters of the integrators are those of Table 7.2 except for the sampling frequency that now is 26MHz.

Figures 7.3(a) and 7.3(b) show the power spectral density (PSD) for the sampled signal with jitter, and the second-order multi-bit $\Sigma\Delta$M using the derivative approximation model (dot) and the sampling deviation model (solid), respectively. It can be observed that for both Figures the PSD is very similar. Moreover, the SNDR for the jitter models using the derivative approximation and deviation in sampling process were 70.7128dB and 70.4322dB, respectively.

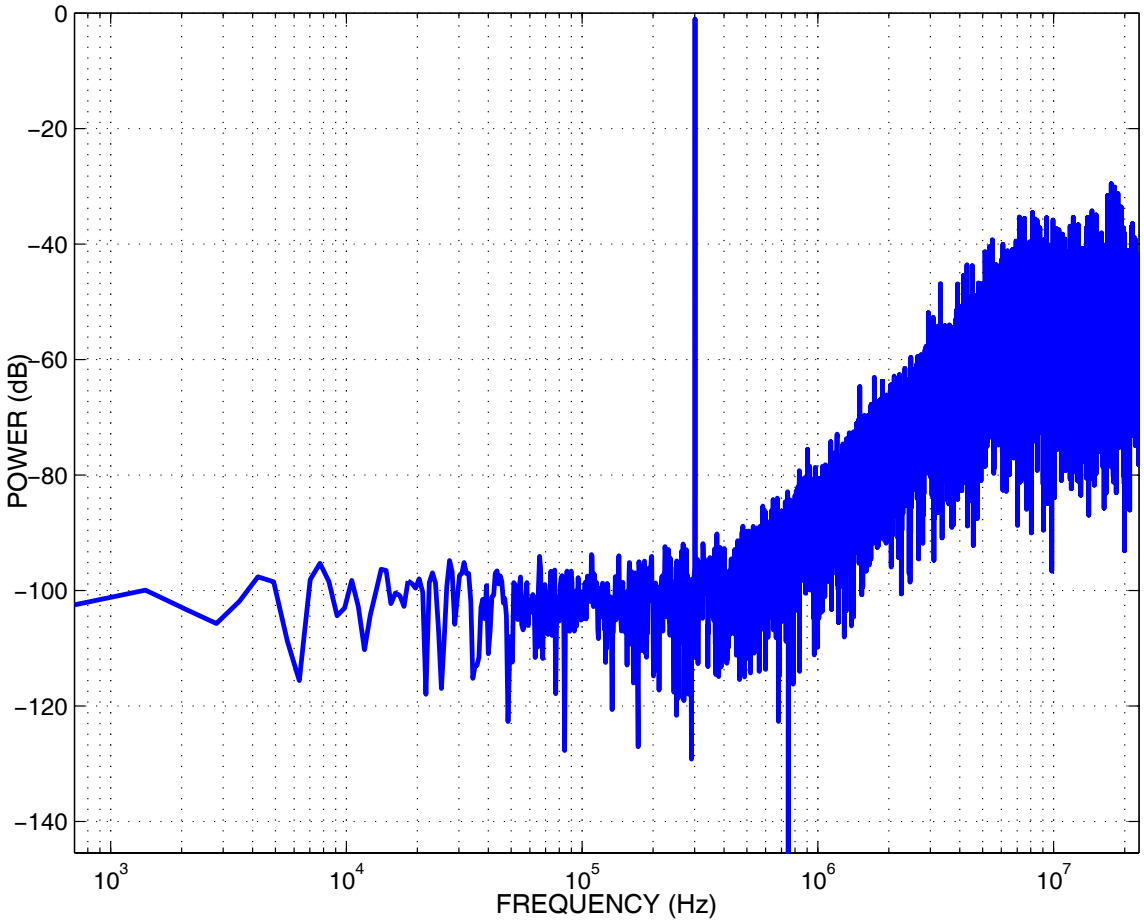
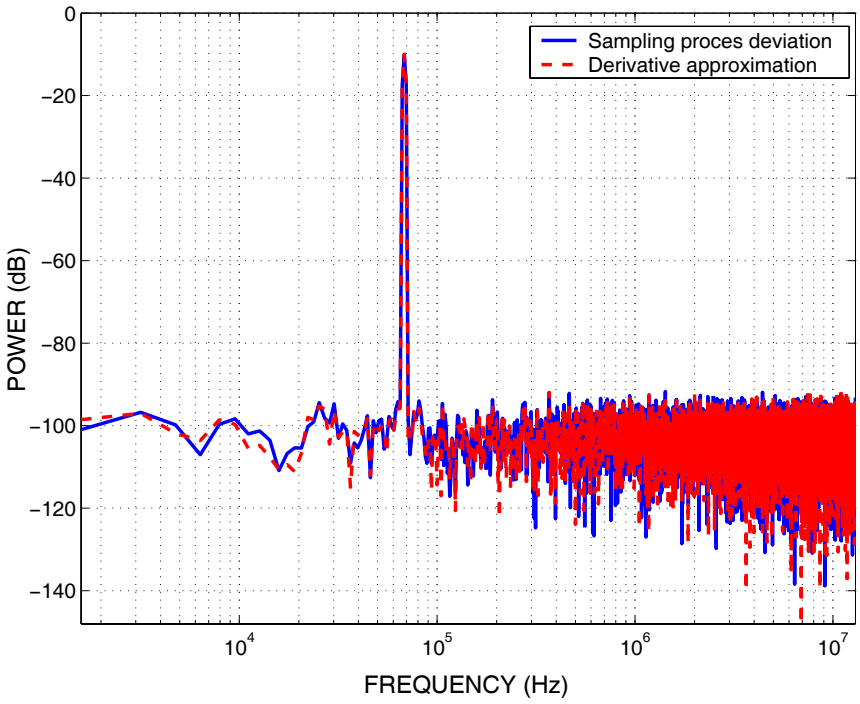
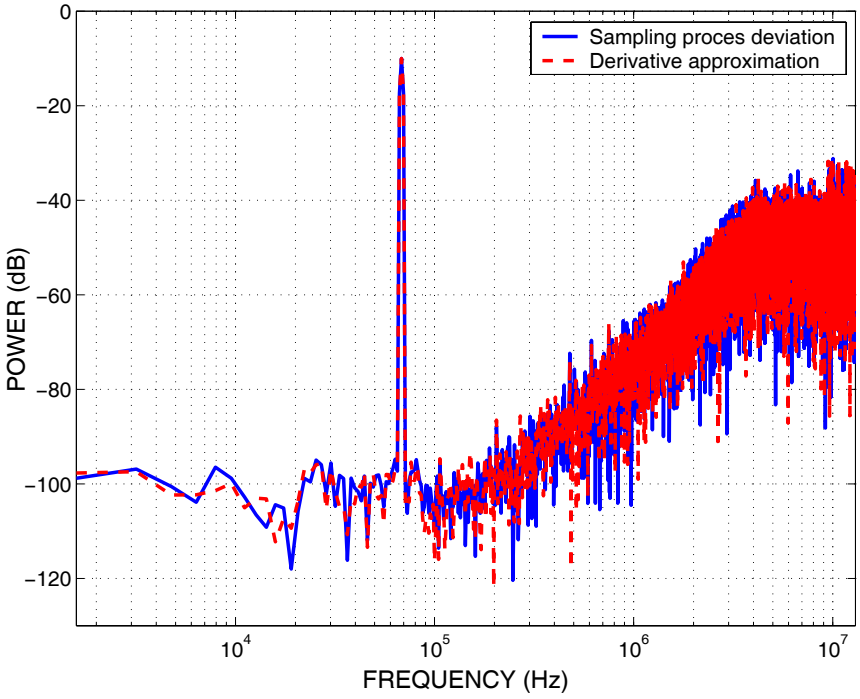


Figure 7.2. Power spectrum density for VHDL-AMS model validation in WCDMA mode at a target bandwidth of 2.0MHz.



(a) PSD for sampled signal using jitter behavioral models



(b) PSD of a second order ΣΔM using jitter behavioral models

Figure 7.3. Power spectral density of (a) sampled signal and (b) second-order multi-bit ΣΔM using the jitter models of the derivative approximation (dash), and sampling process deviation (solid).

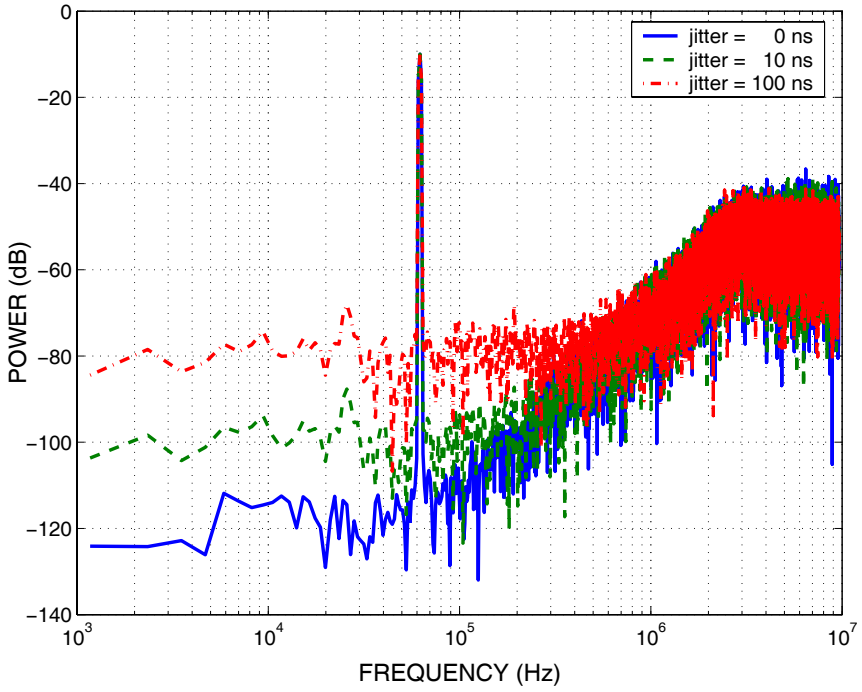
The effect of clock jitter on ΣΔ Modulators is completely determined by computing its effect at the input signal as mentioned in Section 5.3. It is implicit in equation (5.40) that the jitter noise power increases with the standard deviation of the sampling jitter and the frequency of the input signal. To asses the correctness of the jitter model, simulations were carried for a second-order multi-bit ΣΔ Modulator model.

To illustrate the jitter noise dependence on its standard deviation, Figure 7.4(a) shows the power spectral density (PSD) of a second-order modulator with an input signal of 62kHz, with jitter standard deviations of 0ns (solid), 10ns (dot), and 100ns (dash-dot). It is noticeable how the floor noise increases from approximately -125dB to -80dB as the jitter standard deviation increases.

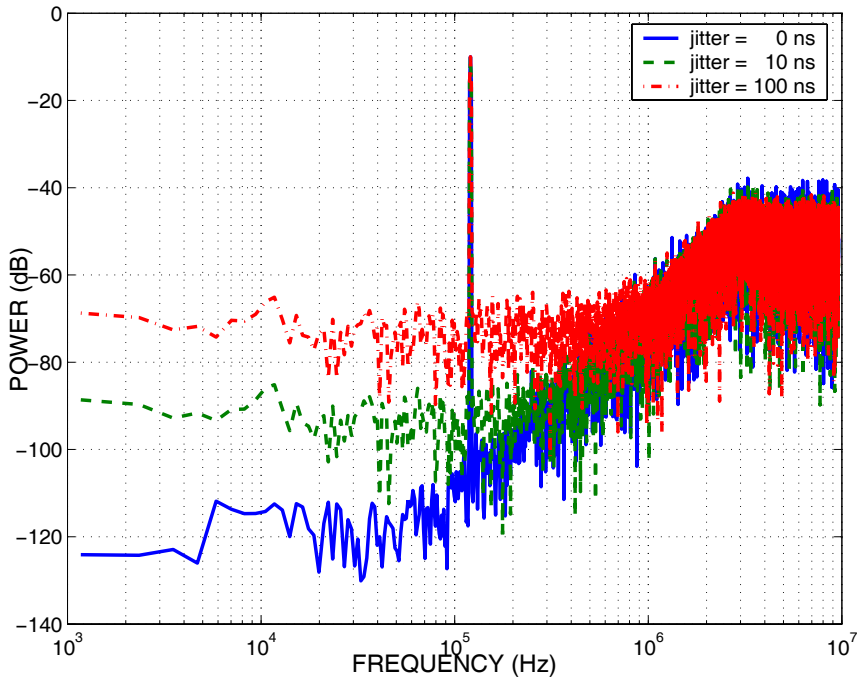
The second factor affecting jitter noise is the input signal frequency. Figure 7.4(b) shows the PSD for the same second-order ΣΔ Modulator with an input signal of 120kHz, and standard deviations of 0ns (solid), 10ns (dot), and 100ns (dash-dot). It is clear that an increase in the input signal from 62kHz in Figure 7.4(a) to 120kHz in Figure 7.4(b) corresponds to an increase in the floor noise from -80dB to -70dB for the signal with a jitter standard deviation of 100ns (dash-dot), and -100dB to -90dB for the signal with 10ns (dot) standard deviation. The presented results point to the similarity and practicality of the jitter behavioral models.

7.2.2 Thermal Noise

Thermal noise in SC circuits affects the floor noise of the PSD. As expressed in equations 5.37 and 5.38, the noise power is proportional to the temperature. Simulations were carried for a second-order multi-bit ΣΔM with temperatures of -30^oC, 27^oC and 100^oC. All other parameters remain the same as in Table 7.2. Figure 7.5(a) shows the PSD for temperatures of -30^oC (solid), 27^oC (dot) and 100^oC (dash-dot).



(a) PSD of a second-order ΣΔM with jitter and input of 62kHz



(b) PSD of a second-order ΣΔM with jitter and input of 120kHz

Figure 7.4. Power spectral density of a second-order multi-bit ΣΔM with jitter standard deviations of: 0ns (solid), 10ns (dash) and 100ns (dash-dot) for input signal of -10dB and (a) 62kHz and (b) 120kHz.

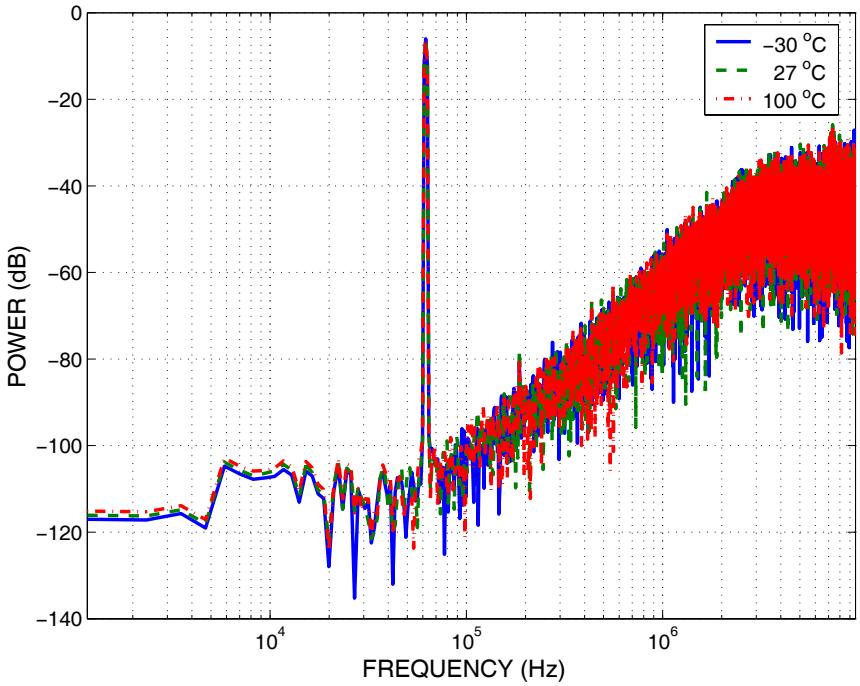
Moreover, Figure 7.5(b) illustrates a zoomed section of the PSD floor noise. It is noticeable how the floor noise increases with an increase in temperature. The increase in the noise floor is small due the chosen temperatures which relate to possible real scenarios and span over a small range.

In addition to the temperature variation, simulations were carried with changes in capacitance values. Thermal noise is often called kT/C noise since there is a proportional relation with temperature (T) and an inversely proportional relation with the total associated capacitance (C). Equations 5.37 and 5.38 express this kind of relation with the total input capacitance. Figures 7.6(a) shows the PSD for a second order $\Sigma\Delta$M at 27^{o}C with capacitors at nominal size, twice the nominal size and four times the nominal size. A zoomed section of the PSD floor noise is illustrated in 7.6(b). It can be seen how the floor noise is reduced with an increase in the size of the capacitors from -116dB to -122dB for the capacitors at nominal size (solid) and four times the nominal size, respectively.

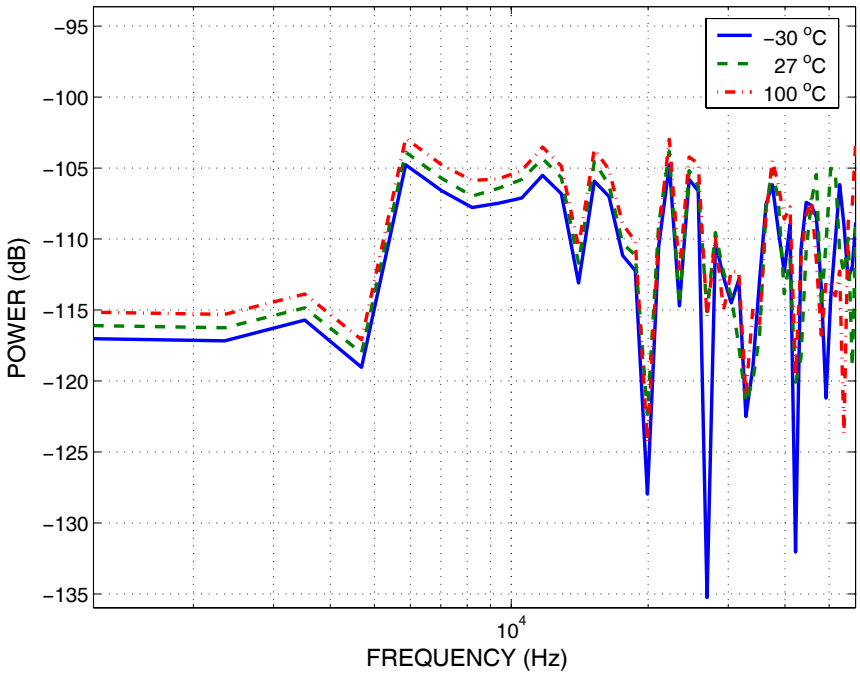
7.3 Capacitance Mismatch

As explained in Section 5.4 gains in SC integrators are implemented using capacitance ratios. Consequently, capacitance mismatch alters the integrator noise transfer function (NTF). To measure the effect of capacitance mismatch on the NTF simulations were carried on a second-order multi-bit $\Sigma\Delta$M using the parameters of Table 7.2 and an input signal with frequency of 100kHz and amplitude of -8dB. For these experimental runs thermal noise and sampling jitter were not considered.

Figure 7.7 shows the PSD for the second-order modulator with the gains of 0.3, 0.5 and 0.7 for the first integrator. The nominal gain for the first integrator was 0.5. Although the small gain variations had a negligible effect on the SNDR, it can be

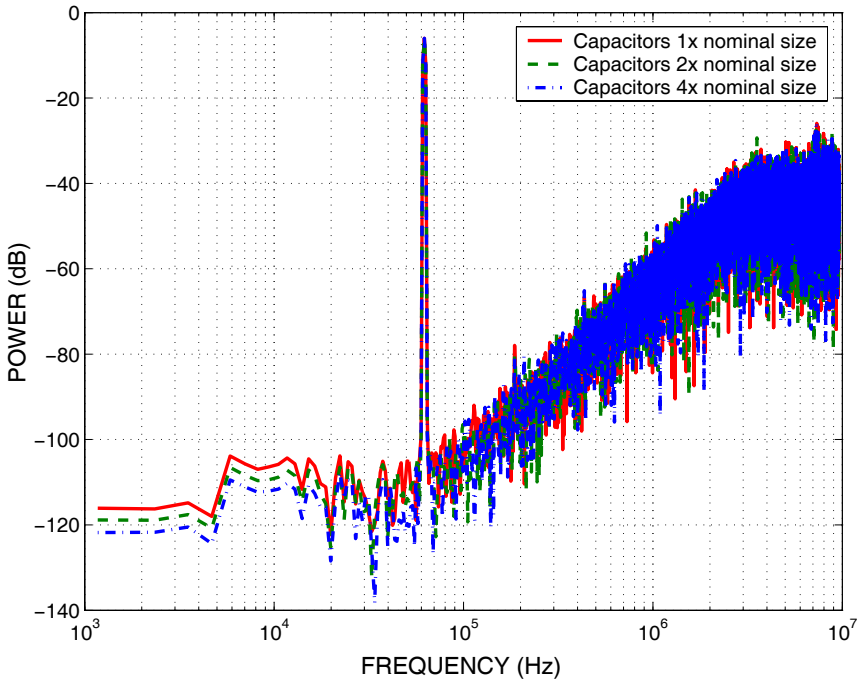


(a) PSD of a second-order ΣΔM at temperatures of -30^oC, 27^oC and 100^oC

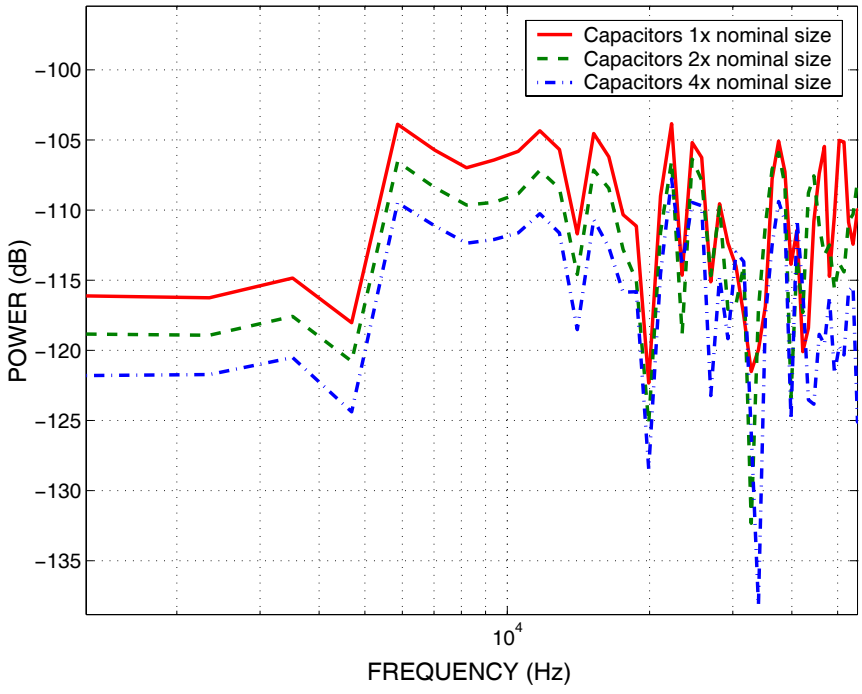


(b) PSD floor noise of a second-order ΣΔM at temperatures of -30^oC, 27^oC and 100^oC

Figure 7.5. Power spectral density of a second-order multi-bit ΣΔM with at temperatures: -30^oC (solid), 27^oC (dash) and 100^oC (dash-dot) for input signal of 62kHz and -9dB (a) PSD and (b) floor noise.



(a) PSD of a second-order with capacitors at different sizes



(b) PSD floor noise of a second-order with capacitors at different sizes

Figure 7.6. Power spectral density of a second-order multi-bit $\Sigma\Delta$ Modulator at temperature of 27^{o}C and with capacitors: at nominal size (solid), twice the nominal size (dash) and four times the nominal size (dash-dot) for input signal of 62kHz and -9dB (a) PSD and (b) floor noise.

seen how the harmonic content was slightly changed with the gain alteration. In a similar way, Figure 7.8 illustrates the PSD when the gain for the second integrator was 0.9, 1.0 and 1.1, in that order, showing the change in the harmonic content. For the second integrator a nominal gain of 1.0 was considered.

7.4 Mismatch in D/A Converter

In Section 5.5, the effect of DAC mismatch was introduced. Mismatch in the local DAC of a multi-bit ΣΔM, led to erroneous output levels such that harmonic distortion was introduced to the system. The ILA is one of the DEM techniques to reduce the effect of such errors. Simulations were run for a second-order multi-bit ΣΔM including DAC mismatches of 0.0% (solid), 0.1% (dot) and 1.0% (dash-dot) when the ILA was inactive and active. In addition an input signal of 15kHz and -8dB is used.

Figures 7.9(a) and 7.9(b) show the PSD for the second-order ΣΔM when the DAC error is 0.0%, 0.1% and 1.0% when the ILA is inactive and active, respectively. The figure shows how the DAC mismatch introduces harmonic distortion degrading the SNDR from 71.4dB to 38.0dB for a mismatch of 0.0% (solid) and 1.0% (dash-dot), respectively. Moreover, it is noticeable in Figure 7.9(b) how by employing the ILA algorithm the harmonic distortion is reduced. For the worst case of 1.0% of mismatch the use of ILA improved the SNDR from 57.8dB to 70.4dB.

7.5 Comparison to other Models

Simulations were carried to compare results between established models presented by Rio [14] and Fernandez [20], and the presented model. The relevant parameters

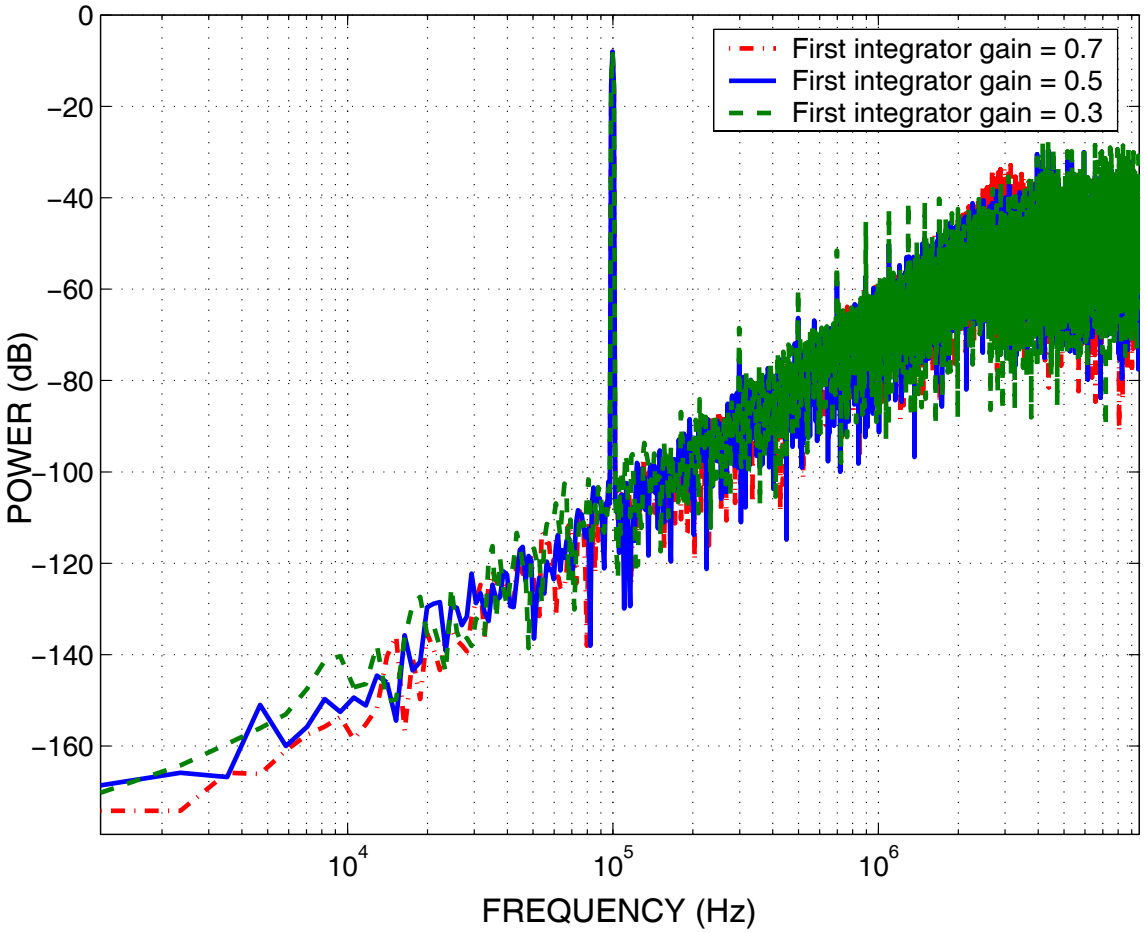


Figure 7.7. Power spectral density of a second-order multi-bit ΣΔM with first integrator gain at 0.3 (dash), 0.5 (solid) and 0.7 (dash-dot).

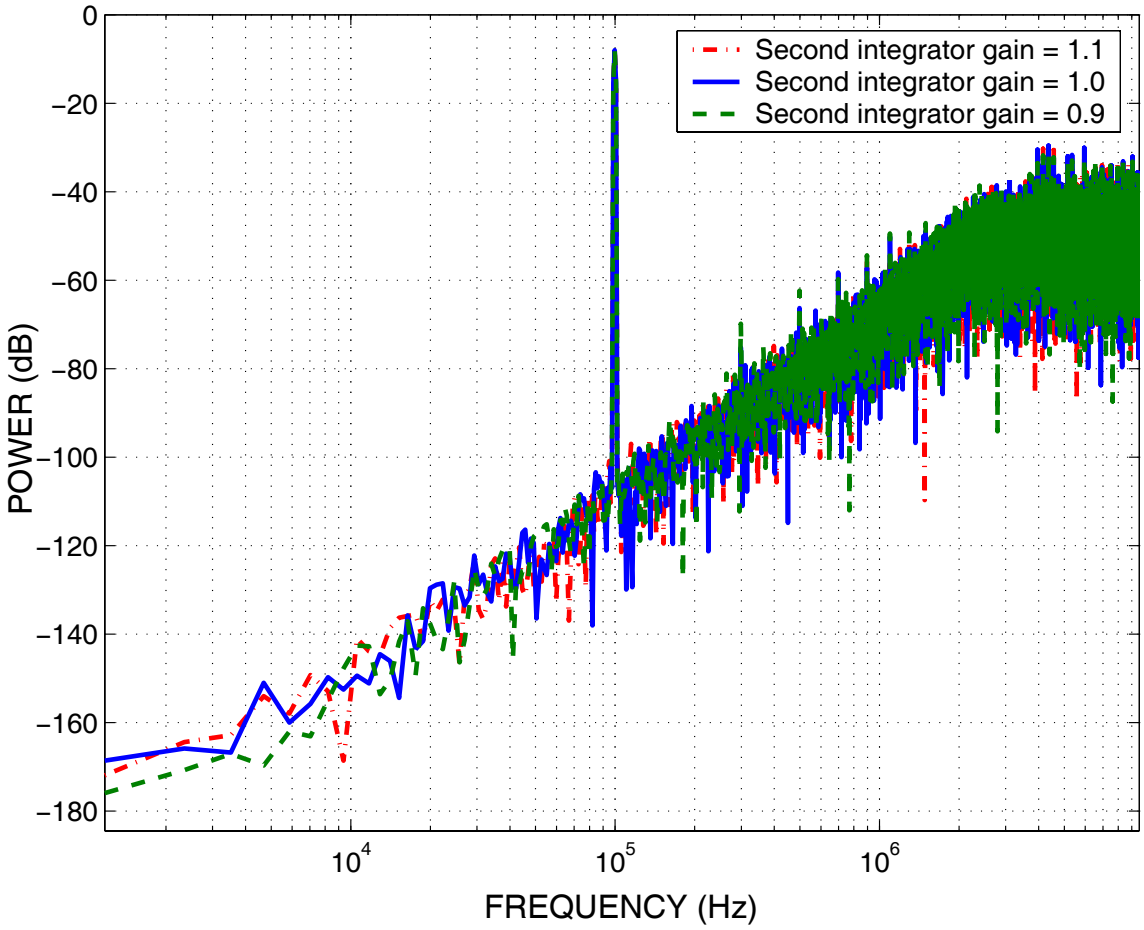
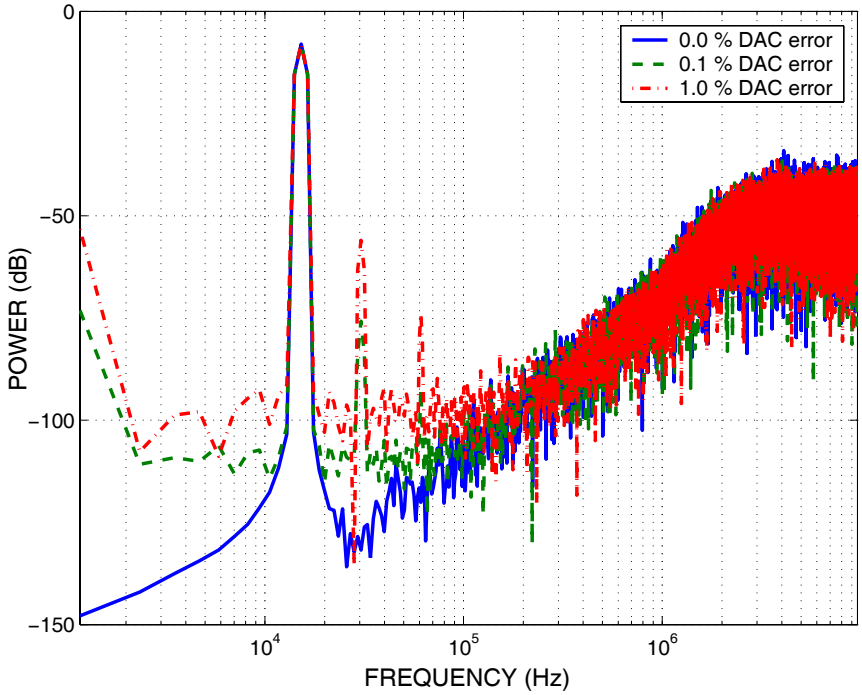
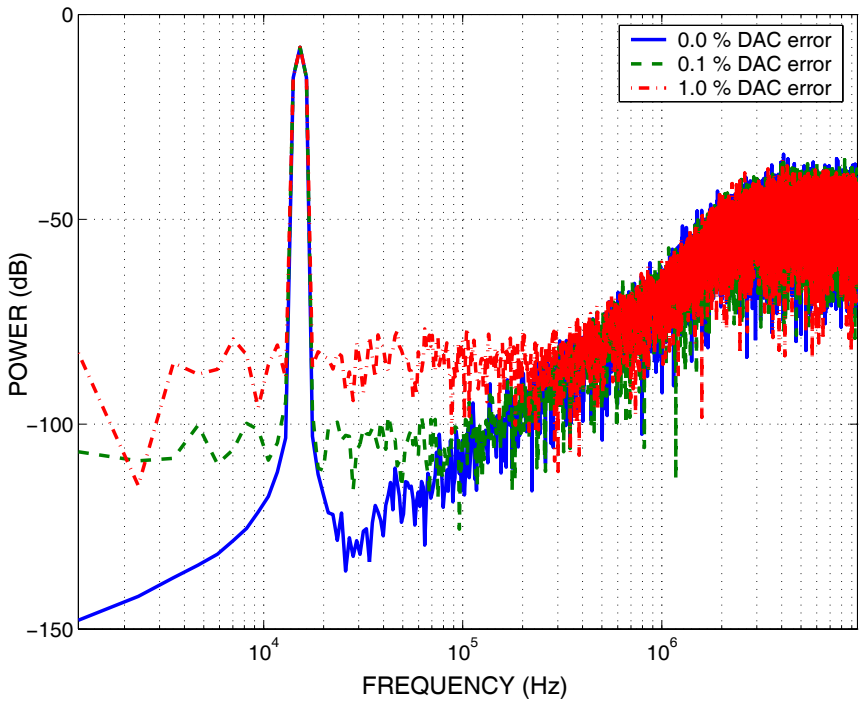


Figure 7.8. Power spectral density of a second-order multi-bit ΣΔM with second integrator gain at 0.9 (dash), 1.0 (solid) and 1.1 (dash-dot), respectively.



(a) PSD of a second-order ΣΔM with DAC error and ILA off



(b) PSD of a second-order ΣΔ Modulator with DAC error and ILA on

Figure 7.9. Power spectral density of a second-order multi-bit ΣΔ Modulator with ILA off and DAC error of 0.0% (solid), 0.1% (dash) and 1.0% (dash-dot) for: (a) ILA off and (b) ILA on.

are: oversampling ratio of 65, sampling frequency of 26MHz and input signal with frequency of 33kHz and -6dB amplitude. In addition to a temperature of 27^oC, jitter of 1ns and 0.05% of error in the DACs were added. Additional parameters used in the simulation are listed in Table 7.8. The used parameters for the amplifier transconductance g_m, output conductance g_o, and maximum output current I_o are those for a low-power design.

Figures 7.10, 7.11 and 7.12 show the power spectrum for the traditional model, the admittance matrix model and the presented model, respectively. As shown in Figure 7.12, the presented model improves the characterization of system harmonics. This is evidenced by a more distinguishable third harmonic. As explained in Section 5.1.1, the third harmonic has a direct relationship with the operational transconductance amplifier (OTA) characteristics such as the DC gain, the finite gain-bandwidth, and the slew-rate.

7.6 Speed

As mentioned, the presented model uses VHDL-AMS as the modeling language while the previous model [20] uses MATLAB Simulink as the modeling language. Moreover, the Ansoft SIMPLORER was used as the VHDL-AMS simulator. Given the commercial nature of these simulation tools, the information needed to make an algorithmic-level analysis of the time and space complexity of these approaches is not readily available. Despite this limitation, and the given the fact that factors other than algorithmic characteristics might affect, running times of both methods were recorded while running the same test cases, as an attempt to shed some light on the time requirements of both methods.

Simulations were carried for 8192, 16384, 32768 and 65536 clock cycles in both

Table 7.8. Values for Integrator Parameters.

Parameter	First Integrator	Second Integrator
C_i	0.4pF	0.3pF
C_r	0.4pF	0.3pF
C_{inp}	0.5pF	0.7pF
C_{int}	0.8pF	0.3pF
C_{intp}	0.08pF	0.03pF
C_{inxt}	0.3pF	0.8pF
C_o	0.7p	0.35pF
g_o	3e-7Ω^{-1}	1.5e-7Ω^{-1}
g_m	0.3mA/V	0.15mA/V
I_o	30μA	30μA
R_{on}	200Ω	200Ω
fs	26MHz	26MHz

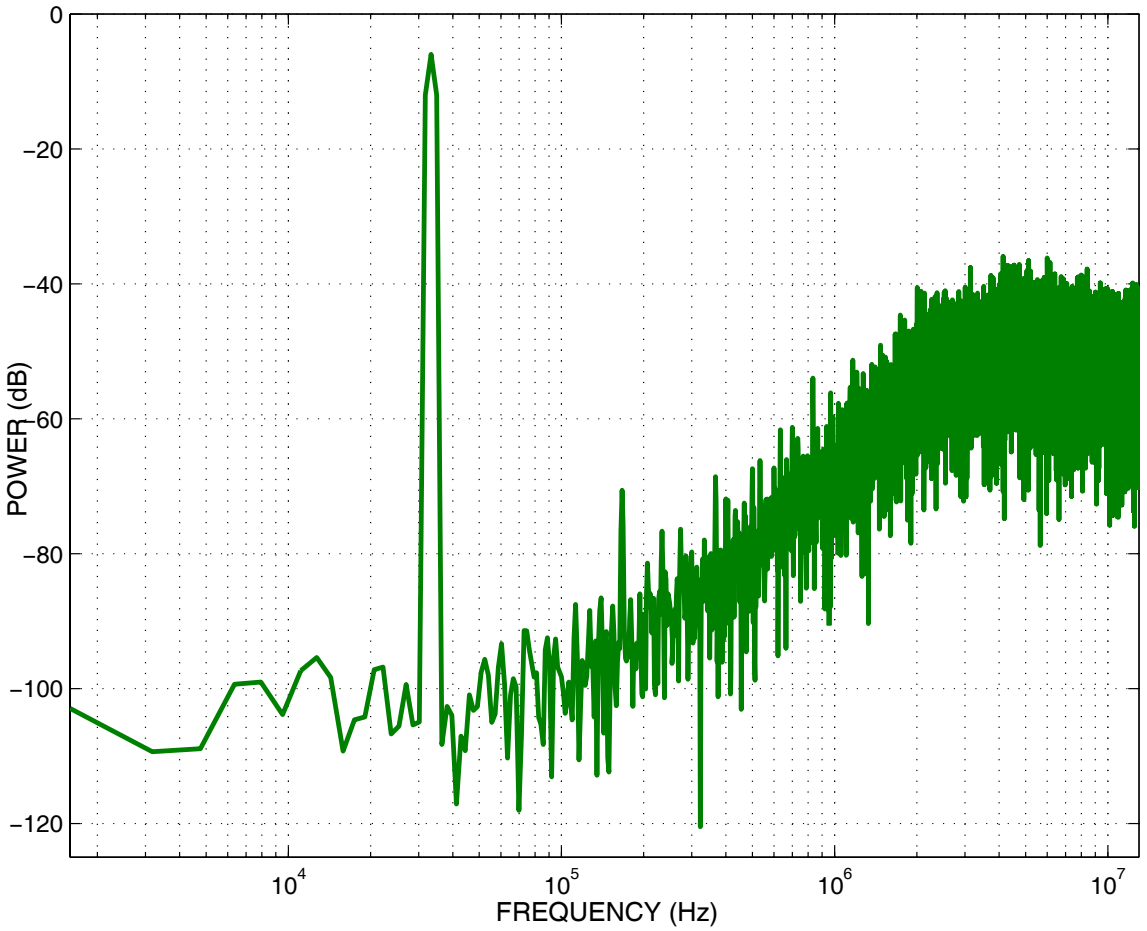


Figure 7.10. Power spectral density of a second-order multi-bit $\Sigma\Delta$ Modulator for traditional model.

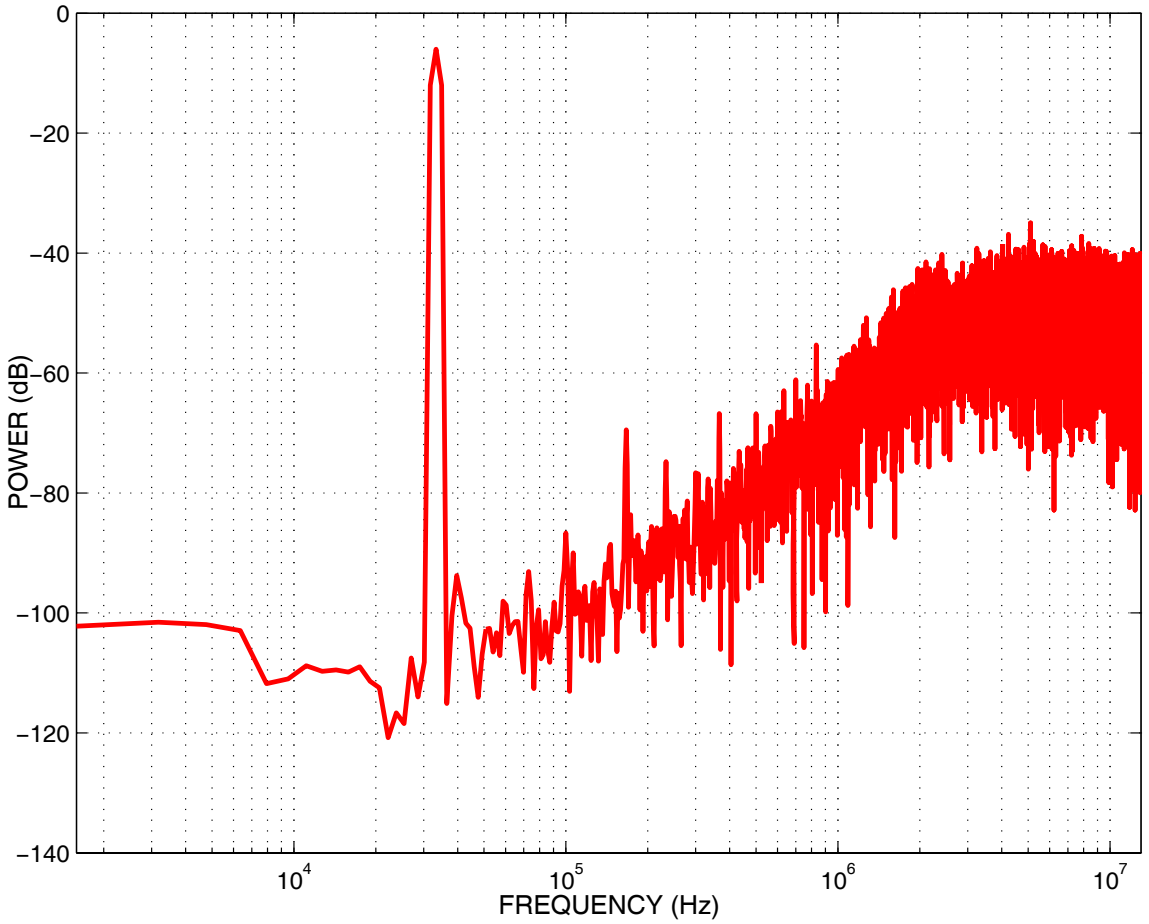


Figure 7.11. Power spectral density of a second-order multi-bit $\Sigma\Delta$ Modulator for admittance matrix model.

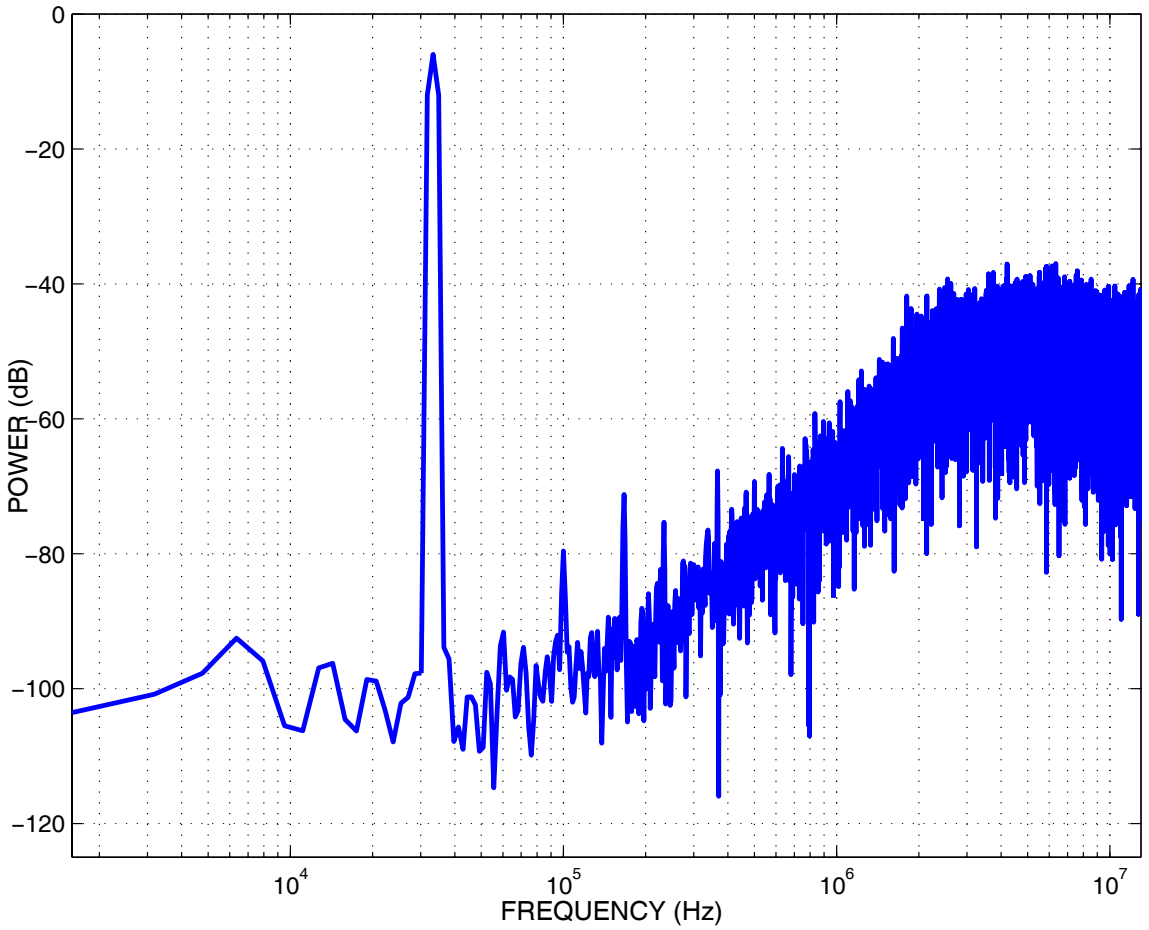


Figure 7.12. Power spectral density of a second-order multi-bit ΣΔ Modulator for presented model.

cases. Table 7.9 summarizes the recorded time results for each simulation and the corresponding model. Simulations were carried on a Pentium 4 PC with 2GB memory running at 3.0GHz. It deserves mentioning that the transient model in VHDL-AMS exhibits an average of 0.002 sec/cycle while the admittance matrix model in Simulink was limited to 0.24 sec/cycle.

Table 7.9. Simulation time for the presented models.

Cycles	**Admittance Matrix Model**	**VHDL-AMS Transient Model**
8192	31 min 42 sec	15 sec
16384	1 hr 4 min 42 sec	30 sec
32768	2 hr 12 min 8 sec	1 min
65536	4 hr 13 min 5 sec	2 min 11 sec

CHAPTER 8

Conclusion and Future Work

8.1 Conclusion

Oversampling ΣΔMs have been used as key components in oversampled A/D and D/A converters. As the technology advances, current research on these circuits shows the potential of ΣΔ converters in high-speed and low-power interfaces for mixed-signal ICs. Although, transistor-level or device-level circuit simulation is the most accurate approach known for these components this method becomes impractical for complex systems due to the long computational time. Consequently, device-level simulation in most cases is performed at the end of the design cycle as a final verification step. This situation has led designers to consider behavioral modeling as an alternate technique being a more time-efficient and practical solution. The use of behavioral modeling provides the designer with a set of building blocks representing elements and nonidealities improving reusability.

This work presented a comprehensive behavioral model of a high speed second-order multibit ΣΔM implemented using VHDL-AMS as the modeling language. The model addresses the main noise sources and nonidealities including: thermal noise during sampling and integration phases due the amplifier and switch resistance, sam-

pling jitter, capacitance mismatch and integrator dynamics.

The main noise sources in ΣΔMs were discussed in Sections 5.2 and 5.3. Thermal noise in ΣΔMs is due the OTA and the finite switch resistance of the SC integrator during the sampling and integration phases. The developed model in VHDL-AMS provides a white spectrum noise proportional to temperature and inversely proportional to the sampling capacitors sizes, which proves to be similar to that of reality. Modeling jitter noise is feasible using the models based on the derivative approximation, and the sampling process deviation. Moreover, results for VHDL-AMS simulations of a second-order multi-bit ΣΔM using the developed sampling jitter model shows the proportional relation with the jitter standard deviation and the input signal frequency.

Internal gain factors in SC integrators are implemented using capacitor ratios. Consequently, capacitance mismatch in these circuits alter their transfer function affecting the signal and quantization noise. Results from simulations where mismatch was introduced in the integrator's gains, evidenced the effect on the transfer function by means of the PSD characteristics. A second effect of capacitance mismatch becomes critical in multi-bit ΣΔMs directly related to the internal DAC. The mismatch in the internal DAC generates of additional harmonic distortion, thus degrading the SNDR of the modulator. Consequently, a DEM technique called ILA was included in the model to suppress such harmonic distortion. Simulations were carried introducing mismatch in the internal DAC up to 1%, evidencing the increase in harmonic distortion. Furthermore, results for simulations using the ILA algorithm showed the suppression of the harmonic distortion introduced by the DAC mismatch and the improvement in the SNDR.

The defective settling of the SC integrator has become the main limiting factor in the performance of discrete-time (DT) ΣΔMs. The incomplete settling is mainly

caused by the operational transconductance amplifier (OTA) characteristics such as the finite DC gain, finite gain-bandwidth (GBW), and slew-rate (SR) limitations. A transient model of the SC integrator that includes the effects of the amplifier transconductance, output conductance and the dynamic capacitive loading effect on the settling time was presented. The model proves to be accurate with less than 7.0% and 3.0% of error when compared with SPICE simulations and experimental data, respectively. Moreover, a comparison with published models evidenced that the presented model provides an improved behavioral characterization of the degrading effects of settling errors on high-speed low-power ΣΔMs.

8.2 Contribution of this Work

The major contribution of this work is the development of an accurate behavioral model of a second-order multi-bit ΣΔM using VHDL-AMS as the modeling language. It provides an improved behavioral characterization of the degrading effects of settling errors on high-speed low-power ΣΔMs and a good estimate of the SNDR as well. The model provides proper representation of significant nonidealities including:

- Jitter noise
- Thermal noise
- Capacitance mismatch
- Integrator dynamics

The integrator dynamics are the main source of performance degradation in ΣΔMs. This is mainly due the defective settling due the amplifier characteristics. The presented model includes the following integrator characteristics:

- Amplifier slew-rate limitations
- Amplifier transconductance g_m and output conductance g_o
- Capacitive load changes
- Parasitic capacitances
- Representation for sampling and integration phases

In addition, it offers a time advantage since computations are only made at the points of interest, thus reducing the simulation time. The flexibility and reusability of the modeling blocks, namely the integrator, thermal noise, sampling jitter, A/D converter, D/A converter and ILA makes feasible the modeling of other ΣΔM topologies. Furthermore, the presented behavioral models are suitable to be used in a top-down design approach.

8.3 Future Work

The use of a single-pole amplifier is, evidently, an approximation. A two-pole amplifier model can provide a better approximation and description of the dynamics effects of the amplifier. However, this two-pole model requires a higher level of knowledge and detail of the system that sometimes is not available at early stages of the design process. Moreover, the use of VHDL-AMS proves to be a good choice for the behavioral modeling and simulation of ΣΔMs. Similarly, the use of Verilog-A and Verilog-AMS could also be good choices to the modeling and simulation of ΣΔMs. The use of such analog hardware description languages (AHDL) can also be fully incorporated in leading CAD tools such as the Cadence IC as part of a top-down design methodology.

BIBLIOGRAPHY

[1] O. Altun, Jinseok Koh, and P.E. Allen. A 1.5v multirate multibit sigma delta modulator for GSM/WCDMA in a 90 nm digital CMOS process. *IEEE International Symposium on Circuits and Systems ISCAS*, pages 5577–5580, 2005.

[2] P. Arpaia, F. Cennamo, and H. Schummy. Modeling and Characterization of Sigma-Delta Analog-to-Digital Converters. *IEEE Instrumentation and Measurement Technology*, pages 742–752, 1998.

[3] P. J. Ashenden, G. D. Peterson, and D. A. Teegarden. *The System Designer's Guide to VHDL-AMS*. Morgan Kauffmann Publishers, 2003.

[4] R.J. Bishop, J.J. Paulos, M.B. Steer, and S.H. Ardalan. Table-Based Simulation of Delta-Sigma Modulators. *IEEE Transactions on Circuits and Systems*, 37:447–451, 1990.

[5] B.E. Boser and B.A. Wooley. The Design of Sigma-Delta Modulation Analog-to-Digital Converters. *IEEE Journal of Solid-State Circuits*, 23:1298–1308, 1988.

[6] G.T. Brauns, R.J. Bishop, M.B. Steer, J.J. Paulos, and S.H. Ardalan. Table-based modeling of delta-sigma modulators using ZSIM. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 9:142–150, 2000.

[7] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, and F. Maloberti. Modeling Sigma-Delta Modulator Non-Idealities in Simulink. *IEEE International Symposium on Circuits and Systems*, 2:384–387, 1999.

[8] T. Burger and Qiuting Huang. A 3v, 2.8 mw CMOS $\sigma\delta$-modulator for GSM applications. *Digest of Technical Papers for Symposium on VLSI Circuits*, pages 90–91, 1998.

[9] J. C. Candy and G. C. Temes. *Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*. IEEE Press, 1992.

[10] R. Castro-Lopez, F. V. Fernandez, F. Medeiro, and A. Rodriguez-Vasquez. Behavioral Modeling and Simulation of ΣΔM Modulators using Hardware Description Languages. *Medea Conference*, 2003.

[11] Feng Chen and B.H. Leung. A High Resolution Multibit Sigma-Delta Modulator with Individual Level Averaging. *IEEE Journal of Solid-State Circuits*, 30:453–460, 1995.

[12] J. S. Chiang, P. C. Chou, and T. H. Chang. Dual-Band Sigma-Delta Modulator for Wideband Receiver Application. *IEICE Transactions Fundamentals*, 2:311–323, 2004.

[13] C. T. Chuang. Analysis of the Settling Behavior of an Operational Amplifier. *IEEE Solid State Circuits*, 17:74–80, 1982.

[14] R. Del Rio, F. Medeiro, B. Perez-Verdu, and A. Rodriguez-Vazquez. Reliable Analysis of Settling Errors in SC Integrators - Application to the Design of High-Speed Sigma-Delta Modulators. *IEEE International Symposium on Circuits and Systems*, 4:417–420, 2000.

[15] A. Dezzani and E. Andre. A 1.2-v dual-mode WCDMA/GPRS $\sigma\delta$ modulator. *International Solid-State Circuits Conference ISSCC*, pages 58–59, 2003.

[16] V.F. Dias, V. Liberali, and F. Maloberti. TOSCA: A User-Friendly Behavioural Simulator for Oversampling A/D Converters. *IEEE International Sympoisum on Circuits and Systems*, 5:2677–2680, 1991.

[17] J.Y. Dong and A. Opal. Dithering Effect Simulation for Sigma-Delta Modulators with the Presence of Thermal Noise. *IEEE Canadian Conference*, 1:353–356, 1998.

[18] Y. Dong and A. Opal. An Overview on Coumputer Aided Analysis Techniques for Sigma-Delta Modulators. *IEEE International Symposium on Circuits and Systems*, 5:423–426, 2001.

[19] B.J. Farahani and M. Ismail. A low power multi-standard sigma-delta ADC for WCDMA/GSM/bluetooth applications. *The 2nd Annual IEEE Northeast Workshop on Circuits and Systems NEWCAS*, pages 241–243, 2004.

[20] Felix Fernandez. Behavioral Modeling of Sigma-Delta Modulators. Master's thesis, University of Puerto Rico, Mayaguez Campues, 2003.

[21] F.O. Fernandez and M.A. Jimenez. Behavioral Modeling of Dynamic Capacitive Loads on Sigma-Delta Modulators. *Seminario Anual de Automatica Electronica Industrial e Instrumentacion*, 1:119–122, 2002.

[22] J. H. Fisher. Noise Sources and Calculation Techniques for Switched Capacitor Filters. *IEEE Journal of Solid State Circuits*, 4:742–752, 1982.

[23] K. Francken, P. Vancorenland, and G. Gielen. DAISY: a simulation-based high-level synthesis tool for $\Sigma\Delta$modulators. *IEEE/ACM International Conference on Computer Aided Design ICCAD*, pages 188–192, 2000.

[24] K. Francken, P. Vancorenland, and G. Gielen. DAISY-CT: a simulation-based high-level tool for CT-$\Sigma\Delta$modulators. *IEEE Proceedings on Design, Automation and Test in Europe Conference and Exhibition*, page 1110, 2002.

[25] Y. Geerts, M. Steyaert, and W. Sansen. *Design of Multi-bit Delta-Sigma A/D COnverters*. Kluwer Academic Publishers, 2002.

[26] G. Gomez and B. Haroun. A 1.5 V 2.4/2.9 mW 79/50 dB DR SD modulator for GSM-WCDMA in a 0.13 μm digital process. *ISSCC*, pages 467–469, 2002.

[27] Kershaw, S.M. and Sandler, M.B.;. Simulation of sigma-delta data converters using SPICE. *IEEE Colloquium on Advanced A-D and D-A Conversion Techniques and Applications*, pages 1–5, 1993.

[28] M Kozak and I. Kale. *Oversampled Delta-Sigma Modulators*. Kluwer Academic Publishers, 2003.

[29] L. A. Williams and B. A. Wooley. MIDAS - A functional simulator for mixed digital and analog sampled data systems. *IEEE International Symposium on Circuits and Systems ISCAS*, 5:2148 – 2151, 1992.

[30] C. F. Lee, R. D. Davis, and W. K. Jenkins. Sensitivity and Nonlinear Distortion Analyses for Switched-Capacitor Circuits Using SCAPN. *IEEE Transactions on Circuits and Systems*, 31:213–221, 1984.

[31] B.H. Leung and S. Sutarja. Multibit $\Sigma\Delta$M A/D Converter Incorporating a Novel Class of Dynamic Element Matching Techniques. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 39(1):35–51, 1992.

[32] K. U. Leuven. Selection of the simulation approach for ΣΔM Modulators. *SYSCONV Systematic Top-Down Design and System Modeling of Oversampling Converters*, 2001.

[33] Xiaopeng Li and M.; Ismail. Fast simulation of sigma-delta modulators using SPICE. *IEEE Circuits and Devices Magazine*, 15:7–9, 1999.

[34] J. C. Lin and J. H. Nevin. A Modified Time-Domain Model for Nonlinear Analysis of an Operational Amplifier. *IEEE Solid State Circuits*, 21:478–483, 1986.

[35] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto. Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators. *IEEE International Symposium on Circuits and Systems*, 50:352–364, 2033.

[36] F. Medeiro, B. Perez-Verdu Ans A. Rodriguez-Vazquez, and J.L. Huertas. A vertically integrated tool for automated design of Sigma Delta modulators. *IEEE Journal of Solid-State Circuits*, 30:762 – 772, 1995.

[37] Medeiro, F. and Perez-Verdu, A. and Rodriguez-Vazquez, A. *Top-Down Design of High-Performance Sigma-Delta Modulators*. Kluwer Academic Publishers, 1999.

[38] L. W. Nagel. SPICE: A computer program to simulate semiconductor circuits. *Technical Report ERL-M520, Univeristy of California - Berkeley*, 1975.

[39] R. Naikanaware and T. Fiez. Power optimization of sigma-delta analog-to-digital converters based on slewing and partial settling considerations. *IEEE International Symposium on Circuits and Systems*, 1:360–364, 1998.

[40] E. Normark, L. Yang, C. Wakayama, P. Nikitin, and R. Shi. Vhdl-ams behavioral modeling and simulation of a /spl pi//4 dqpsk transceiver system. In *Behavioral Modeling and Simulation Conference, 2004. BMAS 2004. Proceedings of the 2004 IEEE International*, pages 119–124, 2004.

[41] Norsworthy, S. R. and Schreirer, R. and Temes, G. C. *Delta-Sigma Data Converters: Theory Design and Simulation*. IEEE Press, 1997.

[42] A. Opal. Sampled data simulation of linear and nonlinear circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System*, 15:295 – 307, 1996.

[43] A. Opal. Simulation of oversampled sigma delta convertors. *IEEE International Symposium on Circuits and Systems*, 4:727 – 730, 1996.

[44] S. Park. *Principles of Sigma-Delta Modulation for Analog-to-Digital Converters*. Motorola Press, 2001.

[45] Peic, R. V. Simple and Accurate Nonlinear Macromodel Operational Amplifiers. *IEEE Journal of Solid State Circuits*, 26:896–897, 1991.

[46] B. Perez-Verdu, B. Cruz, J.and Linares-Barranco, A. Rodriguez-Vazquez, J.L. Huertas, and E. Sanchez-Sinencio. Nonlinear time-domain macromodeling of OTA circuits. *IEEE International Symposium on Circuits and Systems*, 2:1441 – 1444, 1989.

[47] K. Rowley and C. Lyden. SIGGEN: A Sigma-Delta DAC Autogeneration Tool. *Proceedings of the 21st International Conference on Microelectronics*, 2:729–732, 1997.

[48] J. Ruiz-Amaya, J. M. de la Rosa, F. Medeiro, R. del Río, J. Moreno-Reina, J. B. Pérez-Verdú, R. Tortosa, R. Romay, and A. Rodríguez-Vázquez. SIMSIDES Toolbox: An Interactive Tool for the Behavioural Simulation of Discrete- and Continuous-time SD Modulators in the MATLAB/SIMULINK Environment. 2003.

[49] J. Ruiz-Amaya, J. M. De la Rosa, F. Medeiro, R. Del Rio, B. Perez-Verdu, and A. Rodriguez-Vasquez. MATLAB/SIMULINK-Based High Level Synthesis of Discrete Time and Continuous Time $\Sigma\Delta$M Modulators. *IEEE International Workshop on Behavioral Modeling and Simulation*, 2004.

[50] A. Rusu and S.; Lungu. Table-based modeling of delta-sigma modulators using ZSIM. *The 8th IEEE International Conference on Electronics, Circuits and Systems ICECS*, 1:297–300, 2001.

[51] Sansen, W. Transient Analysis of Charge Transfer in SC Filters: Gain and Error Distortion. *IEEE Journal of Solid State Circuits*, 22:268–276, 1987.

[52] R. Schreier. Delsig: Delta-sigma toolbox. *www.mathworks.com*, 2000.

[53] M. Schubert. VHDL Based Simulation of a Sigma-Delta A/D Converter. *IEEE/ACM International Workshop on Behavioral Modeling and Simulation*, pages 71–76, 2000.

[54] Z.Q. Shang and J.L. Sewell. Efficient sensitivity analysis for large nonideal switched capacitor networks. *IEEE International Symposium on Circuits and Systems*, 2:1405 – 1407, 1993.

[55] Z.Q. Shang and J.L. Sewell. Efficient Noise Analysis Methods for Large Non-Ideal SC and SI Circuits. *IEEE International Symposium on Circuits and Systems*, 5:565–568, 1994.

[56] Z.Q. Shang and J.L. Sewell. Development of efficient switched network and mixed mode simulators. *IEEE Proceedings on Circuits and Systems*, 145:24–34, 1998.

[57] C. Shi and I. M. Mostafa. *Data Converters for Wireless Standards*. Springer, 2001.

[58] X. Shi and P.E. Allen. Use of VHDL to Model and Simulate Analog-Digital IC's. *Proceedings of the 35th Midwest Symposium on Circuits and Systems*, 2:908–911, 1992.

[59] G. Suarez and M. Jimenez. Behavioral Modeling of $\sigma\delta$ Modulators using VHDL-AMS. *IEEE Midwest Symposium on Circuits and Systems*, 2005.

[60] K. Suyama and S. C. Fang. *User's Manual for SWITCHCAP2*. Department of Electrical Engineering and Center for Telecommunications Research Columbia University New York NY 10027, 1.1 edition, February 1992. S. C. Fang is the author of the original SWITCAP manual which was written in.

[61] M. Szermer, M. Daniel, and A. Napieralski. Modeling and simulation of sigma-delta analog to digital converters using VHDL-AMS. *CADSM The Experience of Designing and Application of CAD Systems in Microelectronics*, pages 331–333, 2003.

[62] R. J. Trihy and R. A. Rohrer. AWEswit: A switched capacitor circuit simulator. *IEEE Proceedings on Custom Integrated Circuits Conference*, 29:18.4.1–18.4.4, 1993.

[63] R. J. Trihy and R. A. Rohrer. A Switched Capacitor Simulator: AWESwit. *IEEE Journal on Solid State Circuits*, 29:217–225, 1994.

[64] R.J. Trihy and R.A. Rohrer. Simulating Sigma-Delta Modulators in AWEswit. *IEEE/ACM International Conference on Computer-Aided Design*, pages 141–144, 1993.

[65] M. Vogels, B. De Smedt, and G. Gielen. VHDL-AMS Models for Continuous-Time Delta-Sigma Modulators. *ProRISC IEEE Workshop on Circuits and Systems and Signal Processing*, pages 706–709, 2001.

[66] M. Vogels, K. Francken, and G. Gielen. Modeling and Simulation of a Sigma-Delta Digital to Analog Converter Using VHDL-AMS. *IEEE/ACM Proceedings International Workshop on Behavioral Modeling and Simulation*, pages 5–9, 2000.

[67] Jerry Wayne Bruce. *DYNAMIC ELEMENT MATCHING TECHNIQUES FOR DATA CONVERTERS*. PhD thesis, Howard R. Hughes College of Engineering, May 2000.

[68] P. R. Wilson, Y. Kilie, J. N. Ross, M. Zwolinski, and A. D. Brown. Behavioral modeling of operational amplifier faults using VHDL-AMS. *Design, Automation and Test in Europe Conference and Exhibition*, page 1113, 2002.

[69] J. Wu and L.R. Carley. A table-based time-domain simulation method for over-sampled microelectromechanical systems. *IEEE/ACM International Workshop on Behavioral Modeling and Simulation*, 15:37 – 41, 2000.

[70] F. Yuan and A. Opal. Adjoint Network of Periodically Switched Linear Circuits with Applications to Noise Analysis. *IEEE Transactions on Circuits and Systems Fundamental Theory and Applications*, 48:139–151, 2001.

[71] F. Yuan and A. Opal. Computer methods for switched circuits. *IEEE Transactions on Circuits and Systems Fundamental Theory and Applications*, 50:1013 – 1024, 2003.

[72] H. Zhang and A. Doboli. Fast Time-Domain Symbolic Simulation for Synthesis of Sigma-Delta Analog-Digital Converters. *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2004.