ANALYTICAL MODEL DEVELOPMENT FOR LC PARASITIC ESTIMATION IN POWER ELECTRONICS CIRCUITS

By

Angel R Rivera Ramos

A project report submitted in partial fulfillment of the requirements for the degree of

MASTER OF ENGINEERING

in

ELECTRICAL ENGINEERING

UNIVERSITY OF PUERTO RICO
MAYAGÜEZ CAMPUS

May, 2010

Approved by:

Rogelio Palomera, Ph.D Member, Graduate Committee	Date
Miguel Velez, Ph.D Member, Graduate Committee	Date
Manuel Jiménez, Ph.D Chairman, Graduate Committee	Date
Arturo Portnoy, Ph.D Graduate Studies Representative	Date
Hamed Parsiani, Ph.D Chairperson of the Department	Date

Abstract of Project Report Presented to the Graduate School
of the University of Puerto Rico in Partial Fulfillment of the
Requirements for the Degree of Master of Engineering

ANALYTICAL MODEL DEVELOPMENT FOR LC PARASITIC ESTIMATION IN POWER ELECTRONICS CIRCUITS

By

Angel R Rivera Ramos

May 2010

Chair: Manuel Jimenez
Major Department: Electrical and Computer Engineering

Technology trends in Power Electronics (PE) design continue to move toward board size reduction and increasing operating frequencies. However, as board sizes are reduced and operating frequencies increased, Electromagnetic Interference (EMI) increasingly becomes a real limiting issue. The inherent parasitic resistance, capacitance, and inductance present in PE Printed Circuit Board (PCB) traces has been identified as one of the main causes of EMI. As a result, PCB parasitics need to be estimated and minimized. This work presents the development of a fast and accurate PCB parasitic estimation tool, applicable to Power Electronics circuits. This tool uses a semi-lumped approach that divides each PCB trace into simpler segments where analytical equations can be directly applied to obtain the desired parasitic elements. The total parasitic estimate in a trace is computed from the contributions of all its sub-segments and their interactions. The speed advantage gained by this method created the opportunity of using it into automated PCB layout parasitic minimization methods.

Resumen de Reporte de Proyecto Presentado a Escuela Graduada
de la Universidad de Puerto Rico como requisito parcial de los
Requerimientos para el grado de Maestría en Ingeniería

DESARROLLO DE MODELOS ANALÍTICOS PARA LA ESTIMACIÓN DE PARASÍTICOS LC EN CIRCUITOS DE ELECTRÓNICA DE POTENCIA

Por

Angel R Rivera Ramos

Mayo 2010

Consejero: Manuel Jimenez
Departamento: Ingeniería Eléctrica y Computadoras

Las tecnologías de diseño en electrónica de potencia continuan avanzado en la dirección de producir circuitos cada vez más pequeños y capaces de operar a frecuencias más altas. Sin embargo, a medida que cumplimos con los requisitos de diseño previamente mencionados, la Interferencia Electromagnética se convierte en una gran limitante. Una de las principales causas de Interferencia Electromagnética es la prescencia de componentes resistivos, inductivos y capacitivos, llamados comúnmente parasíticos. Para solucionar este problema es necesario estimar los parasíticos presentes en un circuito impreso para entonces aplicar estrategias con el, destinadas a reducirlos al mínimo. Con este objetivo en mente, presentamos el desarrollo de una herramienta de estimación de parasíticos, aplicada a circuitos de electrónica de potencia. Esta herramienta divide cada trazo de un circuito impreso en segmentos más simples, a los cuales se le aplica ecuaciones analíticas para hallar los parasíticos presentes en los mismos. El estimado total de parasíticos en un trazo es calculado mediante la contribución individual de sus segmentos e interacciones. La rapidez

computacional alcanzada en el método crea la oportunidad de utilizar el mismo en métodos automáticos de minimización de parasíticos.

To my wife for her dedication and inconditional support during this stage of my career.

ACKNOWLEDGMENTS

This work was supported primarily by the ERC program of the national science foundation under the award number EEC-9731667.

To Profesor Manuel Jimenez (INEL), for pushing me towards the completion of this work.

TABLE OF CONTENTS

page

ABSTRACT ENGLISH ii

ABSTRACT SPANISH iii

ACKNOWLEDGMENTS vii

1 Introduction 1

1.1 Research Motivation 1
1.2 Background 2
1.2.1 Elements in an EMI Problem 4
1.2.2 Evaluation and Design Issues 5

2 Previous Work 9

2.1 Previous Work 9
2.1.1 EMI Evaluation Methods 9
2.1.2 EMI Minimization Techniques and Optimization Methods . 10
2.1.3 PCB Parasitics Extraction Tools 12
2.1.4 Other Methods 16
2.2 Relevance of Previous Works 17

3 Problem Statement 19

4 OBJECTIVES 21

5 METHODOLOGY 23

5.1 PCB Layout Representation 24
5.2 Traces geometry and materials identification 24
5.3 Manage Complicated Geometries 24
5.3.1 Trace Segmentation 25
5.4 Analytical Equations Development and Trace Parasitic Extraction 25
5.5 Inductance Calculation 26
5.5.1 Trace Segment Self-Inductance Calculation 26
5.5.2 Mutual Inductance Calculation Between Segments 28
5.5.3 Total Trace Self-inductance Calculation 31
5.6 Capacitance Calculations 31
5.7 Resistance Calculations 32

6 RESULTS 35
6.1 Validation 35
6.2 Test Case Layout 35
6.3 Maxwell Q3D 35
6.4 Analytical Parasitic Extraction 37
6.5 Compare Results 37
6.6 Inductance Calculation Results 38
6.7 Capacitance Calculation Results 39
6.8 Resistance Calculation Results 40
6.9 Running Time 41
6.10 Relevance of Results 41
6.11 Assumptions and Limitations 42
7 CONCLUSION 44
REFERENCES 46

CHAPTER 1
Introduction

1.1 Research Motivation

The Center for Power Electronics Systems (CPES) is contiuosly researching for advanced electronic power conversion technologies. One of the most significant milestones of CPES, is the development of Integrated Power Electronics Modules (IPEM). The IPEM design is applicable to a wide range of distributed power systems and applications. One of the IPEMs developed by CPES is the IPEM Generation II. It is shown in Figure 1–1. A 25 cents coin is shown in this figure to give an idea of its small size.

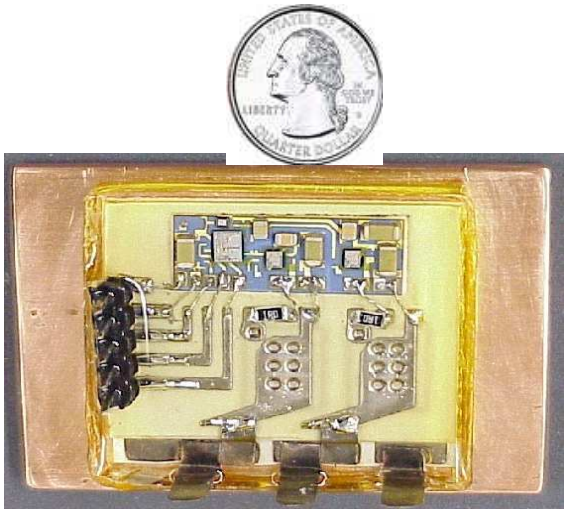


Figure 1–1: Gen II IPEM Gate Driver

Figure 1–2 shows the schematic of the IPEM Generation II. It is composed of two Power MOSFETs configured in a half bridge arrangement and a gate driver. The

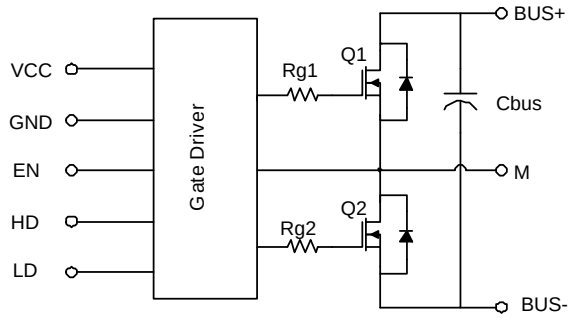


Figure 1–2: IPEM Schematic

gate driver is a triggering circuit that activates the power MOSFETs in an alternate way. This IPEM is used in Switch Mode Power Supplies (SMPS) applications.

SMPS are widely used in most power electronics applications like celullar phones, computers, medical equipment, and transportation vehicles among others. Almost everyting that needs electrical power uses a SMPS. SMPS design technology trends move forward circuit size reduction and operational frequency increase.

The IPEM Gen II works at a switching frequency of 200kHz. Technology trends require to operate the IPEM at 400kHz. At this frequency the Electromagnetic Interference (EMI) and noise generation on the IPEM was found to be considerably high.

The presence of parasitic elements on Printed Circuit Board (PCB)-which are resistance, inductance, and capacitance(RLC)- has been identified as one of the main causes of EMI generation in SMPS. This work presents the development of analytical models to estimate parasitic parameters (RLC) for power electronics circits in a fast and accurate way. This model is intended for use as one of the main components of automatic PCB layout optimization tools for power electronic circuits.

1.2 Background

Electromagnetic Interference (EMI) can be defined as an electromagnetic phenomena which, either directly or indirectly, can cause undesirable responses, degradation in performance, or malfunction of any electrical or electronic device or system.

Its nature can be explained with the help of Maxwell equations, which show the relationship between electricity and magnetism. Maxwell equations are based on four fundamental laws:

1. **Gauss law for electricity** This law defines the relationship between static electric charge density (ρ_v) and their accompanying static electric field (D) with the following statement : The electric flux through any closed surface is proportional to the enclosed electric charge. This relationship is defined by equation 1.1.

$$\nabla \cdot D = \rho_v \tag{1.1}$$

2. **Gauss law for magnetism** Magnetic field (B) has divergence equal to zero, shown in equation 1.2. It means that magnetic flux (B) is always present in closed loops, not as a single charge. It is equivalent to the statement that magnetic monopoles do not exist.

$$\nabla \cdot B = 0 \tag{1.2}$$

3. **Ampere law** It relates the integrated magnetic field around a closed loop to the electric current passing through the loop. Every time-varying electric field (D) is accompanied by a magnetic field (H). This law is expressed by equation 1.3.

$$\nabla \times H = J_c + \frac{\partial D}{\partial t} \tag{1.3}$$

4. **Faraday's law for induction** It shows the generation of electrical voltage and current due to a changing magnetic field (B). The induced electromotive force or EMF in any closed circuit is equal to the time rate of change of the magnetic flux through the circuit, as shown in equation 1.4.

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{1.4}$$

1.2.1 Elements in an EMI Problem

In order to exist an EMI problem, three components must be present: a source, a receptor, and a propagation path.

1. A source is the place where EMI is generated. Switching elements, like power transistors, represent typical EMI sources as they induce noise voltage and/or current. These sources are also present in the form of electromagnetic radiation, emitted by circuit interconnections carrying rapidly changing signals, as a by-product of their normal operation, which cause noise to be induced in other circuits.
2. A receptor or victim is an element affected by EMI. EMI may affect the operation of nearby suceptible integrated circuits (ICs) and induce noise in input-output (I/O) lines.
3. A propagation path is the way of transmission of EMI from source to receptor. EMI can be transmitted as electromagnetic radiation through a medium or induced due to the prescence of parasitic parameters in transmission lines. Figure 1–3 shows the interaction between these elements.

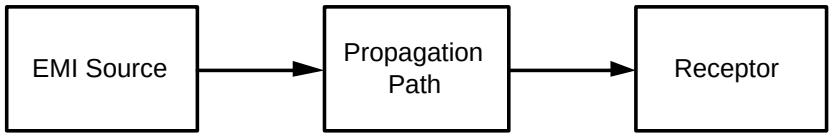


Figure 1–3: EMI components

The propagation path is responsible for EMI transmition. It can be transmitted form one system to another in two ways:

1. Radiated: transmitted in the form of electromagnetic radiation trough a medium, like air, to a receiving device, as an electromagnetic field.
2. Conducted: transmitted through a conducting path, like interconnection cables, due to the presence of parasitic parameters. It can appear in two forms:
   (a) Common mode: occurs when the unwanted noise consists of multiple currents flowing in the same direction along the conducting wire. Common mode

currents flowing in multi-conductor cables induce a magnetic flux around the conductors, thus inducing noise along the conductors.

(b) Differential mode: occurs when the unwanted noise consists of multiple currents flowing in opposite directions along the conducting wire.

Conducted EMI represents one of the most common EMI problems in Power Electronics (PE) circuits. This phenomena is strongly related to the layout of their printed circuit boards (PCB). Some common design techniques to reduce conducted EMI noise are discussed next.

1.2.2 Evaluation and Design Issues

The evaluation of the EMI performance for a PCB layout has to take into account a list of design issues. Among them we can mention:

1. Component placement. The relative position of the components in a board have a significant impact in the amount of interference induced by a source or agressor line in a victim trace or circuit. Figure 1–4 shows the relative position of a source and a victim circuit. The farthest the source and victim are placed, the lower the capacitive and inductive coupling will be, resulting in less conducted EMI. In the same manner, the radiated EMI will be less.

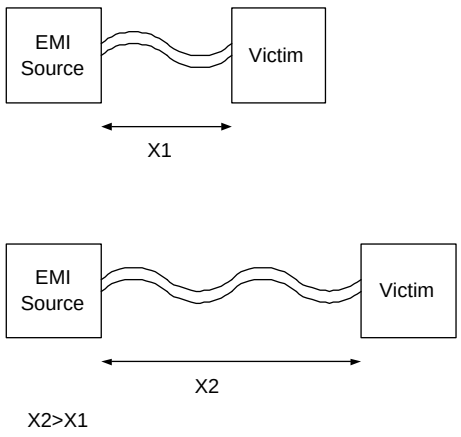


Figure 1–4: Component Placement

2. Loop area. It is defined as the area enclosed by a current loop. EMI is directly proportional to loop area, so loop area reduction is a relevant issue on EMI reduction.

   Figure 1–5 shows the main loops for the layout of the gate driver circuit evaluated as part of this work. These loops are the low and high input loops that control the switching MOSFETS on the gate driver. From visual inspection of the layout it can be noticed that the high input loop (in blue) has greater loop area than the low input loop. In addition this is a loop with a high switching activity. As a result, this loop is expected to generate the most interference in the circuit and its area needs to be reduced.

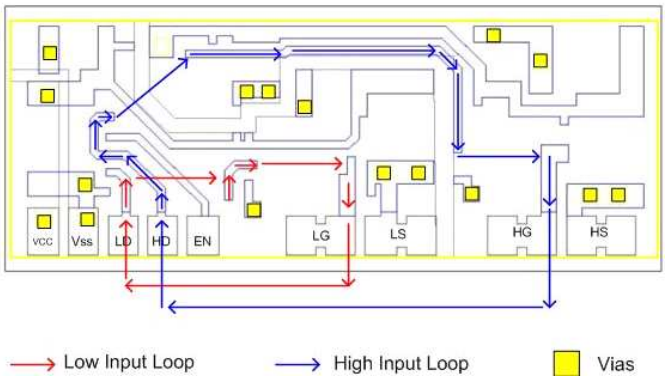
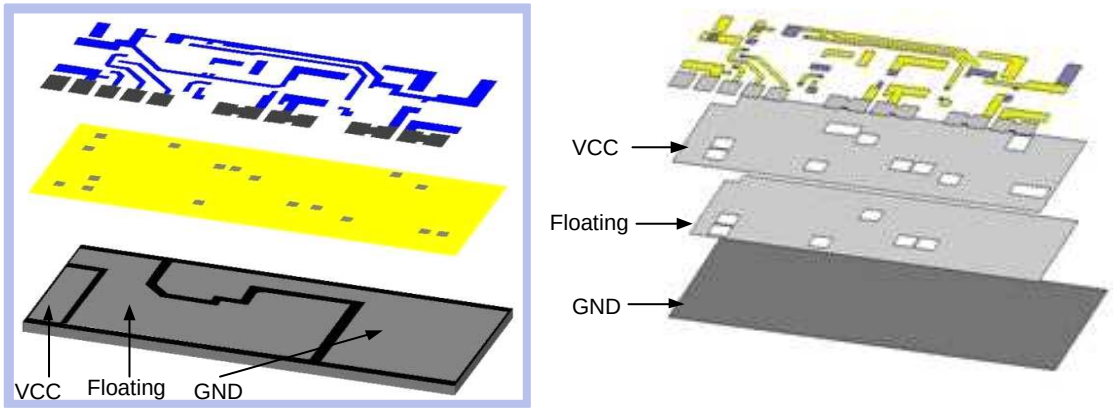


Figure 1–5: Loop Areas

3. Power and ground planes: Refers to the arrangement of conducting layers providing the supply levels and ground reference. The distribution of currents in these planes has a significant effect on PCB parasitics.

   Figure 1–6 shows two layouts for the gate driver under study on this work. The layout on the left has the VCC, GND, and Floating Plane on the same layer. The floating plane has high switching activity. EMI generated on it is transmitted thorough the rest of the board. The layout on the right shows a multilayer design, where the floating plane is placed between the VCC and GND planes. This arrangement has the effect of shielding, confining the EMI between the VCC and GND planes, and avoiding to trasmit it to the rest of the board.



Gate Drive Layout - coplanar design

Gate Driver Layout - multi-plane design

Figure 1–6: Power Ground Plane Arrangements on Gate Driver

4. PCB parasitics are the resistance, inductance and capacitance inherent to circuit elements and traces. These are ignored in ideal models. The evaluation of PCB parasitics plays a significant role in EMI estimation and reduction. The most important aspects in PCB parasitic evaluation include: self and mutual inductance, trace to ground and trace to trace capacitance, resistance, frequency effects, and power and ground plane effects.

PCB parasitics can be modeled as shown in Figure 1–7. This model is a lumped half pi model where Rx, Ry, Lx, and Ly are half the resistance and self inductance for traces x and y respectively. $M_{L_X L_Y}$ and C are the mutual inductance and capacitance between traces. Cx and Cy are the traces capacitances with respect to ground. The obtained model can be used for PCB EMI evaluation.

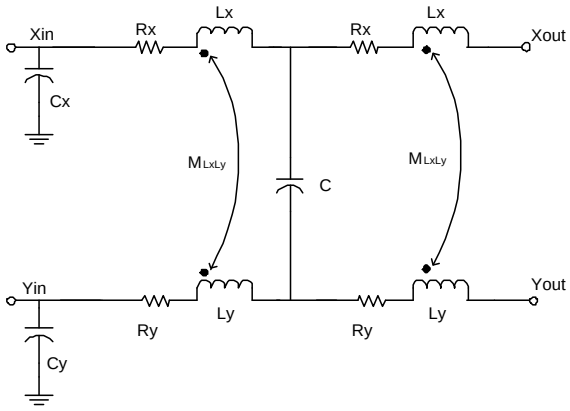


Figure 1–7: PCB traces model

CHAPTER 2
Previous Work

2.1 Previous Work

The way the layout for a power electronic circuit PCB is done has a significant impact on the EMI produced on it. While still at the PCB layout design stage most EMI problems can be alleviated, and in some cases eliminated, without changing the circuit topology or adding components to it, saving design time and cost.

Previous work in PCB layout with EMI considerations is discussed in this section. Most relevant work in this area include:

1. EMI evaluation methods: computational methods developed for evaluating EMI sources and their propagation through the circuits.
2. EMI minimization techniques and optimization methods: design techniques and guidelines used to minimize EMI in power electronics PCBs.
3. PCB parasitics extraction tools: tools and methods for obtaining parasitic PCB parameters.

2.1.1 EMI Evaluation Methods

In order to solve an EMI situation, EMI must be evaluated to determine the magnitude of the problem, if any. Computational methods have been developed for this purpose. These methods include finite difference time domain and method of moments, among others.

A systematic approach to analyze EMI is proposed by Liu [1]. This approach analyzes the propagation path and EMI source characteristics separately. The propagation path is characterized as a non linear function in the frequency domain, and

the EMI source by direct measurement. In this work, EMI for power electronic equipment operating at rated voltage is predicted by making measurements at lower voltages. In addition, this method avoids complex evaluation of parameters. However, this is a remediative non-preventive method that relies on direct measurements on existing equipment.

Circuit models for PCB tracks, passive components, and EMI sources have to be taken into account in order to obtain automatic PCB layout design tools. Some models are based on partial element equivalent circuit (PEEC). One of these models has been developed by Zhang [3]. He presents an approach to the analysis of conducted EMI usign the PEEC method where parasitic elements are extracted. The parasitic elements were determined by the geometrical structure of the circuit layout and packaging by using simplified Maxwell equations. The PCB was modeled with lumped partial inductor, resistor, and mutual coefficients. As a result of this work he developed design guidelines on circuit layout and packaging for EMI noise minimization. In addition, equivalent circuits were derived for EMI filter design. However this work was oriented towards analysis and not to optimization.

2.1.2 EMI Minimization Techniques and Optimization Methods

EMI minimization techniques have been developed at the design stage of power electronics PCB, having the advantage of solving most EMI issues before the circuit prototype is made. The effectiveness of EMI reduction methods is highly dependent on the speed and accuracy of the estimators used to quantify the magnitude of parasitic components.

Xin *et al.* developed a field oriented PCB layout CAD method aimed at reducing electric field coupling by developing an emission map of noisy traces [2]. This work applies a Genetic Algorithm to optimize PCB layout traces and separate them into critical and non-critical sections. The emission map generated on this work provides a visual guide to the designer, so he or she can place victim traces (susceptible to

EMI) in areas of less emission. However, this work focuses only on capacitance limiting its applications to digital circuits.

Another interesting approach takes into consideration component placement. Joshi and Agarwal presented a set of guidelines for proper component placement, oriented to EMI minimization [4]. Maxwell software was used as a tool in the development of these guidelines. Joshi and Argawal perfomed a proper component placement by identifying the points of minimum and maximum EMI. This work highlights guidelines for: control circuit placement, MOSFET and diode terminals connection, and electromagnetic analysis with Maxwell. It is limited to component placement.

A layout optimization methodology, based on analytical or semi-analytical models for EMC prediction was proposed by Schanen [5]. This optimization method included component models, EMC spectrum calculations, layout corresponding to minimal surface, and EMC contraints. This works presents a set of geometrical and EMC constraints for layout optimization, and leads to the best possible layout for a given structure. This approach was limited to rectangular shaped tracks, was technology specific to Insulated Metal Substrate, did not model track inductance, and neglected the modeling of the EMI source and its interaction with the layout.

Nagesware developed an expert system approach for obtaining an automatic process for PCB design [6]. This method was based on a set of known design rules and an initial layout file in order to begin an optimization process. These rules were implemented into a set of procedures in C++. A user interface highlighted the areas that have EMC problems like: floating pins, IC's without appropriate decoupling, sharp twists, and track stubs. As a result of this work a software prototype that analyzed simple designs identifying out most common flaws was developed. The effectiveness of these methods was dependent of its rules database and it was limited to simple designs.

2.1.3 PCB Parasitics Extraction Tools

PCB parasitics have a significant impact on the EMI performance of any given layout. Thus, the effectiveness of most EMI evaluation and extraction tools will depend on the speed and accuracy of its parasitic estimators. Developed techniques for PCB parasitic extraction include domain methods, integral equations approaches, and analytical methods.

Domain Methods

Domain methods are based on the solution of the differential Maxwell equations (used to obtain R, L, and C). Commonly used methods include:

1. Finite Difference (FD): Finite-difference is a numerical method used to approximate the solutions of differential equations by replacing derivative expressions with approximately equivalent difference quotients. This method is based on the definition of the first derivate of a function, that can be approximated by equation 2.1 for small values of h.

$$f'(x) \approx \frac{f(x+h) - f(x)}{h} \tag{2.1}$$

2. Finite Element (FE): is used for finding approximate solution of Partial Difference Equations (PDE) as well as of Integral Equations. The solution approach is based either on eliminating the differential equation completely or rendering the PDE into an equivalent ordinary differential equation.

By using finite difference formulation, Dengi developed a hierarchical two-dimensional field solution technique for capacitance extraction for Very Large Scale Integrated Circuit (VLSI) interconnetcs modeling [7]. He developed library element capacitance matrix macromodels that were combined at run time to produce accurate field solutions of entire interconnect cross sections. This work deals accurately

with arbitrary conductor vertical cross sections and multiple conformal and/or planarized dielectrics. It was capable of solving complex geometries typical of Integrated Circuits (IC) vertical cross sections, but limited to capacitance extraction only.

Costache developed a two dimensional (2D) FE approach to quasi-static Transverse Electro-Magnetic (TEM) analysis of shielded or open conductive strips [8]. His methodology has applications to VLSI parasitic elements of transmission line characteristics of printed circuit boards. This approach applies a Finite Element method to microstrip transmission line structures to calculate the AC resistance and reactance, taking into account the current distributions due to skin and proximity effects. AC resistance and reactance that can be used as input parameters for spice simulations are the obtained results from his work. In addition, results show an agreement with results obtained by other methods, such as Finite Fourier Transform. However, the limitation of this work is that it uses a time expensive algorithm.

Integral Equation Approaches

Integral Equation Approaches solve the integral equation instead of diferential equations. Commonly used methods include:

1. Method of Moments (MOM): Is a numerical computational method for solving linear partial differential equations wich have been formulated as integral equations. [9]
2. The boundary element method (BEM): Is an important technique for solving partial differential equations in the computational solution of engineering or scientific problems. In applying the boundary element method, only a mesh of the surfaces is required, making it easier to use and often more eficient than the finite element method.

The boundary element method is derived through the discretization of an integral equation that is mathematically equivalent to the original partial differential

equation. The essential re-formulation of the PDE that underlies the BEM consists of an integral equation that is defined on the boundary of the domain and an integral that relates the boundary solution to the solution at points in the domain. The former is termed a boundary integral equation (BIE) and the BEM is often referred to as the boundary integral equation method or boundary integral method.

Dengi developed a 2D hierarchical field solution method for capacitance extraction for VLSI interconnect modeling, based on the boundary element method [10]. From this method a capacitance matrix can be obtained for VLSI interconnects. Results from his work lead to a better trade-off between accuracy and efficiency compared to finite diference method. This work only focused on capacitance.

Analytical Equations

The use of analytical equations to approximate PCB parasitics results in faster algorithms by sacrificing some accuracy.

One concept used for inductance calculation is known as partial inductance. Partial inductance is defined as the inductance of a single conductor with respect to infinity as the reference for return current. By defining each trace segment as forming its own return loop with infinity, partial inductances are used to represent the eventual loop interactions without prior knowledge of the actual current loops.

The mutual inductance between two segments a and b, like shown in Figure 2–1, with cross sectional areas a_a and a_b, and lenghts l_a and l_b can be obtained by using the partial inductance concept in equation 2.2.

$$L_{ab} = \frac{\mu}{4\pi}\frac{1}{a_a a_b}\int_{a_a}\int_{l_a}\int_{a_b}\int_{l_b}\frac{\vec{dl_a}\cdot\vec{dl_b}}{\left|\vec{r_a}-\vec{r_b}\right|}d_{a_a}d_{a_b} \tag{2.2}$$

Paoletty discussed the limitations on the use of image theory to obtain partial inductance and added some correction terms on the image theory method to overcome these limitations[11]. In his method, he used simple filamentary images that can reduce calculation times. This work showed that it is possible to calculate

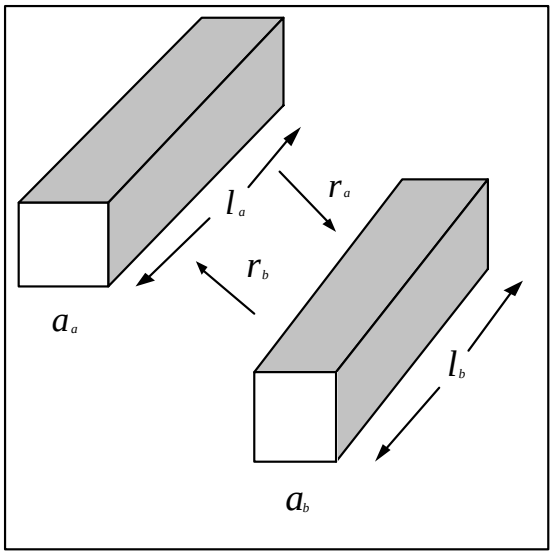


Figure 2–1: Partial Inductance Concept

partial inductance matrices with the image package when the proposed correction terms are used. It also showed that it is possible to use simple filamentary image, wich can reduce calculation time. This work is limited to inductance calculation.

Xiaoning *et al.* developed analytical formulas for quick and accurate inductance estimation [12]. The formulas presented in his work apply for traces with a length greater than its width. In this particular case, PCB traces can be approximated as filaments without losing accuracy.

Another consideration from Xiaoning work is the addition of a special frequency dependent term X, represented by a Bessel function. The resulting expression is shown in equation 2.3.

$$L_{self} = \frac{\mu_0 l}{2\pi}\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235\,(w+t)}{l} - \mu_r\,(0.25 - X)\right], \tag{2.3}$$

where l,w, and t are the segment lenght, width, and thickness, respectively. X is defined by the set of equations 2.4-2.6

$$X = \begin{cases} 0.4372x & \text{if} \quad x < 5 \\ 0.0578x + 0.1897 & \text{if} \quad .05 \leq x \leq 1 \\ 0.25 & \text{if} \quad x > 1 \end{cases} \tag{2.4}$$

$$x = \frac{\delta}{0.2235\,(w+t)} \tag{2.5}$$

$$\delta = \sqrt{\frac{1}{\omega\mu\sigma}} \tag{2.6}$$

where ω is the frequency, μ is the permeability, and σ is the conductivity.

Xiaoning's work only took into consideration the calculation of inductance for traces composed of orthogonal straight segments. It did not include the calculation of inductance for traces oriented at an angle.

Goddard made a revision of analytical and numerical methods for computing high frequency and low frequency inductance and resistance components of isolated conductors [13]. High and low frequency resistance extraction was performed by using conformal mappings for regular polygons. Equations for obtaining DC inductance of infinitely thin strips were also used. Main results from this work highlight that for rectangular conductors, high frequency and low frequency AC resistance can be obtained by using semi-analytical methods without requiring finite-element-based software. This work did not take into consideration inductance for wide traces.

2.1.4 Other Methods

Courtial-Goutaudier developed a method to evaluate the characteristics of PCBs containing magnetic films This method finds the circuit parameters R, L, and C using the finite element method in combination with the strategic dual image method [14]. Equivalent circuit parameters extraction takes into account conductive and

displacement currents. This work highlights the advantage of including magnetic material to decrease EMI in an efficient way. It is a time expensive method.

M. Xu and L. He developed a table-based model for frequency dependant on-chip inductance estimation. This model is applied to compute mutual inductances between random wires and loop inductances for cascaded wires. It is also applied to generate RLC circuit models for on-chip interconnects [15]. In their work, they proposed a normalized model that resulted appropiate for use in iterative improvement algorithms due to its simplicity. However this model is in general not applicable to non-aligned wires. The developed model only considers orthogonal structures, without making considerations for structures at an arbitrary angle.

2.2 Relevance of Previous Works

In general, previous work done on PCB layout with EMI considerations falls into one of these three general categories:

- High precision, but computational expensive
- Particular to a parasitic parameter or technology
- Do not include necessary particularities.

A summary of some of the most relevant efforts made in this area is shown in table 2–1

The developed tools show a high level of precision for PCB traces parasitic extraction. However, there is still margin for improvement because these methods are computationally expensive. This imposes a limitation in the development of automatic layout optimization tools. These tools use iterative improvement algorithms like Simulated Annealing, which evaluate thousands of possible solutions in order to find an optimal one. As a direct result, fast parasitic extraction tools are needed to make this possible.

Table 2–1: Previous work highlights

Author	Objective	Results	Limitations
Liu	Analyze EMI propagation	Predicts EMI behavior avoiding complex evaluation	Remediative method that relies on direct measurements
Xin	Layout method to reduce EMI	Emission map provides visual aid to PCB design	Only focus on capacitance
Zhang	Parasitic extraction PEEC method	Improved layout design Derive an equivalent circuit	Time consuming
Joshi	Component placement guidelines	Full set of guidelines for component placement to reduce EMI	Do not take into account routing
Schanen	Layout optimization to reduce EMI	Got geometrical constraints for layout optimization	Rectangular shapes only Technology specific
Nageswara	Knowledge base system for EMI prediction	Software prototype analyze simple PCBs find out common flaws	Limited to simple PCBs Rules database dependant
Aykut Dengi	VLSI interconnect capacitance extraction	Extract capacitance for complex geometries by finite diference	Do not include capacitance and resistance
Costache	Finite Element approach for VLSI parasitic elements	Applied to skin effect problem in conducting strips	Time expensive
Dengi	Field solution method to obtain capacitance	Better accuracy vs efficiency compared to finite diference	For capacitance only
Paoletti	Image theory to calculate partial inductance	Corrected image theory for partial inductance calculation	Applies only to inductance
Xiaoning	Analytical formulas for inductance calculation	Obtained quick inductance for whole wires	Limited to cases where cable length is greater that width
Goddard	Review of analytical formulas and numerical methods	Semi-analytical method for inductance and resistance calculations	Do not include capacitance
Cortial	Evaluate PCB parasitics containing magnetic films	Accounts for conductive and displacement currents	Time expensive

CHAPTER 3
Problem Statement

Electromagnetic Interference (EMI) is a problem of major concern in power electronics systems. This is mainly due to two reasons:

1. It limits the integration level achievable in circuit implementations: As circuit sizes are reduced, potential EMI sources get closer to susceptible components and traces, worsening their performance. This tendency imposes hard limits on the minimum distance between components.
2. It limits systems' maximum operating frequency: Higher operating frequencies imply larger levels di/dt and dv/dt being generated within a circuit. This causes high perturbances in susceptible elements, and therefore imposes a limit in the highest frequency allowed to guarantee proper system performance.

Most EMI problems in Power Electronics (PE) circuits are strongly related to the layout of their printed circuit boards (PCB). The PCB layout essentially defines the parasitic Resistance, Capacitance, and Inductance (RLC) components introduced by PCB traces, direct responsible for EMI. As a result, parasitic extraction is a key element for EMI evaluation and minimization.

The problem this research is adressing is: How to develop a fast and accurate parasitic extraction tool suitable to be used in PCB layout optimization algorithms.

Available models for parasitic extraction and simulation include: Method of Moments, Finite Element Analysis, and Partial Element Equivalent Circuit among others. These models were discussed on Chapter 2. Commercial tools such as Maxwell Q3D are based in these types of methods. Despite their accuracy, these

models are complex and time consuming, in particular when considering their application in iterative improvement approaches for EMI reduction.

Parasitic extraction methods have become of utmost importance in the development of methods aimed at improving the EMI performance of PE circuits while still in their design stage. The effectiveness of a particular RCL estimator is highly dependent on the speed and accuracy with which estimates are produced, particularly if the estimator is to be used as part of an EMI reduction tool. This work deals with the problem of obtaining a parasitic extraction tool with feasible running time and limited effect in the accuracy of the estimate.

The hypothesis of this work states that the development of a fast and accurate PCB layout parasitic extraction tool is possible with the implementation of an analytical model. In particular, breaking traces with irregular geometries into sets of maximal lenght rectilinear segments, would allow to use semi-lumped estimation techniques. This is expected to reduce the time required to analyze complex irregular geometries without a sensitive loss of accuracy in the estimates.

CHAPTER 4
OBJECTIVES

The main objective of this study is to obtain a fast and accurate parasitic extraction tool, applied to power electronics PCB's. This tool shall be able to be implemented as part of an automatic layout parasitics optimization tool. In order to achieve this, the following objectives must be met:

1. Obtain a layout representation for a given PCB. This representation shall contain the geometrical information of the PCB traces, as well as the materials used on it.
2. Identify and manage complicated geometries found on Power Electronics PCBs in such way, that analytical equations can be directly applied. Typical Power Electronics PCB traces include a combination of 45 degree bends, sharp turns, and trace width changes in their geometries. Examples of these geometric particularities found in Power Electronics PCB traces are shown in Figure 4–1.

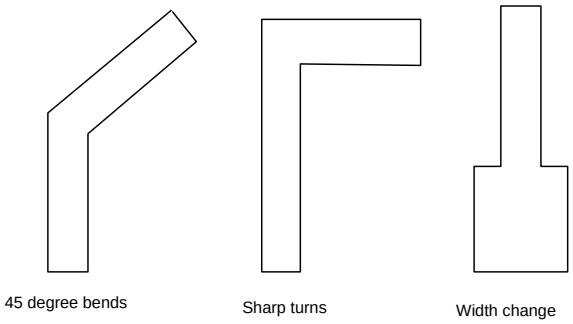


Figure 4–1: Typical PCB geometries

3. Develop a set of analytical equations for obtaining parasitic LRC parameters for simple rectilinear geometries. This objective needs to be accomplished in order to reduce computational complexity.

4. Apply obtained equations to estimate LRC parasitics for Power Electronics PCB traces.
5. Validate the extraction results by comparing the results obtained in our model with an acceptable commercial extraction tool.
6. Assess timing requirements to determine if our model is fast enough compared to available commercial extraction tools and iterative methods.

CHAPTER 5
METHODOLOGY

By following the objectives of this work as a guideline, our methodology follows the cognitive map shown in Figure 5–1. These steps are explained in datail in the following sections.

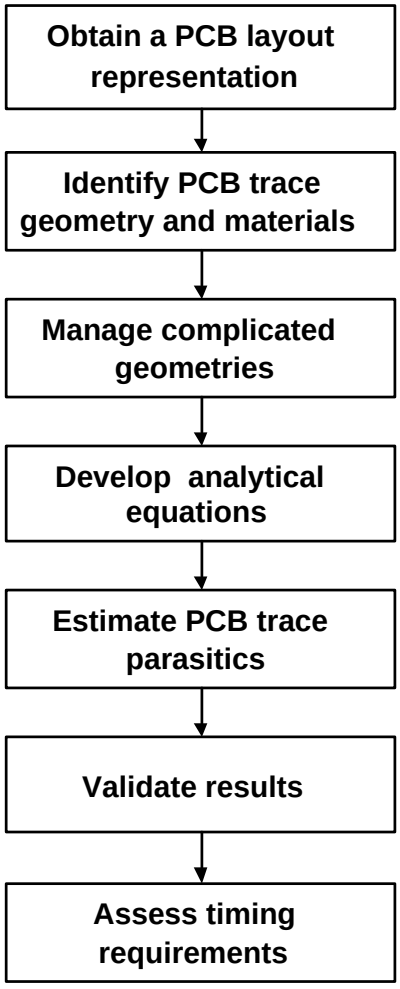


Figure 5–1: General methodology cognitive map

5.1 PCB Layout Representation

A PCB layout representation is needed in order to identify traces geometries and materials. This can be obtained in the form of a gerber file format. A gerber file is a generic layout file format used to extract the geometrical properties of a PCB. Figure 5–2 shows a two-dimensional representation of the gate driver.

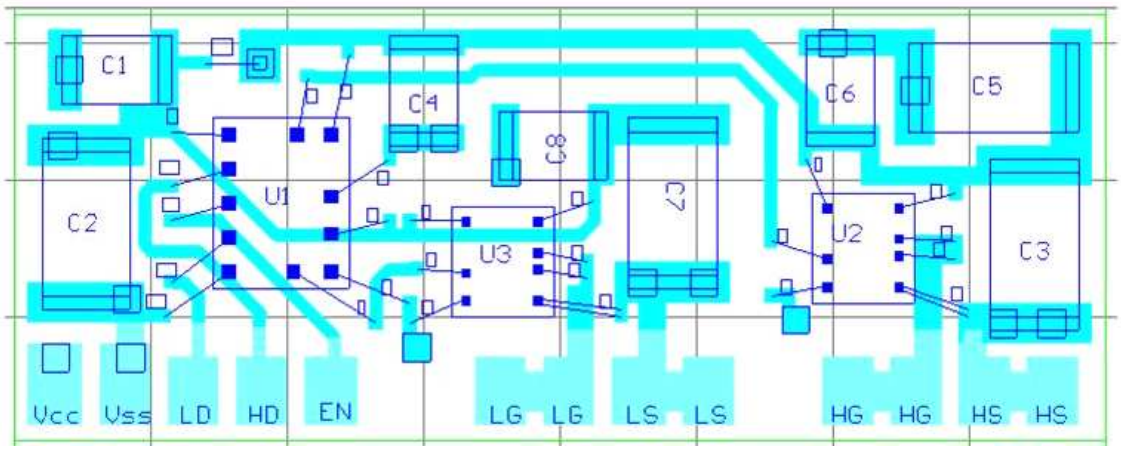


Figure 5–2: Gate Driver layout representation

5.2 Traces geometry and materials identification

PCB traces dimensions can be obtained from the gerber file. Geometrical information obtained was trace lenght l, width w, and thickness t. Material information is the following: The gate driver is composed of gold conducting paths, a silver top pad, an FR4 epoxy board, silver vias, a bottom trace, and an aluminum oxide (Al_2O_3) layer.

5.3 Manage Complicated Geometries

Analytical equations apply to simple geometries, where the rectilinear segment is the most typical case. Power Electronic PCBs geometries are more complicated than that. In order to solve this problem a trace segmentation methodology has been implemented in this work. This will be discussed next.

5.3.1 Trace Segmentation

In this step, the selected trace is divided into a set of maximal lenght straight segments ($S_1, S_2, \ldots S_N$), as shown in Figure 5–3. A maximal lenght straight segment is defined as a rectilinear segment with the maximum lenght possible. For each segment, geometrical data is obtained. This data consists of the segment length (l), thickness (t) and width (w).This segmentation scheme uses a set of straight segments with the maximum possible length, depending on trace geometry. One segmentation example is shown in Figure 5–3. In this case a new segment is obtained for each change in trace geometry: S_1 is the first segment obtained, then S_2 is obtained by a change in trace width, finally S_3 and S_4 segments are obtained with a change of direction in the trace.

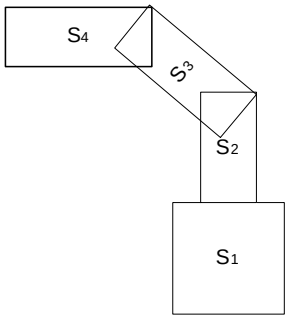


Figure 5–3: Segmented Circuit Trace

The segmentation process is repeated with all traces of the board. Once finished, a set of analytical equations needs to be obtained to find the parasitics of the obtained segments. This is discussed in the next section.

5.4 Analytical Equations Development and Trace Parasitic Extraction

A set of analytical equations needs to be developed to find parasitic parameters RLC for the PCB traces. These parameters can be calculated in parallell as shown in Figure 5–4. The next sections will explain the process for inductance, capacitance, and resistance calculation.

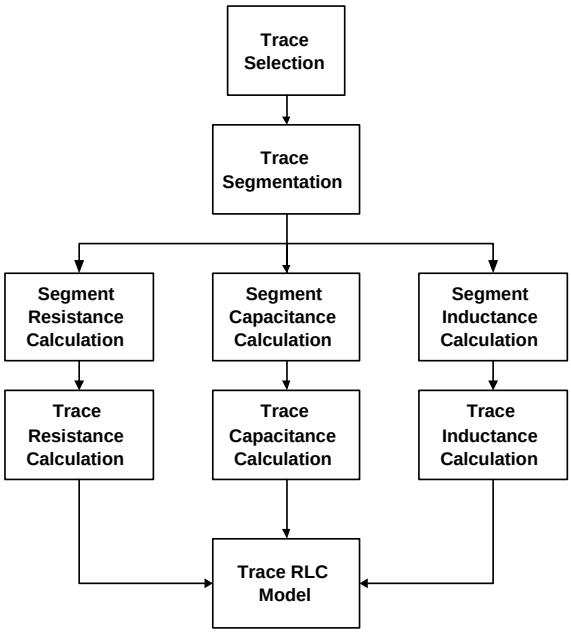


Figure 5–4: PCB parasitic extraction methodology

5.5 Inductance Calculation

The inductance calculation of a PCB trace considers the self inductance of its segments and the mutual inductance between them. This process is shown in Figure 5–5.

5.5.1 Trace Segment Self-Inductance Calculation

The self-inductance calculation for each segment is done individually. This process depends on the following condition: $l >> w + t$, where l, w, and t are the trace lenght, width, and thickness respectively. It is important to mention that l is defined by the direction of the current flow in the segment. If this condition is true by at least 5 times, the segment is classified as long, otherwise it is calssified as wide.

If the condition $l >> w+t$ is true, the self inductance of the segment is obtained with equation 5.1. This equation was obtained from Xiaoning work[12], where w, l,

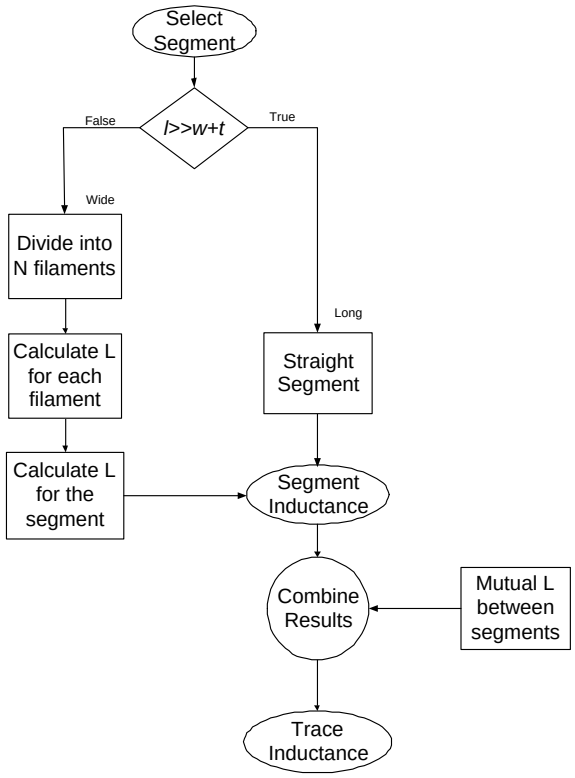


Figure 5–5: Trace inductance calculation process

and t are the segment width, length and thickness respectively, as shown in Figure 5–6.

$$L_{self} = \frac{\mu_0 l}{2\pi}\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235\,(w+t)}{l}\right] \tag{5.1}$$

Figure 5–6: Geometrical parameters of a trace segment

Wide segments do not meet the condition $l >> w + t$. In order to estimate the inductance of these segments, we propose a methodology based on Gupta's work, who uses a bi-dimensional array to find mutual inductance between two segments [16]. In our case, we used a simplified version of Gupta's model, where segments are divided into N parallel elements (making an unidimensional array) $E_1, E_2, ..., E_N$ as

shown in Figure 5–7, in such way that trace length is greater than its width by at least five times.

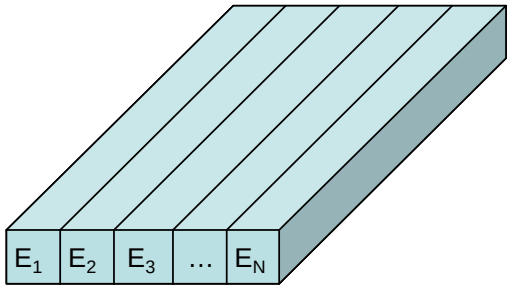


Figure 5–7: Wide segment divided into N elements

The self-inductance for each element is treated as a long segment, whose inductance is obtained with equation 5.1. Then the total self-inductance of the segment is calculated as the parallell combination of its filaments according the equation 5.2:

$$\frac{1}{L_{trace}} = \frac{l}{L_{E_1}} + \frac{l}{L_{E_2}} + \frac{l}{L_{E_3}} + ... + \frac{l}{L_{E_N}} \tag{5.2}$$

After the self-inductance of each trace segment is obtained, the mutual inductance between trace's segments is also needed.

5.5.2 Mutual Inductance Calculation Between Segments

The mutual inductance between trace's segments needs to be taken into account for estimating the self inductance of a trace. Depending on segment size, position, and orientation, the following classifications are used in order to obtain the mutual inductance for a segment pair:

- Equal and parallell.
- Unequal and overlapping.
- Oriented at an angle.

Equal and parallell segment pairs are not typically found within a trace in power electronic circuits. However this is the base case used for obtaining the other segment pair combinations. The mutual inductance of equal parallel segments, as shown in Figure 5–8, can be approximated by using equation 5.3.

Figure 5–8: Equal parallel segments

$$M = \frac{\mu_0 l}{2\pi}\left[ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}}\right) - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l}\right] \tag{5.3}$$

where l is the segment length and d is the center to center distance between segments.

Special cases for parallel segments, where segments are unequal, or there is an overlap between them are shown in Figure 5–9.

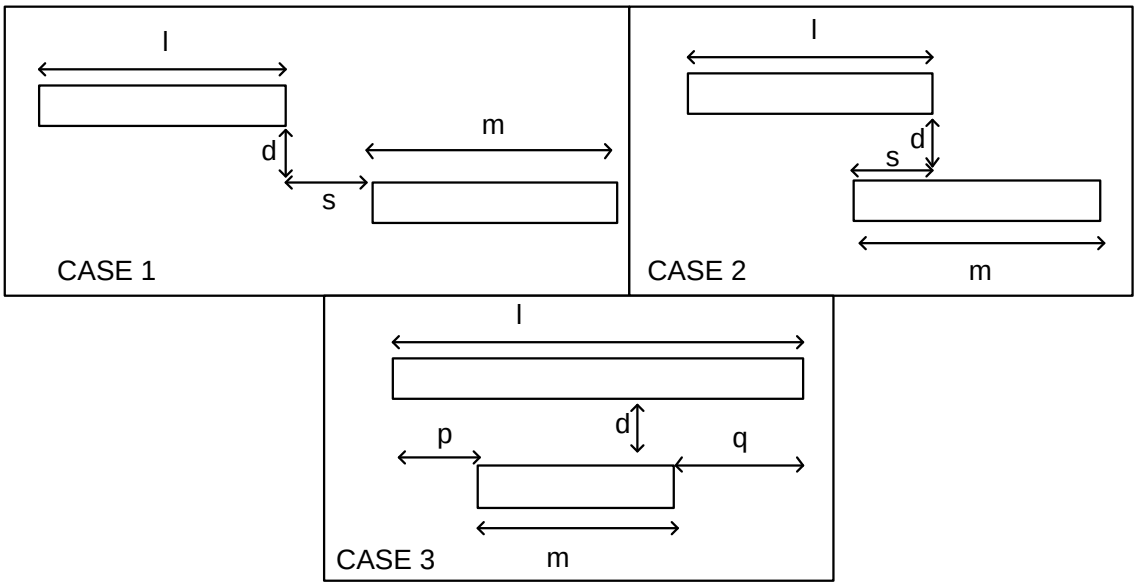


Figure 5–9: Special cases for mutual inductance calculations

Mutual inductance calculations for cases 1-3 are done with equations 5.4 to 5.6, where the subscript in the equations means finding the mutual inductance between two equal and parallel segments with a length indicated by the subscript.

$$M = \frac{1}{2}\left[(M_{l+m+s} + M_s) - (M_{l+s} + M_{m+s})\right] \qquad \text{Case1} \tag{5.4}$$

$$M = \frac{1}{2}\left[(M_{l+m-s} + M_s) - (M_{l-s} + M_{m-s})\right] \qquad \text{Case2} \tag{5.5}$$

$$M = \frac{1}{2}\left[(M_{m+p} + M_{m+q}) - (M_p + M_q)\right] \qquad \text{Case3} \tag{5.6}$$

Segments Oriented at an Angle

For traces at an angle of multiples of 45 degree, an approximation is made as shown in Figure 5–10. This approximation is done by taking the projection of the inclined segment ($l2$) above the axis of the other segment ($l1$), and rotating around its center to approximate it as parallel conductors as special case 2 in Figure 5–9.

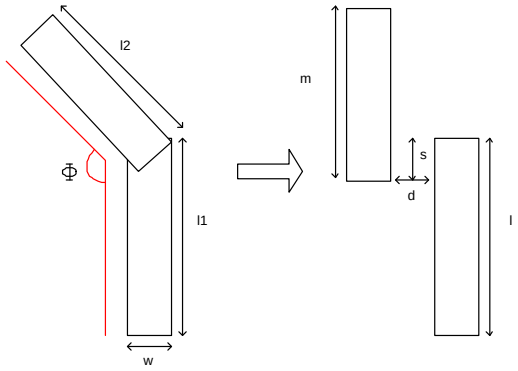


Figure 5–10: Mutual inductance approximation for segments at 45 degree angle

For a particular angle ϕ , variables in figure 5–10 are defined as: $l = l1$, $m = l2$, $d = \frac{l2}{2}cos\phi - \frac{w}{2}$, and $s = \frac{l2}{2} - \frac{l2}{2}sin\phi$

For the special case of a 45 degree angle, variables in figure 5–10 are defined as: $l = l1$, $m = l2$, $d = \frac{l2}{2\sqrt{2}} - w/2$, and $s = \frac{l2}{4}\left(2 - \sqrt{2}\right)$. This is the case most typically found in power electronics PCBs.

5.5.3 Total Trace Self-inductance Calculation

The trace inductance is obtained with the contributions of the segments self inductance and mutual inductance between segment pairs. It can be obtained with equation 5.7.

$$L_{self} = \sum_{i=1}^{N} l_i + \sum_{i=1}^{N} \sum_{j=i+1}^{N} 2k_{ij}M_{ij} \tag{5.7}$$

Where l_i is the self inductance of the i^{th} segment, M_{ij} is the mutual inductance between the i and j traces, and k_{ij} is a correction factor that depends on the orientation of the traces, that is defined with equation 5.8:

$$k_{ij} = \begin{cases} 0 & \text{if traces are orthogonal} \\ 1 & \text{if current flows in the same direction} \\ -1 & \text{if current flows in opposite directions} \end{cases} \tag{5.8}$$

This process is repeated for each trace in the circuit.

5.6 Capacitance Calculations

The segmentation scheme used for self inductance calculation can also be used to capacitance extraction. The only difference in this case is that mutual effects are not considered, and trace capacitance is obtained by the parallel combination of the segment's capacitance.

Equations 5.9 to 5.11 are used to estimate the parasitic capacitance per unit lenght of a PCB segment with width w, length l, and thickness t, over a ground plane at h distance, as shown in Figure 5–11 [17].

$$C = 2.85\epsilon_{eff} \frac{1}{ln\left\{1 + \frac{1}{2}\left(\frac{8h}{w_{eff}}\right)\left[\left(\frac{8h}{w_{eff}}\right) + \sqrt{\left(\frac{8h}{w_{eff}}\right)^2 + \pi^2}\right]\right\}} \tag{5.9}$$

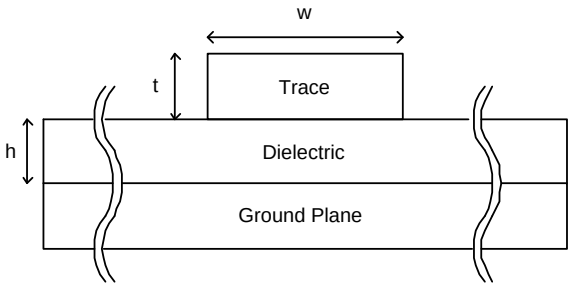


Figure 5–11: Circuit trace over ground plane

$$w_{eff} = w + \frac{t}{\pi} ln \left\{ \frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left[\frac{1}{\pi\left(\frac{w}{t}+1.10\right)}\right]^2}} \right\} \tag{5.10}$$

$$\epsilon_{eff} = \frac{\epsilon + 1}{2} + \frac{\epsilon - 1}{2} \left(1 + \frac{10h}{w}\right)^{-1/2} \tag{5.11}$$

where w_{eff} and ϵ_{eff} are the effective width and dielectric constant respectively.

These equations were adopted from Bogatin's work [17]. They are used to obtain the parasitic capacitance with respect to ground for microstrips taking in consideration fringing field effects and assumes an infinite ground plane.

5.7 Resistance Calculations

The same segmentation scheme used for inductance and capacitance extraction can also be used for resistance extraction. Due to time constraints, resistance calculation was not fully developed as part of this work. Instead, a set of guidelines for resistance calculation has been obtained as well as preliminary results obtained using the segmentation scheme with rectilinear traces.

Trace resistance estimation can be achived with the following steps:

1. Divide the trace into regions (common shapes) , for which there are equations to calculate resistance.
2. Wires that split, treat each portion as a segment and do series/parallel combinations

The basic formula for finding the resistance of a PCB trace with length l, width w, and thickness t can be obtain with equation 5.12.

$$R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right) \tag{5.12}$$

where ρ is the resistivity of the material.

Equation 5.12 applies for rectilinear traces only. This equation does not take into account the skin effect. However, for the particular case presented in this work, the trace width is too small comparable to the skin effect. As a result the skin effect can be neglected.

Commonly non-rectangular shapes are shown in figures and 5–12 [18].

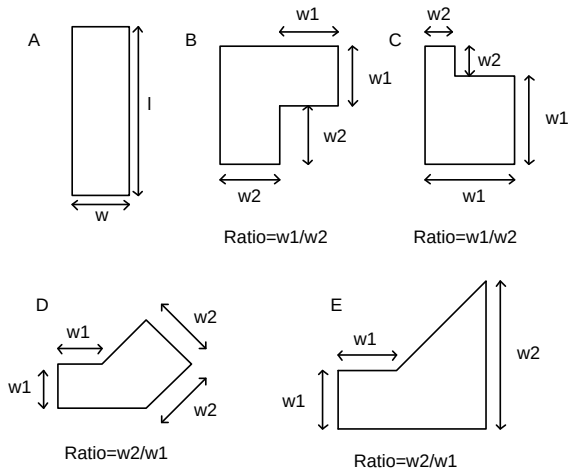


Figure 5–12: Resistance for non-rectangular shapes

The resistance for the non-rectangular shapes can be obtained by following these steps:

- Identify the non-rectangular shape as one of the cases (A,B,C,D,E) shown in figure 5–12.
- With the shape already identified, determine, by using figure 5–12, the ratio $w1/w2$, or $w2/w1$, depending on the case.
- By having the shape identified and the aspect ratio, use this information in table 5–1, and obtain the resistance value.

Table 5–1: Resistance for non-rectangular shapes

Shape	Ratio	Resistance	Shape	Ratio	Resistance
A	1	1	B	1	2.5
A	5	5	B	1.5	2.55
			B	2	2.6
			B	3	2.75
C	1.5	2.1	D	1	2.2
C	2	2.25	D	1.5	2.3
C	3	2.5	D	2	2.3
C	4	2.65	D	3	2.6
E	1.5	1.45	E	3	2.3
E	2	1.8	E	4	2.65

- Multiply the resistance value found on the table and multiply it by ρ/t, where ρ is the material resistivity and t is the trace thickness.

CHAPTER 6
RESULTS

6.1 Validation

Validation of our work is needed to determine the folowing:

- Acceptability of the results: how close are our results from reality. In other words, how good is the estimate.
- Speed advantage: how fast is our method compared to commercial tools
- How practical is our tool: is the design trade-off speed vs accuracy worth it?
- Advantages and drawbacks: on which situations our methodology applies?
- Impact of using our tool into power electronics design.

Our general validation approach is shown in Figure 6–1, where a parasitic extraction is performed to a test case board with our methodology and Maxwell Q3D parasitic extraction tool. Then, results are compared to determine if our method met its objectives.

6.2 Test Case Layout

The gate driver layout shown in Figure 6–2 was used as our case study. This is a two layer board where the top layer is used for components and traces and the bottom layer is a split power/ground plane. The board is 800 mils long by 330 mils wide. Traces are made of silver with gold pads. These pads are identified within a dotted line in Figure 6–2. In the same figure the circuit nets were identified.

6.3 Maxwell Q3D

Maxwell is the leading electromagnetic field simulation software used for the design and analysis of 3D/2D structures. Based on the Finite Element Method

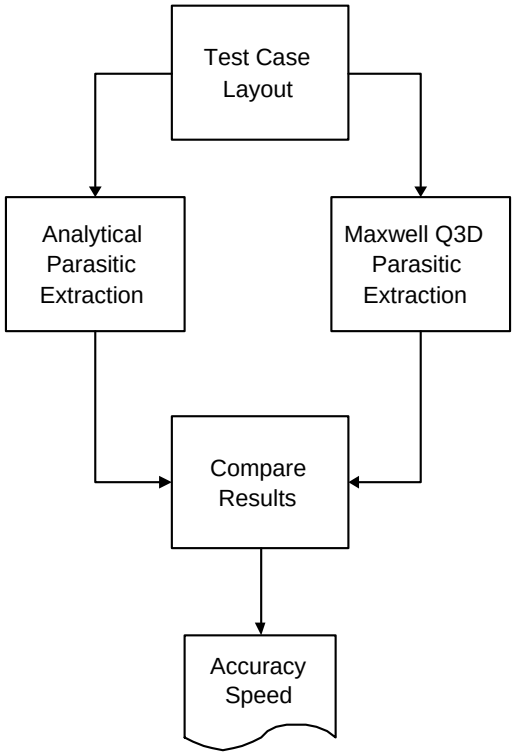


Figure 6–1: Validation flowchart

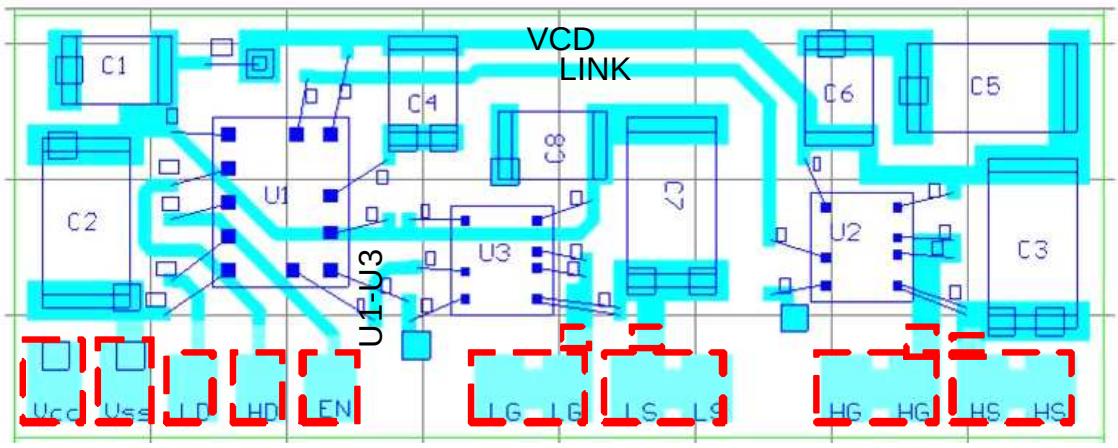


Figure 6–2: Gate Driver Layout

(FEM), Maxwell accurately solves static, frequency-domain and time-varying electromagnetic and electric fields. This tool has also been used in the past for Integrated Power Electronics Modules (IPEM), showing good agreement with simulation and measured results, where the worst case error obtained was around 10 % [19].

Maxwell Q3D uses a tri-dimensional model of the gate driver layout to make the parasitic extraction. A current direction assignment is also required by Maxwell. Figure 6–3 shows the gate driver tri-dimensional model and current assignments.

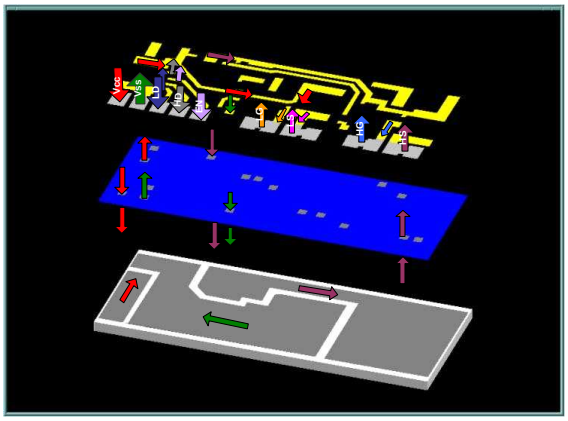


Figure 6–3: Maxwell Q3D current assignments

6.4 Analytical Parasitic Extraction

For this layout, a trace segmentation was performed for all the nets on the board. Physical dimensions (w,l, and t) for the obtained segments were stored into an Excel spreadsheet. On the same spreadsheet, parasitic extraction was performed by using our analytical equations based method.

6.5 Compare Results

The results obtained with our method were compared to a parasitic extraction, performed to the same layout, with the help of Maxwell Q3D software.Tabulated results, showing the parasitic parameters obtained with both methods, as well as the error percent between them are shown in tables 6–1, 6–2, and 6–3

6.6 Inductance Calculation Results

Table 6–1 compares Analytical vs. Maxwell results for the self-inductance of each net of the case-study layout. The first column on this table shows a list of the board traces. The second and third columns show the inductance obtained with analytical equations and Maxwell Q3d extraction respectively. The error percent values with respect to Maxwell are shown in the last column. Here, positive and negative signs denote over and underestimation of the parameters, respectively. Results show an average absolute error of 9.79%.

Table 6–1: Analytical Model Vs Maxwell Results for Calculating Self-Inductance

Trace	**Analytical (nH)**	**Maxwell (nH)**	**Error** %
EN	2.15	2.307	-7.00
HD	1.875	2.216	-15.00
HG	0.705	0.681	4.00
HS	1.146	1.01	13.48
LD	0.512	0.569	-10.0
LG	0.385	0.461	-16.42
LINK	8.641	8.352	3.46
LS	3.093	3.511	-11.93
U1-U3	0.351	0.369	-5.00
VCD	7.396	7.797	-5.15
VCC	7.483	8.935	-16.25

The top three nets that presented the highest error in our estimations were:

- HD: this trace contains high switching activity and has irregular shapes on it, inlcuding 90 degree bents.
- LG: another high switching activity net with irregular shapes
- VCC: this net connects to the ground plane on the bottom layers of our board.

In general the traces that present the highest errors are traces with high switching activities, irregular shapes, and connected to power and ground planes.

In particular the traces with the highest error percent on the inductance estimation have the following common characteristics:

- These traces are the most complicated structures in the board. Current path distribution was estimated to be across or down the segments. Details for 90 degree corners were not taken under consideration for these calculations
- Most of these traces are connected to power/ground planes through vias. The influence of the power/ground plance was neglected on this process.
- Frequency effects were not considered.

In addition it can be noticed that the results tend to overestimate for traces with high activity and sharp corners and to underestimate in signal traces with low voltage and current levels.

6.7 Capacitance Calculation Results

Table 6–2 shows the results for the capacitance estimation in the same fashion as Table 6–1. For this case the absolute average error is 5.48, due to model considerations of fringe capacitance. A possible cause of error is the effect of capacitive coupling between traces. However adding this effect to the model will add a computational difficulty that will not compensate for the accuracy gain that can be obtained.

Table 6–2: Analytical Model Vs Maxwell Results for Calculating Capacitance

Trace	**Analytical (pF)**	**Maxwell (pF)**	**Error** %
EN	7.4802	7.2236	3.55
HD	7.6698	7.7022	-0.42
HG	11.8078	12.357	-4.44
HS	49.268	53.583	-8.05
LD	4.8503	5.1961	-6.65
LINK	9.5493	8.9684	6.48
LS	62.4296	58.187	7.29
U1-U3	1.3319	1.4845	-10.28
VCD	30.7266	31.039	-1.01
VCC	27.5647	25.014	10.2
LG	10.493	10.697	-1.91

The top three nets that presented the highest error in our estimations were:

- U1-U3: this trace is surrounded with high activity traces
- VCC: this net connects to the power plane in the bottom of the board.
- HS: high activity net, with irreguar shapes and connected to the bottom floating plane.

In general the traces that present the highest error are surrounded by near traces with high switching activity. This is because the model does not include trace-to-trace capacitance.

6.8 Resistance Calculation Results

Preliminary results for resistance extraction are shown in Table 6–3.

Table 6–3: Analytical Model Vs Maxwell Results for Calculating Resistance

Trace	**Analytical** (Ω)	**Maxwell** (Ω)	**Error** %
EN	0.034617	0.033769	2.51
HD	0.036582	0.035276	3.70
HG	0.008219	0.006643	23.71
HS	0.005542	0.004807	15.29
LD	0.014006	0.011178	25.30
LG	0.006947	0.005301	31.05
LINK	0.084885	0.083589	1.55
LS	0.007392	0.006986	5.82
U1-U3	0.009096	0.008187	11.10
VCD	0.065119	0.054172	20.11
VCC	0.079297	0.071501	10.90

As with the previouscases the highest errors can be found in the traces with irregular shapes. It can be noticed that all results are over-estimating. Peak values are suspected to be caused by changes in current distribution caused by sharp corners and 45 degree corners. Our current model only consider a uniform current distribution in the traces. The use of a current distribution estimator is recomended for future developments.

6.9 Running Time

The running time is one important aspect for parasitic estimation algorithms. This is important for its application into automated parasitic minimization tools. These tools use iterative improvement algorithms like simulated annealing that evaluated thousands of solution in order to find the optimal one.

The running time for our methodology was estimated by measuring the time Excel takes to obtain the results once the data has been entered. Excel has an option that let the user to decide when to calculate the results. For this work all data has been entered manually, then by the push of a button Excel calculate the results.

In terms of running time, a Maxwell extraction for our test case took over 12 hours to complete, while our analytical model was able to complete the same layout in approximate 0.5s. A strict time complexity analysis of both methods is recommended if a more accurate measure of speed-up is desired. However, this simple assesment highligts speed-up advantage of our method when compared to traditional finite element analysis methods. The same speed advantage would impact on EMI estimation and reduction algorithms that could use them.

6.10 Relevance of Results

In order to assess the impact of the expected reductions a series of manual transformations were performed to the layout of the gate driver under study. The original and the modified layout are shown in figure 6–4. The changes were made to reduce the parasitics of the trace that provides the VCC connection to the circuit components. The inductance of this trace was significantly reduced by 50 percent. This significant reduction is also expected when using an automated tool developed with our method.

Figure 6–5 shows a spice simulation that was performed to both layouts at 40kHz to show the effects on EMI for the modifications done. Results show a

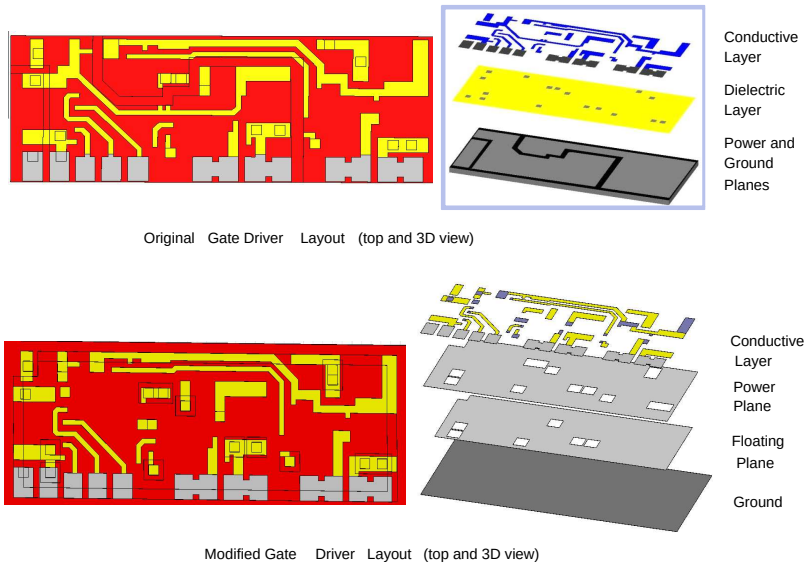


Figure 6–4: Gate driver layout changes

minimization on the voltage spikes and a reduction of the RMS up to 41 percent in the RMS noise on the trace with more activity on the circuit.

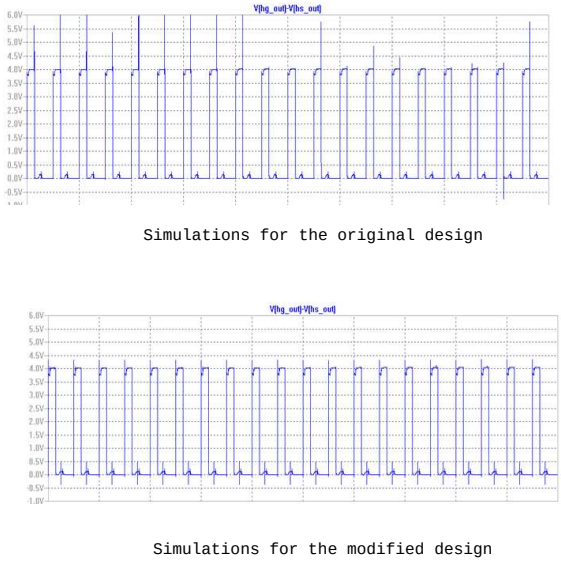


Figure 6–5: Gate Driver Modification Results

6.11 Assumptions and Limitations

The applicability of our methods asumes a planarity requirement. Planarity requirement asumes that all the traces are in the same layer. Layer that connects to power and ground plannes present high error in the estimates. This method applies to boards where traces are located on the top level of the board. It is not intended

to multilayer designs with various signal layers in between. However most of power electronics circuits boards met our planarity requirement.

In order to produce faster results our methodology divides irregular shapes into rectangular ones and uses a semi-lumped approach to make calculations. This method sacrifices some accuracy, however the speed gain advantage compensates the loos of accuracy by letting us to use this method into automated layout tools that focus on parasitic reduction.

CHAPTER 7
CONCLUSION

An analytical model to estimate trace inductance, and capacitance for power electronics PCBs has been presented. Guidelines for resistance estimation were presented as well. This model was based on semi-lumped elements, using the concept of maximal lenght straight segments. This approach provides a good compromise between computational speed and accuracy. Our segmentation model efficiently managed complicated geometries in order to use analytical equations.

Preliminary results indicates huge reductions in running time, while still providing estimates with an acceptable level of accuracy. These results, highlight the suitability of our method for use in iterative EMI reduction tools. Despite these good results, our work also creates opportunities for further research in two main aspects: extraction results for this work can be improved while still maintaining our speed requirements.

The fast estimation method developed as part of this work have a significant impact on Power Electronics PCB design process. PCB traces that may present EMI issues on the assembled board can be identified during early design stages. While still at this stage, RLC parasitics on these lines can be significantly reduced with a fast layout optimization tool. As a direct result, design efforts on remediative actions (like shielding, filtering, and possible re-design) can be minimized as early as the design stage of the board. For the manufacturing industry this results in huge reductions in time and money.

Future work in this project include:

1. Estimation of trace-to-trace capacitance. Including trace-to-trace capacitance is expected to reduce the errors on capacitance calculation. However this may add a computational complexity that may not compensate for the accuracy gained.
2. Calculating plane effects on inductance. The traces that presented the highest errors on the inductance estimation were connected to power and ground planes. The effect of them on inductance resutls need to be considered in future works. Adding the power and ground plane effects can make this work applicable to more complicated PCB designs.
3. Implementation of a current distribution estimator. The error on resistance calculation increases due to non-uniform current distribution on traces that presents bends or 45 degree angle turns.
4. Cosiderate the effect of segmentation order in the methodology. The segmentation order may affect the results in areas where the current distribution is not uniform. Considering this effect may have a positive impact on the accuracy obtained.

REFERENCES

[1] D.H. Liu, J.G Jiang, and Z.M. Zhao. A systematic approach to analyze EMI in control circuit of power electronic equipment. *Applied Power Electronics Conference and Exposition*, Vol. 1:208 – 212, 2001.

[2] W. Xin, C.M. Lee, M.H. Pong, and Z.M. Qian. A novel approach base on electric field analysis to reduce crosstalk problem on PCB. *IEEE PESC*, 1999.

[3] W. Zhang, M.T. Zhang, and F.C. Lee. Conducted EMI analysis of a boost PFC circuit. *Twelfth Annual Applied Power Electronics and Conference Exposition APEC*, Vol 1:223–229, Feb 1997.

[4] M. Joshi and V.Agarwal. Component placement for improved EMI performance in power electronic circuits. *IEEE APEC'98*, pages 911–917, 1998.

[5] J.-L. Schanen, L. Jourdan, and J. Roudet. Layout optimization to reduce EMI of a switched mode power supply. *IEEE 33rd annual Power Electronics Specialist Conference*, 4(23-27):2021–2026, June 2002.

[6] K. Nagesware Rao and P.V. Ramana. EMC analysis in PCB designs using an expert system. *International Conference on EMI and EMC*, pages 59–62, 1995.

[7] R. Dengi, E. Rohrer. Hierarchical 2-d field solution for capacitance extraction for VLSI interconnect modeling. *Proceedings 34th ACM/IEEE Design Automation Conference*, pages 127–132, 1997.

[8] C. Costache. Finite element method applied to skin effect problems in strip transmission lines. *IEEE Transactions on Microwave Theory Tech*, MTT-35:1009–1013, 1987.

[9] R. Mantz J. Sarkar T. Cao, W. Harrington. Multiconductor transmission lines in multiple dielectric media. *IEEE Transactions on Microwave Theory Tech*, MTT-32:439–450, 1984.

[10] R. Dengi, E. Rohrer. Boundary element method macromodels for 2-d hierarchical capacitance extraction. *Proceedings 35th ACM/IEEE Design Automation Conference*, pages 218–223, 1998.

[11] O. Wada U. Paoletti, T. Hisakado. On the extension of the image theory to partial inductance calculation. *Electrical Design of Advanced Packaging and Systems Symposium*, pages 151–154, 2008.

[12] Gaoefeng Wang Zhiping Yu Xiaoning Qi and Robert W. Dutton. Onchip inductance modeling and rlc extraction of vlsi interconnects for circuit simulation. *IEEE 2000 Custom Integrated Circuits Conference*, page 487490, 2000.

[13] A.A.Roy K.F.Goddard and J.K.Sykulski. Inductance and resistance calculations for isolated conductors. *IEEE Proceedings Sci. Measurement and Technology Vol. 152, No 1*, pages 7–14, 2005.

[14] F. Cortial-Goutaudier, S. Hoshino, M. Iwanami, H. Tohya, and Y. Saito. Characterization of printed circuit boards including magnetic film using finite element analysis. *International Symposium on Electromagnetic Compatibility*, pages 13–16, May 1999.

[15] M.Xu and L.He. An efficient model for frequency-dependent on-chip inductance. *GLSVLSI*, 2001.

[16] A. Gupta. *Inductor Geometries and inductance calculations for power transfer in biomedical implants*. Master's Thesis, North Carolina State University, 2003.

[17] E. Bogatin. Design rules for microstrip capacitance. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, pages 253–259, 1988.

[18] N. Weste and K. Eshraghian. *Principles of CMOS VLSI Design, 2nd. Edition*. Addison Wesley, 1993.

[19] D.Boroyevich G.Odendaal J.Chen, L.Yang. Modeling and measurements of parasitic parameters for integrated power electronics modules. *Nineteenth Annual Applied Power Electronics Conference Vol 1*, pages 522–525, 2004.