

**A Switched Opamp Comparator to
Improve the Conversion Rate of Low-Power Low-Voltage
Successive Approximation ADCs**

By

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ABSTRACT

The continued drive toward technology scaling in VLSI design has provided greater integration levels in silicon chips. Thanks to the reduction in minimum feature size and the corresponding decrease in power supply voltage, digital circuits have benefited from savings in area and power consumption. This approach presents a number of challenges in Complementary Metal-Oxide Semiconductor (CMOS) analog circuit design. As the gate oxide of transistors becomes thinner and power consumption increases, a lower supply voltage must be used, even though it results in performance degradation of analog circuits. This must be done in order to avoid silicon punch-through. In applications requiring low power consumption and moderate conversion speed, one of the most frequently used analog-to-digital converter (ADC) architectures is the successive approximation. As data converters are mixed-signal circuits, containing both analog and digital circuits, they suffer from the same problems just described. This thesis presents the design of a low-voltage successive approximation ADC based on a Switched Opamp comparator. The proposed comparator architecture provides high-resolution and low-power consumption without compromising speed. The results obtained from extensive simulations have validated the design of the ADC prototype, showing comparable performance to those found in recent publications, while achieving a higher conversion speed.

RESUMEN

El impulso continuo hacia la reducción del tamaño mínimo ofrecido en tecnologías VLSI ha brindado mayores niveles de integración en dispositivos de silicio. La reducción en el tamaño mínimo realizable y la disminución de la fuente de alimentación de voltaje, ha resultado en menor área ocupada y consumo de energía. Esto ha traído un gran número de desafíos en el diseño de circuitos analógicos de tipo CMOS. Según la capa de óxido de los transistores se hace más angosta y el consumo de energía aumenta, surge la necesidad de utilizar fuentes de alimentación de menor voltaje. Aunque hacer esto resulta en menor rendimiento para los circuitos analógicos, es necesario para así evitar el efecto de “silicon punch-through”. En aplicaciones que requieren bajo consumo de potencia y moderada velocidad de conversión, el convertidor analógico digital (ADC) de aproximación sucesiva es uno de los más usados. Ya que los convertidores de datos son circuitos de señal-mixta que utilizan circuitos analógicos y digitales, los mismos sufren de los problemas antes mencionados. Esta tesis presenta el diseño de un ADC de aproximación sucesiva para bajo voltage, basado en un comparador con amplificador operacional conmutable. La arquitectura propuesta para el comparador provee alta resolución y bajo consumo de potencia, sin comprometer su velocidad. Los resultados obtenidos a través de simulaciones validan el diseño del ADC, demostrando rendimiento comparable con el que se puede encontrar en la literatura reciente, proveyendo a la vez mayor velocidad de conversión.

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DEDICATION

To my parents Carlos A. Vega and Nélica de la Cruz, for all their support and unconditional love through out my college studies. To my brother Christian and my sister Carla, for they were my inspiration that make my work harder into achieving my goals. To the rest of my family, for their continued support and for always believing in me and what I do.

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CHAPTER 1

Introduction

The continued increase in the integration level of VLSI technologies gives designers the ability to add greater functionality to a silicon chip. The savings in area and power consumption obtained in digital circuits are the result of a reduction in minimum feature size and the reduction in power supply associated with the reliability issues introduced by silicon punch-through effects.

Signal processing systems are the combination of a number of mixed-signal circuits requiring both analog and digital domain functions. To change from one domain to the other, analog-to-digital (A/D) and digital-to-analog (D/A) converters are used. System on a chip (SoC) solutions require that analog and digital circuits reside on the same chip. As the boundary between these two domains is moved closer to the real world, which is analog in nature, the required performance and conversion rates of A/D converters becomes more stringent. The reason for this is the limited voltage headroom available for the converter's analog circuit components to do signal processing. Furthermore, computer-aided-design (CAD) tools for analog circuits have not reach the maturity of those used for digital circuits. As a result, there is a bottleneck in the design cycle that prolongs the time-to-market of the system. Consequently, the design of analog circuits becomes one of the most critical design aspects of SoC

design.

The focus of this research is the performance improvement of low-voltage analog-to-digital converters (ADCs). The reduced supply voltage used in SoC solutions degrades the performance of the analog circuits components present in the latter. The design of these system components is a current challenge that will increase in difficulty as new technology processes become available. Portable battery-operated equipment, such as those used in data acquisition and microcontroller applications, is an example of a SoC design. One of its main requirements is low power consumption in order to prolong battery life. In these applications, low-to medium resolution and low-to-medium speed are typical requirements for data processing. The flexibility for tradeoffs of speed, power, and resolution, makes the successive approximation ADC one of the most frequently used in applications with such requirements. The minimal number of active components needed by the architecture makes it one of the best choices for low-power applications demanding no compromise in conversion speed.

To alleviate the problem associated with low-voltage operation new techniques are needed at the architectural and circuit level. As the voltage continues to be scaled down and analog circuits are pushed to their operational limits, new circuit structures are required that make optimal use of the available voltage headroom. The main issues in low-voltage circuit design are the insufficient gate-overdrive of switches, sampling linearity and SNR degradation due to limited input/output swings, and the increase in power consumption in the analog circuit components. The low-voltage issues addressed in this work include those related to the switch gate-overdrive problem, which is one of the major limiting factors in achieving optimal circuit speed and linearity.

The main goal of this thesis is to search for and develop techniques at the architectural and circuit level that would aid in the design of low-voltage low-power

data converters, such as the successive approximation ADC. Particular emphasis has been given to the comparator, the main active analog circuit component present in successive approximation ADCs. These comparators requires high-resolution and moderate-speed, without consuming large amounts of power. The best approach to achieve such requirements is to employ an architecture which contains a preamplifier stage and a latch stage. As these stages must be activated in different clock phases, the use of switches becomes unavoidable. The limited gate-overdrive present in switches, results in speed degradation due to their high on-resistance. This brings the challenging task of designing comparators which make a minimal use of switches while maximizing their gate-overdrive voltage.

The rest of the chapters are organized as follows:

Chapter 2 introduces the topic of data conversion and discusses the performance parameters that characterize an ADC. This knowledge will provide a better understanding of the tradeoffs made when comparing the different ADC architectures available.

Chapter 3 presents in more detail the issues associated with the design of the most frequently used ADC circuit blocks, namely, S/H circuits, D/A converters, and comparators.

Chapter 4 discusses different low-voltage circuit techniques, as applied to successive approximation ADCs found in the literature. Most of these techniques, generally, can be applied to other ADC architectures.

Chapter 5 presents the circuit components used in the design of a successive approximation ADC prototype. It is based on a number of existing low-voltage components and a new comparator architecture proposed in this work. The performance specifications, as obtained from Spice simulations, are presented to validate the design.

Chapter 6 presents the ADC characterization results as obtained from Spice simulations and subsequent calculations made from Matlab scripts.

Chapter 7 draws conclusions on the research topic and highlights areas where improvement is possible, which suggests opportunities for further research.

CHAPTER 2

Principles of Data Conversion

Data conversion is an essential aspect of any signal processing system. It can be divided into two parts: analog-to-digital (A/D) and digital-to-analog (D/A) conversion. A basic diagram illustrating how these form part of a signal processing system is shown in Figure 2.1.

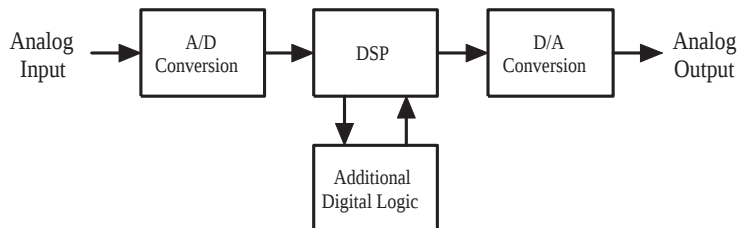


Figure 2.1. Block diagram of a signal processing system.

An analog input signal is sensed from the “outside world” (i.e., voice) and processed by the analog-to-digital converter (ADC). The analog input is a signal defined over a continuous amplitude and time range. The ADC takes the analog signal and gives a digital representation which is defined over a finite set of values in amplitude and time. Once the input is in digital form, the data can be processed by the digital-signal processor (DSP). Depending on the application, additional digital logic might be interfaced to the DSP to provide extra processing functions to the system. After

the data is processed, it is converted back into analog form by the digital-to-analog converter (DAC).

This chapter gives first a general overview of ADCs along with their main characterization parameters. It follows with a brief description of different types of ADC architectures. Particular attention is paid to Nyquist-rate converters such as *successive approximation* ADCs. Finally, a comparison is made among the more popular ADCs in industry for low-power applications. The advantages and disadvantages of each one are highlighted. They are categorized according to power, speed, and resolution requirements.

2.1 Analog-to-Digital Converters

2.1.1 General Considerations

The main function of an ADC is to approximate a continuous-time continuous-amplitude (analog) signal into a discrete-time discrete-amplitude (digital) signal [1, 3, 14]. With the aid of Figure 2.2, the conversion process of an ADC will be discussed next.

The conversion process begins by first conditioning the input signal with an anti-aliasing filter. The purpose of this filter is to limit the signal's bandwidth to no more than half the sampling frequency, to comply with the *Nyquist criterion*. This is necessary in order to prevent aliasing of the frequency spectra. The sample-and-hold (S/H) circuit is responsible of converting the input signal from a continuous-time domain into one of discrete-time. This is done by sampling the analog signal at specific time intervals. The conversion process ends at the quantizer's output, where the digital signal is produced by converting the continuous-amplitude discrete-

time signal into a discrete-amplitude discrete-time signal. The number of bits that represent the digital signal depends on the resolution of the converter.

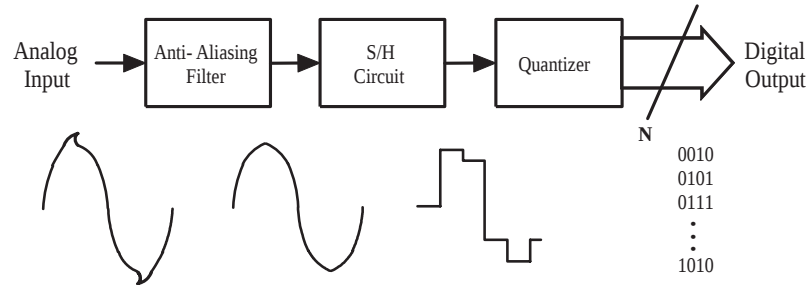


Figure 2.2. Analog-to-digital conversion system.

Figure 2.3 shows the input/output characteristics of a 3-bit ADC. To approximate the sampled signal into a digital code, the ADC fractions a reference voltage into a set of quantization levels and selects the one closest to the sampled signal as the digital output code. This difference between the input signal and the output code is called *quantization error*, e_q . There will be a region of input voltages that will be mapped into the same output code, because of the minimum step change or accuracy necessary to produce a transition from one output code to another.

It has just been illustrated that even an ideal converter introduces errors in the conversion process. Yet, real ADCs exhibit other type of errors that arise due to the non-ideal effects present in its internal components. How the quantization error can be reduced and how the non-ideal errors affect the performance of the converter will be discussed in the following section.

2.1.2 Performance Metrics

The following is an introduction to the main parameters that characterize the performance of an ADC. These parameters are limited by the performance of the

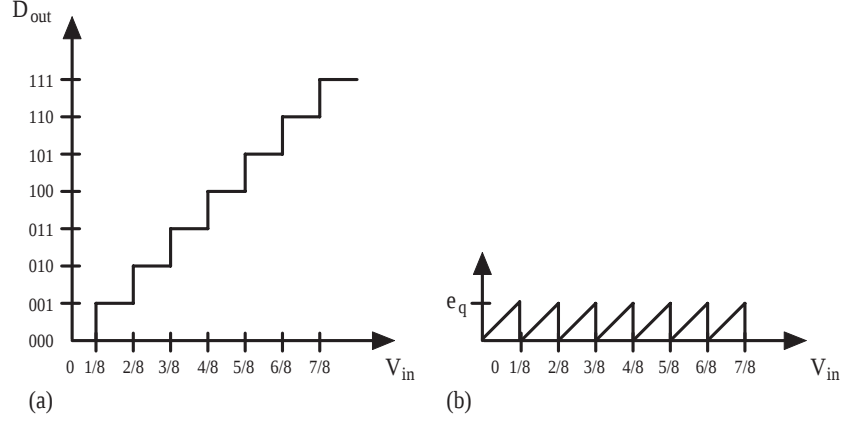


Figure 2.3. (a) Transfer characteristic and (b) quantization error of an ADC.

ADC circuit blocks. As such, the discussion presented here is general. Chapter 3 presents in more detail the operation of these circuit blocks and how they influence the operation of an ADC.

Static Parameters

The *resolution* is the minimum input voltage required to produce a transition between two of the 2^N possible output codes of the ADC. The incremental difference between adjacent codes is defined in terms of the least-significant-bit (LSB) by the following equation

$$LSB = V_{ref}/2^N \quad (2.1)$$

In Eq. (2.1) V_{ref} is the reference voltage used by the ADC and N is the number of bits present in the output code. It can be seen that by increasing N , and hence the resolution, the number of quantization levels increases. Since the sampled input signal has more digital codes into which it can be mapped, the amount of quantization error will decrease.

In an ideal ADC an input voltage of zero produces a “zero code” at the output.

Due to the limited matching of the internal components of circuits such as operational amplifiers (op amps), real ADCs need certain amount of input voltage in order to produce a “zero code” at the output. The difference between the ideal and actual input voltage needed results in a digital *offset error* at the output. This is illustrated in Figure 2.4(a) for a 3-bit ADC.

The *gain error*, illustrated in Figure 2.4(b), is the difference in slopes between the actual transfer characteristic of an ADC and that of an ideal one.

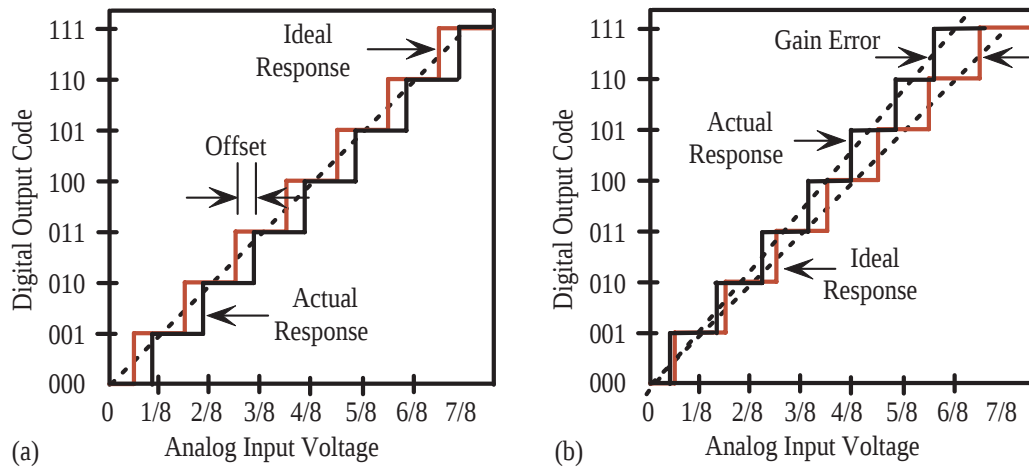


Figure 2.4. (a) Offset and (b) gain errors in a 3-bit ADC.

The *Differential Non-Linearity* (DNL) error is the difference between the actual input step and the ideal step of 1 LSB. This is illustrated in Figure 2.5(a). For an actual input of 1 LSB this means that the DNL would be zero. For example, a DNL of -1 LSB means that for a 1 LSB input signal increase the ADC output remained with the same digital code or skipped the corresponding one. The *Integral Non-Linearity* (INL) error is illustrated in Figure 2.5(b). It represents the difference between the actual input transition and that of an ideal converter.

For an ADC with no significant DNL and INL errors (i.e., ± 0.5 LSB), the input/output characteristics shows that for an increase in the input signal, the digital output code will increase accordingly. This characteristic of an ADC is referred to

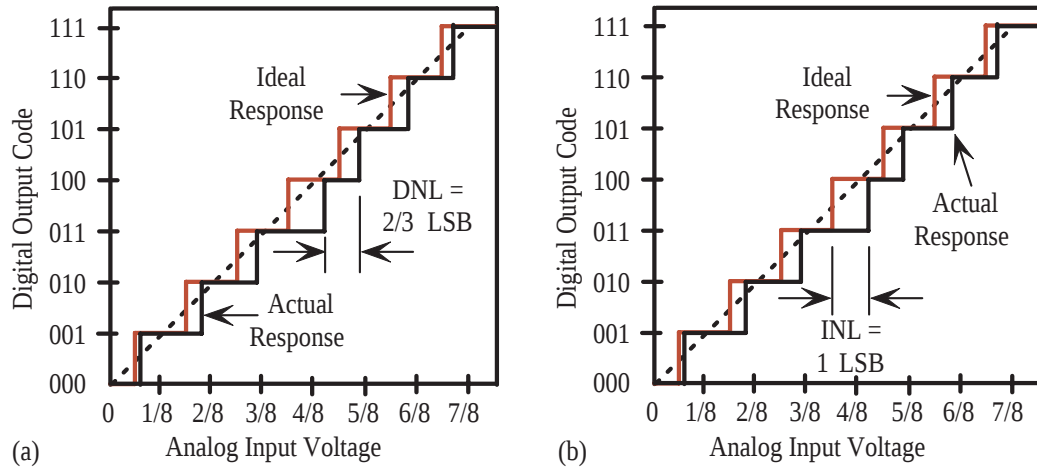


Figure 2.5. (a) DNL and (b) INL errors in a 3-bit ADC.

as *monotonicity*. Figure 2.6 shows nonmonotonic behavior in an ADC during the transition from 101 to 110 in the output code.

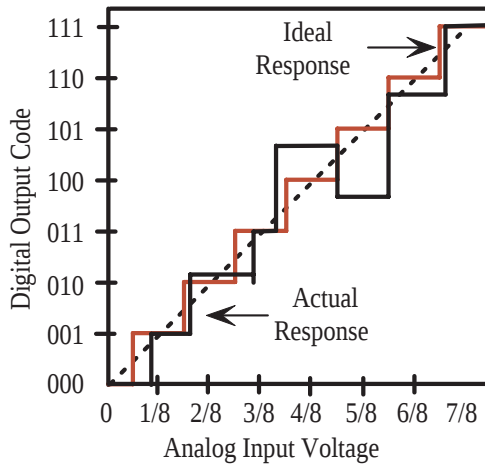


Figure 2.6. Nonmonotonic behavior in an ADC.

Dynamic Parameters

Among the dynamic parameters, the *dynamic range* can be specified as the ratio of the full-scale input signal to the smallest signal that can be detected by the converter. Measured in decibels, it is the difference between the power of a full-scale input to the power of the smallest input signal that can be detected.

The *signal-to-noise ratio* (SNR) is the ratio of the full-scale input signal to the total noise (including quantization) presented at the output. For an N-bit ADC, it is described by the following equation

$$SNR = 6.02N + 1.76 \text{ dB} \quad (2.2)$$

A figure-of-merit (FOM) often used to compare the performance of different types of converters is the *effective number of bits* (ENOB). Since it includes all other errors it is one of the most frequently used methods of assessing the performance of an ADC.

$$ENOB = \frac{SNR_{actual} - 1.76}{6.02} \quad (2.3)$$

2.2 ADC Architectures

In chapter 3 the most important circuit blocks of an ADC are presented in detail, namely the S/H circuit, the DAC, and the comparator. Here the discussion is focused toward explaining the general operation principle behind some of the most popular ADC architectures, highlighting the advantages and disadvantages that each one possesses.

2.2.1 Flash ADC

The flash ADC is the fastest architecture available because it performs the conversion in parallel form. A block diagram illustrating this architecture is shown in Figure 2.7. A string consisting of equally-valued resistors is used to generate 2^N voltage references. The comparators use these references to compare against the input signal. All those comparators whose reference voltage is lower than the input voltage

will generate a “1” at its output while the remaining comparators on top will generate a “0” at its output. The set of comparator outputs produce a thermometer code that is converted into binary form by the decoder.

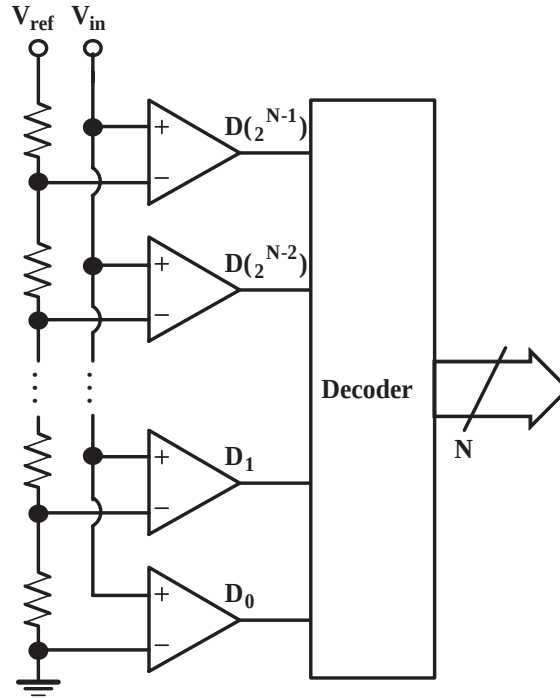


Figure 2.7. Block diagram of a Flash ADC.

By using comparators composed of a preamplifier and a latch (refer to section 3.3.2) an inherent sampling function is achieved. The preamplifier tracks the analog input for a specified amount of time, then the latch is strobed and the input difference is stored in the latch. The absence of an explicit S/H circuit is another reason why this architecture achieves a high conversion rate.

One obvious disadvantage of this architecture is the large area and power consumption required, due to the exponential growth (2^N) of comparators as the resolution is increased. The large input capacitance presented by the comparators at the input can affect the performance of the previous circuit connected to it. The latch strobing starts a regeneration process in which the differential input is being resolved. The

time at which the latch is strobed must not overlap with the preamplification phase, otherwise the resulting *kickback noise* can be reflected to the input and affect the conversion. The lack of a front-end S/H circuit can result in different sampling points among comparators, ultimately leading to distortion in the sampled signal.

2.2.2 Two-Step ADC

The two-step architecture resulted from the need to provide high-resolution high-speed analog-to-digital conversion without the increase in power and area. A block diagram of a two-step ADC is shown in Figure 2.8. By reducing the number of parallel stages and hence the number of comparators required, this architecture reduces silicon area and power consumption. However, it comes at the cost of some speed loss.

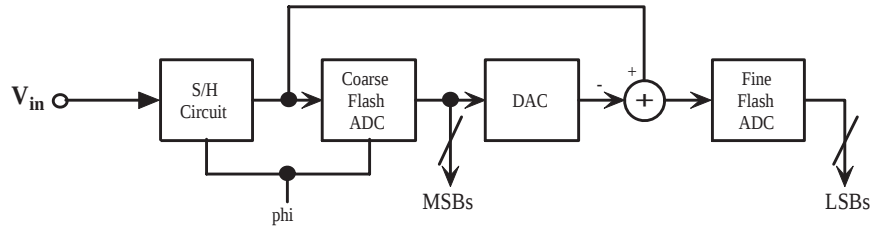


Figure 2.8. Block diagram of a Two-Step (flash) ADC.

The conversion procedure begins by sampling the analog input with a S/H circuit. Once the sampled signal has settled to within ± 0.5 LSB of its final value, the coarse ADC makes a rough approximation of the sampled signal. The latter represents the MSBs of the digital output code. The DAC converts the coarse digital approximation into analog form so that it is subtracted from the original sampled signal at the S/H circuit's output. The difference between the two signals is sent to the fine ADC to produce a high-precision conversion that represents the LSBs or remaining bits of the digital output code.

One of the most critical components needed in this architecture is the S/H circuit. Due to the settling time imposed by the DAC, the subtraction cannot begin until the sampled signal has reached the required degree of accuracy. Moreover, in order to relax the resolution requirements of the fine ADC an amplifier is placed at the output of the subtractor. However, the delay associated with the linear response of the amplifier and its nonlinear effects must be taken into account during the design process.

2.2.3 Pipeline ADC

The concept of *pipelining*, popular in digital circuits and microprocessors, consists of performing a number of operations serially in order to obtain a higher data throughput. The idea of using pipelining for analog-to-digital (A/D) conversion came after realizing that in a two-step ADC four operations were carried out, namely coarse A/D conversion, D/A conversion, subtraction, and fine A/D conversion. However, not all operations were performed at the same time since the fine A/D conversion could not be done until after the S/H circuit's output had settled properly. Pipelining in ADCs makes use of analog preprocessing in order to execute all these operations concurrently for different input samples.

A block diagram of a pipeline ADC is illustrated in Figure 2.9. It consists of N stages, each producing a digital output of k bits. The last stage is usually a flash ADC of j bits. The total resolution of the ADC is given by the sum of the bits of the stages. The operation of each stage starts by first sampling the analog output of the previous stage (for the first stage the sampling is done on the input of the converter). The k -bit ADC makes a coarse conversion which is converted back to analog by a k -bit DAC. The subtractor then generates a residue corresponding to the difference between the sampled signal and the approximation of the sampled signal.

The residue is then amplified by 2^k and sent to the next stage in the pipeline. Using digital correction techniques the digital output of all the stages are added to produce the digital output of the ADC.

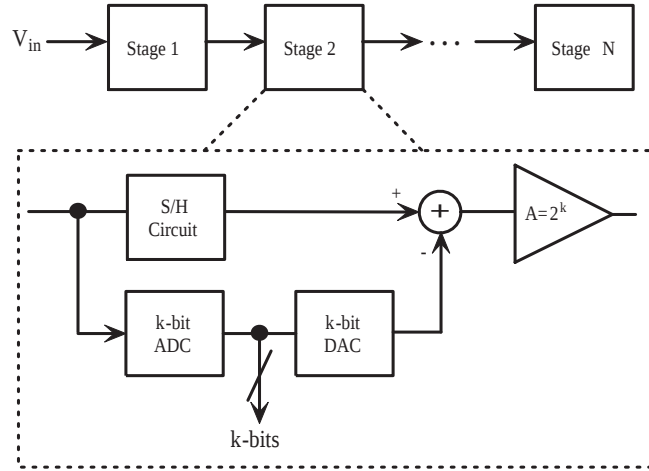


Figure 2.9. Block diagram of a Pipeline ADC.

Due to the extensive use of analog preprocessing, the speed is limited by the S/H circuits and the op amps used for residue amplification. The precision required by these two blocks depends on the number of bits remaining to be resolved at each stage. This means that the first stage in the pipeline demands the greatest precision, requiring high-gain op amps with as large as possible bandwidth. The main advantage of this architecture is its reduced area and power consumption when compared to flash configurations.

2.2.4 Successive Approximation ADC

The Successive Approximation (SAR) ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and digital logic. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine

the value of each bit in a sequential or successive manner based on the outcome of the comparison between the outputs of the S/H circuit and DAC. Figure 2.10 illustrates a block diagram of the converter.

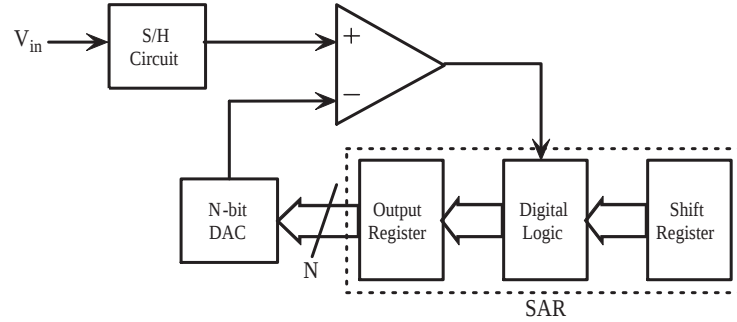


Figure 2.10. Block diagram of a Successive Approximation ADC.

The conversion sequence starts at the S/H circuit, where the analog input signal is converted from the continuous-time domain into the discrete-time domain. The digital logic then sets the Most-Significant-Bit (MSB) to '1'. With the remaining bits set to '0', the digital word produced corresponds to the midscale of the reference voltage, V_{ref} . The digital word is applied to the DAC in order to produce an analog output voltage that, once settled within $\frac{1}{2}$ LSB of accuracy, is compared with the sampled voltage by the comparator. A comparator output of '1' means that the sampled signal is larger than the DAC's output. If this is the case the MSB remains as '1', otherwise, it is set to '0'. The process is repeated by setting the next bit of the digital word to '1' and applying the digital word to the DAC for comparison of its output signal with that of the S/H circuit. Just as before, depending on the outcome of the comparison the bit either remains as '1' or is set to '0'. The comparison cycle will continue until all bits have been successively determined.

Figure 2.11 illustrates how the output of the DAC changes as it is compared with the sampled signal, V_{in} . For an N-bit SAR ADC, it takes N cycles to determine the digital value corresponding to that of the sampled signal. Moreover, the precision

required by the comparator increases as the converter goes from the MSB to the LSB in the approximation algorithm of the output code.

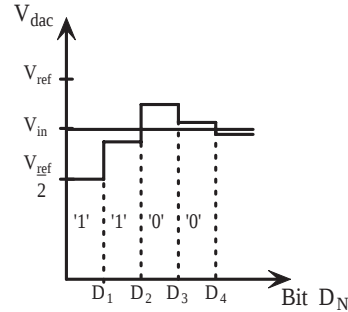


Figure 2.11. Successive approximation conversion procedure [1].

The main advantage of the SAR ADC is that the circuit complexity and power dissipation are less than those found in most other types of ADCs [3]. Its main disadvantage is the required resolution and speed of the comparator. As it takes N cycles for the ADC to complete a conversion, the speed of the converter is limited by the output settling time of the DAC and the time needed by the comparator to resolve the input difference in each 1-bit cycle. Furthermore, the comparator must eventually be able to do the comparison within 1 LSB of precision, meaning that the input-referred noise must be kept to a minimum in order to avoid errors.

2.2.5 Delta-Sigma ($\Delta\Sigma$) ADC

The ADCs discussed thus far sample the input signal at two-times the input signal's bandwidth, hence the name *Nyquist-rate* converters. In order for these ADCs to avoid aliasing of the sampled signal, they require an analog filter with a sharp corner-frequency. Not only the design of such a filter is very challenging, but the tight matching requirements of IC components prevent Nyquist-rate ADCs of achieving very high resolutions.

The $\Delta\Sigma$ ADC is referred to as an *oversampling ADC* because it samples the input signal at a frequency much higher than that specified by the Nyquist criterion. A block diagram of a $\Delta\Sigma$ ADC is shown in Figure 2.12. It consists of an integrator, a 1-bit ADC, a 1-bit DAC and a decimation filter. The operation principle consists of sampling multiple times the input signal and computing the average of the quantization error between the input signal and its estimate generated by the DAC. This average is calculated by the decimation (digital) filter. The fact that a coarse (1-bit) quantization is done and the separation between the signal bandwidth and the sampling frequency is wide, the requirements for the anti-aliasing filter are very relaxed. This allows the use of a simple 1st. or 2nd. order analog filter, requiring small silicon area.

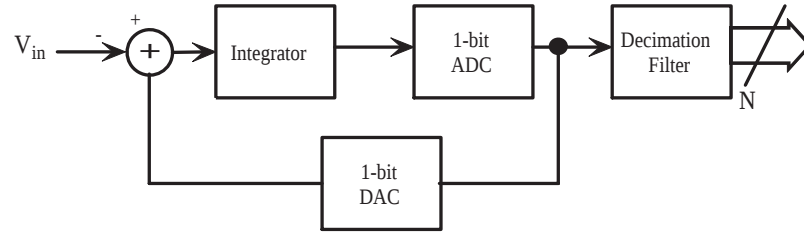


Figure 2.12. Block diagram of a $\Delta\Sigma$ ADC.

2.2.6 Final Remarks

In the previous sections an introduction to data conversion systems was presented and a number of analog-to-digital converters were described. From various manufacturer catalogs and datasheets it has been found that the most popular and widely available ADCs are those based on the Pipeline, the Successive Approximation (SAR), and the Delta-Sigma ($\Delta\Sigma$) architectures [13]. Moreover, as will be discussed in later chapters, these three types of converters have been under extensive study with the advent of low-voltage low-power applications.

Table 2.1 shows a classification of these converters in terms of resolution, speed, and power. Although a trade-off exists among these three parameters, for a given application (i.e., resolution requirements) more than one type of converter might be used. For example, for medium- to high-resolution applications one will have to choose between the SAR and the $\Delta\Sigma$ ADCs. Which one to use will depend to a certain degree on the specifications needed for the application or design. For extreme low-power requirements the $\Delta\Sigma$ will be the ideal choice. Yet, if the speed requirements are not met, the SAR ADC has to be chosen. A similar design trade-off occurs for low to medium-resolution applications. When speed is the number one design parameter, the Pipeline ADC offers the fastest conversion speed. However, if the power consumption requirements are not met the SAR ADC must be selected.

Table 2.1. Resolution, speed, and power requirements for popular ADCs [13].

	Low Resolution (8-12 bits)	Medium Resolution (14-18 bits)	High Resolution (20-24 bits)
$\Delta\Sigma$			
- speed	n/a	128S/s - 40kS/s	12S/s - 105kS/s
- power	n/a	0.27 - 122mW	0.6 - 35mW
SAR			
- speed	20kS/s - 1MS/s	40kS/s - 1.25MS/s	n/a
- power	0.6 - 250mW	1.95 - 200mW	n/a
Pipeline			
- speed	2MS/s - 105MS/s	1MS/s - 80MS/s	n/a
- power	54 - 905mW	250 - 1200mW	n/a

The data shown in table 2.1 does not represent the absolute minimum/maximum performance that can be achieved with these converters, but it is a rough estimate based on technical data published by manufacturers [13]. For example, a few high-end $\Delta\Sigma$ ADCs with conversion speeds of 1 MS/s range are available, but in general these converters do not achieve more than a few tenths kS/s.

Based on the data just presented, it can be seen that the best trade-off between speed and power consumption is achieved by the SAR ADC. It achieves higher conversion speed than the $\Delta\Sigma$ ADC while consuming less power than the Pipeline ADC. Moreover, its resolution range is similar to that offered by the Pipeline ADC. Consequently, the SAR ADC can be used in a wide range of applications. Examples of these includes instrumentation and transducers, medium-resolution data acquisition, and systems interfaces. In Chapter 5, the design of a SAR ADC prototype is presented. The objective of this design was to obtain low-power consumption under the constraint of a power supply operating at low-voltages (i.e., 1-2 volts).

CHAPTER 3

ADC Circuit Blocks

In Chapter 2 the basic concepts of data conversion were presented and a number of architectures commonly employed for A/D conversion were described. The S/H circuit, the D/A converter, and the comparator were presented as fundamental components for the operation of an ADC. With a general understanding of data conversion principles, now follows a detailed discussion of how these circuit blocks affects the performance of an ADC. The basic concepts entailing the operation of S/H circuits, DACs, and comparators is presented. The main performance metrics of each circuit block are described along with different techniques available for the implementation of these circuits.

3.1 Sample-and-Hold Circuits

A sample-and-hold (S/H) circuit takes samples of its analog input signal and holds these samples in a memory element. The key feature of this circuit, when used as the front end of an ADC, is that it relaxes the timing requirements of the latter. This means that the precision and speed of the converter will be limited to a certain degree by the S/H circuit.

The operation of a S/H circuit is divided into two modes, sample and hold. Usually this is done at uniform time intervals, set by a periodic clock that divides circuit operation into two phases. During the sample-mode the output of the circuit can either track the input or reset to some fixed value. In the hold-mode, the output of the S/H circuit is equal to the input value obtained (sampled) at the end of the sample mode. Figures 3.1 (a) and (b) illustrate example waveforms for a S/H circuit and a T/H (track-and-hold) circuit. Although here a distinction was made between sampling and tracking, the majority of the circuits are referred to as S/H circuits even though they behave as T/H circuits.

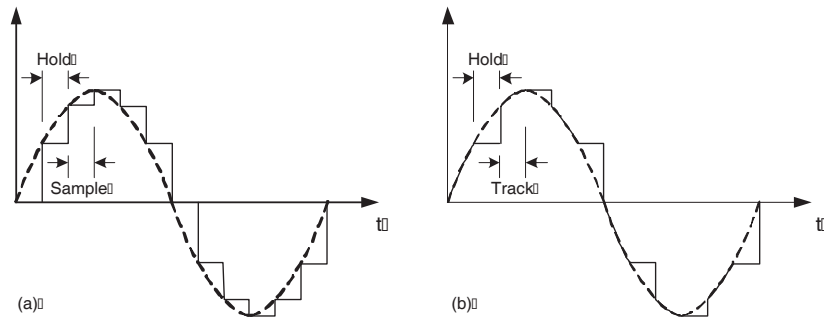


Figure 3.1. (a) S/H circuit and (b) T/H circuit output waveforms.

The most basic form of a S/H circuit combines a switch and a capacitor, as shown in Figure 3.2. The operation of the circuit proceeds as follows. In *sampling mode* the switch is “on”, creating a signal path that allows the capacitor to track the input voltage. When the switch is “off” an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into *holding mode*.

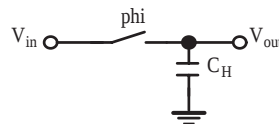


Figure 3.2. Simple sample-and-hold circuit.

3.1.1 Performance Metrics

In order to understand the influence of sample-and-hold circuits in ADCs, a number of parameters describing their main characteristics must be defined. These are described below and illustrated in Figure 3.3.

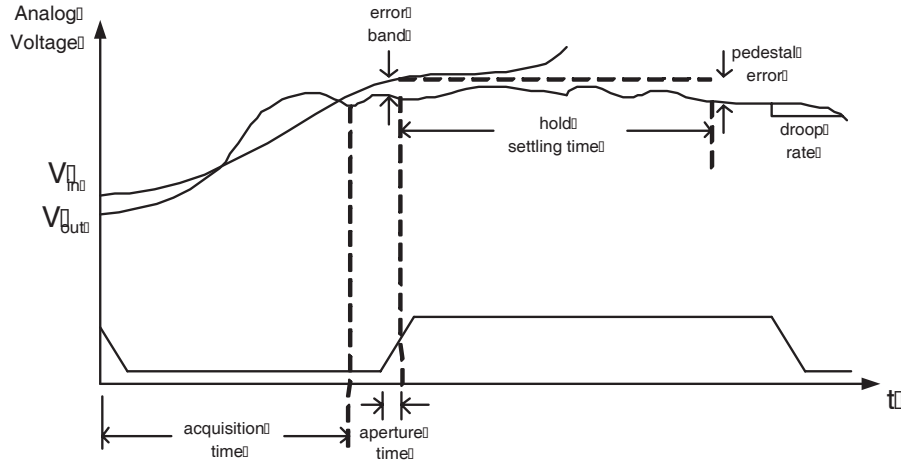


Figure 3.3. Illustration of some performance parameters of a S/H circuit.

- *acquisition time*, t_{acq} , is the time required, after the sampling command, for the S/H circuit to take a new sample, so that its output during the hold mode be within a specified error band.
- *settling time*, t_s , is the time required after the hold command is asserted for the S/H circuit's output to settle within a specified error band of its steady state (or final) value. This is usually the limiting factor on the sampling rate of the circuit.
- *aperture time* is the time required, after the hold command, for the switch to open and the signal to be actually sampled into the storing element.

- *aperture uncertainty*, or *jitter*, is the random variation in the aperture time, arising from the noise that affects the clock transitions and, consequently, the execution of the hold command.
- *pedestal error* is the error introduced at the output of the S/H circuit between the time when the sample mode ends and the time the hold mode is active.
- *droop rate* is the rate of change of the output, due to signal leakage during the hold mode. The parasitic elements present in the circuit is the main reason for the existence of this effect.
- *hold-mode feedthrough* is the fraction of input signal present at the output during the hold mode. It is due to the signal coupling created by the parasitic elements surrounding the internal nodes of the S/H circuit.
- *dynamic range* is the ratio of the maximum allowable input signal and the minimum input signal that can be sampled within a specified degree of accuracy.
- *signal-to-noise ratio* (SNR) is the ratio of signal power to noise power present at the output.
- *signal-to-(noise + distortion) ratio* (SNDR) is the ratio of the signal power to the total noise and harmonic power present at the output.

3.1.2 MOS Sampling Switch

As illustrated in Figure 3.2, the two most basic elements needed in a sampling circuit are the switch and a memory element. The switch allows the circuit to be configured into one of its two operating modes: sample and hold. In CMOS technology, the clear choice for the implementation of a switch is the MOS transistor.

For data storage either voltage sampling or current sampling methods can be used [3]. The first method employs capacitors; the second employs inductors. However, in integrated circuit technology it is easier to fabricate capacitors than inductors, reason for which all S/H circuits are done with voltage sampling [15]. Next, the operation of the MOS transistor as a switch and its most important limitations are discussed.

When a voltage large enough is applied to the gate terminal of an MOS transistor, the formation of the channel between its source and drain terminals allows the transistor to transmit any signal through that channel. The application or removal of a voltage at the gate follows the same operation principle of an ideal switch. When the transistor is turned “on” a signal path is present and when the transistor is turned off the channel vanishes and no signal path exists.

One of the main differences between an ideal switch and a transistor is that when the transistor is “on”, instead of an ideal short circuit, a small on-resistance (i.e., 0.5 - 2 k Ω) is present in the signal path between the drain and source terminals. Similarly, in the “off” state there is a resistance large enough to prevent signals from passing between its two terminals. Figure 3.4 (a) and (b), respectively, shows the basic sampling circuit using an MOS switch and its equivalent circuit during sample mode. When operated in the *triode* or linear region the on-resistance of an NMOS transistor can be approximated as¹

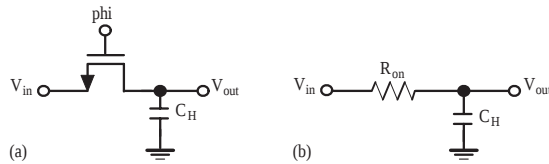


Figure 3.4. (a) MOS-based S/H circuit (b) equivalent circuit during sampling.

¹Although the discussion has focused on an NMOS transistor, it also applies to PMOS transistors.

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{thn})} \quad (3.1)$$

where μ_n represents the electron mobility factor in the channel, C_{ox} , is the oxide capacitance present between the gate terminal and the substrate, W and L are the width and length of the transistor, respectively, V_{GS} is the gate-source voltage, and V_{thn} is the threshold voltage. A similar analysis can be made for a PMOS transistor. As discussed next, the on-resistance and the parasitic capacitance of the transistor affects the speed and precision of a S/H circuit.

Speed Issues

One of the key parameters used to estimate the speed of a S/H circuit is the *settling time*. For a circuit tracking an input, the settling time is specified as the time required for the output voltage to be within the acceptable error band, ΔV , after the hold command has been issued. This is illustrated in Figure 3.5. When used as the front-end of an ADC, the sampled value must have an accuracy of ± 0.5 LSB (least-significant-bit).

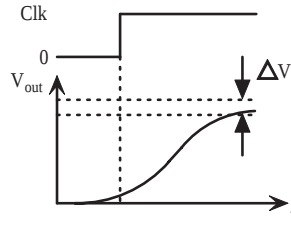


Figure 3.5. Speed measurement in a S/H circuit.

Precision Issues

When an MOS transistor is “on”, the channel formed between its source and drain terminals has charge stored in it. When the transistor switches to the “off” state,

the charge stored in the channel exits through both of its terminals. This effect, called *charge injection*, is illustrated in Figure 3.6. Although the charge injected into the circuit's input introduces no error, the charge injected into the holding capacitor results in a sampled voltage error. The charge of a transistor in strong inversion mode can be approximated by [16]

$$Q_{chn} = WLC_{ox}(V_{GS} - V_{TH}) \quad (3.2)$$

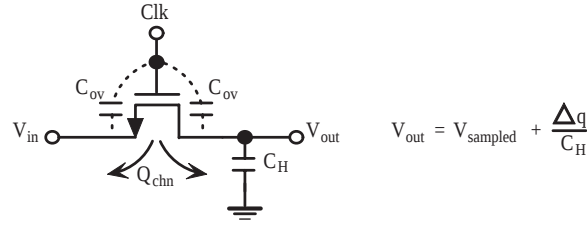


Figure 3.6. Charge injection in an MOS switch.

Another type of error that occurs during the transition of the switch from the “on” state to the “off” state is *clock feedthrough*. The finite slope present in the clock signal transition results in coupling of the clock signal to the holding capacitor through the overlap capacitances C_{ov} (from the gate-to-drain or gate-to-source), causing errors in the sampled voltage. An approximation of the error voltage is given by the following equation [16].

$$\Delta V = \frac{C_{ov}}{C_{ov} + C_H} \cdot V_{clk} \quad (3.3)$$

Thermal noise is also an important source of error. It is due to the random thermal motion of electrons in the switch's on-resistance. In a switched-capacitor circuit (see Figure 3.4), the resulting noise power generated in the sampled signal can be defined as [16]

$$P_{noise} = \frac{kT}{C} \quad (3.4)$$

where k is the Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature (in kelvins), and C is the holding capacitor.

The time at which the transistor turns off depends on the value of the input signal at the time the gate's clock signal is making a transition. As discussed in section 3.1.1, this effect and the noise affecting the clock transitions produces jitter or random variation at the sampling instant.

The input voltage range of an MOS switch is limited by the threshold voltage, V_{TH} , of the transistor. From equation (3.1) and Figure 3.7 it can be seen that the variation in switch on-resistance is maximum when the gate overdrive ($V_{GS} - V_{TH}$) approaches 0. For an n-channel MOS switch the input voltage range at the source terminal is from 0 (i.e., ground potential) to $V_{DD} - V_{THN}$. For a p-channel MOS switch this range goes from V_{THP} to V_{DD} .

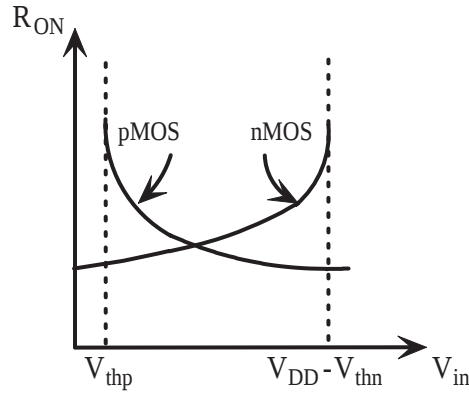


Figure 3.7. Switch on-resistance as a function of the input signal.

A technique used to extend the input range of the sampling switch consists of using complementary transistors in parallel, so that at least one of the two transistors is “on” over the whole input-signal range while the switch on-resistance is maintained

relatively constant. In order to turn “on” or “off” both transistors simultaneously, complementary clock signals are applied at their gate terminals. This is shown in Figure 3.8.

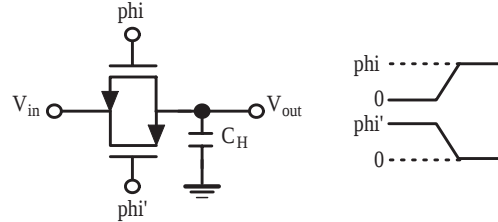


Figure 3.8. CMOS switch using complementary transistors.

3.1.3 S/H Architectures

S/H circuits can be classified into *open-loop* and *closed-loop* architectures. The classification depends on whether or not the hold capacitor is enclosed in a feedback loop. In the following sections these two groups are explained and a few basic implementations are discussed for each.

Open-loop architectures

A typical open-loop S/H circuit is presented in Figure 3.9. It is based on the circuit shown in Figure 3.2. Here, buffers have been added at the input and output of the circuit. The purpose of the input buffer is to prevent loading in the previous stage or circuit. The output buffer is added for driving capability considerations, otherwise the circuit would not be able to drive large loads.

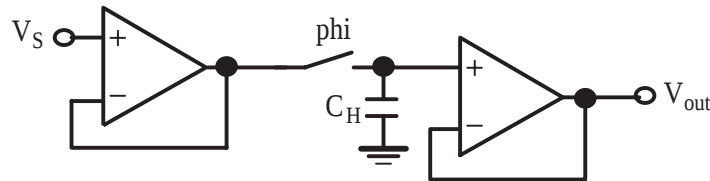


Figure 3.9. Basic open-loop S/H circuit.

The main drawback of this configuration is the signal distortion resulting from the input-dependent charge-injection. Moreover, the speed of this circuit is limited by bandwidth and, hence, settling time of the added buffers. In order to fulfill the linearity requirements of the system, usually imposed by the ADC, the buffers require as high a gain as possible and the use of local feedback [3].

Closed-loop architectures

In order to eliminate the input-dependent charge injection present in open-loop architectures, the hold-capacitor must be enclosed in a feedback loop [16]. A classic implementation of such an architecture is shown in Figure 3.10. This configuration is arranged in such a manner that the charge injected by those switches which are not connected to a constant potential (usually V_{DD} or G_{nd}) introduce no errors into the sampled voltage. As it will now be discussed, the operation of the switches must follow a very specific timing in order to avoid charge-injection errors.

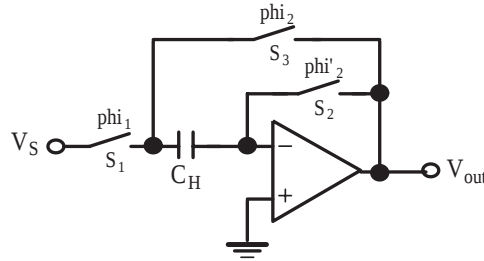


Figure 3.10. Basic closed-loop S/H circuit.

During sampling-mode (ϕ_1), switches S_1 and S_2 are closed and switch S_3 is opened. The op amp is in unity-gain mode and the capacitor is able to track the input voltage. In hold-mode (ϕ_2), switches S_1 and S_2 are opened and switch S_3 is closed. However, to prevent input-dependent charge injection, switch S_2 must turn off (ϕ'_2) slightly before switch S_1 . Since the node at the right-hand terminal of the capacitor is a virtual ground, the charge injected by S_2 is constant and can be

viewed as an offset in the input/output characteristic. As the charge at this node must remain the same before and after S_2 turns off, there is no path for the charge injected by S_1 to flow, hence no error is introduced by the latter. A more detailed analysis of this circuit and other similar configurations can be found in [16].

3.2 Digital-to-Analog Converters

A digital-to-analog converter (DAC) receives a digital code at the input and generates an analog output signal that is a fraction of the full analog range set by a reference. Depending on the architecture, the reference can be treated as a current, voltage, or charge quantity. Figure 3.11 shows the basic block diagram of a DAC with the input/output characteristic shown in Figure 3.12.

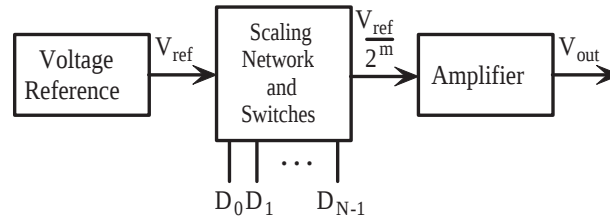


Figure 3.11. Block diagram of a digital-to-analog converter.

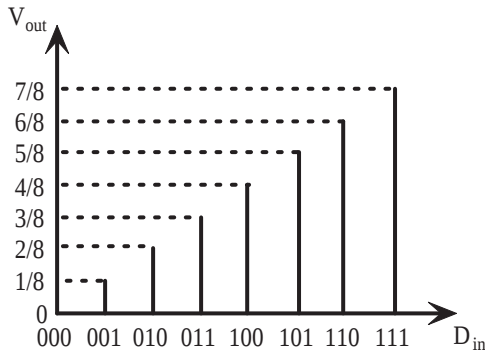


Figure 3.12. Input/output transfer characteristic of a 3-bit DAC.

The output voltage of the DAC can be expressed as

$$V_{out} = V_{ref} \cdot \left(\sum_{m=0}^{N-1} D_m \cdot 2^{-m} \right) \quad (3.5)$$

where (V_{ref}) represents the reference voltage, N is the number of bits, and D_m is the m_{th} -bit of the digital code. The summing term in the equation represents the binary-weighting produced by the division of the reference voltage. The accuracy with which the DAC implements equation (3.5) will determine the linearity of the converter [3].

3.2.1 Performance Metrics

The DAC is a very important circuit component present in ADCs. For this reason it becomes necessary to study the parameters that describe its performance. This provides a better understanding of how it influences the behavior and performance of an ADC. Following is a brief description of the *static* and *dynamic* parameters that characterize a DAC.

Static Parameters

The *resolution* can be defined as the smallest output voltage change for which a transition between input code occurs. For an N -bit converter the total number of digital input codes is 2^N . The DAC fractions the reference into a minimum output value of $1/2^N$ according to equation (2.1).

The *full-scale* (FS) range indicates the output voltage range within which lie the analog voltages corresponding to each possible digital input vector. Due to the DAC's finite resolution, its full-scale range is not equal to the reference. The full scale range is described as

$$FS = V_{ref} - LSB = V_{ref} \left(1 - \frac{1}{2^N}\right) \quad (3.6)$$

It can be the case that, for a zero digital input code, the analog output voltage is not zero but some voltage amount. This type of error is called *offset error* and affects all codes by the same amount; it is illustrated in Figure 3.13(a).

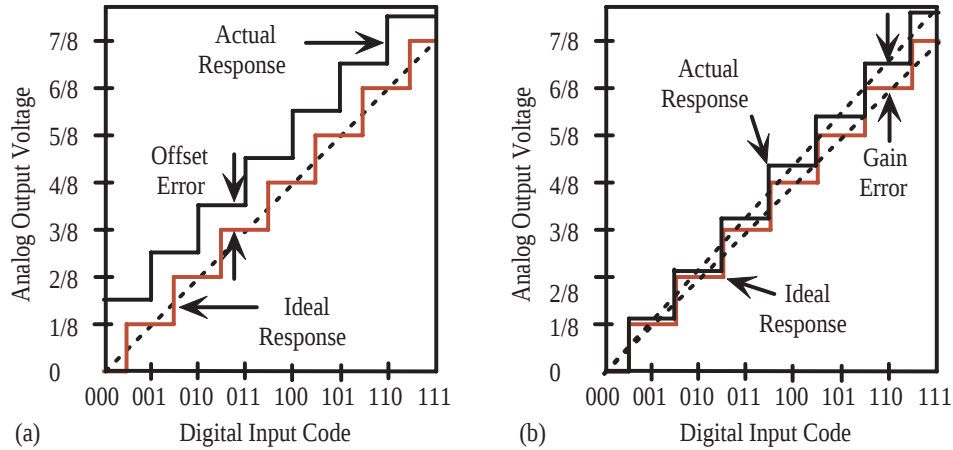


Figure 3.13. (a) Offset and (b) gain errors in a 3-bit DAC..

The *gain error* is the difference in slope between the actual transfer function and that of an ideal DAC when no offset error is present. This is illustrated in Figure 3.13(b).

Figure 3.14 illustrates the *Differential Non-Linearity* (DNL) and *Integral Non-Linearity* (INL) in a DAC. The DNL is the difference between the actual voltage change at the output and the ideal digital code transition of 1 LSB. The INL is the difference between the output voltages in the actual converter response and a straight line drawn between the end points of an ideal converter response.

Dynamic Parameters

One of the most important dynamic parameters of a DAC is the *conversion speed*. It is a measure of how fast the DAC can make successive conversions, as it is the case

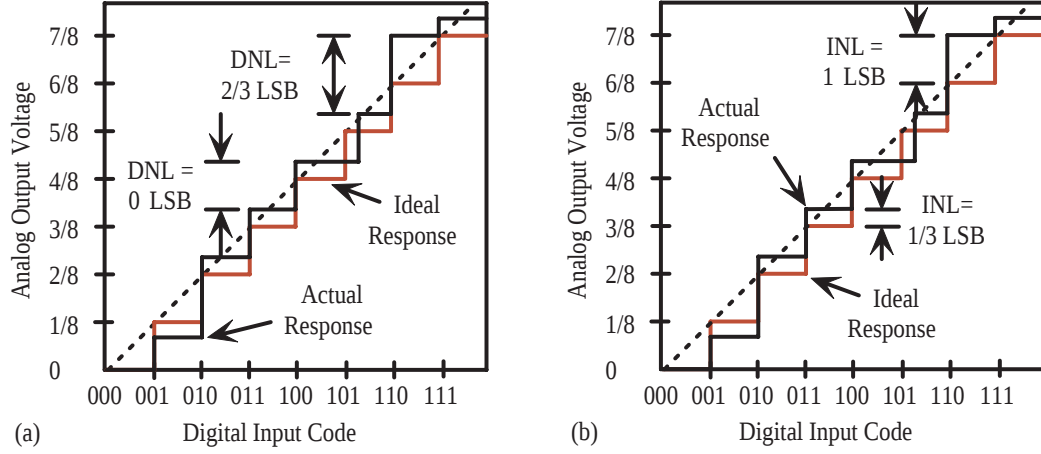


Figure 3.14. (a) DNL and (b) INL errors in a 3-bit DAC..

when the input code has made a transition. A key limiting factor in the conversion speed is the *settling time* of amplifiers and RC circuits, which determine the time needed after an input change for the output voltage to settle within the specified accuracy limits (i.e., ± 0.5 LSB).

The *signal-to-noise ratio* (SNR) is the ratio of the full-scale analog signal to the rms-value of the quantization noise. It is related to the *dynamic range*, which is the ratio of the maximum allowable input voltage and the minimum voltage that can be resolved within a specified degree of accuracy. These parameters measure how robust is the system against noise perturbations.

As with ADCs, to better assess the performance of a DAC against noise, the effective number of bits (ENOB) can be used as shown below.

$$ENOB = \frac{SNR_{actual} - 1.76}{6.02} \quad (3.7)$$

3.2.2 DAC Architectures

Digital-to-analog converters can be grouped into two main categories: *serial DACs* and *parallel DACs* [14]. A serial DAC does the conversion of the digital input code one

bit at a time. For an N-bit DAC it takes N cycles to represent the input as an analog voltage. On the other hand, since a parallel DAC processes all the bits simultaneously, it takes only once cycle to complete the conversion. Since serial DACs make the SAR ADC slower, parallel DACs are the most frequently used in the design of such ADCs. From here on the discussion will focus on parallel DAC based architectures.

Parallel DACs receive a digital input code and generate an analog output that is a fraction of the reference voltage. This output represents the analog estimate of the digital input. These types of DACs can be sub classified according to how the voltage reference is binary-scaled into an analog value. The three most popular methods used for digital-to-analog conversion are current-scaling, voltage-scaling, and charge-scaling; these are discussed next.

The *current-scaling* DAC makes use of current-steering circuits to convert the digital input code into a set of binary-weighted currents. These are added and applied to an op amp for conversion into a voltage signal. The op amp is configured as an inverting-summing amplifier in order to perform the addition and conversion of current to voltage.

Figure 3.15 illustrates a current-scaling architecture, also called binary-weighted resistor DAC [14]. For an N-bit converter, it requires N switches and N resistors sized in binary fashion. The binary-weighted currents generated by the resistors are directed to the op amp according to the operation state of the switches. Those bits asserted with a “1”, will have their corresponding switch set to the reference voltage V_{REF} and the current through it will flow through the feedback resistor R_F . The bits containing a “0” will have their corresponding switch set to ground potential, preventing any flow of current through them.

The output voltage for the circuit of Figure 3.15 can be expressed as follows

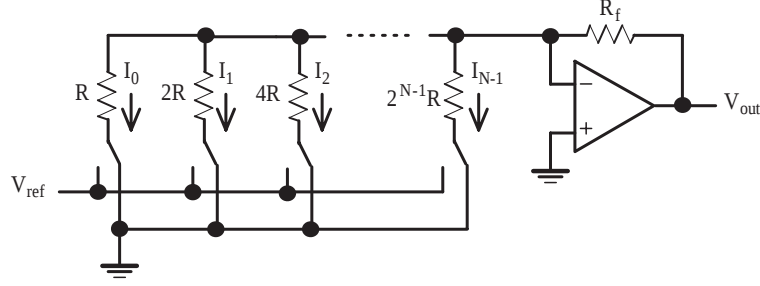


Figure 3.15. Binary-weighted resistor DAC.

$$V_{out} = \frac{R_F}{R} \left(S_N + \frac{S_{N-1}}{2} + \dots + \frac{S_2}{2^{N-2}} + \frac{S_1}{2^{N-1}} \right) \quad (3.8)$$

The main advantage of the current-scaling architecture is that it is insensitive to parasitic capacitors and, hence, can provide fast conversion rates [14]. Disadvantages include the required area and poor matching of resistors that limit resolution below 10 bits. When higher resolution is needed, an alternative circuit solution requiring less area is the circuit shown in Figure 3.16.

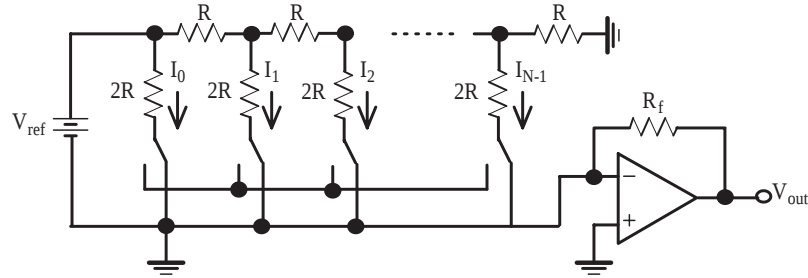


Figure 3.16. R-2R resistor ladder DAC.

The voltage-scaling DAC converts the digital input code into an analog output by scaling the reference voltage into a set of N node voltages. The basic configuration as shown in Figure 3.17, consists of a resistor string and a series of switches. The latter are controlled by the digital input in order to route to the output the appropriate “tap” voltages representing the analog estimate of the input code. The main advantage of this architecture is the guaranteed monotonicity. Its main disadvantage

is the large number of resistors and switches required, limiting the resolution to about 6-bits. Its output voltage can be expressed as

$$V_{out} = \frac{V_{ref}}{2^N} \left(n - \frac{1}{2} \right) \quad (3.9)$$

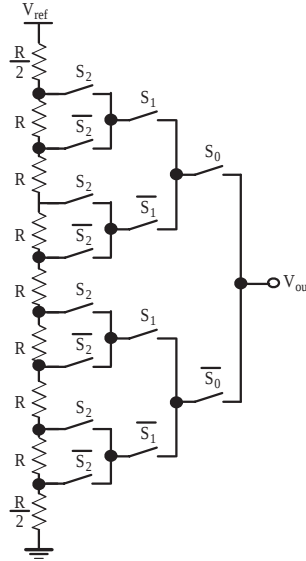


Figure 3.17. 3-bit voltage-scaling DAC.

The charge-scaling method consists of a capacitor array and a combination of switches that distributes the circuit's total charge among the capacitors. The basic architecture used with this method is shown in Figure 3.18. The operation of the circuit is controlled by a two-phase non-overlapping clock. During the *reset phase* the bottom-plate of the capacitors are connected to ground through the switches, allowing them to discharge. During the second phase, the digital input code will control to what potential the switches will be connected. For a bit containing a “1” the switch's terminal will be connected to the reference voltage V_{ref} and for a bit containing a “0” the switch's terminal will remain connected to ground. The equivalent of the digital code will be the sum of the charge distributed through those capacitors connected to V_{ref} . When used as a standalone unit, the DAC requires an

output buffer to prevent the discharge of the unit capacitor due to resistive loads.

$$V_{out} = V_{ref} C \left(\frac{S_N}{2} + \frac{S_{N-1}}{4} + \dots + \frac{S_2}{2^{N-1}} + \frac{S_1}{2^N} \right) \quad (3.10)$$

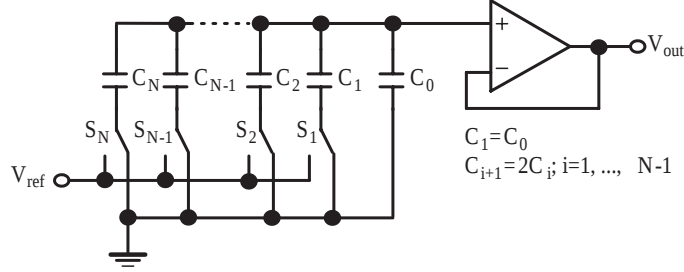


Figure 3.18. Basic charge-scaling DAC..

Similar to the binary-weighted resistor DAC, the accuracy of this DAC is limited by the precision of the passive components. A careful design must be followed so that the capacitors are correctly sized with respect to the parasitic capacitances. In order to achieve precise binary-weighted values for the capacitors the layout must employ techniques such as *common-centroid* [17, 18]. Consequently, the large area and mismatch dependence are disadvantages found in this architecture.

3.2.3 Higher Resolution Architectures

For the architectures described thus far, the primary factor limiting their resolution is the precision of its passive components. For current CMOS technologies, the maximum resolution is around 10 bits. Since the accuracy of these DACs depends on the ratio of the largest to smallest resistor (capacitor), a means to increase the resolution without a significant increase in area must be followed.

One of the techniques available to reduce the required area of these passive components consists of combining subDACs of M-bit and K-bit resolution to form a (M+K)-bit DAC. One of the subDACs is used to process the most-significant bits

and the other is used to process the least-significant bits. A block diagram illustrating this technique is shown in Figure 3.19. First, the output of the LSB subDAC is scaled by a factor of $1/2^M$. Then, the scaled output is added to that of the MSB subDAC. As shown in equation (3.11) below, the resulting analog signal represents the digital input code.

$$V_{out} = \left(\frac{S_{M+K-1}}{2} + \frac{S_{M+K-2}}{4} + \dots + \frac{S_M}{2^M} \right) V_{ref} + \left(\frac{1}{2^M} \right) \left(\frac{S_{K-1}}{2} + \frac{S_{K-2}}{4} + \dots + \frac{S_0}{2^K} \right) V_{ref} \quad (3.11)$$

A similar technique used for increasing DAC resolution consists on scaling the voltage reference of the LSB subDAC instead of scaling its output voltage. Again, the output of an M-bit subDAC is combined with the output of a K-bit subDAC to represent the converted analog output of the complete DAC. The output voltage using this technique is the same as that described by equation (3.11).

An example of a DAC implemented using scaled output voltages is shown in Figure 3.20. Here, an 8-bit charge scaling DAC was formed from the combination of two 4-bit subDACs. This is done through capacitor C_S , which scales the output voltage of the LSB subDAC and produce the least-significant-bit for the MSB subDAC.

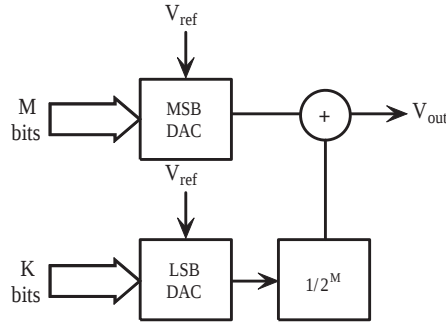


Figure 3.19. Block diagram of an M+K DAC formed by using two subDACs.

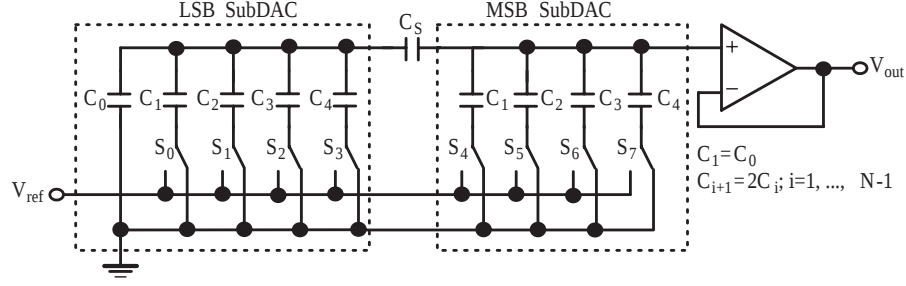


Figure 3.20. 8-bit charge-scaling DAC composed of two 4-bit subDACs.

The series addition of the scaling capacitor, C_S , and the effective capacitance of the LSB subDAC, must terminate the MSB subDAC and, hence, be equal to the unit capacitor C_0 . From this analysis, the C_S value can be obtained from the following equation

$$C_0 = \frac{1}{\frac{1}{C_S} + \frac{1}{2C_0 * 2^{N-1}}} \quad (3.12)$$

In equation 3.12, C_S and C_0 represent the scaling and unit capacitors, respectively, and N represents the DAC's resolution. It should be noted that C_s affects both the LSB and MSB subDACs because it acts as a termination capacitor for the MSB DAC [14]. An approach similar to the one described above can be follow using current-scaling or voltage-scaling methods.

3.3 Comparators

A comparator is a differential amplifier with no feedback loop, whose function is to compare the analog signals presented at its inputs. Depending on the polarity of the differential input will be the logic output produced. As it is the case with several types of ADCs, usually one of the comparator's input is connected to a constant potential or reference. The circuit symbol and ideal transfer function of a comparator is shown

in Figure 3.21. It can be seen that if the voltage difference $V_{in}^+ - V_{in}^-$ is positive the comparator's output will go high (V_{OH}), otherwise its output will go low (V_{OL}).

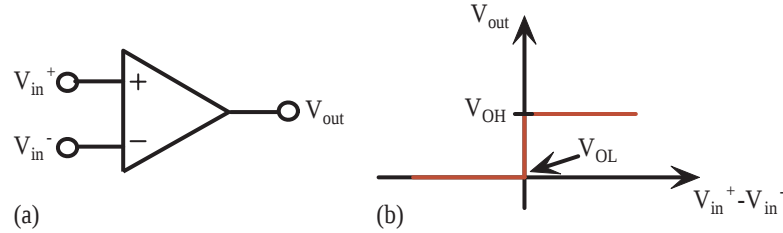


Figure 3.21. Comparator (a) circuit symbol and (b) ideal transfer function.

3.3.1 Performance Metrics

Due to fabrication limits and process variations, the comparator performance is affected by nonideal effects. As a result, the response deviates from the ideal one shown in Figure 3.21(b). Following is a brief description of the main parameters that characterize the performance of comparators.

Static Parameters

The static parameters are those that described the performance of a comparator under DC or steady-state conditions. The main parameters presented here are resolution, gain, offset, noise, and ICMR.

Resolution is the minimum input difference that can be resolved by the comparator in order to switch between its binary states. It is usually limited by the input-referred offset and noise generated by the internal components of the comparator. When employed in ADCs, the resolution specification must be equal or lower than the least-significant-bit (LSB) defined by the converter.

The *gain*, A_v , is one of the key limiting factors in achieving the desired resolution for the comparator. To obtain the ideal response shown in Figure 3.21, a transition

between output logic levels occurs for a zero-input difference. This leads to a gain that approaches infinity, as given by the following equation

$$A_v = \lim_{\Delta V \rightarrow 0} \frac{V_{OH} - V_{OL}}{\Delta V} \quad (3.13)$$

A real comparator has a finite gain, given by

$$A_v = \frac{V_{OH} - V_{OL}}{V_{in}^+ - V_{in}^-} \quad (3.14)$$

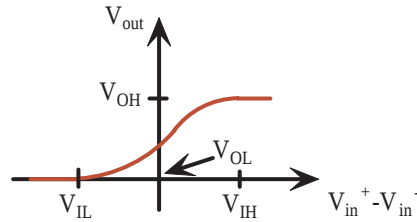


Figure 3.22. Transfer function of a finite-gain comparator.

As mentioned before, the *offset* is a non-ideal effect that limits the resolution of the comparator. Assuming an ideal comparator with zero differential input voltage required to produce an output transition, the offset is defined as the minimum amount of input voltage required for the binary-state transition to take place. In a real comparator the offset adds to the minimum voltage for which the resolution was designed reducing the resolution of the circuit. An illustration of how it affects the response of the circuit is given in Figure 3.23. Section 3.3.3 presents offset-cancellation techniques developed to reduce this kind of error.

Noise has great influence on the operation of the comparator, thus affecting the performance of an ADC. From Figure 3.24, the effect of noise in the circuit's response can be seen as uncertainty in the time when the comparator's output switches between its two states.

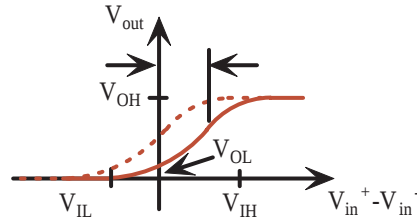


Figure 3.23. Effect of offset voltage in the transfer function of a comparator.

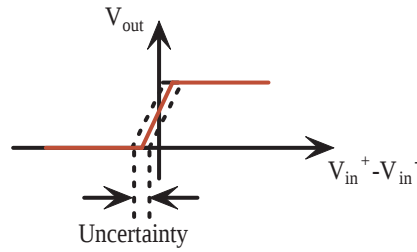


Figure 3.24. Effect of noise in comparators.

The signal presented to the input of amplifiers and comparators is not fully differential but carries a common-mode component with it. Another important parameter is then the *input common-mode range* (ICMR). The ICMR is the permissible voltage-range over which the input common-mode signal can vary while all transistors remain biased in the saturation region. If the input signal exceeds this specification, the comparator won't be able to operate properly as some of its transistors could be in triode or cutoff modes.

Dynamic Parameters

Two of the most important dynamic parameters that determine the speed of a comparator are the *propagation delay* and the *settling time*. The propagation delay is the time that elapses between an input transition and the corresponding output change. As shown in Figure 3.25, it is usually measured at the midpoints between the input and output signals. The settling time, as with a S/H circuit, is defined as the time needed for the output to settled within a specified percent of its final value,

usually 0.1 and 0.01%.

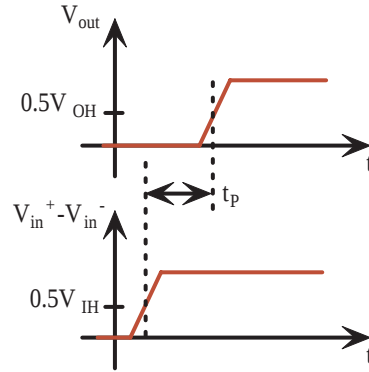


Figure 3.25. Propagation delay in a comparator.

Figure 3.26 illustrates the time response of a comparator to a small input signal. It is based on a first-order approximation for an op amp with a single dominant-pole.

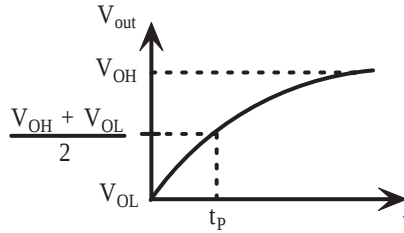


Figure 3.26. Comparator time response to a small input voltage.

The propagation delay for the time response shown in Figure 3.26 can be approximated as [19]

$$t_P = \frac{1}{p_1} \ln(2) = \tau_c \ln(2) \quad (3.15)$$

where p_1 is the comparator's dominant pole and τ_c is its associated time constant.

As with any op amp, the *slew rate* is a large-signal behavior that sets the maximum rate of output change. It is limited by the output driving capability of the comparator. The propagation delay is inversely proportional to the input voltage applied. This means that applying a larger input voltage will improve the propagation delay, up to the limits set by the slew rate.

3.3.2 Architectures

Comparators can be roughly classified into *open-loop* (continuous-time) comparators and *regenerative* comparators. The main difference resides on whether or not feedback is applied to the op amp used. To obtain the benefits offered by both types of comparators, many configurations have been developed that employ a combination of open-loop stages with regenerative stages that use positive-feedback.

Open-loop Comparators

An open-loop comparator is an operational amplifier designed to operate with its output saturated, close to the supply rails, based on the polarity of the applied differential input. The op amp does not employ the use of feedback and hence no compensation is required to achieve stability in the system. This does not poses a problem since the linear operation is of no interest in comparator design. The main advantage of not compensating the op amp is that it can be designed to obtain the largest possible bandwidth, thereby improving its time response (see equation 3.15).

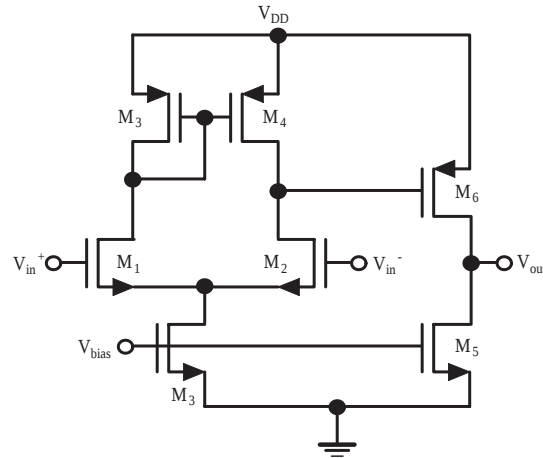


Figure 3.27. Two-stage open-loop comparator.

Figure 3.27 illustrates a circuit example of an open-loop comparator. It is based

on the commonly used two-stage op amp. The first stage is a NMOS *differential-pair* consisting of transistors M_1 and M_2 , with PMOS transistors M_4 and M_5 acting as a diode-connected active load. Transistors M_3 is used to bias the input pair. The output stage is a *current-sink inverter* consisting of transistors M_5 and M_6 . Figure 3.28 illustrates an example of the time response of this comparator.

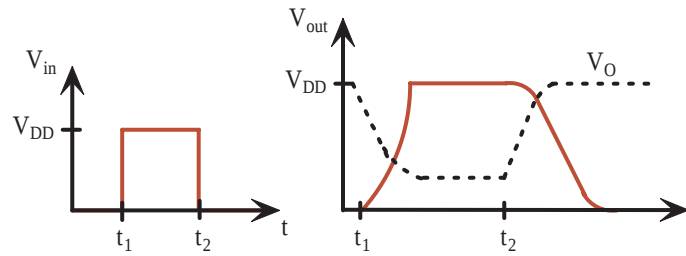


Figure 3.28. Output response of a two-stage comparator.

The main advantage of open-loop comparators is that, if enough gain is provided, the minimum detectable differential input can be very small ($< 1\text{mV}$). Examining equation (3.14), it would be reasonable to think that by simply designing the comparator with the largest possible gain an almost infinite resolution can be achieved. However, increasing the gain also reduces the bandwidth of op amps. This means that although the resolution will improve, the time response of the comparator will degrade. Thus, a tradeoff between speed and resolution must be made. The absolute maximum resolution of open-loop comparators is limited by input-referred noise and the offset voltage present in the op amp used.

Regenerative Comparators

Unlike open-loop comparators, regenerative comparators make use of positive feedback to realize the comparison between two signals. A striking feature of these comparators is that they operate in discrete-time rather than continuous-time form. They operate with a clock that divides the operation of the circuit into two phases. During

the first phase the comparator tracks the input and during the second phase the positive feedback is enabled. Depending on the polarity of the input, the latch's output will go high as the other will go low.

The basic principle of regeneration consists in employing a latch circuit. Shown in Figure 3.29, the latch employs positive feedback through the cross-coupled connection of the NMOS (or PMOS) transistors.

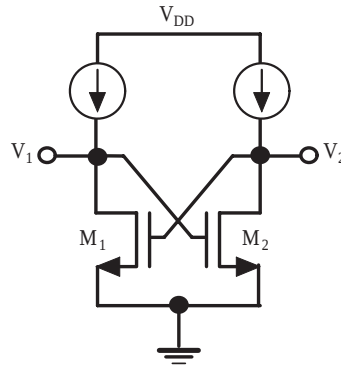


Figure 3.29. Basic latch using NMOS transistors.

In Figure 3.30, a circuit schematic of a latch comparator is shown [2, 14]. The operation of the circuit is divided into two phases, using a non-overlapping clock circuit. During the first phase, the *latch* command is issued and the circuit tracks the input voltage applied between its terminals V_{in}^+ and V_{in}^- . During the second phase ($\overline{latch}$), transistors M_5 and M_6 isolate the latch from the input as these are turned “off”. The regeneration occurs between the drain and gate terminals of transistors M_9 and M_{10} , finalizing when one of its outputs turns high and the other low. When a new comparison cycle begins (latch command), the latch output is reset to V_{DD} through transistors M_7 and M_8 . Not shown in the figure, digital inverters are usually connected at the outputs to raise the signals to full digital logic levels.

One of the advantages of using positive feedback is that the time response can be very fast thanks to the positive exponential transfer characteristic of the latch.

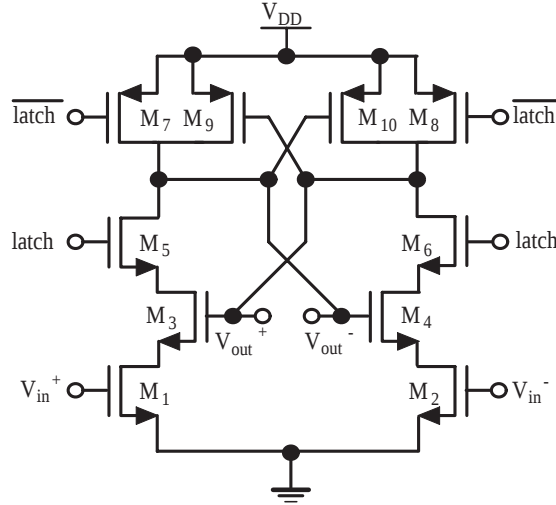


Figure 3.30. Latch comparator circuit [2].

However, due to mismatches present in the transistors, the resulting offset voltage limits the maximum resolution achievable with this circuit. In order for the latch to operate in the exponential region of its transfer characteristic, the minimum resolvable input must be large enough to overcome the large offset voltage, typically in the range from 30 to 100 mV.

Final Remarks

It was described above that the gain required to achieve a high resolution resulted in a comparator with a large delay. The use of a latch comparator would provide a very fast time response, but only for large input differences due to its input offset voltage. The optimal solution that allows to reach a trade-off between resolution and speed consists of combining a pre-amplifier and a latch. The gain needed by the preamplifier will depend on how large is the offset voltage produced by the latch circuit. The idea is to provide enough linear amplification so that the difference seen at the latch input is large enough for the latter to work in the exponential region of its input/output characteristic. In the next section and in later chapters various

architectures that follow this approach will be presented.

3.3.3 Comparator Offset Cancellation

As discussed in Section 3.3.2 the offset voltage inherently present in comparators limits their resolution. Although the offsets resulting from matching errors can be alleviated through the use of layout techniques such as common-centroid, those produced by random process variations call for different techniques. One way to partially eliminate such type of offset errors is using offset cancellation techniques [3, 20]. In the following section, two architectures typically employed for offset cancellation will be discussed along with the advantages and disadvantages of each.

Input-Offset Storage (IOS)

The *input offset storage* scheme is illustrated in Figure 3.31². The comparator makes use of switches and capacitors to store the offset voltage present at its input. Circuit operation is divided into two phases by using non-overlapping clock signals. During the first phase, ϕ_1 , the offset present in the preamplifier and latch is stored in capacitors C_1 and C_2 . This is done by configuring the preamplifier in unity-feedback mode with switches S_1 through S_4 . In the second phase, ϕ_2 , the above mentioned switches are opened while switches S_5 and S_6 are closed. The input signal is connected to the comparator's input, allowing the latter to perform the comparison. This last phase must allow the latch to be strobed in order to sense the amplified output provided by the preamplifier. Under this scheme, the preamplifier must be stable when configured in the unity-feedback configuration. As a result, it becomes necessary to employ compensation techniques.

²Although the discussion shows a comparator composed of a preamplifier and a latch, the concept can also be applied when only a preamplifier is used.

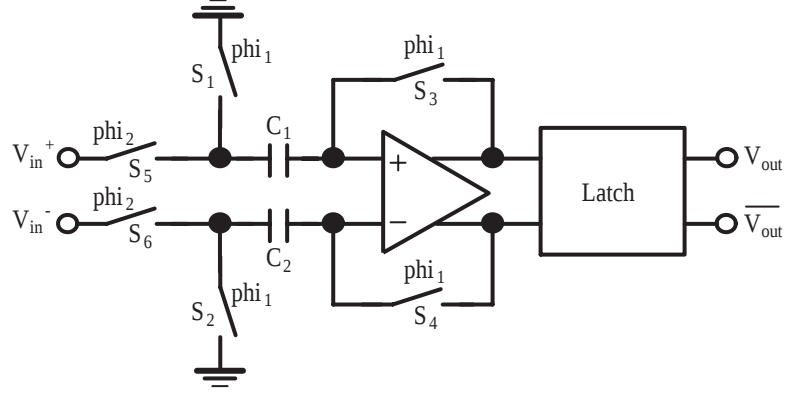


Figure 3.31. Input-offset storage technique [3].

Under the IOS scheme, the remaining offset after cancellation has three components. These are the preamplifier's offset reflected to its input (V_{OS}), the charge injected by switches S_3 and S_4 , and the latch's input offset as seen at the comparator's input ($V_{OS(latch)}$) [20]. Of these offset components, only the one introduced by charge injection is not reduced. An expression for the final offset after cancellation is given by

$$V_{OS(final)} = \frac{V_{OS}}{1 + A_0} + \frac{\Delta q}{C} + \frac{V_{OS(latch)}}{A_0} \quad (3.16)$$

Distinctive features of the IOS scheme are rail-to-rail input common-mode range and the improved overdrive recovery provided by the unity-gain feedback. The most important disadvantage is the kT/C noise, produced by the input sampling capacitors, that will disturb the input signal during the preamplification mode. Increasing the size of these capacitors to minimize the noise will lead to a slower circuit time response. Another disadvantage is the need for compensation in the preamplifier; needed for stable operation under the unity-feedback configuration.

Output-Offset Storage (OOS)

Figure 3.32 illustrates the *output offset storage* scheme. It works in a similar fashion to the previous scheme. The main difference is that in neither of the two clock phases the preamplifier operates in unity-feedback mode. During phase ϕ_1 the MOS switches connected to ground are “on” and the offset is stored in the capacitors. During phase ϕ_2 these switches are “off” and input is connected to the comparator allowing comparisons to be made. As in the previous scheme, this last phase must allow the comparator to fully resolve the input difference.

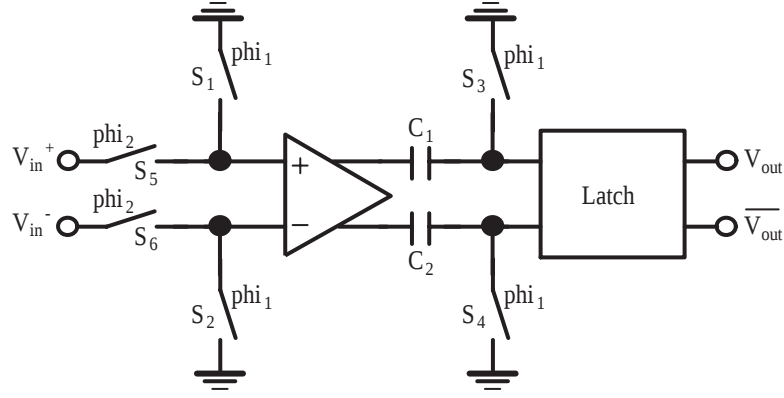


Figure 3.32. Output-offset storage technique [3].

For the OOS scheme the remaining offset after cancellation is reduced to two components, the charge injection of switches S_3 and S_4 and the latch offset [20]. As the sampling capacitors are located at the preamplifier’s output, the offset voltage of the latter is completely canceled when reflected to the input. The final expression for the total offset remaining after cancellation can be written as

$$V_{OS(final)} = \frac{\Delta q}{A_0 C} + \frac{V_{OS(latch)}}{A_0} \quad (3.17)$$

The main advantages of OOS over IOS are the complete cancellation of the preamplifier's offset, the reduction in offset due to charge injection, and the lower input capacitance due to the placement of the sampling capacitors at the preamplifier's output. A disadvantage of OOS is the limited input common-mode range due to the DC coupling present. Moreover, the open-loop configuration in the preamplifier requires a lower gain to avoid saturating the preamplifier if a large offset voltage is present.

CHAPTER 4

Literature Review

Today's CMOS technologies are targeted toward VLSI digital circuits. As the applications in which these technologies are employed require higher level of integration and improved performance, the power consumption of a silicon chip rises. Along with the thinner gate oxides resulting from device scaling, it becomes necessary to lower the supply voltage used in an integrated circuit (IC). Although this works well for digital circuits, such an approach presents a number of challenges in the design of analog circuits. Among these challenges are the limited input range present in amplifiers and sampling circuits, and the consequent decrease in circuit speed due to the need for minimizing power consumption.

Data converters are mixed-signal circuits containing both analog and digital circuits. Hence, ADCs are no exception to the problem described above. When operated by a low-voltage supply these circuits suffer from reduced signal swings that limit their dynamic range. These limitations are produced by the constant transistor threshold voltage (V_{TH}) that results in lower gate overdrive ($V_{GS} - V_{TH}$) as the supply voltage becomes lower. Moreover, unlike digital circuits, analog circuits do not benefit with lower power dissipation as the supply voltage is reduced [21]. The circuit speed also becomes affected since operating the transistors in the triode region results in

decreased bandwidth.

As an example of the problems faced in low-voltage circuit design, consider a 12-bit ADC that must be operated from a 1-V power supply. Generating the quantization levels using a reference voltage equal to the power supply results in a ± 0.5 LSB weight of $122\ \mu\text{V}$. For resolutions higher than 12-bits it becomes very challenging to design such circuits since the LSB approach noise levels. If the trend toward voltage-scaling continues at its present rate, analog circuits will have to operate at 0.8 volts or lower [22]. The urgent need for solutions to the problem of low-voltage circuit operation therefore becomes obvious.

A *technology-driven* technique available to alleviate the problem of low-voltage operation is the use of low- V_{th} CMOS processes. Besides providing transistors with nominal V_{th} , it has optional transistors with threshold voltages in the 0.1-0.2 V range [23]. The latter transistor is used in critical applications where a high gate-overdrive is needed. A disadvantage of this technique is the higher leakage-currents resulting from the difficulty of maintaining the transistors in the “off” state. Another drawback is the increased complexity and costs due to the additional fabrication steps required by the technology.

In the literature, most of the solutions found to the problem of low-voltage operation have employed *circuit-driven* techniques [24–27]. The main reason for this is that they only use standard CMOS process components, which results in lower costs when compared to the use of technology-driven techniques. Here, the focus is on modifying existing circuit structures, or developing new ones, that can work properly with low supply voltages.

For the reasons outlined above, the ADC prototype presented in this work only made use of circuit-driven techniques since they represent the most cost-effective solution to the problem at hand. Hereafter, the presentation focuses on highlighting

the circuit techniques employed in recent low-voltage SAR ADCs while identifying their advantages and disadvantages. A study of these provides a better understanding of the design choices that must be made in low-voltage data converter design.

Since the introduction of the first MOS implementation of a SAR ADC [4,17], its architecture has remained relatively unchanged [28–34]. As shown in Figure 4.1, the basic architecture consists of a charge-scaling DAC, a comparator, and digital control logic to implement the successive approximation algorithm. The only noticeable change found in some recent implementations has been the separation of the S/H function inherently present in the DAC [5,6,9,35,36]. When a charge-scaling DAC is employed in the ADC, using a separate S/H unit makes the input capacitance independent from the capacitor array. As a result, the ADC contributes less loading to the input circuitry or preceding stage.

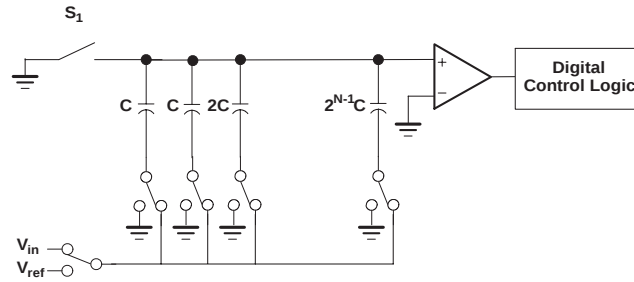


Figure 4.1. MOS Charge Redistribution ADC [4].

Table 4.1 summarizes the performance specifications of some of the most recent low-voltage SAR ADCs found in the literature. As pointed out earlier, there are two major architecture types for the SAR ADC: (1) the charge-scaling DAC with inherent S/H circuit and (2) the ADC with separate DAC and S/H circuit. The choice of the DAC architecture is one of the key aspects in low-voltage designs. It was discussed in Chapter 3 that voltage-scaling DACs are not used for resolution above 8-bits; the practical limit being between 4 to 6 bits. For this reason, the majority of SAR ADCs either employ a single charge-scaling [9,32,34] or current-scaling [5,6] DAC, or they

use a combination of subDACs [29]. The latter is typically used when it is required to obtain resolutions above 10 bits.

Table 4.1. Recent SA ADCs found in the literature.

Reference	Year	Supply	Resolution	Speed	Power	Technology
J. Park	2000	1.5 V	10-bit	500 kS/s	1 mW	0.25 μm
S. Mortezapour	2000	1 V	8-bit	50 kS/s	0.34 mW	1.2 μm
C.J.B. Fayomi	2001	1 V	12-bit	200 kS/s	-	0.18 μm
F. Kuttner	2002	1.2 V	10-bit	20 MS/s	12 mW	0.13 μm
M. Scott	2003	1 V	8-bit	100 kS/s	3.1 μW	0.25 μm
J. Sauerbrey	2003	1 V	9-bit	150 kS/s	30 μW	0.18 μm

Figure 4.2 illustrates a technique used in [5] to design a low-voltage R-2R ladder. The technique consists in setting the input common-mode (CM) level of the op amp close to ground in order to provide enough gate overdrive to the NMOS switches. Since the sum of the NMOS and PMOS threshold voltages (0.6 and -0.8 V, respectively) is greater than V_{DD} , the use of transmission gates is not possible. The reason for this, as illustrated in Figure 4.3, is the presence of a nonconducting zone where both type of transistors are “off”. The lowest supply voltage that can be used with this architecture depends on technology and noise considerations. As the supply voltage decreases so must the input CM level at node V_X . Otherwise, the switches won’t operate properly for a specific technology (i.e., V_{th} value). On the other hand, setting V_X too close to ground results in increased noise levels that degrade the SNR.

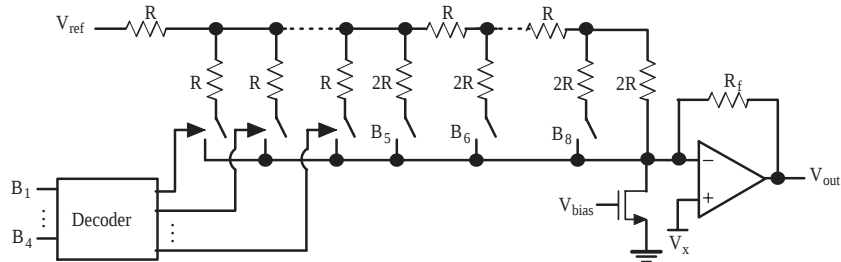


Figure 4.2. Low-voltage DAC (R-2R ladder) from [5].

In the ADC from [6] two DAC architectures were investigated. The first one, shown in Figure 4.4, consisted of an R-2R ladder working in voltage-mode. As the

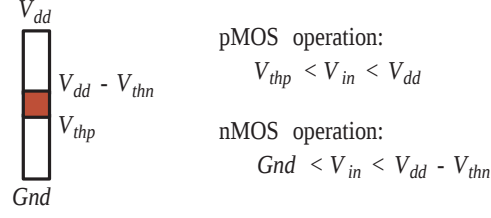


Figure 4.3. Operation range of a CMOS switch.

DAC output is connected to a high impedance node (i.e., comparator's input) no output buffer is required. The other implementation (see Figure 4.5) made use of MOS transistors to scale the current across the network. Its main limitation is the need for a low-voltage current-to-voltage converter (IVC) which not only complicates the design but also limits the circuit's speed and increases the power consumption. The proposed IVC from [6] made use of *clock boosting techniques* to properly turn-on the switches. This is not a true low-voltage technique due to the excessive oxide stress generated by the boosted clock signal (usually $2 \cdot V_{DD}$).

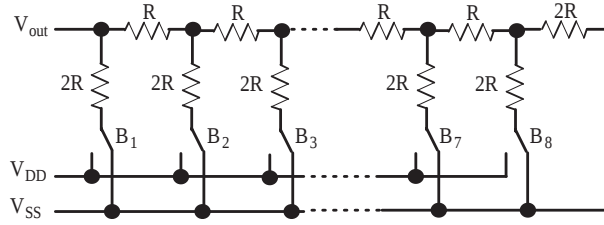


Figure 4.4. Low-voltage R-2R DAC from [6].

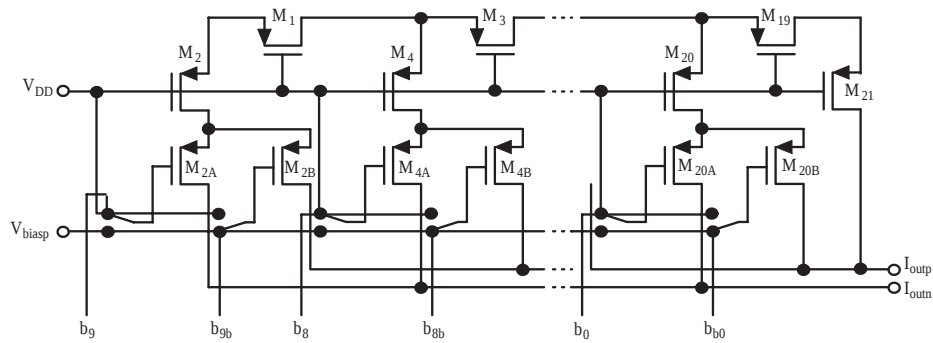


Figure 4.5. MOSFET-based current DAC from [6].

In the conventional charge-scaling DAC from Figure 4.1, switch S_1 is normally referenced to a mid-supply analog ground in order to avoid leakage currents. However, this can not be done under ultra low-voltage conditions ($V_{DD} < V_{thn} + V_{thp}$) due to the limited gate-overdrive available for the switches. In [9], the problem was avoided by separating the S/H function and referencing all switches to V_{DD} and V_{SS} . A second modification made to the circuit was to incorporate an additional capacitor, acting as a voltage divider, to make the DAC's output voltage range compatible with the comparator's input range. This guarantees proper ADC operation over the full input voltage range.

From the previous discussion it becomes obvious that one of the most critical components in low-voltage DAC design is the MOS switch. For proper function, it must be referenced to V_{DD} (PMOS) or ground (NMOS) for maximum gate overdrive. For rail-to-rail input range, the CMOS switch can only be used if $V_{DD} > V_{thn} + V_{thp}$. The use of clock-boosting or bootstrapping techniques do not constitute true low-voltage techniques since they introduce reliability issues to the circuit.

The input voltage range of low-voltage op amps is limited to around $V_{DD}/2$ or less when their input stage incorporates a single NMOS or PMOS differential pair. A technique incorporating complementary input differential pairs can be used to increase the input voltage range [24]. The complementary pair, shown in Figure 4.6, is composed of an NMOS differential pair and a PMOS differential pair. The first one operates for common-mode input voltages close to V_{DD} and the latter operates for common-mode input voltages close to V_{SS} . For mid-supply input voltages, both differential pairs operate simultaneously. However, the technique can not be used at ultra-low supply voltages due to a nonconducting gap that exists where both input pairs are “off”.

Since the comparator requires no compensation, it suffers from the same input

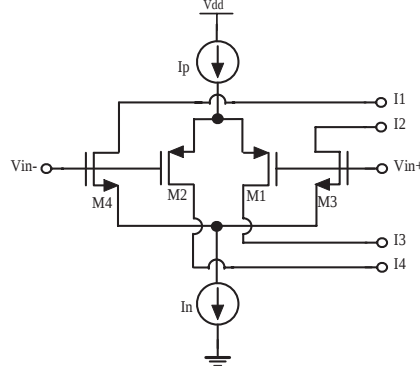


Figure 4.6. Rail-to-Rail input-stage.

range limitations discussed above. Besides the work presented in [25, 26, 37], few solutions have been proposed for the design of op amps with rail-to-rail inputs. One of those solutions is found in [5], where a current-mode approach was followed for the design of a 1-V comparator (see Figure 4.7). The main limitation of this comparator is that most of its gain is provided by the latch (the input stage consists of an low-voltage current mirror). As this leads to a slower time response, the ADC's conversion rate was not high (50 kS/s).

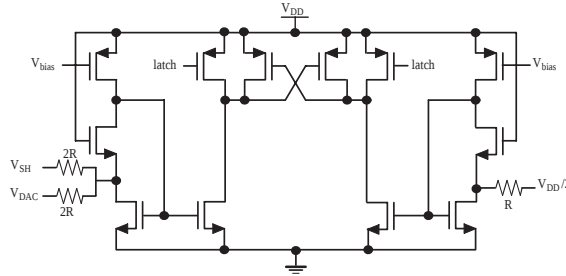


Figure 4.7. Low-voltage regenerative comparator from [5].

The conventional comparator implementation found in the literature consists of a preamplifier followed by a regenerative latch. A typical circuit with such architecture is shown in Figure 4.8. As mentioned in Chapter 3, the preamplifier is needed to overcome the latch's offset voltage, which has limited resolution. This is specially true in SAR ADCs where no redundant bits are used and the resolution of the comparator

must be better than an LSB. An advantage of this type of circuit is that the latch's regenerative nodes are not capacitively coupled to the input. As a result, this comparator exhibits low kickback noise. A disadvantage is the static power consumption of the preamplifier.

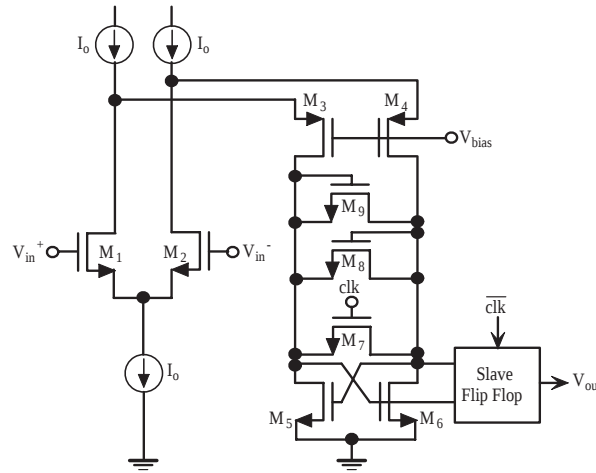


Figure 4.8. Typical comparator with a preamplifier and a latch [7].

To reduce the power consumption of the previous comparator, dynamic-type comparators have been devised. A circuit example is shown in Figure 4.9. Its operation proceeds as follows. During the preamplification phase, the “latch” signal is high and transistors M_7 and M_8 are off. Transistors M_9 and M_{10} now operate as the active load of the input transistors M_3 and M_4 . Since transistors M_5 and M_6 are on, the input voltage is temporarily stored at the drain nodes of M_9 and M_{10} . When the latch signal falls, the latch stage is activated and the input stage is disabled. Depending on the polarity of the input signal, one of the drain nodes of M_9/M_{10} will go high while the other will go low. The digital inverters are used to raise the comparison outputs to full digital logic levels. In general, the disadvantage of such circuits is the kickback noise present at the input. Since the latch is typically used as the load of the input stage, the comparator input is not properly isolated from the latch during the regeneration phase.

Such comparator is well suited for use in successive approximation ADCs.

CHAPTER 5

Circuit Design

The proposed SAR ADC prototype (1.2-V, 8-bit, 615 kS/s, 705 μ W) was designed using IBM's 0.18 μ m CMOS process. The technology provides six levels of metal (copper and aluminum) with V_{th} values of 0.38 V and -0.4 V for the NMOS and PMOS transistors, respectively. An extension to that technology provides optional passive devices for analog circuit design, including MIM (Metal-Insulator-Metal) and thick oxide MOS capacitors.

In previous chapters the basic data conversion principles were discussed. Understanding these concepts provides the necessary knowledge for proper ADC design. The rest of this chapter focuses on describing the circuit design of the SAR ADC prototype. The design choices made for each circuit block are discussed and their respective performance specifications are presented through analytical calculations and simulations.

Figure 5.1 illustrates the block diagram of the ADC prototype. It consists of a S/H circuit, a DAC, a comparator, and digital logic. The latter implements the successive approximation algorithm and generates the necessary control signals to synchronize the operation of all the ADC circuit blocks.

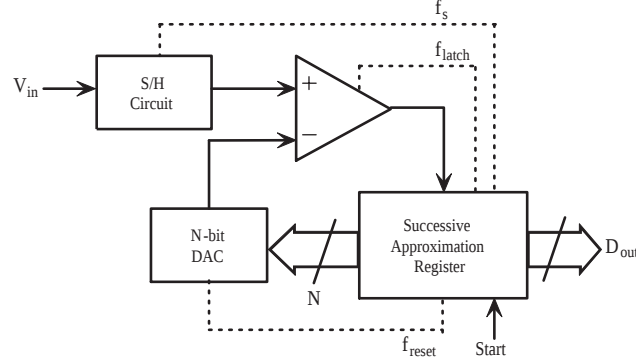


Figure 5.1. Block diagram of the SAR ADC prototype.

5.1 Sample-and-Hold Circuit

The conversion process of a successive approximation ADC begins at the S/H circuit. Figure 5.2(a) shows the S/H circuit used for this work. It is composed of a sampling switch transistor, M_S , and a holding capacitor, C_H . Besides these, two dummy switch transistors, M_{d1} and M_{d2} , were added. The selection of this circuit was driven by simplicity and power consumption considerations. The main disadvantage of such circuit is the distortion introduced by the input-dependent charge injection of M_S . To minimize this source of error, *dummy switch compensation* was employed with switches M_{d1} and M_{d2} [16]. Moreover, if the comparator's input capacitance is negligible, its high input resistance eliminates the need for an output buffer in the S/H circuit (see section 5.3.3).

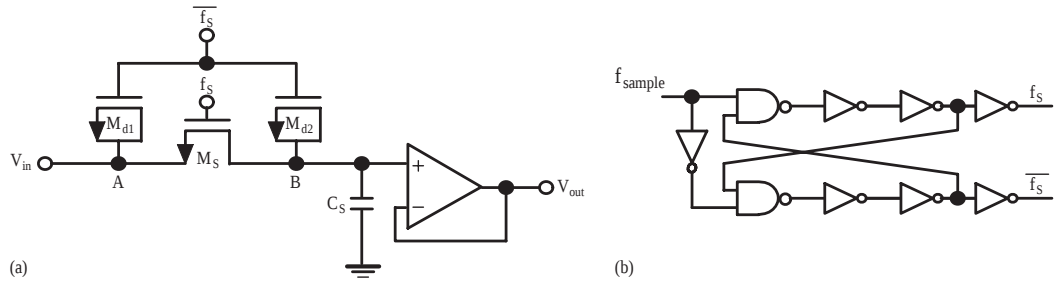


Figure 5.2. (a) S/H circuit [9] and (b) nonoverlapping clock circuit [10].

The operation of the circuit proceeds as follows. When the external “Start” signal

is asserted, the control logic (SAR) initiates the conversion process by sending a signal, f_{sample} , to the clock circuit of Figure 5.2(b). This circuit generates a pair of nonoverlapped signals, f_s and $\overline{f_s}$, that initially are set to “1” and “0”, respectively. With this condition, sampling switch M_S is “on” and dummy switches M_{d1} and M_{d2} are off; setting the S/H circuit into sample mode. During the following clock cycle, f_{sample} falls to “0” and the nonoverlapped signals interchange states. Now M_S is off and the dummy switches are on, which establishes the S/H circuit’s hold mode operation. The sampled signal stored in capacitor C_H can now be used by to subsequently produce its corresponding digital code.

It is important to understand how transistors M_{d1} and M_{d2} realize the charge-injection cancellation. When transistor M_S is turned off at the end of the sample mode, the charge present in its channel exits through terminals A and B (see Figure 5.2(a)). Since each dummy switch has its drain and source terminals connected together, the operation of these transistors reflects that of a capacitor. When the dummy switches are activated at the end of the sampling mode, M_{d1} and M_{d2} absorb the charge released by M_S . Although part of the charge will be absorbed by C_H , the charge-injection error introduced into the sampled value will be smaller.

The settling time of the S/H circuit is another important design consideration, as it influences the conversion speed of the ADC. The output of the circuit is considered settled when it is within ± 0.5 LSB of its final value. Based on the exponential response, the permissible settling error in the sampled signal is given by

$$\varepsilon_{settling} = e^{-t/R_{on}C_S} < \frac{1}{2^{N+1}} \quad (5.1)$$

where R_{on} is the switch on-resistance, C_H is the sampling capacitor, and N is the ADC resolution. For 8-bit accuracy, the settling time is 6.2 time constants ($6.2R_{on}C_S$).

The sampling switch M_S , shown in Figure 5.2, was sized with a width, W_s , of $12\ \mu\text{m}$. Choosing this width reduces the worst-case on-resistance for input voltages near mid-supply range (i.e., $V_{DD}/2$). To minimize charge injection errors, the switch must be made as small as the linearity and speed requirements allow. Assuming equal charge injection in nodes A and B, transistors M_{d1} and M_{d2} were each sized with a width, M_d , equal to $0.5W_s$ (i.e., $=6\ \mu\text{m}$)¹. Minimum length sizes were used for all switches. Since nonoverlapping clock signals are used (see Figure 5.2 (b)), the sampling speed is not influenced by the dummy switches.

For a worst-case condition of $V_{in} = V_{DD}$, the switch's (M_S) on-resistance obtained from PSpice² simulations was 400 ohms. The actual on-resistance will be smaller since the maximum input voltage specification for the ADC is 0.55 volts (see section 5.3). The value of the sampling capacitor was selected as 6 pF, based on speed requirements and noise considerations. Using equation (5.1), the required settling time for the S/H circuit is 15 ns.

5.2 8-bit Digital-to-Analog Converter

The DAC used for the SAR ADC is based on the charge-scaling architecture. A circuit schematic of the DAC is shown in Figure 5.3. The main advantages of this architecture over current-scaling DACs are the minimal changes needed for low-voltage operation and its lower power consumption. As is the case for the S/H circuit, a large comparator input capacitance requires that a buffer be placed at the DAC's output. This buffer is needed to isolate the DAC output voltage from the voltage

¹The charge injected at each terminal depends on the impedance seen by these and by the clock transition time. As a result, the actual charge injected by a transistor can not be predicted. However, using $W_d = 0.5W_s$ slightly reduces the charge injection error.

²The PSpice software is copyrighted by Cadence Design Systems, Inc.

attenuation introduced by the nonlinear input capacitance (see section 5.3.3).

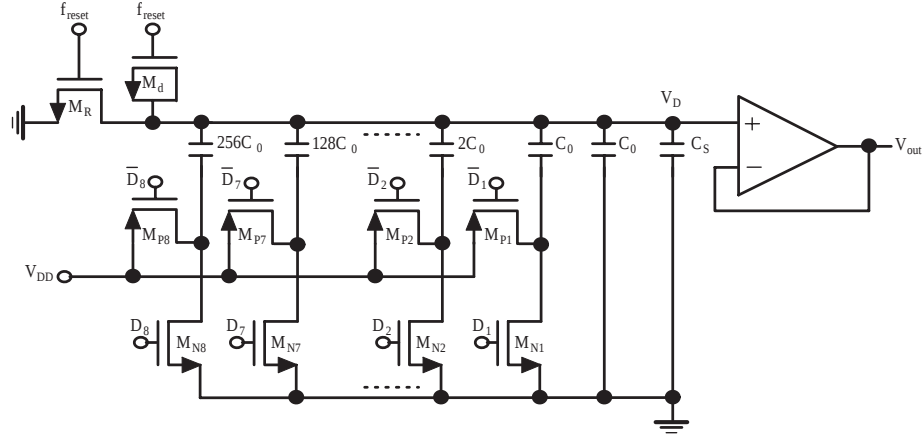


Figure 5.3. 8-bit charge-scaling DAC.

The circuit, as shown in Figure 5.3, has two modes of operation. During the sampling phase of the S/H circuit, the SAR logic enables the DAC's reset mode. At this time, switches M_R and M_{N8} through M_{N1} are activated and the capacitor array is discharged. Once the reset phase ends, which coincides with the end of the S/H circuit's sampling phase, the reset switch M_R is deactivated and the dummy switch M_d partially cancels the offset error introduced by M_R . The second operating mode marks the beginning of the successive approximation cycle. As explained in section 2.2.4 it lasts N clock cycles.

5.2.1 Capacitor Array

The accuracy of the DAC sets the limit on the maximum resolution that can be obtained in the ADC. This is directly influenced by capacitor matching. In order to minimize matching errors, the array design begins by properly sizing the unit capacitor, C_0 , for the required linearity (i.e., 8-bits). The remaining capacitors are designed based on the required resolution and the binary weighted values of the unit capacitor.

In the design of the DAC, parasitic capacitances must also be taken into account. Generally, the bottom plate of the capacitor has larger parasitics than the top plate [4, 34]. To minimize the voltage attenuation introduced by these, the top plate of the capacitors are connected to the DAC output node. However, this increases the settling time since the switches will drive a larger capacitive load.

Accounting for array parasitics and buffer input capacitance, the output voltage of the DAC becomes

$$V_{out} = V_{ref} \left(\frac{C_{array}}{C_{total} + C_s + C_{buffer}} \right) \quad (5.2)$$

In equation (5.2), V_{ref} represents the reference voltage which is equal to the supply voltage. C_{array} is the total array capacitance that must be charged in a given bit approximation cycle. C_{total} and C_{buffer} are the total array capacitance and the buffer's input capacitance, respectively. C_s is the scaling capacitor used to adjust the DAC's output voltage according to the comparator's input voltage range.

To save power consumption, the value of the unit capacitor should be as small as the linearity requirements allow. In [34] and [9], the chosen unit capacitance values were 15 fF and 20 fF, respectively. These choices were made for a 0.25 μm process in [34] and for a 0.18 μm process in [9]. Based on the limited process data available and the design presented in [9] for a similar process (i.e., 0.18 μm), a 20 fF unit capacitor was chosen in this work. The capacitor array is not silicon area intensive thanks to the large capacitor densities provided by the process (up to 7.9 fF/ μm^2). Table 5.1 shows the capacitor values for the array.

The value of the C_s capacitor was selected based on the input voltage range of the ADC, as imposed by the comparator (i.e., 0 - 0.55 volts). This is required in order to guaranteed proper comparator operation over the whole input range. With

Table 5.1. Design parameters for the capacitor array.

Capacitor	Value
C_0	20fF
C_1	20fF
C_2	40fF
C_3	80fF
C_4	160fF
C_5	320fF
C_6	640fF
C_7	1,280fF
C_8	2,560fF
C_s	6,050fF

$C_{array} = 5120fF$ and $V_{ref} = 1.2V$, the C_s capacitor is calculated from the following equation

$$V_{out,max} = V_{ref} \left(\frac{C_{array}}{C_{array} + C_s} \right) \quad (5.3)$$

With the reference voltage and output range of the DAC already established, the least-significant-bit can be calculated. Using equation (2.1) and the selected values for V_{ref} and C_s , the LSB value of the 8-bit DAC is 2.15 mV. Since the quantization levels of the ADC are set by those of the DAC, the LSB of the ADC is equal to that obtain with equation 2.1.

5.2.2 Switches

For low-voltage operation, the transistor switches need maximum gate overdrive (i.e., $V_{DD} - |V_{th}|$). To achieve this, the voltage references must be selected as V_{DD} and ground for the PMOS and NMOS transistors, respectively. The main disadvantage of this approach is the degradation of Power Supply Rejection Ratio (PSRR). Variations in power supply voltage will be reflected in the DAC's output voltage and, consequently, in the output codes of the ADC. Under extreme operating conditions

following this approach will result in conversion errors, requiring the use of a supply-independent reference voltage. The downside to this solution is that the ADC's power consumption will increase due to the complexity of the reference voltage circuitry.

The settling time of the DAC depends on the RC path created by the switch on-resistance and the array capacitance. When used as part of a SAR ADC, the DAC's worst-case settling time occurs during the approximation of the MSB (i.e., $\approx V_{DD}/4$). This case corresponds to a transition in the input code from 00000000 to 10000000 and, hence, the charging of capacitor C_8 ($=256C_0$). Similar to the S/H circuit, the required settling time must comply with equation (5.1).

A fast time response can be obtained by selecting large transistor widths for the switches. However, this will produce an increase in parasitic capacitances, degrading the accuracy of the DAC. When designing the switches, a tradeoff must be made between speed and accuracy. In this work, the switches were designed with the smaller possible widths that would satisfy the speed requirements while complying with equation (5.1). Table 5.2 summarizes the design parameters for the DAC.

Table 5.2. Design parameters for the switch network.

Device	Design value	R_{on}	$T_S = 6.2R_{on}C$
M_N	5 μm	960 Ω	15.27 ns
M_P	15 μm	655 Ω	10.4 ns
M_R	1.2 μm	-	-
M_d	0.6 μm	-	-

As shown in Figure 5.3, the NMOS transistors (M_N) are used to connect the capacitors to ground, while the PMOS transistors (M_P) are used to connect the capacitors to V_{DD} . Using equation (5.1), the estimated DAC settling time is 10.4 ns. Although the NMOS switches have a slightly larger on-resistance, this is not of concern since the worst-case discharge only occurs during the reset phase. In this phase node V_D is also connected to ground through reset switch M_R , creating

a short circuit that accelerates the discharge of the capacitor array. To reduce the charge injection error introduced by M_R , its size must be chosen close to minimum size. A dummy switch, M_D , is used to suppress the charge injected by M_R . The resulting offset error obtained from simulation was $10\ \mu\text{V}$, well below the ± 0.5 LSB specification.

5.2.3 Conversion Time

The conversion time of the ADC depends on three things: the duration of the sampling phase, the settling time of the DAC, and the time required by the comparator to accurately resolved the difference between the sampled signal and the DAC's output. It must be noted that since the hold command is issued at the beginning of the first approximation cycle, enough time must be given for the sampled value to settle. The conversion time is then define as

$$T_{conversion} = t_{sampling} + N(t_{DAC} + t_{comp}) \quad (5.4)$$

where the buffer's settling time is negligible compared to that of the DAC and the comparator, t_{DAC} and t_{comp} , respectively.

5.3 Comparator

The ultimate limit on the conversion time of a SAR ADC is set by the comparator. The conversion of the analog signal into a digital code is done through the comparator by successively approximating each code bit. Since eventually the comparator must be able to resolve the input signal down to ± 0.5 LSB of precision, a high precision

circuit is required. Consequently, each comparison must be done in the shortest possible time frame.

5.3.1 Proposed Circuit

Chapter 3 discussed the benefits of a comparator architecture that uses both a preamplifier and a latch circuit. Specifically, it explained the speed/resolution tradeoff that can be made by combining a moderate-gain preamplifier with a fast regenerative latch. Chapter 4 highlighted the speed degradation found in recent low-voltage comparators. This problem is produced by the limited gate overdrive of MOS switches and the time constant resulting from their high on-resistance. As a result, the minimum allowable supply voltage is limited. Moreover, the low-gain provided by the preamplifier limits their use in successive approximation ADCs.

To overcome the above mentioned limitations, the solution proposed in this work consists of employing the Switch Opamp technique [27] in the preamplifier stage of the comparator. By making the output stage switchable, the critical switches connecting the preamplifier with the latch can be eliminated. In this way, the speed performance of the comparator will not be limited by a signal path with high resistance. Furthermore, during the regeneration phase the preamplifier is disconnected from the latch, thus reducing the kickback noise reflected to the comparator input.

The proposed “Switched Opamp Comparator” is based on the low-voltage op amp presented in [11] and the dynamic latch used in [12]. These are shown in Figure 5.4 and Figure 5.5, respectively.

The low-voltage op amp is composed of three stages. The first stage is a PMOS differential pair (M_1/M_2) with an NMOS cross-coupled active load (M_4-M_7). The NMOS cross-coupled load also serves as a Common-Mode Feedback (CMFB) circuit that maximizes the signal swing by maintaining the output CM level near mid-supply

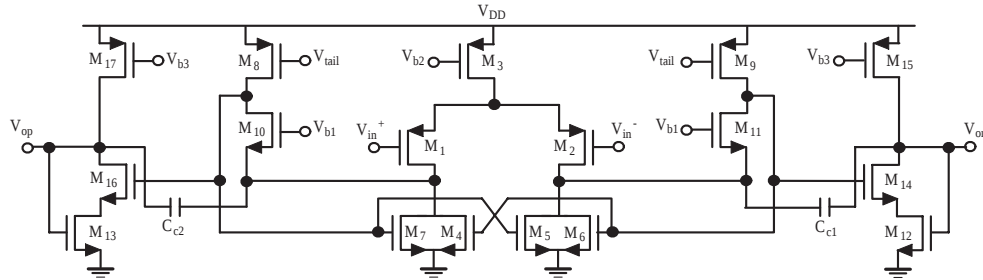


Figure 5.4. Low-voltage op amp from [11].

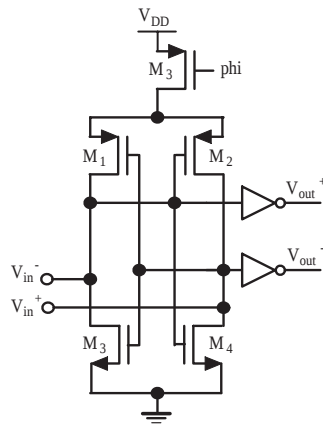


Figure 5.5. Dynamic latch from the comparator presented in [12].

range. A common-source inverter (M_{15}/M_{14} and M_{17}/M_{16}) is used as the output stage, with transistors M_{12}/M_{13} acting as its CMFB circuit. A folded-cascode stage (M_9/M_{11} and M_8/M_{10}) is use to raise the low output level of the first stage and properly drive the output stage.

The main characteristics needed in a preamplifier are moderate gain (i.e., 40-60 dB) and high bandwidth. The gain sets the maximum resolution for the comparator, while the bandwidth determines its time response. The circuit from Figure 5.4 was deemed suitable for this work, since its performance specifications for the original application [11] provided high-gain (100 dB) and 205 MHz³. The small-signal voltage gain of the op amp is given by [40],

$$A_v = \left(\frac{-g_{m1}R_O r_{O9}(1 + g_{m11}r_{O11})}{R_O(1 + g_{m11}r_{O11}) + r_{O11} + r_{O9}} \right) \cdot g_{m14}(r_{O14} // r_{O15}) \quad (5.5)$$

where $R_O = r_{O2} // r_{O7}$.

The dynamic latch of Figure 5.5 consists of complementary (NMOS and PMOS) cross-couple loads. These are followed by inverters that raise the output to full digital logic levels. The use of both types of transistors results in a faster time response (i.e., <2 ns).

The circuit operation proceeds as follows. Once a large input (i.e., 100 mV) has been applied between terminals V_{in}^+ and V_{in}^- , the latch is activated by signal “phi” at the gate of M_3 . Using positive feedback, the PMOS flip flop starts the regeneration process. Once the drain and gate voltages of the NMOS flip flop have reached appropriate levels, the NMOS flip flop is activated and contributes to the regeneration. Operated at 1.5 V in the original work [12], the latch provided 4-bit

³This specifications are based on the use of the Replica Amplifier technique. The specifications of a single op amp were not presented in [11]

accuracy (i.e., 93.75 mV) at a regeneration speed of 2 ns and a power consumption of 69 μ W.

The op amp from Figure 5.4 was modified as follows. First, transistors M_{12}/M_{13} were changed to operate as switches instead of acting as a CMFB circuit. The CMFB of the first stage is enough to allow proper operation of the latch, which will set the comparator output into one of its binary states. Then, PMOS switches M_{18}/M_{19} were added between V_{DD} and the drain terminal of transistors M_{15}/M_{17} . The NMOS switches disconnect the output stage from ground while the PMOS switches disconnects the output stage from V_{DD} . With these modifications, complementary nonoverlapping clock signals can be used to operate these switches and turn “on” and “off” the output stage. The control signals are derived from the SAR’s master clock, with a circuit such as that shown in Figure 5.2(b). Transistors M_{23A}/M_{24A} were added for resetting the comparator outputs during the preamplification phase. The proposed comparator is shown in Figure 5.6.

It is important to note that since only a PMOS differential pair was used in the input stage, the Input Common-Mode Range (ICMR) of the comparator is not defined as rail-to-rail. To guaranteed proper comparator operation, the DAC circuit was modified as shown in Figure 5.3 [9]. The comparator’s minimum and maximum common-mode voltages, V_{icm}^- and V_{icm}^+ respectively, are given as

$$V_{icm}^- = 0 \quad (5.6)$$

$$V_{icm}^+ = V_{DD} + V_{thp} - V_{DS3} \quad (5.7)$$

With an overdrive voltage, V_{DS3} , of 200 mV and V_{thp} being equal to 400 mV, the maximum common-mode voltage allowed is 0.6 V. This specification allows all transistors to operate in the saturation region. To guarantee proper operation against

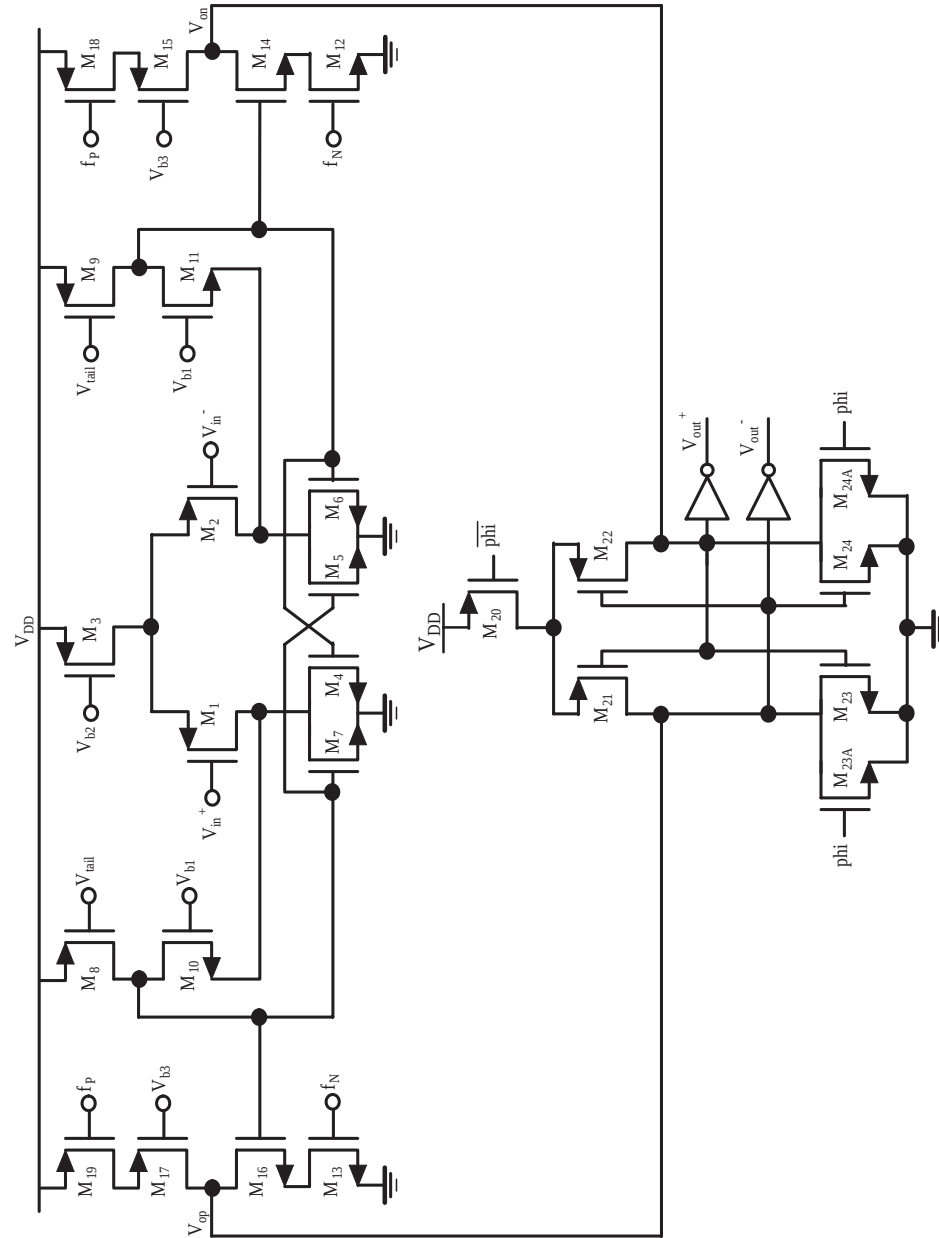


Figure 5.6. Proposed Switched-Opamp Comparator.

process variations, the ICMR of the comparator was defined from 0 to 0.55 volts.

5.3.2 Preamplifier and Latch Design

Table 5.3 summarizes the design parameters used for the comparator circuit presented in the previous section. To reduce the effects of channel length modulation upon matching, the length of transistors (M_1/M_2) was selected as two times the minimum length. As suggested in [41], the cross-coupled load (M_4 - M_7) used four times the minimum length. To obtain optimal regeneration speed, the ratio between the width of the PMOS (M_{21}/M_{22}) and NMOS (M_{23}/M_{24}) transistors must be less than the ratio of the conductivity of the NMOS and PMOS transistors [12]. It must be highlighted that to minimize the offset errors, a physical realization would required the use of common-centroid layout techniques for the complete circuit.

Table 5.3. Design parameters for Switch Opamp comparator.

Device	W (μm)	L (μm)
M_1/M_2	75	0.36
M_3	30	0.36
$M_4 - M_7$	30	0.72
M_8/M_9	25	0.36
M_{10}/M_{11}	30	0.36
M_{15}/M_{17}	25	0.36
M_{14}/M_{16}	15	0.36
M_{18}/M_{19}	20	0.36
M_{12}/M_{13}	10	0.36
M_{20}	10.8	0.18
M_{21}/M_{22}	21.6	0.18
M_{23}/M_{24}	10.8	0.18
M_{23A}/M_{24A}	10.8	0.18
M_{25}/M_{26}	28.8	0.18
M_{27}/M_{28}	14.4	0.18

To simplify the design of the comparator, circuit biasing was done using the circuit shown in Figure 5.7. However, to provide temperature-insensitive biasing, a circuit

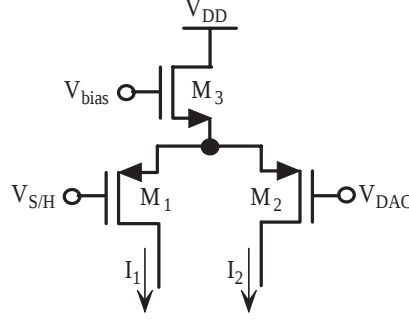


Figure 5.8. Preamplifier's input stage: a PMOS differential pair.

The gate capacitance is composed of three main components: the gate-to-source capacitance, C_{GS} , the gate-to-drain capacitance, C_{GD} , and the gate-to-bulk capacitance, C_{GB} . In practice, the C_{GB} component is negligible compared to the other terms, such that the gate capacitance can be approximated as

$$C_G \approx C_{GS} + C_{GD}$$

The problem with this parasitic capacitance and, hence, the comparator's input capacitance is that its value depends on the voltage applied to the gate terminal. As a result, the value of C_G follows a nonlinear dependence on the gate voltage. For the ADC prototype, both the S/H circuit and the D/A converter exhibit an output voltage range from 0 to 0.55 volts. As the output of these two circuits will not necessarily have the same output voltage at a given time, the capacitance seen from their respective comparator connections will not be the same. This results in a voltage attenuation that will differ among the two outputs, leading to possible conversion errors.

To solve the above problem, buffers were added at the outputs of the S/H circuit and the D/A converter. As shown below, the buffers consists of a one-pole op amp macromodel, as presented in [42]. The op amp has a low input-capacitance, C_{in} ,

a high input-resistance, R_{in} , and an open-loop gain given by the voltage-controlled source ea0. The buffer's bandwidth is 200 MHz, as given by resistor R_{eq} and capacitor C_{eq} .

```
* Dominant-pole op amp (buffer) macromodel
* open-loop gain (a0)=10 V/mV, f3db=200MHz
.SUBCKT Buffer Vn Vp Vout
Rin Vn Vp 500Meg ; input resistance
ea0 1 0 Vp Vn 10000 ; open-loop gain
Req 1 2 8k
Ceq 2 0 100fF ; f3db=1/2*pi*Req*Ceq
ebuf 3 0 2 0 1 ; output buffer
ro 3 Vout 50 ; output resistance
.ends Buffer
```

Although few implementations at the integrated circuit level are found in the literature [43], there are a number of discrete commercial implementations which could be ported into an IC with the ADC prototype presented in this work. More importantly, the performance specifications of those commercial circuits (i.e., Texas Instruments OPA 354) are similar or better than those specified in the macromodel used here.

A better alternative, not evaluated in this thesis, is to design the preamplifier of the comparator as a multi-stage gain op amp (typically 2-3 gain stages). By designing the first gain-stage with smaller transistors, the input capacitance of the comparator can be reduced. However, each gain-stage must be designed with higher bandwidth so that the settling time or comparison rate of the comparator remains relatively the same.

5.3.4 Simulation Results

To validate the design of the comparator and obtain its performance specifications, a number of Spice simulations were performed. The results obtained from these are now discussed. Then, the simulation results obtained for the S/H circuit, the DAC and the comparator (sections 5.1, 5.2, and 5.3, respectively), will be used to calculate the conversion speed of the ADC. The discussion ends with a summary of the performance specifications obtained for various comparator designs considered.

Frequency Response

As shown in Figure 5.9, the preamplifier achieved a voltage gain of 54 dB up to a 3dB frequency (f_{3dB}) of 4.2 MHz. Together with the exponential transient response of the latch stage, this lead to a resolution of 1 mV (± 0.5 LSB).

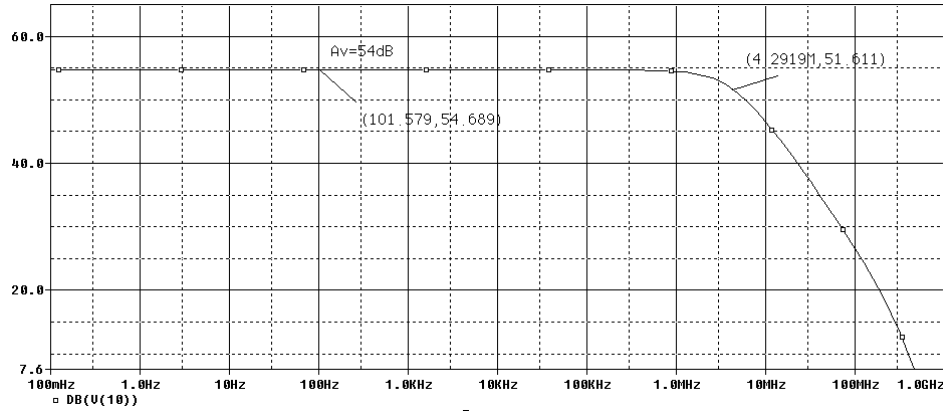


Figure 5.9. Preamplifier frequency response.

To verify that the resolution of the comparator was not limited by circuit noise, *AC-sweep* noise simulations were performed. As obtained from the simulations (see Figure 5.10), the input-referred circuit noise is less than $14nV/\sqrt{Hz}$ up to a frequency of 1MHz.

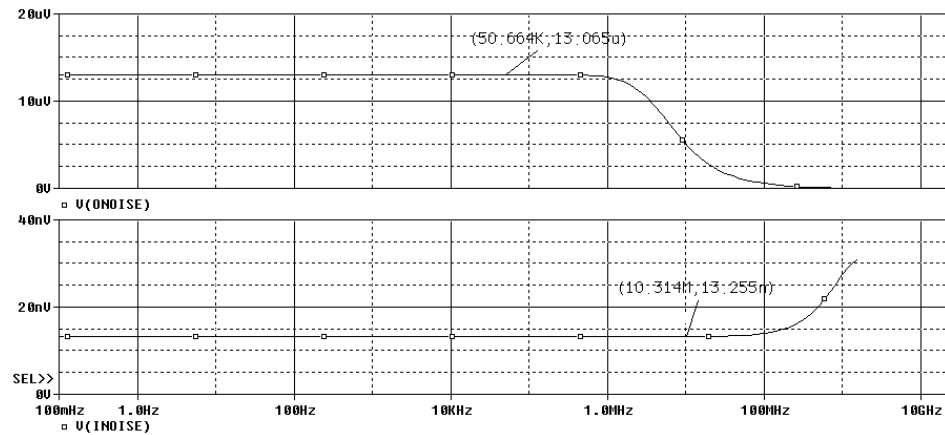


Figure 5.10. Preamplifier input (bottom) and output (top) noise response.

Transient Response

Figure 5.11 shows the response of the preamplifier to an input step of 1 mV. This is one of the most stringent tests performed on a comparator, since this is the case where the circuit takes the longest time in resolving the polarity of its input. It is seen that after 80ns the preamplifier output has already reached 800 mV.

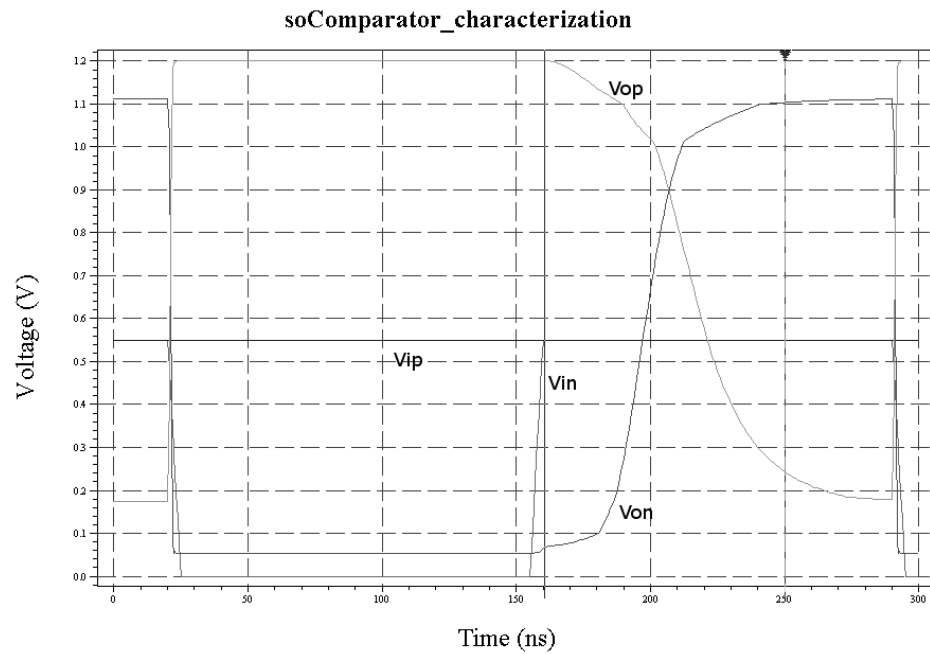


Figure 5.11. Preamplifier response to an input step of 1-mV input step.

Since the offset voltage of a typical latch has a value between 30 and 100 millivolts, the preamplifier's output level during the above mentioned case is sufficient to achieve proper comparator operation. For this reason, the latch can be activated right after the specified settling time has being reached even though the preamplifier's output is not fully settled. The response of the complete comparator circuit to such input step (i.e., 1 mV) is shown in Figure 5.12.

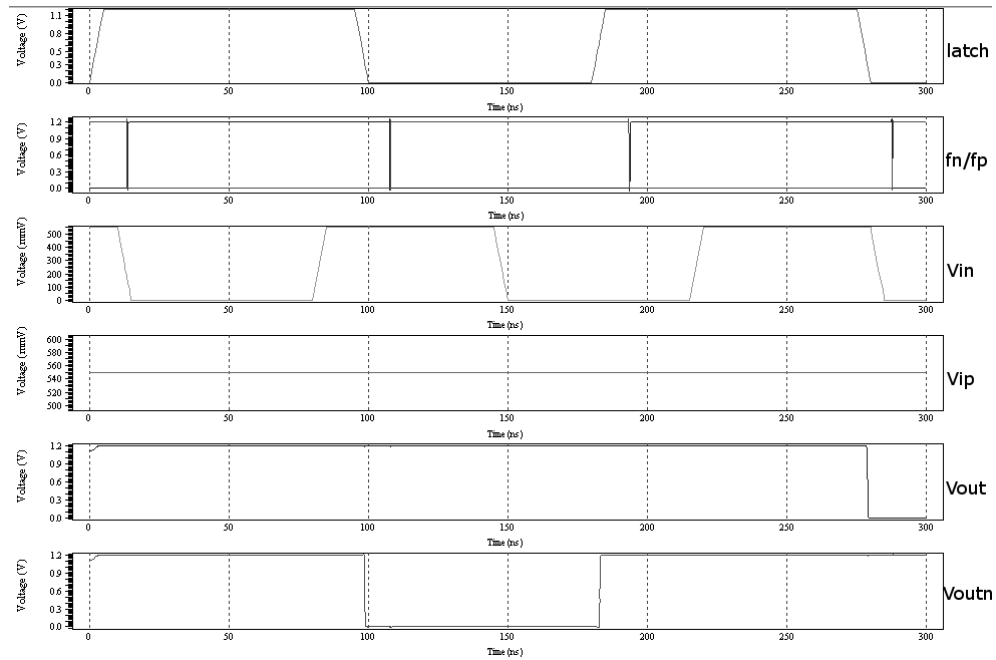


Figure 5.12. Comparator response to an input step of 1-mV.

Table 5.4 summarizes the performance specifications obtained for various designs of the proposed comparator. Originally, the design was done using AMI's 0.5 μm process. However, as seen from the table, a lower supply voltage was achieved using IBM's 0.18 μm process. The reason for the lower supply voltage achieved was the use of transistors with substantially lower threshold voltages ($V_{thn} = 0.38\text{V}$ and $V_{thp} = -0.4\text{V}$, against $V_{thn} = 0.6\text{V}$ and $V_{thp} = -0.9\text{V}$ for AMI's process). As a result, the first design was discarded in favor of the improved performance obtained with the IBM process.

Two designs were made for this process. The first design made (labeled #1) achieved a settling time of 40 ns; a decrease of 25 ns when compared to the original design. This

Table 5.4. Performance specifications of various comparator designs.

	AMI 0.5 μm	IBM 0.18 μm #1	IBM 0.18 μm #2
Supply voltage	1.8V	1.2 V	1.2 V
Gain	42 dB	48 dB	54 dB
Resolution	1.2 mV	1 mV	1 mV
f_{3dB}	13 MHz	19 MHz	4.5 MHz
Propagation delay	65 ns	40 ns	90 ns
Power dissipation	1.92 mW	1.54 mW	690 μW
SR^+	-	-	39.25 V/ μs
SR^-	-	-	15.3 V/ μs
Input capacitance	0.5 pF	0.1 pF	0.13 pF
V_{icm}^+	0.6 V	0.55 V	0.55 V
V_{icm}^-	0 V	0 V	0 V
Input noise	41.05 nV/ $\sqrt{Hz}$	8 nV/ $\sqrt{Hz}$	14 nV/ $\sqrt{Hz}$

can potentially lead to a higher ADC conversion rate. A slight improvement is also found in gain and, hence, resolution. Another notable difference can be seen in the comparator's input capacitance. Since the AMI process uses larger devices, the gate area occupied by each transistor results in large parasitic capacitances. Regardless of the application for which the comparator is employed, these capacitances can produce excessive loading to the driving circuitry.

The downside of the previous design is the power consumption obtained (i.e., 1.54 mW). Since the focus of this thesis was to achieve low power consumption, the design was modified (design #2) in order to decrease the power consumption of the circuit. The use of a class A output stage sets an absolute minimum in the power consumption of the circuit. Shown at the far right column of Table 5.12, the power consumption was reduced by a 50% factor compared to design #1. This comes at the cost of speed reduction, as reflected by the decrease in preamplifier's bandwidth and, hence, settling time. The operation of the circuit was also verified against temperature variations. The circuit was deemed operational for a temperature range from 20°C to 55°C .

Based on the worst-case settling times presented in sections 5.1 through 5.3, equation (5.4) can now be used to calculate the conversion time. Accounting for the S/H circuit and DAC settling times, a 5 MHz (180 ns) clock signal was used for the SAR logic. One half

of the clock period is used for the preamplification phase and the other half is used for the regeneration (latch) phase. Based on the 9 clock cycles (see section 5.4) needed by the SAR ADC to complete a conversion, the conversion speed is 615 kS/s.

5.4 Successive Approximation Register (SAR)

The successive approximation logic is based on the ring counter/shift register presented in [44]. Figure 5.13 shows the circuit schematic and Figure 5.14 illustrates its operation through a timing diagram. During the reset phase (clock cycle #1) all flip flops (FFs) are cleared; this activates the sample phase and triggers the start of a new conversion cycle. In the following clock cycle, the sample phase ends, setting the S/H circuit into hold mode. During the following eight clock cycles (2 through 9) the SAR logic uses the DAC and comparator to convert the sampled signal into a digital code (signals D_8 through D_1). The second row of FFs is used to store the decisions made by the comparator during each successive approximation cycle. An additional clock cycle was added to read the output data at the end of the conversion cycle, as indicated by the “Ready” signal.

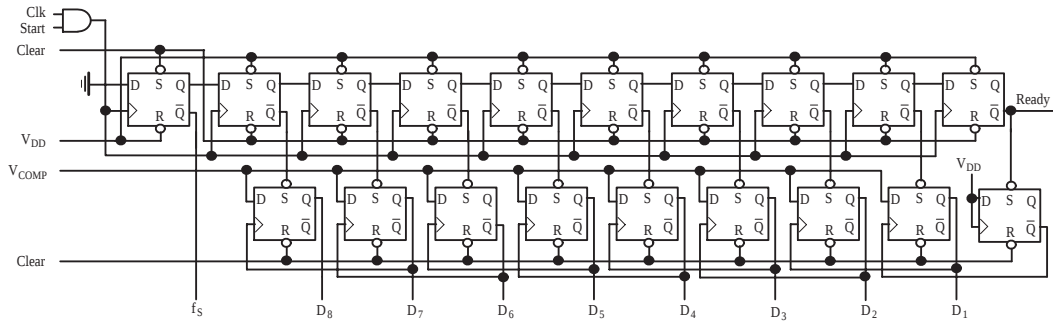


Figure 5.13. Circuit schematic for SAR logic.

The FFs and additional SAR logic were custom designed for this circuit. To minimize power consumption, small devices ($5\ \mu\text{m}$) were used for the NMOS transistors. PMOS transistors were sized four times as large in order to obtain a midpoint (V_M) transition region near mid-supply voltage. When the ADC is disabled ($\overline{\text{Start}}$), no clock transitions

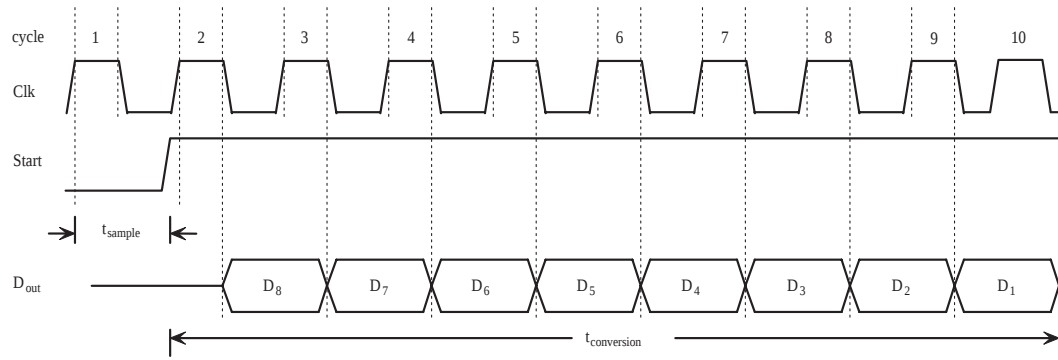


Figure 5.14. Timing Diagram for the SAR logic.

occur at its internal nodes so that the power consumption is dominated by the static power in the input stage of the comparator's preamplifier ($488 \mu\text{W}$).

CHAPTER 6

Simulation Results

Extensive verification and testing are required to correctly specify the performance of an ADC. In this work, the ADC design was validated through a number of Spice simulations based on physical test setups. Although a large number of parameters is usually provided for commercial ADCs, definitions for all of them are not clearly established among manufacturers. For this reason, the parameters presented here are limited to those found in recent publications of low-voltage ADC prototypes.

6.1 Static Measurements

The static (or DC) measurements are used to determine the time-independent parameters that characterize the performance of an ADC. The main parameters that are used for characterizing these circuits are DNL and INL. Once these parameters are measured, the input/output characteristic of the ADC can be obtained.

Figure 6.1 illustrates a typical setup used for the physical characterization of ADCs. For an N-bit converter, it uses a DC reference source that slowly increases in value up to the full-scale range, over a test time equal to 2^N conversion cycles. In a converter with minimal errors, the resulting data will contain a digital code for each quantization level. In practice, the code widths are not equally spaced by 1 LSB. This requires to take more samples for each quantization level so that every code width can be accurately determined.

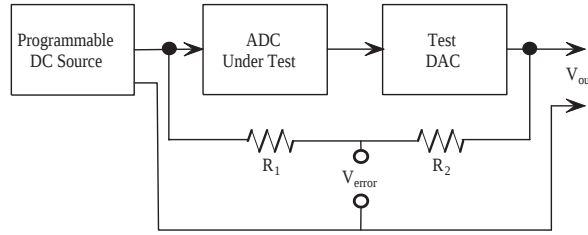


Figure 6.1. Test setup for static (or DC) measurements in an ADC [1].

The ADC presented in Chapter 5 was characterized with a transient simulation. The total transient simulation time was $460.8 \mu\text{s}$ to include the 256 digital codes. A full-scale ramp signal (from 0 to 0.55 volts) was applied, and a digital output code was produced every $1.8 \mu\text{s}$. In essence, the sampled input voltage of the ADC is incremented by an LSB for each successive conversion cycle until the full-scale value is reached.

Using a Matlab script (see Appendix A), the analog estimate corresponding to each digital code was calculated from the PSpice simulation output file. Figure 6.2 and Figure 6.3 show the DNL and INL plots, respectively. From the figures, it can be seen that the maximum DNL error does not exceed ± 0.45 LSB. Similarly, the maximum INL error does not exceed ± 0.47 LSB. Since an INL specification of ± 0.5 LSB was obtained, it can be said that the response of this ADC is monotonic and, hence, no missing codes resulted. The major contribution of DNL and INL errors can be attributed to the S/H circuit's input-dependent charge injection and the limited number of samples per code taken.

6.2 Dynamic Measurements

The dynamic measurements are used to determine the time-dependent parameters of an ADC. In this type of measurements it is of interest to study the behavior of the converter under high-frequency input signals.

Figure 6.4 illustrates a typical test setup for the dynamic characterization of an ADC. The main idea is to analyze the frequency spectrum of the converter across the full input signal bandwidth. A full-scale sinusoidal signal is applied to the ADC under test and,

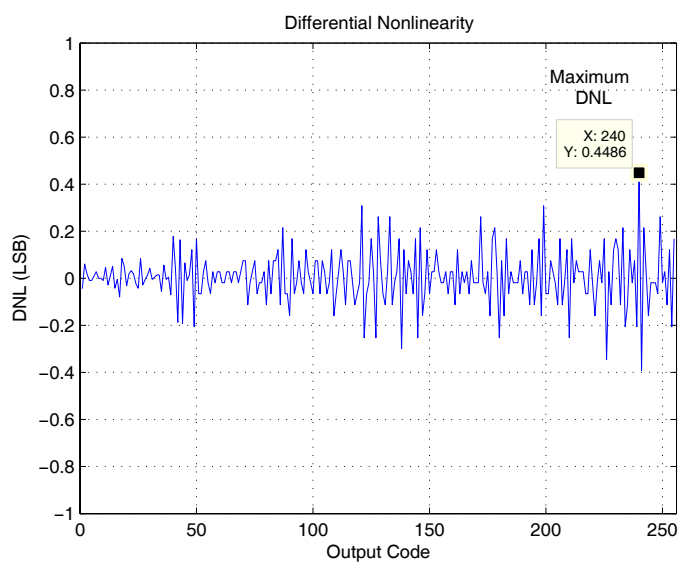


Figure 6.2. Differential Nonlinearity for the 8-bit ADC.

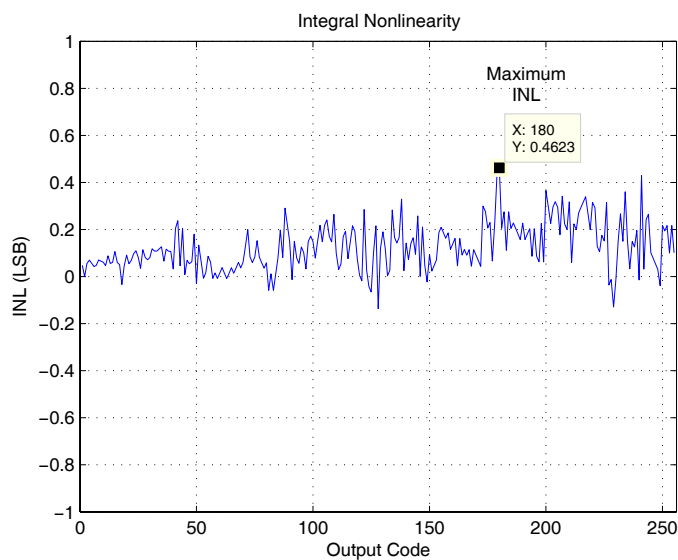


Figure 6.3. Integral Nonlinearity for the 8-bit ADC.

using a DAC of higher resolution (i.e., at least two more bits), the analog equivalent of the digital output is analyzed with a distortion analyzer. From the frequency output spectrum, parameters like SNR, SFDR, and ENOB can be calculated.

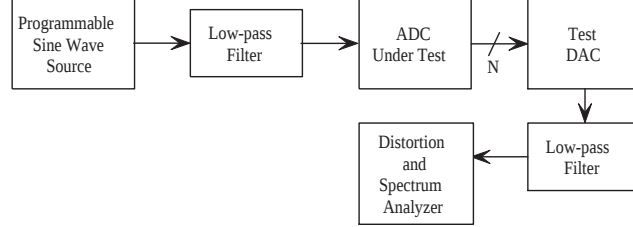


Figure 6.4. Test setup for dynamic measurements in an ADC [1].

For the ADC presented in this work, the dynamic characterization was done by applying a full-scale sinusoidal signal in a transient PSpice simulation, lasting 20 ms. Such a long simulation time is required in order to obtain more than 10,000 data points and accurately described the frequency spectrum of the converter. At the simulation level, it is important to select an input signal frequency at least 20 times smaller than the sampling frequency (i.e., $f_{signal}=19.67$ kHz and $f_S=615$ kHz). Choosing a frequency close to the Nyquist-rate will not allow to identify the harmonic components needed for the calculations.

Figure 6.5 illustrates the ADC's output spectrum for an input signal of 19.67 kHz and a sampling frequency of 615 kHz. Due to the difficulty in estimating noise floor for Spice simulations, parameters like SNR can not be calculated from Figure 6.5. As the noise component is dominated by quantization noise, the SNR specification is given by the theoretical value of $6.02N + 1.76$ dB. The proper parameter to look for is the Spurious Free Dynamic Range (SFDR). The SFDR is defined as the ratio of the maximum signal amplitude to the amplitude of the largest harmonic component. The resulting SFDR specification is approximately 63 dB. As expected from the good integral linearity, the SFDR is greater than the theoretical SNR value of 49.92 dB. In table 6.5 the performance specifications of the ADC prototype are summarized.

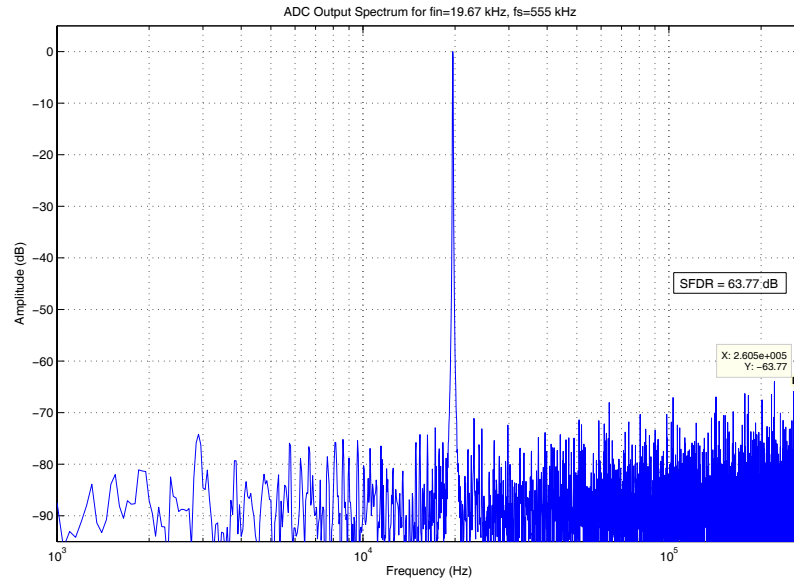


Figure 6.5. Spurious Free Dynamic Range measurement.

Table 6.1. Performance specifications for ADC prototype.

Technology	IBM 0.18 μ m
Supply Voltage	1.2 V
Resolution	8 bits
Input range	0 - 0.55 V
Conversion rate	615 kS/s
Power consumption	705 μ W
DNL	± 0.5 LSB
INL	± 0.5 LSB
SFDR ($f_{in}=19.67$ kHz @ 615 kHz)	63 dB

6.3 Performance Comparison of ADCs

To validate the design of the ADC prototype and verify that the research goals were met, it is useful to compare the ADC's performance with that of recent low-voltage SAR ADCs found in the literature. Table 6.2 below summarizes the performance specifications obtained for the ADC prototype along those found in recently-published ADCs. Based on table 4.1 from Chapter 4, it includes the characterization parameters obtained in this chapter.

Table 6.2. Comparison of ADC prototype against recent ADCs.

Reference	Supply	Resolution	Speed	Power	Technology	DNL	INL	SFDR
[29]	1.5 V	10-bit	500 kS/s	1 mW	0.25 μm	< 0.7	< 1.25	-
[5]	1 V	8-bit	50 kS/s	0.34 mW	1.2 μm	< 0.47	< 1.14	-
[34]	1 V	8-bit	100 kS/s	3.1 μW	0.25 μm	< 0.5	< 0.5	60 dB
[9]	1 V	9-bit	150 kS/s	30 μW	0.18 μm	< 0.8	< 0.8	< 65 dB
SO Comparator	1.2 V	8-bit	615 kS/s	705 μW	0.18 μm	< 0.5	< 0.5	63 dB

It is seen from table 6.2 that even some ADCs found in the literature do not comply with the typical DNL and INL specifications of ± 0.5 LSB. In this work the static specifications obtained did not surpass the previously mentioned limit. Since many publications included experimental data for their designs, most of these only provided the SNR specification. However, [9, 34] included the FFT plot from which the SFDR specification could be estimated. The SFDR figure obtained in this work is very similar to that found for the ADCs from those publications, which was around 60-65 dB. It can be concluded that the ADC prototype has static and dynamic specifications at par with those found in the literature. Although the supply voltage and power consumption specifications are slightly larger than those found in [34] and [9], the conversion rate was greater than that obtained in [29] with a lower supply voltage.

6.4 Comparator Performance

As a way to validate the design of the Switched-Opamp (OP) Comparator presented in section 5.3, Spice simulations of the circuit were performed (refer to sections 6.1-6.2). The obtained ADC specifications were at par or exceeding those found in the literature [5, 9, 29, 34]. To validate the figures of merit of the SO Comparator, its performance against that of similar circuits must be compared within the same ADC architecture. This comparison must be done using the same supply voltage and with the same technology process.

In order to better assess the conversion rate obtained with the SO Comparator, the SAR ADC prototype was simulated using three additional comparators [9, 12, 45]. The analysis presented here has not taken into consideration the input-referred offset voltage produced by mismatch. In order to minimize these errors below the required comparator resolution, common-centroid layout [18] and offset-cancellation techniques [3, 20] must be employed.

The first comparator evaluated is based on a complementary (PMOS) version of the circuit presented in [45]. Shown in Figure 6.6, the circuit operates as follows. When the Clk signal is high, the supply current is cutoff by cascode switches M_{P5} and M_{P6} , while the outputs ($V_{out}/\overline{V}_{out}$) are reset to V_{DD} through switches M_{N3} and M_{N4} . When the Clk is low, the differential input signal applied between the gate of transistors M_{P3} and M_{P4} is latched by the comparator through the regeneration loop consisting of transistors M_{N1}/M_{N2} and M_{P1}/M_{P2} .

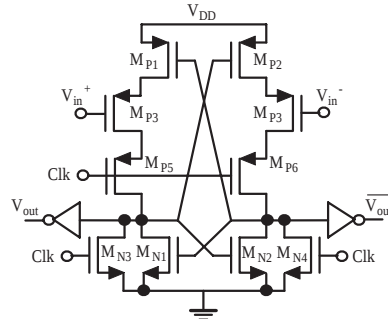


Figure 6.6. Regenerative comparator from [12].

The second comparator considered is shown in Figure 6.7. It is based on the circuit

presented in [9]. The circuit consists of a PMOS differential pair M_2/M_3 and a cross-coupled load M_5/M_6 . The output of the comparator is reset to V_{DD} through transistors M_1 and M_7 . When the Clk signal toggles to high, the differential input provided between the V_{in}^+ and V_{in}^- terminals is latched by the regeneration loop M_5/M_6 . Based on which drain terminal (M_2/M_3) has a higher voltage, one of the outputs will go high and the other low.

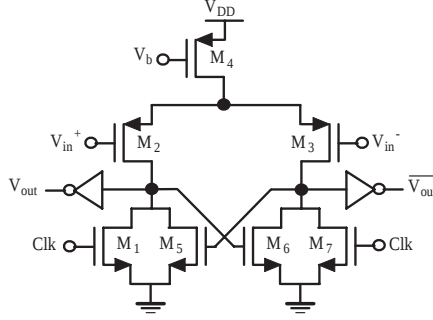


Figure 6.7. Regenerative comparator from [9].

The last comparator evaluated is based on the circuit presented in [12]. Figure 6.8 shows the comparator's schematic. The preamplification stage consists of a PMOS differential pair (M_1/M_2) and a triode load (M_3/M_4). Cascode switches M_5 and M_6 are used to enable operation of this stage when the Clk signal is high. The latch stage consists of PMOS device M_{11} and the regeneration loop formed by transistors M_9/M_{10} and M_7/M_8 . When the Clk signal toggles to low the input stage is disabled and M_{11} turns on, biasing the latch stage and allowing the comparator to latch the input signal.

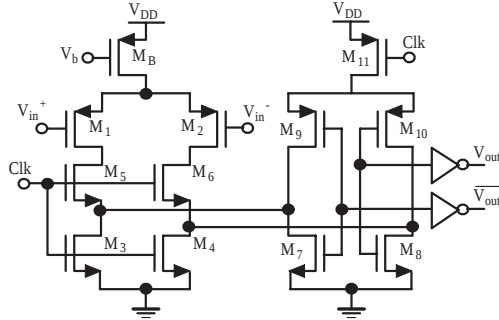


Figure 6.8. Regenerative comparator from [12].

Table 6.3 summarizes the simulated performance specifications obtained for each comparator circuit, including the Switched-Opamp comparator. All circuits were designed using IBM's 0.18 μm process models, operating with a power supply of 1.2 V. The design was targeted for a resolution of 1 mV and a power consumption within 400-600 μW . The Figure of Merit (FOM) used to compare the circuits was defined as the ratio of clock rate to power consumption. It can be seen from the table that the highest comparison rate was obtained with the SO Comparator proposed in this work. Although its power consumption was higher than that of the other three circuits, it obtained a better FOM. It is worth to mention that, even though the circuits from [12, 45] have been presented in [12] with regenerations speeds of 2 ns, the design reported on these articles was targeted for a very low resolution (4-bit at $V_{DD}=1.5$ V). As a result, the speed of these circuits was not limited by the minimum detectable input signal. Since our target specifications required a comparator resolution of 1 mV, a longer time was required to properly resolve the input signal and produce a valid binary output.

Table 6.3. Simulated comparator performance specifications.

Author	VDD	Power	Resolution	Time	Clock	FOM
Chul Song	1.2 V	510.15 μW	1 mV	210 ns	4.76 MHz	0.933058
Amaral	1.2 V	505.28 μW	1 mV	210 ns	4.76 MHz	0.942051
Sauerbrey	1.2 V	494.8 μW	1 mV	200 ns	5.26 MHz	1.064777
SO Comparator	1.2 V	604 μW	1 mV	120 ns	8.33 MHz	1.379139

As a final analysis step, each designed comparator was simulated as part of the SAR ADC prototype presented in Chapter 5. All were operated at the clock rate presented in Table 6.3. A ramp signal was applied to the converter, covering input values near the lower (00000000...00000011), middle (011111110...10000010), and higher (11111100...11111111) region of the specified input range (0 to 0.55 volts).

Table 6.4 presents the estimated ADC performance specifications for each comparator, based on the above mentioned simulation results. It can be seen that since the SO Comparator can operate at a higher clock frequency, the attainable ADC conversion rate was higher when employing this comparator circuit.

Table 6.4. Estimated ADC performance specifications.

Author	VDD	Resolution	Power	Speed
Chul Song	1.2 V	8-bit	520 uW	529 kS/s
Amaral	1.2 V	8-bit	515 uW	529 kS/s
Sauerbrey	1.2 V	8-bit	505.3 uW	555 kS/s
SO Comparator	1.2 V	8-bit	628 uW	925 kS/s

CHAPTER 7

Conclusion

The design of analog-to-digital converters is one of the most critical and challenging aspects in the development of new and more powerful electronic systems. The trend toward system on a chip (SoC) solutions, and hence low-voltage operation, requires the analog circuit components to reside on the same chip as the digital circuits. This results in savings of area and power consumption, essential for extending the battery life of current portable equipment or remote location devices, such as that used in instrumentation systems. Depending on the type of measurement to be monitored by the data acquisition system, the speed requirements are also a concern. Of the A/D converter choices available today, the successive approximation (SAR) ADC represents the optimal trade-off among speed and power consumption within low- to medium-resolution requirements.

The design of low-voltage low-power SAR ADCs makes imperative greatly minimizing the errors associated with technology matching and the SNR degradation. The circuit design techniques applied must result in an ADC with reasonable performance specifications when compared to their high-voltage, or nominal, counterparts. Most of these techniques are based on the use of modified circuit structures that optimize the use of the available voltage headroom. In this way, active devices such as comparators do not suffer from the limited gate-overdrive present in transistors. As a result, the performance of such circuits is optimized. The work produced with this research resulted in the complete design of a

SAR ADC based on the use of recently-published low-voltage circuit techniques and the creation of a new architecture for one of its most critical circuit blocks, the comparator. These included:

- Charge injection cancellation to eliminate undesired offsets.
- Sampling-switch compensation to reduce input-dependent charge injection.
- DAC output range adjustment for compatibility with the comparator's input range.
- Elimination of critical switches in the comparator architecture that can result in speed degradation.

The effects of channel charge-injection in S/H circuits and the DAC's input/output characteristic were discussed in Chapter 3. The results obtained from Spice simulations show that, when switches are referenced to V_{DD} or ground, the use of dummy switches helps in reducing the charge-injection errors below $20\ \mu\text{V}$.

The power consumption requirements imposed for the ADC design, restricted the choices of S/H architectures to open-loop configurations that suffer from input-dependent charge-injection. To mitigate this nonlinear error, the sampling switch was compensated using dummy switches at its drain and source terminals. These resulted in sampled signal errors less than ± 0.3 LSB.

The limited input range of the comparator made necessary to adjust, or scale, the output range of the DAC. This guaranteed proper comparator operation over the whole input range. A drawback of using this technique is that the required resolution of the comparator needs to be increased in order to compensate for the decrease in the LSB value (i.e., $2.15\ \text{mV}$) and the associated quantization levels. As a result, the voltage gain specification for the comparator's preamplifier stage became more stringent.

In this work, a novel solution was proposed to eliminate the critical switches that plague the speed performance of low-voltage high-resolution comparators. It is based on the Switched Opamp technique, which in the literature has prove useful in the design of

switched-capacitor circuits. To the author's knowledge, this technique has not been previously used in comparator design. As was discussed in Chapter 5, any switch without one its terminals connected to a constant reference (i.e, V_{DD} or ground) will suffer from high on-resistance if a signal close to rail-to-rail swing must be transmitted. By making the preamplifier's output stage switchable, the series switch connected between preamplifier and latch was eliminated.

The techniques just outlined lead to the design of a 1.2V 8-bit 615kS/s 705 μ W SAR ADC prototype, suitable for low-voltage, low-power, and low- to medium-resolution applications. Simulations were made to validate the design and characterize the performance of the ADC. The DNL and INL specifications obtained were in agreement with the typical specification of ± 0.5 LSB. The dynamic performance of the converter was assessed through the SFDR specification. Through Matlab Power Spectral Density (PSD) calculations, the output spectrum of the converter was obtained; leading to an SFDR specification of 63 dB. Based on the linearity results obtained and the theoretical SNR specification, the dynamic performance of ADC is good. The overall performance of the ADC is similar to that found in the literature. However, in this work the speed performance of SAR ADCs has been improved. This was done with a new comparator architecture that achieved higher resolution and moderate speed without a large increase in power dissipation.

7.1 Future Work

The performance of the ADC prototype produced by this research proved to be at par with that found in recent low-voltage ADC prototypes, nonetheless achieving a higher conversion rate. However, there is room of improvement in certain areas of the design presented in this work. One of those areas is related to the S/H stage. The ADC would benefit from using a more robust architecture that suppresses the harmonic distortion introduced by charge injection errors. The most prominent way to eliminate this source of error is by employing a closed-loop architecture. Since such architectures require the use of op amps,

the development of new ultra low-power (i.e., $< 100\mu W$) op amps is an interesting area of research.

The preamplifier stage found in the comparator suffered from reduced signal swing. Although some solutions were described in Chapter 4, they all had limitations. In ultra low-voltage conditions none of those techniques can be applied. New ways to circumvent this problem must be found. Another area of concern in the comparator is the input offset voltage. In this work, offset cancellation schemes were avoided in order to minimize the number of critical switches employed. In higher-resolution applications, the input offset voltage must be canceled out or the comparator will not be able to resolve very small signals. Finally, the comparator's preamplifier stage could benefit from a Class-AB output stage which would result in lower power consumption without a significant decrease in circuit speed. Since the comparison time was the major limitation in the conversion speed of the ADC prototype, improving the slew rate of the op amp would result in better time response.

APPENDICES

APPENDIX A

Matlab Code

This appendix presents the Matlab script used to calculate the performance parameters presented in Chapter 6. The output file produced by PSpice provided the voltage present at each bit line of the ADC for every time step of the transient simulation. As described in Chapter 6, only the voltages present at the end of each conversion cycle are of interest. As a result, the data had to be filtered so that only valid output codes are used in the calculations. In section A.1, the Matlab code used to calculate the DNL and INL parameters is presented. Then, section A.2 presents the code used to plot the ADC's frequency spectrum needed to determine the SFDR specification. The latter is based on the use of Matlab's Power Spectral Density (PSD) function as suggested by [46].

A.1 DNL and INL Calculations

```
index=size(adcData);  
  
% Columns for adcData matrix:  
  
Vin=2;Vs=3;D8=4;D7=5;D6=6;D5=7;D4=8;D3=9;D2=10;D1=11;  
  
% Columns for Dout matrix:  
  
Vout=1;Vsample=2;Vshifted=3;  
  
% OUTPUT CODE DATA RETRIEVAL  
  
j=1;
```

```

k=181; % row with first sampled value
for i = 181:180:index(1,1)
    Dout(j,Vout)=(round(adcData(i,D8))/2 + round(adcData(i,D7))/4 +
        round(adcData(i,D6))/8 + round(adcData(i,D5))/16 +
        round(adcData(i,D4))/32 + round(adcData(i,D3))/64 +
        round(adcData(i,D2))/128 + round(adcData(i,D1))/256)*0.55;
    Dout(j,Vsample)=adcData(k,Vs);
    k=k+180;
    j=j+1;
end
totalCodes=size(Dout);
LSB=(Dout(256,Vout)-Dout(1,Vout))/256;
% END OF OUTPUT CODE DATA RETRIEVAL
idealLSB=0.55/256;
for i=1:totalCodes(1,1)
    idealVT(i)=(i-1)*idealLSB;
end
Offset=Dout(2,Vsample)-idealVT(2);
for i=1:totalCodes(1,1)
    Dout(i,Vshifted)=Dout(i,Vsample)-Offset;
end
% DNL/INL CALCULATION
for m=1:totalCodes(1,1)-1
    DNL(m)=(Dout(m+1,Vshifted)-Dout(m,Vshifted)-LSB)/LSB;
    INL(m)=(Dout(m,Vshifted)-idealVT(m))/LSB;
end

```

A.2 Spurious Free Dynamic Range Calculation

```

index=size(adcData);

% Columns for adcData matrix:
Vin=2; Vs=3; D8=4;D7=5;D6=6;D5=1;D4=2;D3=3;D2=4;D1=5;

% OUTPUT CODE DATA RETRIEVAL

% Scans all rows of the data matrix and calculates
% analog estimate of digital code

Vsample=1; Vout=2;

j=1;

for i = 181:180:index(1,1)

    Dout(j,Vout)=(round(adcData(i,D8))/2 + round(adcData(i,D7))/4 +
        round(adcData(i,D6))/8 + round(adcData(i,D5))/16 +
        round(adcData(i,D4))/32 + round(adcData(i,D3))/64 +
        round(adcData(i,D2))/128 + round(adcData(i,D1))/256)*0.55;

    Dout(j,Vsample)=adcData(i,Vs);

    j=j+1;

end

% END OF OUTPUT CODE DATA RETRIEVAL

% Power spectral density calculation to obtain frequency spectrum
dataPoints=length(Dout(:,Vout));

[Spectrum,Freq]=psd(Dout(:,Vout),dataPoints,fs,kaiser(dataPoints,20))

```

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